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Rapid Thermal Oxidation Process for 100Å SiO_2

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Abstract- **An examination of RIT's AG Associates Heatpulse 410 rapid thermal processing system has been conducted to look at the possibilities of an in-control, high quality, 100Å oxide growth process. Some of the complications involved with modifying the existing system to have the oxidation capability are discussed. Growth rate curves for various temperatures have been developed through a designed experiment. MOS capacitors have been fabricated using an optimized 100Å recipe to characterize the electrical properties of the oxide.**

The process for growing 100Å oxides was tested for uniformity, repeatability, and oxide quality. Ellipsometry mapping of the wafers showed a 5.8% uniformity across the oxide surface. The results of the repeatability tests proved the process to be stable from wafer-to-wafer. High and low frequency C-V tests of MOS capacitors showed an effective oxide charge of $-6*10^{11}$ q/cm. Voltage-ramp breakdown tests resulted in an average breakdown strength of 9MV/cm.

I. Introduction

As RIT's Microelectronic Engineering department strives to advance the capabilities of its cleanroom to make sub-micron CMOS devices, very thin oxides will be required for the devices. The current state of our student run cleanroom's furnaces makes high-quality thin oxides difficult to grow reproducibly. Rapid thermal oxidation is a viable technique to accomplish high-quality very thin oxides in an undergraduate, student run facility.

The present rapid thermal processor has been an under utilized piece of equipment since its introduction to the Microelectronic Engineering Facilities in 1993. The system is capable of handling five different source gases. However, it has been primarily used for dopant activation and metal sintering, both done in an inert Nitrogen ambient.

Relative temperature growth rates were statistically derived using a 2-Factor 3-Level designed experiment. The temperature settings for the experiment were: 1100, 1150, 1200 °C. With limited ability to calibrate the system, assumptions regarding the temperature read by the pyrometer had to be made. A non-symmetric time factor was used to observe initial oxide growth kinetics. The time settings for the experiment were: 45, 60, 120 seconds. Thickness ranged from 60 to 200Å.

Rapid thermal oxidation (RTO) for tunnel oxides has been tested for over 10 years. The process would be simpler than its furnace equivalent, which could have upwards of 4 soak temperatures and can take as much as 9 hours. The quality of the oxides grown would be as good if not better than the furnace grown equivalent.

RTO was not widely implemented at the time or since then due to the incredible throughput of a furnace process. The wafer to wafer uniformity of an RTO process is suspect. Over the past 10 years, not much has changed.

1996 is determined to be a year of change for the semiconductor industry. 300mm wafers will be the next size wafer. These wafers will not be batch processed at any step. Wafer warpage will make furnace use impractical, if not impossible. As the world begins to implement 300mm processing, the diffusion furnace will become a relic for museums. RTO is one viable technology available now, that will work on wafers at 300mm.

Along with giving future RIT Microelectronic engineering students the ability to use RTO on their projects, this project will allow RIT to example a possible "next generation" technology to future students in preparation for their jump into the semiconductor industry.

II. Experimental

After the modification of the GHS-01 Gas Handling System was made to allow Oxygen to be used as a source gas, a 2-Factor 3-Level designed experiment was utilized to determine some baseline growth curves. *(See Figures 1,2,3,4)*

Temperature Levels:	1100, 1150, 1200 Degrees Celsius		
Time Levels:	45, 60, 120 Seconds		
Wafer Number	Temperature	Time	Program
T1	1100	45	RTO1
T2	1100	60	RTO2
T3	1100	120	RTO3
T4	1150	45	RTO4
T5	1150	60	RTO5
T6	1150	120	RTO6
T7	1200	45	RTO7
T8	1200	60	RTO8
T9	1200	120	RTO9

Figure 1. Experimental Worksheet for Designed Experiment

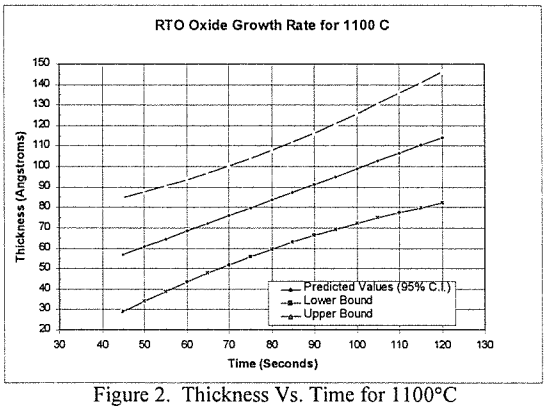

Figure 2. Thickness Vs. Time for 1100°C

The results of this experiment did not closely match those observed in similar experiments [1]. This can be attributed to a number of equipment issues, most notably the calibration of the pyrometer. However, the predictable behavior based on these graphs can be counted on for later experiments done at RIT.

Using the data from these graphs the focus of experimentation shifted to the repeatability of a high quality 100Å film.

Five separate repeatability tests were performed using the following 100-104Å recipe:

30 Sec O_2 Soak; Room Temperature
30 Sec RTO; 800° Celsius
60 Sec RTO; 1150° Celsius
(O_2 Flowrate of 5 slms)

The two-step process is utilized to stabilize the chamber, and to allow the wafer to reach the oxidation temperature as quickly as possible [2]. A similar two-step rapid thermal anneal done in Nitrogen (5 slms) was done close-coupled with the oxide growth.

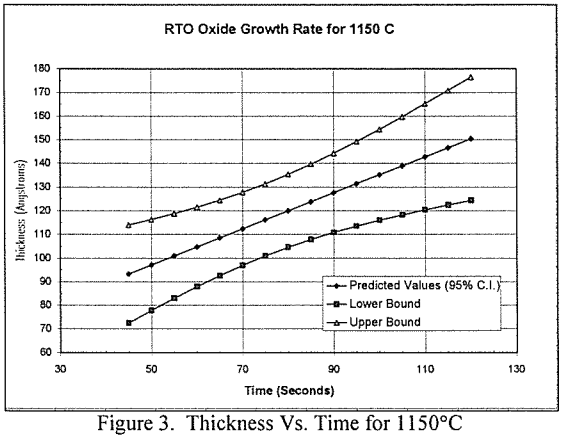

Figure 3. Thickness Vs. Time for 1150°C

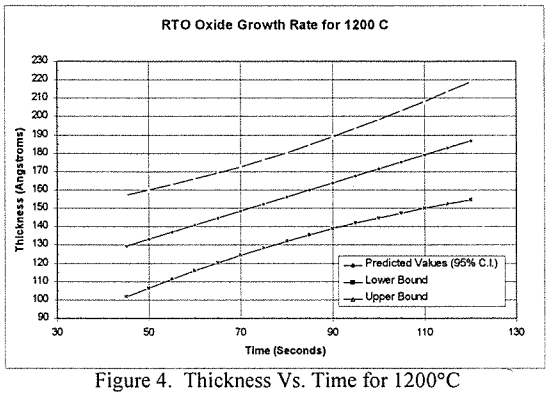

Figure 4. Thickness Vs. Time for 1200°C

The focus of the experiment then shifted to capacitor fabrication using the 100Å RTO process. Both N and P-type <111> wafers with a resistivity of 5-10 Ω-cm were processed. The process flow for the fabrication of the MOS capacitors is pictured on the following page. (See Figure 5)

The RCA clean was performed in the APM -HF Dip - HPM - DI Rinse order [3]. The thickness of the evaporated Aluminum was approximately 4000 Å. Figure 6 shows the layout of the wafer after the patterning. The chemical Aluminum etch endpoint was determined optically. Photoresist strip was 2 to 3 minutes agitated in Acetone followed by a Methanol rinse..

Oxide thickness was measured using either a Rudolph Auto-Ellipsometer, or an Applied Materials Manual Ellipsometer. Oxide quality was measured using Semitest's Surface Charge Analyzer. Voltage-Ramp capacitor breakdown tests were conducted on an HP-4145 parameter analyzer. CV tests were done using Keithly CV test equipment. Wafer mapping was

conducted at CVC Products, Rochester, NY using a PLAS MOS automatic ellipsometer.

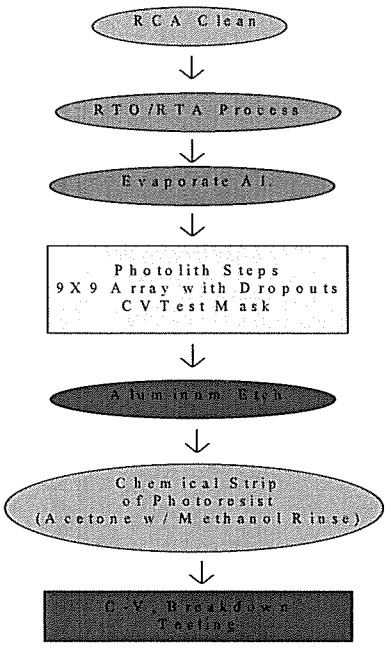

Figure 5. Process Flowchart.

III. Results

There were numerous difficulties in the modification of the RTP system. Most were focused around the lack of a proper manual to follow. Detailing all of the different problems would not be appropriate here, however one situation which cause the most difficulties was the microcontroller's "confused" state.

On two separate occasions microcontroller went into what is known as the "confused" state. This situation is very troublesome and can cripple the system if the proper recovery is not known. On the first occasion the communications cable was removed while the microcontroller was operating. On the second occasion is occurred from an overload in the microcontroller's memory.

While the microcontroller is confused nothing can be done with the system. A very simple way to detect this situation is to enter the UDF command "***MAIN***," which would normally return the user to the Main Menu. If the microcontroller is confused, the screen will simply lock up.

The remedy for this problem requires opening up the microcontroller, removing the daughterboard (a small board underneath the main board), and pulling jumper **W-21**. The jumper needs to remain pulled for at least 10 minutes. As with any electrical system, **the power should be off and all cords disconnected prior to opening the microcontroller.**

This procedure will recover the system from the "confused" state. Pulling the **W-21** jumper disconnects the battery back-up to the microcontroller's memory. Removing it will clear the memory. This will also erase any User Defined Functions(UDF's) which were stored in

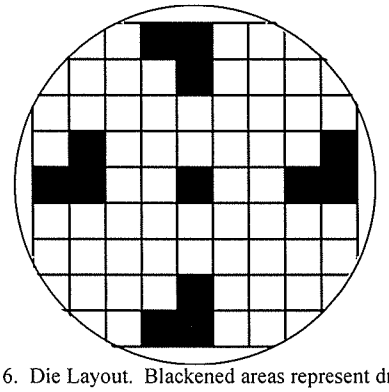

Figure 6. Die Layout. Blackened areas represent dropouts.

the memory at the time. All RTO processes are UDF's.

The oxide thickness readings for the designed experiment were obtained from the average of a 5 point test, with a fixed refractive index at 1.46. Manual ellipsometer readings were not sensitive enough for this experiment. Readings taken on a Nanometrics Nanospec were considerably different for the thinner oxides.

	Ellipsometer	**Nanospec**
Wafer T1	**60.4Å**	**117Å**
Wafer T5	**104Å**	**127Å**
Wafer T9	**201Å**	**213Å**

Particle counts showed very little particulate contamination due to the RTO process.

Using the Surface Charge Analyzer (SCA) the oxides for 3 test wafers were looked at. Initial tests showed a negative effective oxide charge on the order of $-1*10^{+11}$ q/cm.

Investigation surrounding possible metal contamination of the system was conducted where it was discovered that wafers containing electroplated, uncommon, heavy-metal elements such as Er, Y, and Mn were processed through the RTP earlier this past year. These metal contaminants could cause the phenomenon noticed in the SCA tests. Furthermore, the contamination may have caused an unknown V_{th}

shift in devices which went through RTP for anneal. Once the RTO/RTA process for 100Å oxides was determined, 3 repeatability studies were conducted with acceptable results.

The uniformity of the process was determined by mapping the thickness at approximately 80 points across the surface. The uniformity was as low as 5.4% across the wafer, with an average of about 5.8%. From run to run, the process had a 2% variation.

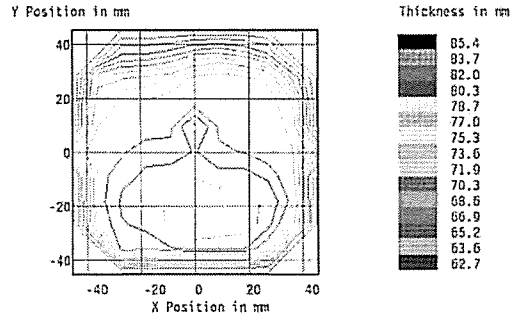

Figure 7. Thickness Contours of 100Å repeatability test wafer. Thickness calculated based on a fixed n=1.46.

The fabricated N-type MOS capacitors were initially tested using a voltage ramp breakdown test method [4]. Three different area capacitors were tested at ten sites on 2 wafers.

Wafer	Avg. V_{bd}	MOS Capacitor Area	
	200 kμ²	800 kμ²	1.6 Mμ²
N1	9.3MV/cm	8.88MV/cm	8.26MV/cm
N2	9.57MV/cm	8.77MV/cm	7.94MV/cm

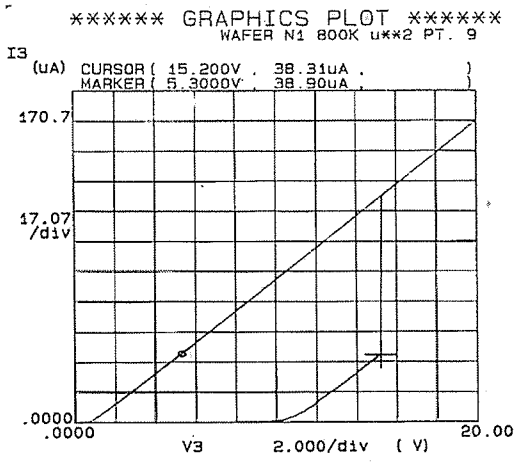

Figure 8. Breakdown Characteristics for N-Type Wafer. 800kμ² area MOS Capacitor. Wafer N1. 9.9 MV/cm Breakdown.

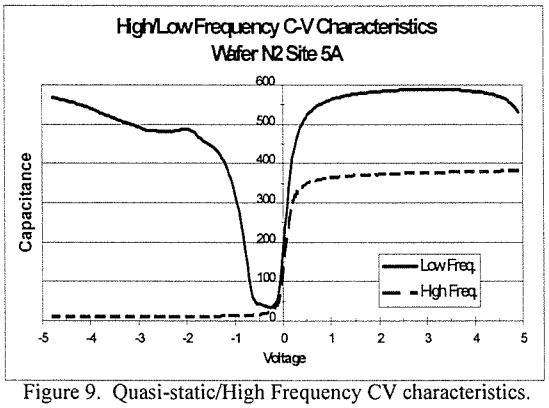

Figure 9. Quasi-static/High Frequency CV characteristics. **N-Type** wafer. C_{ox} = 537pF. V_{fb} = -0.035V. V_{thresh} = -0.62V.

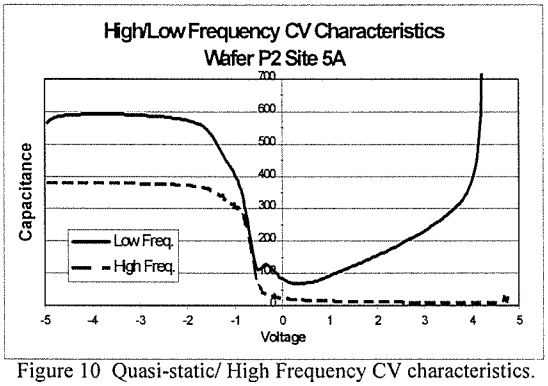

Figure 10 Quasi-static/ High Frequency CV characteristics. **P-Type** wafer. C_{ox} = 526pF. V_{fb} = -0.58V. V_{thresh} = 0.026V.

Initial tests done on the P-type MOS capacitors yielded no significant results. Further testing is needed for the P-type wafers Of the many sites tested only 5 capacitors experienced breakdown.

Quasi-static and high frequency CV tests were conducted on 200 kμ² area capacitors at 4 sites on both N- and P-type wafers using Keithly CV test equipment. Voltage was swept from -5 to 5 Volts.

The C_{ox} values obtained from the quasi-static CV curve gave an electrical oxide thickness of approximately 115Å.

The oxide charge estimated from the flatband voltage was about -6.3*10+11 q/cm. This agrees with the initial SCA readings done on the original test oxides.

IV. Summary

An investigation of rapid thermal oxidation using an AG Associates Heatpulse 410 at the Rochester Institute of Technology was conducted. Emphasis was placed on the uniformity,

repeatability and quality of the oxides grown by RTO.

The system has been successfully modified to include oxygen as a source gas, enabling RTO processing. A manual and growth rate curves have been placed on-line at the RTP. A process for growing a 100Å oxide was investigated with acceptable results on the uniformity and repeatability of the process.

The quality of these initial oxides is suspected to be degraded by metal contamination in the RTP. The breakdown and CV characteristics are reasonable for this initial processing of rapid thermal oxides. Once the contamination issue has been addressed the oxide quality should improve to the standards needed for tunnel or gate oxides.

V. ACKNOWLEDGMENTS

The technical support of AG Associates was very helpful from the very beginning of this project. Special thanks to Vera Versteeg and her group at CVC Products in Rochester, NY for use of the PLAS MOS wafer mapping equipment. Drs. Santosh Kurinec and Michael Jackson provided much needed guidance and assistance throughout this project.

REFERENCES

1 J.Nulman, J.P. Krusius, A. Gat, "Rapid Thermal Processing of Thin Gate Dielectrics. Oxidation of Silicon,"*IEEE Electron Device Letters,* Vol. EDL-6, No. 5, May 1985, pp. 205-207.

2 *ibid,* Ref. 1.

3 B. Kasprowicz, "Effects of Variations in RCA Clean on Breakdown Characteristics of Thin Gate Oxides," 14th Annual Conference on Microelectronic Engineering, Rochester Institute of Technology, May 1996.

4 *ibid,* Ref. 3.