

Improvement in Polysilicon Etch Process for the RIT Factory

Thomas F. Flynn, Jr.
Microelectronic Engineering
Rochester Institute of Technology

Abstract

Investigations of the polysilicon etch process utilized by the RIT factory for CMOS fabrication were conducted. The RIT factory process utilizes a dry polysilicon etch process that employs SF_6 and O_2 chemistry, with flow rates of 42 sccm and 7.5 sccm, at 400 mTorr pressure and 40 Watts of RF power in a GEC PlasmaCell. This process was found to suffer from uniformity problems. Studies were done to attempt to improve the etch uniformity, by varying the chamber pressure. A significant improvement in the uniformity was achieved for a much lower chamber pressure of 175 mTorr under the same conditions of power and flow rates. Results consisting of etch rate, linewidth loss, sidewall angle, and selectivity with regards to silicon dioxide have been included in this paper.

I. INTRODUCTION

Etching is the procedure that transfers the 3-D pattern obtained from the preceding lithography step to the underlying layer. Dry etching or plasma etching is used to transfer patterns that consist of very small geometries. A physical etch process tends to allow for increased sidewall angles but with poorer selectivity. Chemical etches tend to be much faster with poorer uniformity and a large amount of undercutting.

The following characteristics are desirable for any type of etch process: uniformity of etch rate across the wafer, minimal pattern loss, steep sidewalls, and high selectivity over the underlying layer.

Plasma etches are functions of four specific parameters; these parameters being RF power, chamber pressure, gas ratios and flow rates. Varying any of the above parameters either in combination or by itself will lead to changes in the etch characteristics. An increase of RF power leads to ions that are more directional with a chance for more vertical side walls. The lowering of chamber pressure tends to have the same effect but because there are fewer particles in which to change the direction of the etching species.

The polysilicon etch used at RIT is often characterized by its lack of uniformity. This is often characterized by the Bull's Eye phenomenon, which

occurs when the edges etch faster than the center. This occurs from a lack of etchant gas at the wafer's center. The RIT etch parameters are as follows: pressure of 400 mTorr, RF power of 40 Watts, and gas flows of 42 sccm for SF_6 and 7.5 sccm for O_2 . The pressure of 400 mTorr seemed too high and a possibility for the non-uniformity experienced with this process. The main objective of this project was to vary the pressure to gain a uniform etch rate.

II. EXPERIMENTAL PROCESSING

The starting point of this experiment was to study the effect of varying the chamber pressure, on etch rate uniformity. A range of pressures from 400 mTorr to 150 mTorr was examined, keeping the power, gas ratios, and flow rate parameters constant.

Preparation of wafers both for the pressure experiment and future poly line sizing data was similar. First, a 1000 Å thermal oxide layer was grown in wet O_2 for 49 minutes at 900° C. The purpose of this film was to allow for polysilicon thickness measurements by the Nanometrics Nanospec using a standard thickness measurement program of polysilicon over a 1000Å of SiO_2 . A polysilicon layer was then deposited by LPCVD with silane gas with a gas flow of 90 sccm at 610° C, for 70 minutes. This resulted in a average thickness of 0.6 µm. A cross section of the processed wafers is given in Figure 1.

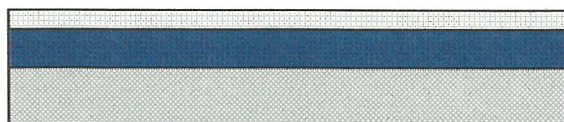


Figure 1.

The thickness of each layer was measured at 5 locations on the wafers as shown in Figure 2.

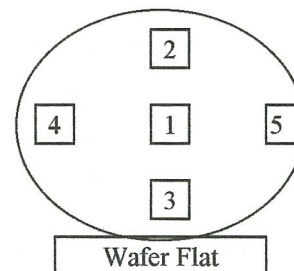


Figure 2.

Wafers were then etched in the GEC Plasma Cell for 30 seconds at the varying pressures with the other parameters held constant at 40 Watt, RF Power, and flow rates 42 sccm, SF_6 , and 7.5 sccm, O_2 . After the etch the wafers were then re-measured to determine the amount of polysilicon loss and the uniformity.

Upon determining the optimum chamber pressure with regards to uniformity, the polysilicon was patterned to determine linewidth loss as well as to later look at the sidewall angle of the final poly lines. The polysilicon layer was patterned with the g-line Kasper Contact Aligner, and an ARC (Anti-Reflecting Coating) dark-field mask. Figure 3 show a cross sectional view of the processed wafers up to this point.

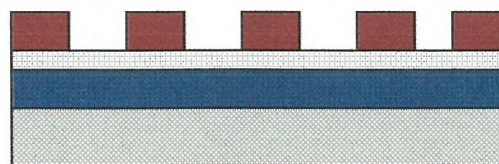


Figure 3.

The mask contained line/space dimensions of 5, 10, and 20 µm. The contact aligner was used because the ARC mask would not work in conjunction with the GCA stepper.

Linewidth measurements were made following the completion of the photo processing. The Nanometrics Nanoline III was used to measure the resist lines. This allowed for a linewidth loss due to photo processing to be determined.

Final etching was done to determine the final sizing of the polysilicon lines in the GEC Plasma Cell. All parameters were held constant except the pressure which was 400 mTorr (RIT) and the optimum pressure, with etch times of 60 seconds. Following, removal of the photoresist, linewidth measurements were taken with the Nanoline. This allowed for a determination of linewidth loss due the plasma etching. Similar measurements were taken of the oxide, using the same layout as in Figure 2. The final processing cross-section is given in Figure 4.

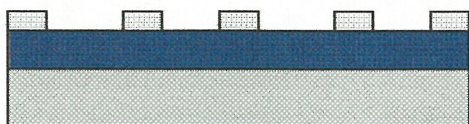


Figure 4.

III. RESULTS & DISCUSSION

The results of the uniformity experiment are summarized in Table 1. Uniformity was calculated as the difference of the maximum and minimum thickness loss after the 30 second etch.

Pressure mTorr	Uniformity Å	E.Rate, C Å/min	E.Rate, E Å/min
400	1054	6604	5205
325	1050	7134	5341
275	547	6668	5796
200	302	5458	5415
175	178	5302	5314
150	272	4301	4801

Uniformity Results

Table 1.

It can be observed that a pressure of 175 mTorr yielded the best uniformity in etch rates across the wafer.

Subsequently, the linewidth loss, oxide thickness loss, and sidewall profiles were studied for the pressures of 175 mTorr and 400 mTorr. Linewidth loss measurements were collected for the 5 and 10 μm line

geometries. The initial linewidth loss that occurred was a result of development portion of the lithographic step. The linewidth loss measurements are included in Table 2, and the oxide thickness loss results are summarized in Table 3.

Process	5 μm	10 μm
Photo	0.7 μm	0.8 μm
Photo & 400 mTorr (RIT)	1.01 μm	1.16 μm
Photo & 175 mTorr Etch	1.17 μm	1.30 μm

Linewidth Loss

Table 2.

It can be seen from Table 2 that at a 175 mTorr etch pressure, the final linewidth loss has increased by about 14%.

Process	Edge	Center
RIT, 400 mTorr	26 Å	89 Å
175 mTorr	173 Å	200 Å

Oxide Thickness Loss

Table 3.

The oxide thickness loss with the etch pressure of 175 mTorr was increased. However, this thickness loss was found to be more uniform from edge to center.

The 5 μm polysilicon lines following the etch process were viewed under a scanning electron microscope (Phillips 501 SEM). Figures 5 and 6 show a 5 μm

line etched by a 400 mTorr process and a 175 mTorr process respectively.

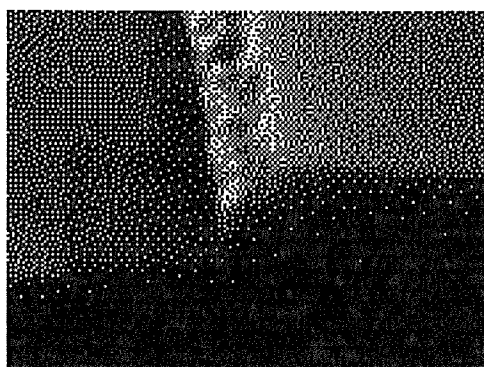


Figure 5.
400 mTorr
Magnification: 20k

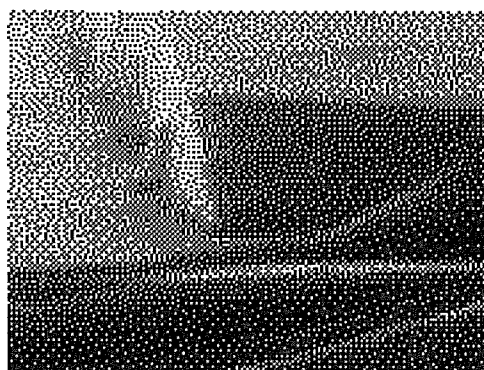


Figure 6.
175 mTorr
Magnification: 20k

The sidewall appears to be much more vertical for the 175 mTorr process.

The pressure of 175 mTorr did yield a more uniform etch rate across the wafer, and did eliminate the Bull's Eye Effect, by allowing more etchant to be at the center because of fewer collisions. The linewidth loss did increase with the lower pressure but this loss would be uniform across the wafer. This could allow for correctly biasing the mask to counter this linewidth loss. An increase of oxide

thickness loss was observed at the lower pressure. However, in actual processing this would have been the field oxide, which normally has a thickness of 5000 Å to 7000 Å. It seems that a 200 Å loss would not seriously effect the final transistor. The 175 mTorr pressure did give steeper sidewalls which lends itself that this new pressure gives a more anisotropic etch. This also follows with the concept that the lower pressure gives a more directional etch due to the lower possibility of collisions in the chamber.

IV. CONCLUSIONS

It was determined that the current etch recipe using a 400 mTorr pressure is plagued with non-uniformity and slanted sidewalls. A lower pressure of 175 mTorr yielded a very uniform etch rate across the wafer, with a difference of 12 Å from center to edge.

ACKNOWLEDGMENTS

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REFERENCES

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