

# Development of Bonding and Etchback Silicon on Insulator Wafers

Bobby Mozumder, *Rochester Institute of Technology*

**Abstract-** Bonding and Etchback Silicon on Insulator wafers were successfully developed at the Rochester Institute of Technology's Microelectronics facilities. [100] and [111] wafer pairs were successfully bonded using SOG and Thermal Oxides and etched back using timed KOH etch. The results were successfully bonded wafers with a large Silicon layer.

## I. INTRODUCTION

The past few years have seen a significant growth in the attempts to create electronics grade silicon on an insulating substrate. These silicon on insulator wafers have been demonstrated to have several advantages that are useful for modern submicron CMOS processes. Processing is simpler because of the elimination of the well as isolation structures. This also helps to dramatically increase density. The existence of a underlying layer of silicon creates a much more ideal transistor structure that improves device performance. The elimination of the source-drain to well junction helps to reduce capacitance, which increases speed and reduces power requirements of the circuit. This also reduces leakage currents by using dielectric as device isolation instead of electrical junctions. Parasitic bipolar transistors in the CMOS, an effect that has hindered the development of CMOS for years, are eliminated, thus eliminating the possibility of latch-up. This also helps to reduce area because substrate contacts are not required. And SOI devices are very resistant to transient radiation because radiation particles tend to go right through the silicon layer instead of being trapped in them because the silicon layer tends to be small.

There are several methods of creating SOI wafers. The two most popular are SIMOX and bonding with etchback. SIMOX relies on a high energy high current implantation of oxygen ions onto the top surface of a silicon layer to create a buried oxide layer underneath the silicon surface. The disadvantage to this process is that it causes damage to the crystal structure on the top silicon layer. The wafer must therefore go through steps of high temperature annealing to repair the damage to the crystal, but rarely will the crystal structure be fully repaired.

Bonding and etchback, introduced by Latsky et. al at IEDM '85 [7], relies on the bonding of a pair of oxide coated wafers in various temperature ranges to create a buried oxide layer. One of the wafers is then etched until a thin layer of silicon is left. This becomes the device layer and the other wafer becomes the handling substrate. The advantage to the bonding and etchback scheme is that it allows a perfectly crys-

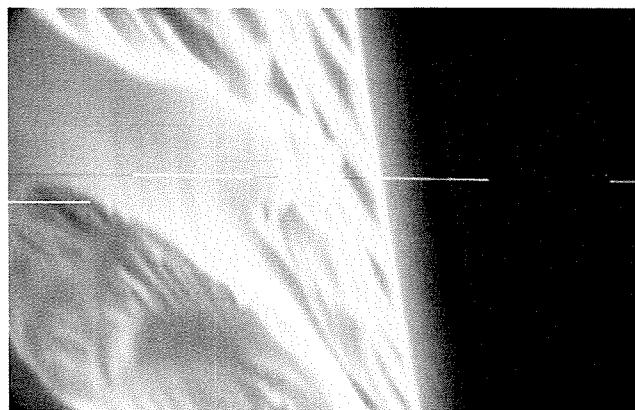


Fig 1: 20000x SEM of the bond. 1  $\mu\text{m}$  lines and spaces are displayed for scale. The underlying oxide is 3000 Å. The [100] wafer is on the left side of the bond.

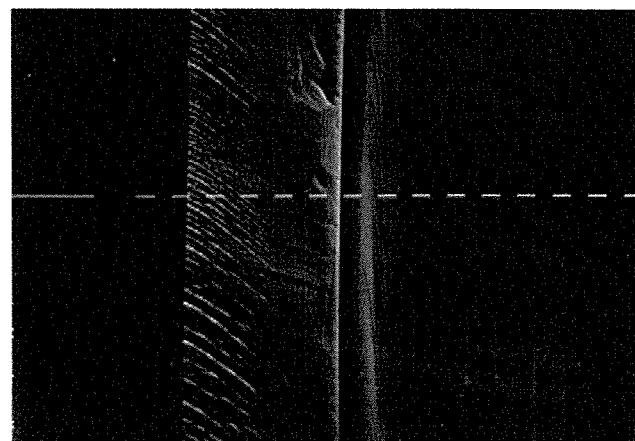


Fig 2: 380x SEM of the bond. 10  $\mu\text{m}$  lines and spaces are displayed for scale. There is about 90 microns of [100] wafer left on the left side of the bond.

talline silicon layer. The disadvantage is that the silicon layer tends to have nonuniform thicknesses. The etch process has been the major obstacle to the acceptance of this technology.

This experiment evaluates both the bonding and etching schemes available at RIT for the manufacture of SOI wafers at the RIT Microelectronics facilities.

## II. EXPERIMENTAL PROCEDURES

Several factors affect the quality of the physical bond between the wafers in bonded SOI wafers. The quality of the oxides, the surface particle counts, the uniformity of the wafers, the bonding temperatures, and initial bonding methods are several factors that affects the bond between the wafers.

Several experiments were run to create high quality bond between the wafers. Pairs of [100] and [111] 2" wafers were coated with 3000 Å Spin on glass or 1200 Å thermally grown oxides. The thermally grown oxides were created using a TCA clean process and dry O<sub>2</sub> with slow ramp-down to create a high quality Si-SiO<sub>2</sub> interface. Surface particle counts were recorded at every process step. The [100] wafers were then bonded to the [111] wafers in the furnaces. The SOG wafers were bonded at 700 °C for 30 minutes and the thermally grown oxide wafers were baked in the furnace at 1250 °C for 8 hours. These bonding operations took place in inert N<sub>2</sub> ambient. SEM's were then taken of the actual bonds.

After bonding operations, tests for etchback were done. The goal is to get a final silicon layer thickness of about 700 Å and a high rate of throughput. This would leave a fully depleted layer of silicon underneath any gate poly structure. The advantages to having such a thin fully depleted layer of silicon on insulator are many, such as the reduction of SOI CMOS I-V kink effects and no need for substrate contacts.

Wafers were etched back in a 30% by weight KOH solution set to 80 °C. This process etches the [100] much faster (1 micron per minute) than the [111] wafers [2], which was the reason to bond separate wafers types. The [111] wafer acts as the supporting substrate after the [100] wafer is etched. Timing and visual observation was used as the etch stop method. This process should result in a final silicon layer thickness within tens of microns, which although is nowhere near the accuracy required for 700 Å final silicon layer thickness, it still creates a silicon on insulator structure. To get a more accurate thickness measurement during etch, a laser interferometer setup was used, with the goal of it being able to detect HeNe laser interferometer patterns as the silicon thickness becomes thin enough to be translucent, and that the interference patterns could be used to accurately determine the thickness of the silicon layer so that etch stop could be done at 700 Å.

### III. RESULTS

The bonding experiments were successful for both the SOG and the thermal oxide wafers. Several bonding mechanisms occur, from room temperature contacts to high temperature bonding. Initial contact for bonding was easy, because wafers with oxide on them stick together upon being touched after sliding around while there is still air in between the wafers. Wafers were initially contacted from the center and points were made in a spiral fashion outwards. This provided a central contact point and helps remove the air from the inside out. SEM of a thermally oxidized wafer bond (fig. 1) shows a smooth surface without voids or particles on about 4000 Å of oxide. Current theory has it that voids are consumed during the bonding process at high temperature bonding and that the consumption of the voids also pulls in the wafers together to fix the warp. Bonding temperatures and times could be reduced and still maintain bond strengths, provided there are fewer voids or particles. It was interesting to

note that particle counts were greatly reduced after wafers were thermally oxidized, with the oxidation process acting as a particle removing step. Also, particles didn't affect the bonding for the thermally oxidized wafers. Even with dozens or hundreds of particles on the wafers. (A true particle effect analysis requires electrical characterization, which was not performed.)

The etch results weren't as successful. The main problem was that the interferometry detection was ruined by the bubbles coming out of the wafers surfaces. This prevented measurement of silicon layer thickness until it was completely etched already. Interferometry methods might be used at reduced KOH solution temperatures because of the lower reaction rates reduces the number of bubbles, but that reduces etch rate and throughput. Because endpoint detection or thickness measurements couldn't be made, the etch stop was done through visual detection of tens of microns of silicon remaining (fig. 2). Also, there was significant [111] wafer etching, which made the substrate thinner, and that the surface of the [100] was really rough after the etch. CMP was attempted at smoothing the wafers, but the wafers broke because there were no 2" wafer templates for the CMP machine and 4" wafer templates were attempted instead. Future processing of the wafers also requires a thermal oxidation step after CMP to reduce the damage incurred by the etch process and CMP process. It is also possible to use other forms of wafer thinning, such as a wafer grinder for quick and rough wafer thinning and dry etch for slow but accurate wafer thinning.

### IV. SUMMARY

The project was successful at creating bonded SOI wafers. Two inch wafers were oxidized, bonded, and then etched to create the wafers. More process optimizations need to be done to make the project successful, such as to fix the interferometry detection, adding grinding and CMP polishing, and thermal oxidation damage removal, but the RIT microelectronics facilities are capable of creating device quality bonded SOI wafers.

### ACKNOWLEDGMENTS

The author would like to thank Dr. Santosh Kurinec and Dr. Richard Lane as Faculty Advisors, Gregory Mlynar for running CMP, Shahid Butt for running SEM, and Tom Neal at National Security Agency and Achim Gratz at University of Technology, Dresden, Germany for SOI expert Advice.

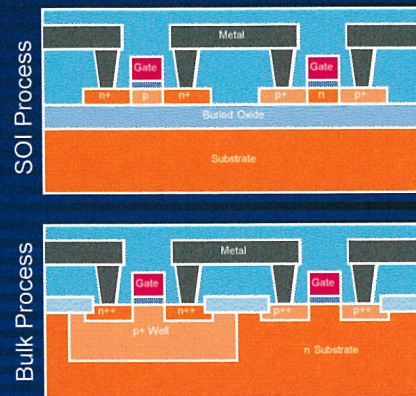
### REFERENCES

- [1] J. B. Latsky, S. R. Stiffler, F. R. White, and J. R. Abernathy, *IEDM Technical Digest*, p. 684 (1985)
- [2] D. L. Kendall and D. R. de Guel, *Micromachining and Micropackaging of Transducers*, p. 107 (1985)
- [3] S. Cristoloveanu and S. S. Li, *Electrical Characterization of Silicon-On-Insulator Materials and Devices*, (1995)

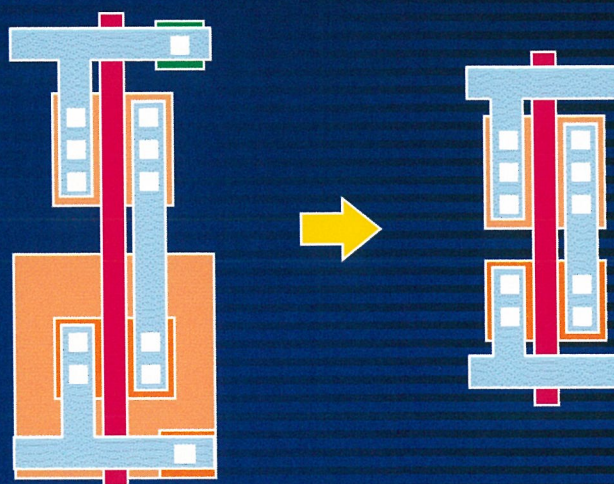
## APPENDIX

## Why SOI?

- ① Simpler Processing
- ② Smaller Devices
- ③ Faster Circuits
- ④ Lower Power
- ⑤ No Latch-up
- ⑥ Radiation Resistant
- ⑦ Fewer Short Channel Effects



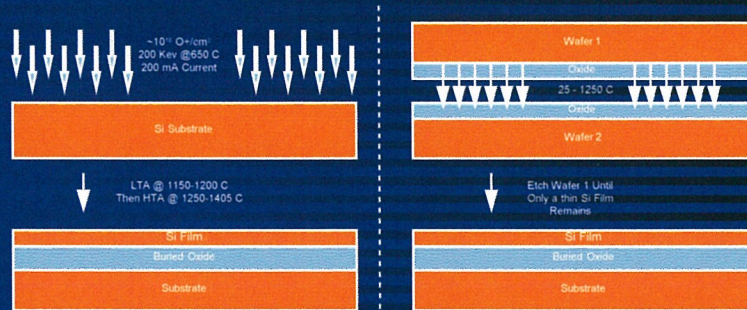
## Bulk vs. SOI Inverter Layout





## How to Create SOI Wafers?

Two Popular Methods are:  
SIMOX and Bonding with Etch-Back



## Future Work: Example Process

