14th Annual Microelectronic Engineering Conference, 1996

Formation of Sidewall Spacers and Titanium Salicide for RIT's Sub-micron CMOS

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Abstract- **Low Temperature Oxide (LTO) sidewall spacers have been successfully fabricated using etchback an technique. The process for forming these features was optimised for repeatability for RIT's sub-micron CMOS. In addition, a reliable process for forming low resistive self aligning titanium silicide was also developed using these sidewall spacers.**

I. Introduction

The fabrication of sub-micron transistors demands the formation of sidewall spacers. As the device length gets smaller, there will be an increase in the lateral electric field caused by the supply voltage. If the electric field is strong enough, it can lead to the formation of *hot-carriers*. Hot-carriers can give rise to a number of problems that can degrade the device performance as it ages.

Sidewall spacer technology can be employed in the formation of lightly doped drain (LDD) and source regions (figure 1). This structure is very effective in reducing the lateral electric field, and as a result it inhibits the formation of hot electrons in n-channel devices

Spacers can further be used for the formation of self aligned silicides (salicides). The reaction only takes place where silicon is present and is limited over silicon di-oxide. Silicides are capable of reducing parasitic series resistances in contacts and in sheet resistance of gate electrode, thereby reducing the gate delay.

II. Process Outline

LPCVD Polysilicon (3500 A) was deposited on silicon wafers with 1000 A SiO_2 on them. The poly was then doped n-type using Allied Signal N-250 spin-on dopant. After pre-deposition, the sheet resistivity averaged at 50 Ω/□. The polysilicon was then patterned using the Exposure Test Matrix (ETM) mask. Polysilicon was etched in the GEC Cell (a reactive ion etcher (RIE)), using SF_6 and O_2 chemistry.

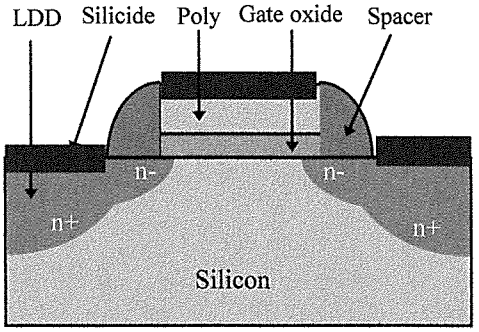

Fig 1. Schematic diagram showing LDD and self aligned silicide.

LPCVD low temperature oxide (LTO at 400°C) was then deposited (6000 A) over the etched polysilicon features followed by LTO densification at 1000°C for 30 minutes. An etchback was then performed using the RIE. The gases used were carbon tetra-fluoride (CF_4, 25 sccm) and hydrogen (5 sccm). The effect of pressure and forward power on the LTO etch rate was investigated, in prior experiment.

The next step involved the sputtering of titanium metal. This was performed in a CVC 601 sputterer, with a magnetron enhanced head. The base pressure in the 10^{-6} torr range, before sputtering. It is necessary to have the chamber water vapour and oxygen free, as these contaminants will affect the final sheet resistivity of the silicide film. Titanium was DC sputtered at 1300 watts for 10 minutes with a pre-sputter time of 15 minutes. The resulting thickness was 1100A.

The sintering was performed using furnace method and rapid thermal processing (RTP). RTP sintering was performed in an AG Associate Heatpulse 410 Rapid Thermal Processor. The silicide formation steps were divided into three steps; 1) first sinter at 700°C, 30 seconds, N_2 gas, 2) removal of unreacted titanium in $NH_4OH:H_2O_2:H_2O$ (1:1:5) mixture, and 3) final sinter at 800°C, 30 seconds, N_2 ambient. The chamber was purged with N_2 for 2 minutes prior to any sintering step.

Four point probe measurements and scanning electron microscopy were used for characterising each step.

III. Results and Discussion

The process for the etchback of LTO forming sidewall spacers was optimised to produce an anisotropic etch. Figure 2 is a cross-sectional SEM micrograph showing sidewall spacers on either side of a 2.4 μm polysilicon line.

Titanium salicide was formed using the rapid thermal sintering, which produced better results than furnace sintering. Furnace sintering resulted in partial oxidation of titanium even in inert ambient. Figure 3 is a cross-sectional SEM photograph is showing a poly line after titanium silicidation process. As the titanium silicide is formed, silicon is consumed. This causes a step height difference which is shown in figure 1 and is also evident in figure 3. Approximately 1 A of titanium consumes about 2.3 A of silicon.

The sheet resistivity was measured after each step using a four point probe. Figure 4 summarises the trend observed. After the first sinter, the sheet resistance did not change dramatically. However, after the second sinter at 800°C, the sheet resistivity dropped to about 3 Ω/□. This depicts the formation of low resistive titanium di-silicide phase. Lower values of final sheet resistivity can be obtained if a very low sputter base pressure is achieved (~10^{-7} torr). The observed trend agrees well with other published materials[1,2].

IV. Summary

A process for forming LTO sidewall spacers was found. The optimised recipe for the GEC Cell is: CF_4 = 25 sccm, H_2 = 5 sccm, 100 mTorr, Power = 60 watts, temperature = 19.2°C.

Low resistive titanium salicide was successfully formed. The three step sinter process is as follows: 1) 700°C, 30 seconds, N_2, 2) Selective etch to remove unreacted titanium in $NH_4OH:H_2O_2:H_2O$ (1:1:5), 3) final sinter at 800°C, 30 seconds, N_2 gas.

Sheet resistivity as low as 3 Ω/□ was obtained. Lower resistivities are possible, provided the contaminant level during sputtering and sintering is kept at a minimum.

Acknowledgements

The author would like to thank Dr. L. Fuller, Head of Microelectronic Engineering, Dr S. Kurinec, S. Blondell, D. Yackoff, C. Reynolds toward their contributions for this research. Extended thanks to M. Maslow for his help with RTP.

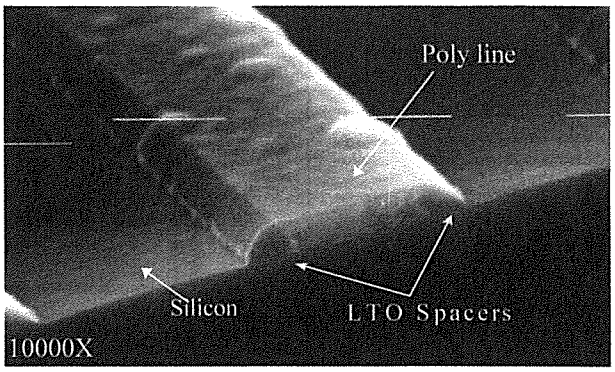

Fig 2. SEM micrograph showing LTO spacers after the etchback.

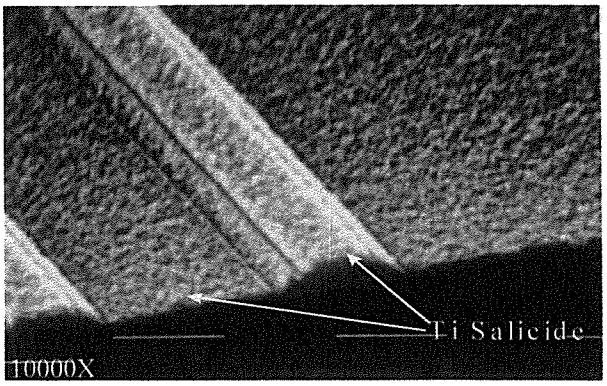

Fig 3. Titanium salicide after the second sinter step.

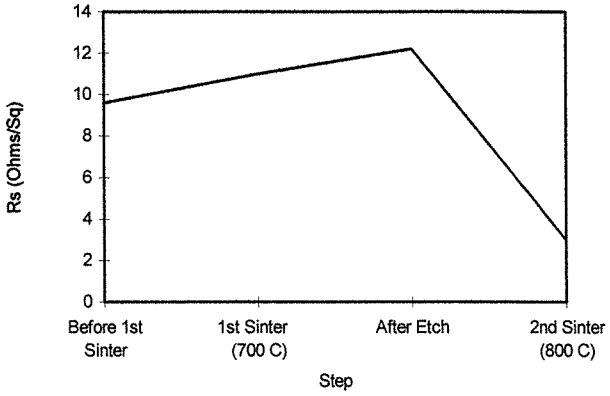

Fig 4. Policide sheet resistivity with processing sequence.

References

1. S. Wolf, "Silicon Processing for the VLSI Era. Volume 2-Process Integration," p. 147-150, 354-361, Lattice Press, 1990.
2. T. L. Huang and S. T. Lee, "Formation and Oxidation of Titanium Silicide," Materials Research Society Symposium Proceedings Vol. 77, p.339-344, 1987 .

APPENDIX

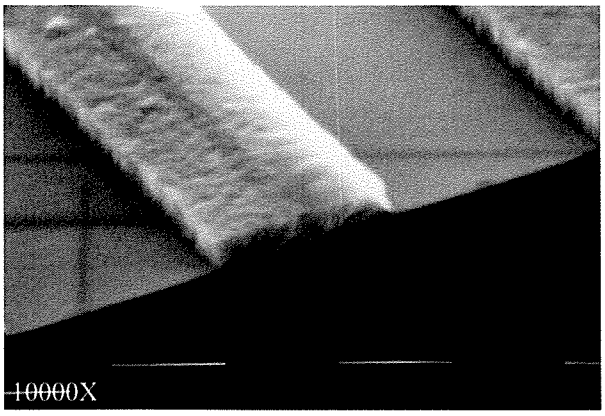

Fig 5. 2.4 μm line after poly etch

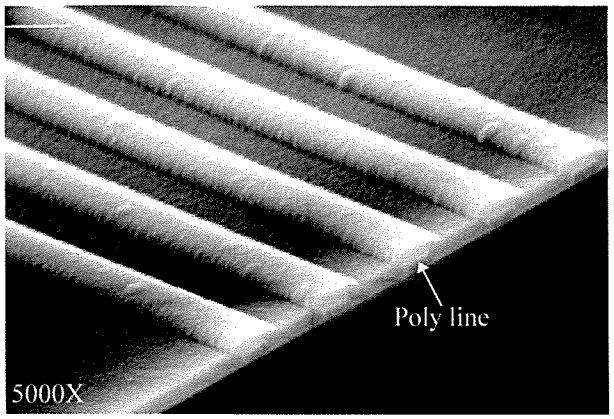

Fig 6. After deposition of LTO

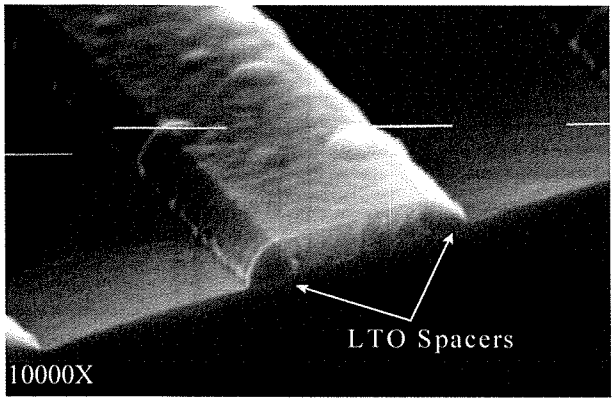

Fig 7. After LTO Etchback

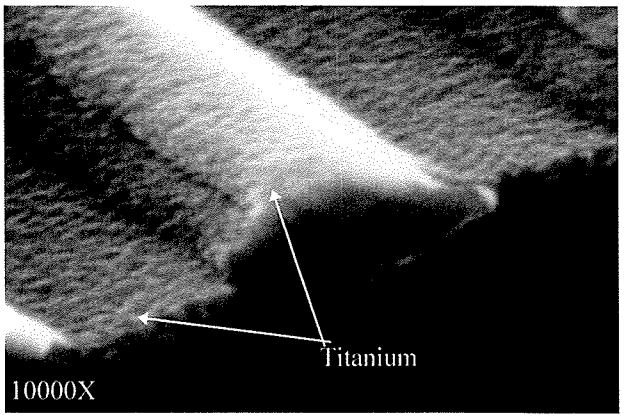

Fig 8. 1.0 μm line after Ti deposition

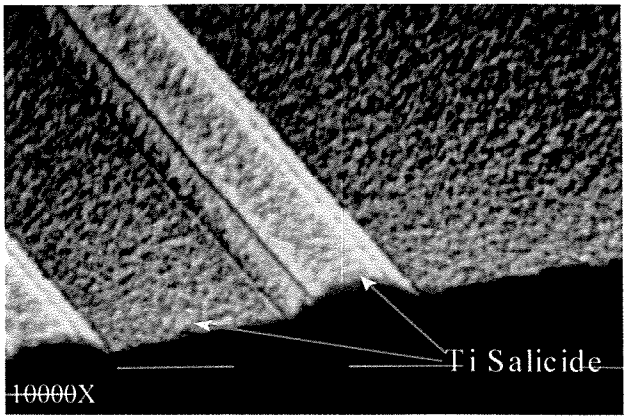

Fig 9. After the second sinter at 800°C