14th Annual Microelectronic Engineer Conference, 1996

Development Of A Polygate PMOS Process Compatible With Micromechanical Sensor Fabrication

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Abstract - **The objective for this study is to develop a device fabrication process that is compatible with the fabrication of on-chip micromachine sensors. It is desirable for the devices to be easily fabricated and to incorporate the least number of additional fabrication steps in the existing procedure of the micromechanical pressure sensor.**

The polysilicon gate PMOS technology was merged into the fabrication of the capacitive pressure sensor with only two additional lithography steps that utilized the same mask. The primary results showed working PMOS transistors with a threshold voltage of -1 V, inverters with gains around 3, and a three stage oscillator with an operating frequency of 6 MHz.

I. Introduction

The capacitive microelectromechanical pressure sensor was designed for measuring the pressures produced in the embryonic chicken heart. The sensor was designed to be small enough to respond quickly to high frequency and insensitive to external stimulations. The capacitive pressure sensor was fabricated using an existing surface micromachine technology. Key fabrication steps include the formation of a stationary bottom plate of phosphorous doped polysilicon, an insulating spacer ring of chemical vapor deposited silicon dioxide to separate the plates, and a top plate composed of a flexible diaphragm of aluminum. Figure I is a cross section of the capacitive sensor.

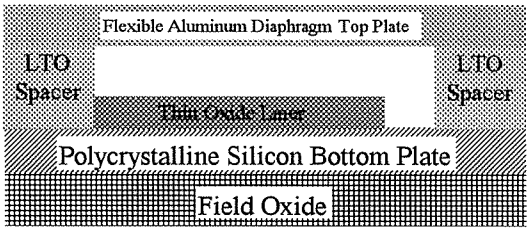

Figure I: Cross Section Of Capacitive Micromechanical Sensor

When a pressure is applied on the flexible diaphragm, the force causes the diaphragm closer to the bottom plate causing the capacitance of the sensor to increase.

The purpose of this project is to develop a device fabrication process that is compatible with the formation of the micromechanical sensor. This would allow an integration of electronic circuitry for amplification and signal process with the sensor component. It is desirable for the devices to be easily fabricated and to incorporate the least number of additional fabrication steps.

Each of the main fabrication technologies were considered as valid candidates for the proposed project. Bipolar junction transistor (BJT) and complimentary metal-oxide-silicon field effect transistor (CMOSFET) technologies were discarded because of

unnecessary process complexity. NMOS was not considered because of the additional process steps of channel stop and threshold voltage adjust implants which are required to fabricate enhancement mode transistors. Metal gate PMOS was also considered but the polysilicon gate PMOS had the additional advantages of having the drain and source implant being self-aligned, and the fabrication technology could be easily incorporated into the existing micromachine procedure. The polygate PMOS process designed required only one additional mask with two extra photolithography steps and the threshold voltage adjust implant is not necessary.

Figure II shows a schematic cross-sectional diagram of a PMOS transistor integrated with the capacitive sensor.

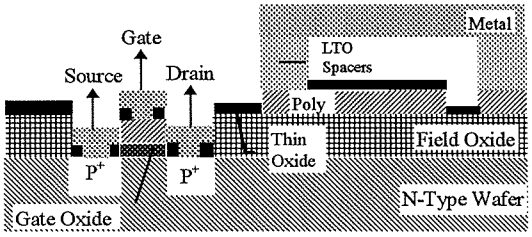

Figure II: Cross-sectional diagram of PMOS transistor integrated with the sensor

The project was divided up into two blocks. The first block was the fabrication of the devices, following the modified polygate PMOS process. The steps that were required for the capacitive sensor were skipped to insure that the process will produce working PMOS devices. The second portion of the project was to fabricate the complete chip, following the modified procedure so the die has the complete package, on board electronics and the pressure sensor.

II. Fabrication Procedure

The following is the fabrication process for the capacitive pressure sensor with on-chip circuitry. Some of the basic steps, like RCA cleans, were omitted for brevity. The additional steps for the integrated circuit fabrication procedure is shown in bold.

1) Wet Oxide Growth
2) **Photo I -- Active regions defined**
3) **Oxide Etch**
4) **Grow Gate Oxide**
5) Polysilicon deposition and doped with phosphorous
6) Photo II -- Bottom plate of sensor and gate formation
7) Polysilicon Etch
8) Low Temperate Oxide Deposited
9) Photo III -- Defines the insulating spacer ring between the two plates
10) Etch Oxide
11) Grow thin Oxide
12) **Photo IV -- PMOS drain and source implant area defined**
13) **PMOS Drain and Source Implant**
14) **Implant Anneal**
15) Photo V -- Contact cuts
16) Photo VI -- Fills spacer ring with photoresist
17) Aluminum Deposition
18) Photo VII -- Metal - top plate of sensor and interconnects define
19) Etch Aluminum
20) Remove photoresist between the two plates
21) **Sinter Contacts**

Appendix I contains the fabrication travel log sheets used for this project. The existing process was only modified by the

addition of seven steps, which include two lithography steps that unitizes the active area mask.

The first portion of the project was completed and tests were made that verified that the modified fabrication procedure can produce working PMOS devices. The second portion of the project was completed and test results did not have the expected outcome.

III. Experimental Results - The devices that were fabricated were transistors, an inverter, and a three stage ring oscillator. Table I contains a summary of the test data for the transistors. Table II contains a summary of the test data for the inverter and Table III is for the ring oscillator. The device characteristic test were performed on a Hewlett Packard 4145 Parameter Analyzer. The ring oscillator measurements were done on a Tecktronics digital storage oscilloscope.

Width	100 μm
Length	10 μm
V_T	-1 V
Sub-threshold Slope	-100 mV/Decade
g_m (Saturation)	0.32 mMhos

Table I: Measured PMOS Transistor Characteristics

V_{IH}	1.75 V
V_{IL}	0.8 V
V_{OH}	3.75 V
V_{OL}	0.6 V
V_{Invert}	1.5 V
NMH	2.0 V
NML	0.2 V
Gain	3

Table II: Measured PMOS Inverter Characteristics

External Capacitance	Frequency	V_{PP}
0	5.7 MHz	82 mV_{PP}
10 pF	453 KHz	150 mV_{PP}
15 pF	393 KHz	200 mV_{PP}
20 pF	341 KHz	250 mV_{PP}

Table III: Measure 3 Stage Ring Oscillator Characteristic

All of the device test measurements were done with a supply voltage (V_{DD}) of -10 V. Appendix II contains typical characteristic waveforms for the devices measured.

The devices that were fabricated along with the capacitive pressure sensor seemed to have poor operating characteristics. An area that is being investigated as a possible cause is the contact cut interface with the device.

IV. Discussion Of Results

The yield of working ring oscillators were below expectations. This could be due to the poor low voltage noise margins (NML) that were measured on the inverters. The ring oscillators that did work showed that their frequency increased with increasing capacitance. This shows that the signal from the micromachine capacitive pressure sensor could be processed and amplified.

The devices that were fabricated along with the capacitor sensor have characteristics that indicate high contact resistance. However, the two sets of devices did not follow the same fabrication procedure as planned. The first set of devices had their drain/sources implanted with BF_2 and the metal was deposited by evaporation. The set of devices that were fabricated

along with the sensor had a B^{11} drain/source implant and their metal was deposited by sputtering. The only other difference was that the wafers with the sensors underwent an acetone bath to remove the photoresist between the two plates. The cause of the poor device characteristics are still being investigated, so a definite reason is not possible to say at this time.

A second area that should be investigated is the formation of a brown film on top of the wafer after the sintering step. The first set of wafers did not form this film, but the second set did. The film was not there or was not noticeable prior to the sintering process.

V. Recommendations

The field oxide should be reduced or other isolation techniques should be considered. The method currently used causes step height on the order of 1 micron. This causes problems in photo and adequate metal coverage. It might be worth the additional process complexity to isolate by using the basic LOCOS process instead of the grow and etch method. Even decreasing the field oxide thickness to 5000 Angstroms would improve the process.

The method of removing the photoresist from between the two plates need some refinements. The last batch of wafers underwent a 36 hour acetone bath, followed by 24 hour isopropyl alcohol (IPA) bath to remove any acetone residue. The IPA was rinsed in a cascade rinser for 30 minutes followed by run in the SRD-1000 rinser/dryer. This process removes the photoresist but the times could be optimized for maximum throughput.

An area of concern is the sputtering of the aluminum. To insure that the steps are adequately covered, the aluminum deposition should be around 1 micron, which requires about 90 minutes sputtering time. Wolf, in his book, Silicon Processing for the VLSI ERA, Volume 2 - Process integration, states the degradation of the gate oxide caused by damage during process steps carried out in a plasma environment (such as sputter deposition of metal) should be minimized. Any modification that could be made to decrease the time required for deposition should improve the device yield and characteristics.

VI. Conclusion

The poly gate PMOS process incorporated into the micromachining of the capacitive pressure sensor produced working devices. This allowed for on-chip signal processing and amplification. This shows that two fabrication technologies can be merged into one so that a micromachine pressure sensor can be integrated with electronic circuitry. As of right now, there are a couple of bugs that still need to be worked out in the overall process, but this project has the potential to aid in the research of the development of the fetal heart.

VII. Acknowledgments

At this time, the author would like to acknowledge the following people: Dr. Lynn Fuller, Department Head, Microelectronic Engineering at Rochester Institute of Technology, Kerstin Babbitt, University of Rochester , and Boahua Zong , Rochester Institute of Technology.

VIII. Reference

[1] Wolf, S. (1990). Silicon Processing For The VLSI Era Volume 2 - Process Integration. Sunset Beach: Lattice Press.