14th Annual Microelectronic Engineering Conference, 1996

Calibration of Process and Electrical Models for RIT Vertical NPN Bipolar Junction Transistors

Lena Zavyalova
Senior Microelectronic Engineering Student
Rochester Institute of Technology, Rochester, NY

Abstract - **Presented study is based on the need in 2D process and device simulations providing a good estimation of in-line process and electrical parameters for RIT vertical NPN bipolar junction transistors. These involve process and electrical modeling adjustments in order to reproduce vertical dopant profiles and show an appropriate electrical behavior of simulated BJTs. Technology Modeling Associates (TMA) software has been implemented to facilitate this task. Theoretical and experimental verification efforts have been performed to examine the validity of the simulation results, and good agreement has been obtained.**

I. Introduction

THE use of computer simulation in the process development has become a widely accepted technique to reduce the high costs and long turn around times of experiments. Our original efforts in this area concentrated on extracting information from the RIT's triple implanted BJT process history. Data on the recently fabricated lots 961205,6&7 containing wafers with successful emitter drive-in splits was used to support the simulation predictions.

The process simulations in 2D were carried out using TMA software package TSUPREM-4 and device simulations were done using TMA's MEDICI simulator program.

Dopant profiles measured by Secondary Ion Mass Spectrometry (SIMS) are especially interesting for the present study as a method of verifying process models.

Figure 1 is a flow-chart representation of the sequence of steps used to verify and calibrate the simulation models.

II. Process Simulations

The correct allocation of grid points was a crucial issue in TSUPREM-4 simulations. A suitable trade-off has been established between tight grid spacing and simulated device area. In order to model a high resolution structure, only an active part of a bipolar transistor has been simulated.

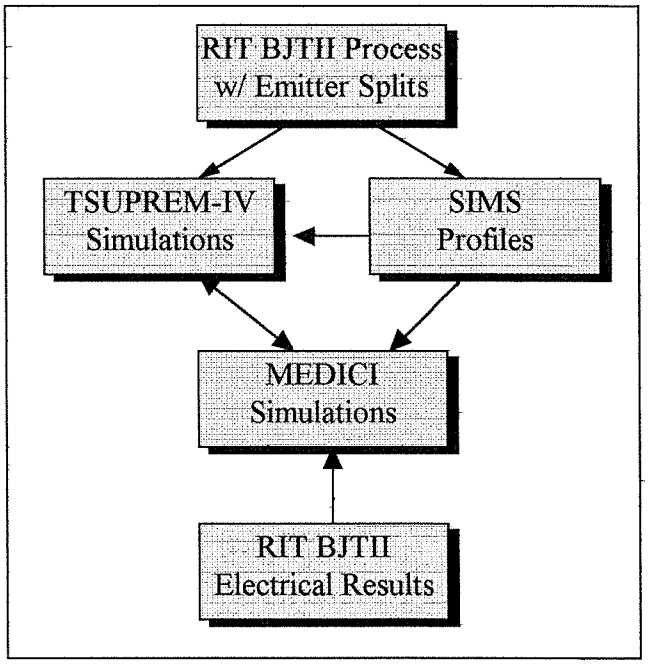


Fig. 1. Models Verification Flowchart

Mathematical models for predicting ion implantation concentration profiles affect the accuracy of the simulation.

For the simulation of ion implantation in two dimensions using analytical expressions very often Pearson-IV distribution is employed. The theoretical profile is characterized by four moments: Rp, ΔRp, skewness, and kurtosis [1].

However, an alternative approach showed itself more suitable for current simulations. Monte Carlo ion implant model has been selected. It is based on numerical solutions rather than on analytical techniques. Ion implantation is simulated by following the history of an energetic ion through successive collision with target atoms. The calculation of each trajectory begins with a given energy, position, and direction. A large number of ions trajectories is calculated and the depth at which each ion stops is determined. The predicted profile is generated by plotting histograms of the number of ions stopped within each interval.

TABLE I
COMPARISON BETWEEN EXPERIMENTAL AND SIMULATED JUNCTION DEPTHS IN A N NPN DEVICE

Emitter	EBj, μm		BCj, μm		Bwidth, μm	
Drive-in	Suprem	SIMS	Suprem	SIMS	Suprem	SIMS
60 min	1.59	1.7	2.32	2.65	0.74	0.95
65 min	1.65	1.9	2.34	2.7	0.69	0.8
70 min	1.71	2	2.37	2.75	0.66	0.75

Finally, the Table I reports the calculated vertical dimensions on the emitter split experiment. The calculated results are compared satisfactorily with preliminary SIMS profiles, suggesting that the overall approach enables correct device modeling (Figure 2).

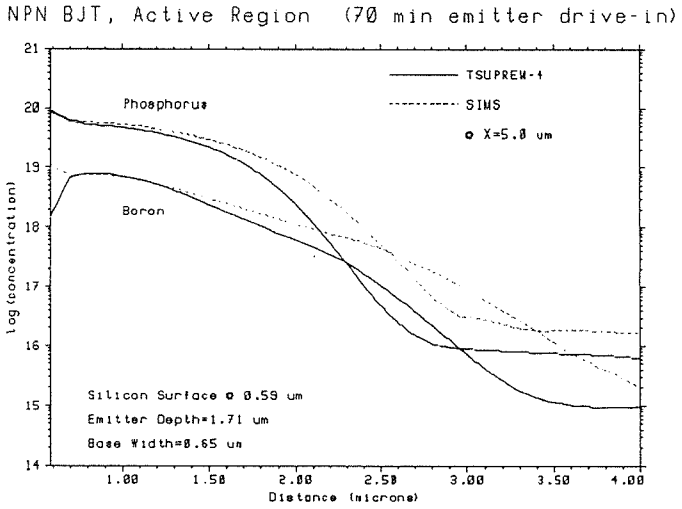


Fig. 2. Illustration of the ability of the TSUPREM-4 model to simulate doping profiles.

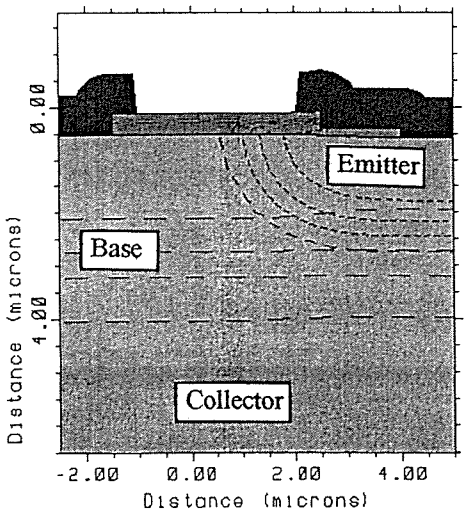
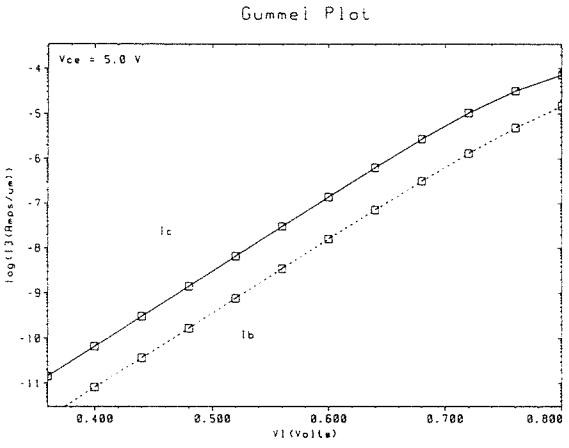


Fig. 3. TSUPREM-4 graphical output representing the final cross section of the simulated BJT structure (active region).

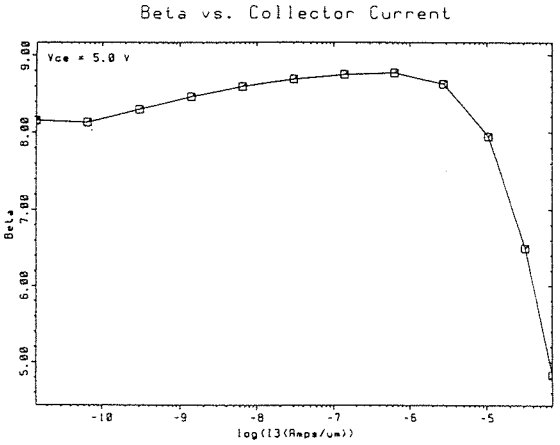
The structure output file is saved in a format that that can be read by TMA's MEDICI device simulation program. The device is truncated at the bottom, electrodes are specified, and collector contact is placed on the backside of a wafer (Figure 3).

III. DEVICE SIMULATIONS

As a consequence, TSUPREM-4 output file information is used as a structure input file to MEDICI for device modeling and parameter extraction. However, the associated output (Figure 4) indicates that later adjustments to electrical simulation data need to be completed. Low gain values (Table II) can be caused by either an error introduced in TSUPREM-4 simulations or an accuracy of the MEDICI model.



(a)



(b)

Fig. 4. MEDICI graphical outputs showing: (a) plot of Ic and Ib versus Vbe; (b) current gain versus collector current.

At this point, it is desired to obtain a solution which can be used as a starting point for a reasonable device behavior simulation. Therefore, the solution obtained most efficiently would be to bring the SIMS profile data directly into MEDICI (Figure 5), which can then eliminate any possible errors generated in the TSUPREM-4 structure, but the accuracy of the structural representation is determined by the accuracy of the SIMS profile measurement.

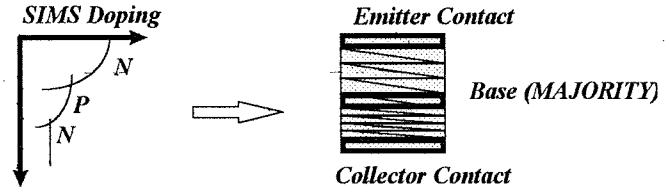


Fig. 5. A one-dimensional bipolar transistor[2].

The initial structure definition consists of a PROFILE statement which is represented by the SIMS data file. A one-dimensional device structure is created in MEDICI using a single column of triangular elements. This produces a structure with two columns of nodes. The resulting structure is not truly one-dimensional since there are two columns of nodes and a true one-dimensional structure would have only a single column of nodes. However, the results of the analysis will be the same as a true 1D analysis as long as there is no variation in the device structure in the direction perpendicular to the column of nodes [2].

The simulation of a bipolar transistor requires that a contact to be made to the base of the transistor. In a 1D simulation this contact is placed across the device within the base of the transistor. A normal electrical contact cannot be used since it would force the electron and hole concentrations to their equilibrium values with the result that no current could cross the base of the transistor from the emitter to the collector. Instead, a *majority* carrier contact is used for the base contact. It only sets the quasi-Fermi potential of the majority carrier to the contact potential. The result is that only majority carriers can leave the base via contact [2].

TABLE II
BETA VALUES FOR VARIOUS EMITTER DRIVE-IN TIMES

Emitter Drive-in Time	Simulated		Measured
	SUPREM Structure	SIMS Structure	
60 min	5.21	13	130
65 min	5.26	16.7	273
70 min	8.8	8.1	377

Currently, the MEDICI program uses following physical models: Shockley-Read-Hall recombination with concentration dependent lifetimes, Auger recombination, band-gap narrowing. Also, the mobility tables are used to model the dependence of carrier mobility on impurity concentration.

Unfortunately, the simulated current gain values remain low for the real doping profiles (Table II). This implies that the simulated profiles agree well with experimental data. However, the MEDICI model does not give accurate results. Various physical mechanisms and models which describe the simulation results in MEDICI are subjects of future work.

IV. CONCLUSION

A reasonable agreement is found on the complete range of emitter drive-in times in process simulations. Although, device simulations are generally pessimistic for all of the emitter splits, they do provide a validation of the proposed process simulation approach.

One of the main conclusions is that SIMS show an improved RIT BJTII process capability.

V. ACKNOWLEDGMENT

The author thanks Dr. R. Pearson, Karl D. Hirschman, Dr. L. Fuller, Frank Casilio, Dr. Santosh Kurinec for their suggestions, discussion and encouragement. Special thanks to Greg Fitzgibbon, IBM Analytical Services, for performing SIMS measurements.

REFERENCES

[1] S. Wolf, " Silicon Processing for the VLSI Era, vol.2. Sunset Beach: Lattice Press, 1990.
[2] Technology Modeling Associates, Inc., Palo Alto, CA.