FABRICATION OF A THREE-PHASE DOUBLE POLYSILICON CHARGE COUPLED DEVICES

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Abstract- **Charge-coupled devices were fabricated using the existing seven level mask design (Scott Kipperman). Previous attempts at RIT (Scott Kipperman, Michael McGranahan) to fabricate working CCD's have not been successful, perhaps due to time constraints and misprocessed lots. Devices were completed using the current CCD process, while overcoming previous process problems. Results include testing of poly1 and poly2 transistors, and an attempt to test a one-dimensional 8-pixel array electrically. Equivalent capacitors were built, the threshold voltages obtained were 6.85V and 6.62V, respectively. The 8-pixel array was shown to be light sensitive, and conduct current as all three phases were pulsed high. Extensive testing of the one-dimensional arrays, both by electrical injection and photoelectrical generation of minority carriers, still needs to be explored further.**

I. INTRODUCTION

Charge-coupled devices have been used in a broad range of applications since their invention in 1969. Some of these include hand-held cameras, digital cameras, signal processing, memory, and astronomy. Not only are charge-coupled devices practical in many applications, but they are also fairly simple to fabricate.

A charge-coupled device works much like a shift register of MOS capacitors. When using a p-type substrate, for NMOS transistors, a large positive potential is applied to the gate and the capacitor goes into deep depletion. With added minority carrier injection, a potential well is formed, and charge is stored. As a series of capacitors in a linear array is pulsed by different voltages, or phases, the minority carriers 'fill' up into the potential wells of the coupled devices. This is demonstrated in Figure 1. The three-phase clocking waveforms can be seen in Figure 2. Before time T1, the electrical input is pulsed at a high voltage to inject minority carriers through a forward-biased junction into the potential well of the first capacitor, which is already under deep depletion. At time T1, the charge stored under the first capacitor is shared with the second capacitor, as its gate voltage also goes high. At time T2, the high voltage is removed from the first capacitor, while being kept on the second capacitor, so the entire charge packet is transferred under the second capacitor. The minority carriers are shifted down the CCD in this manner. The output voltage is sensed through a forward biased diode.

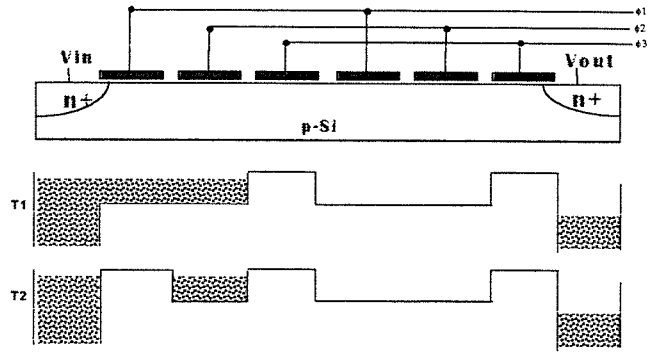

Figure 1. Electrical injection in a charge-coupled device

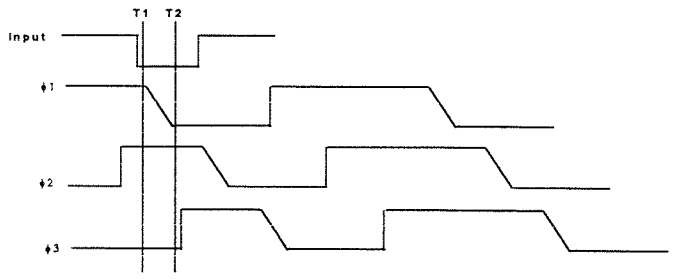

Figure 2. Three-phase clocking scheme with electrical input signal

Another way of generating minority carriers is photoelectrically. Light passes to the silicon substrate, through the transparent gate(polysilicon) and generates an electron-hole pair. If the gate is correctly biased, the minority carriers will be stored under it. Similar to the electrically injected case, the minority carriers will be shifted down the CCD array, and sensed through an output diode.

There are two mechanisms under which the minority carriers transport under the gates; drift and diffusion. The transport is largely due to drift. What determines how much charge is transferred from input to output is the transfer efficiency. With one being an ideal value of transfer efficiency, a satisfactory value could be 0.999. For modern day devices, however, the transfer efficiency needs to be large enough to make several thousand transfers between input and output.[1]

II. Device Structure And Fabrication

The mask set includes a 64x64 pixel array, as well as one-dimensional linear arrays. There are 8-pixel and 4-pixel one-dimensional devices; some contain a channel stop surrounding the device. The channel stop implant confines the charge within a region under the polysilicon gates, to get good charge transfer efficiency. The channel stop can be used to bias the substrate while testing. The one-dimensional devices include poly gates of 20x60μm; the array contains gates of 14x26μm. The linear arrays contain input and output diodes, in order to electrically test the CCD; they were also tested with light.

Implementation of the CCD fabrication process (designed by Scott Kipperman) was modified as needed. Four device and six control wafers were used. Two device and one control wafer received an initial threshold adjust implant of B11(5e13cm-2); from SUPREM simulations, a threshold voltage of ~8.4 Volts was obtained. The threshold adjust was large for two reasons: to ensure the devices would not be depletion mode, and to compensate for the depletion of Boron concentration at the silicon-oxide interface when the following oxides are grown. A field oxide was grown in a wet O2 ambient at 1100°C for 45 minutes, which also annealed the threshold adjust implant. Next, the field oxide was patterned and etched; this defines where the channel stop is implanted. The channel stop, Boron, was implanted at 50keV, with a dose of 5e14cm-2. A blocking oxide was grown to anneal the p-implant, and mask the subsequent n-implant. This was done at 1100°C in dry O2 for 30 minutes, the thickness was 900Å. The oxide was patterned and etched; it defines where the input/output diodes will be. Phosphorous was implanted at a dose of 5e15cm-2, with an energy of 75keV. Mask Level 3 defined the region for the gate oxide, and then field oxide was etched before the gate oxide growth. A TCA was done in the furnace tube before growing the gate oxide. The gate oxide was grown at 1050°C in dry O2 for 90 minutes; the desired thickness was 1000Å. The average thickness obtained was 1360Å. An SCA analysis of a control wafer was performed to monitor the trapped charges (Qox') in the gate oxide. The thick gate oxide was to ensure that the spin-on phosphorous dopant would not diffuse through the gate. Next, the first polysilicon layer was deposited in the LPCVD furnace, desired thickness was 2500Å. The range of poly thicknesses was between 2400Å and 3000Å. The polysilicon was doped with an Arsenic spin-on dopant source, N250, and this was annealed in N2/O2 at 1000°C. A piece of quartz was also put in the tube to see the transparency of the polysilicon at the desired thickness. A low thickness of poly was desired so light would be able to pass through the gate and generate electron-hole pairs in the silicon. The transmission of polysilicon was measured from a quartz sample deposited with poly. The poly was patterned and etched in the GEC Plasma Cell to define the gates. The remaining gate oxide was etched, and a second gate oxide was grown. As before, a TCA was performed on the furnace to clean it, and the oxide was grown in 1050°C in dry O2 for 90 minutes; the average thickness obtained was 1060Å. An SCA analysis of a control wafer was performed to monitor the trapped charges

(Qox') in the gate oxide. A second polysilicon layer was then deposited, with the same desired thickness as with poly1. The range of poly thicknesses was between 2400Å and 3000Å. The poly was doped with N250, in the same manner as before. Poly2 was patterned and plasma etched to define the gates. A low temperature oxide of 5000Å was deposited in the LPCVD furnace to act as the passivation layer. This was densified at 900°C for 30 minutes. The LTO was patterned with Mask Level 6, to define the contact cut openings. The oxide was then etched; this was critical in etching down to bare silicon, so the aluminum makes good contact. The aluminum was sputtered in the CVC Sputterer 601 at a target thickness of 9000Å. Then the aluminum was patterned and etched. Testing was performed on the device wafers. A cross-section of the final device can be seen in Figure 3.

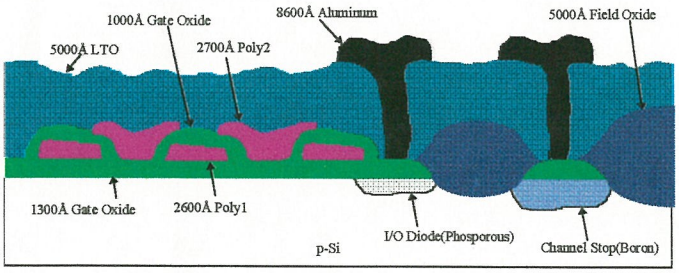

Figure 3. Cross-section of a portion of a linear array

III. Results and Discussion

During the fabrication of the devices, control wafers were used to monitor certain processes, to ensure that no major failures would occur in the final devices. Including these tests were measuring poly sheet resistance, measuring the transmission of polysilicon at 2600Å, and performing surface charge analysis of the gate oxides. The measured poly sheet resistance, after doping, was ~29Ω/sq.; this is a typical value. Obtained from the SCA analysis, done on the Semitest Surface Charge Analyzer, was values of Q'ox, the total charges contained in the oxide. In the RIT factory, a typical value of Q'ox might be in the range of 1e11 to 1e12, in industry, the value might be 1e10. For the first gate oxide, values of Q'ox ranged from 1.49e11 to 2.14e11, and for the second gate oxide, the range was 1.5e11 to 1.85e11. The same control wafer was used for both SCA analyses for consistency in measurements.

For a charge-coupled device to work, light has to be able to pass through the gates. The polysilicon transparency (transmission) was measured from a quartz sample in a spectrophotometer. The transmission was plotted (Figure 4), and with reflectance measurements as well, the coefficient k of the film could be calculated. Using the equation, $T=\exp(-4\cdot\pi\cdot k\cdot t)/\lambda$, where t=thickness of film, λ=wavelength, T=transmission, the actual transmittance of the poly could be found at a given wavelength. This is also shown in Figure 4 (labeled "True" T). Found from this plot is that at longer wavelengths, 700nm and greater, 2600Å polysilicon is completely transparent. Therefore, the fabricated CCD's would be sensitive to long wavelengths(red), but not short (blue).

The transistors tested, both poly1 and poly2, had expected threshold voltages; they were close to what SUPREM simulated. They also demonstrated proper transistor characteristics, family of curves. The sheet resistance obtained from the poly VanderPauws were lower than that of the control wafers; the range of values was 3 to 10Ω/sq.

The 8-pixel one-dimensional array, with an applied electrical signal, was shown to conduct current. When all the capacitors were put at a high voltage, current was detected at the output diode. Since the input and output diodes act as a source and drain of a transistor, the CCD linear array was shown to act as a transistor. Also, the linear array demonstrated a sensitivity to light, the output voltage shifted with the turning off and on of the microscope light. However, the output of the array wasn't expected, the delay between input and output was shorter than predicted. What was found was that the actual design was incorrect at the channel stop mask level. The channel stop implant should be placed so that part of it comes under the electrodes(gates), rather than leaving a space between poly gates and the channel stop region, as

in the current design. One of the main functions of the channel stop region(or P-barrier) is to confine the channel, which is minority carriers. If the channel doesn't come directly underneath the carriers, leakage may occur in the direction perpendicular to way the current is supposed to flow. This would cause a tremendous decrease in output voltage, and obtain very poor transfer efficiency. The channel stop design could be a possibility for why the linear CCD didn't perform as expected.

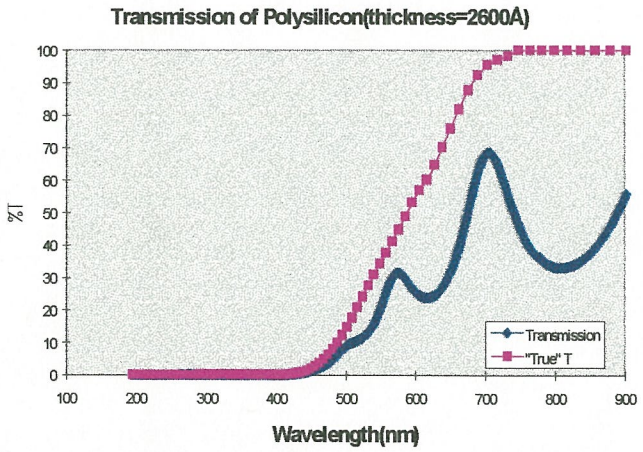

Figure 4. Transmission of polysilicon measured from quartz

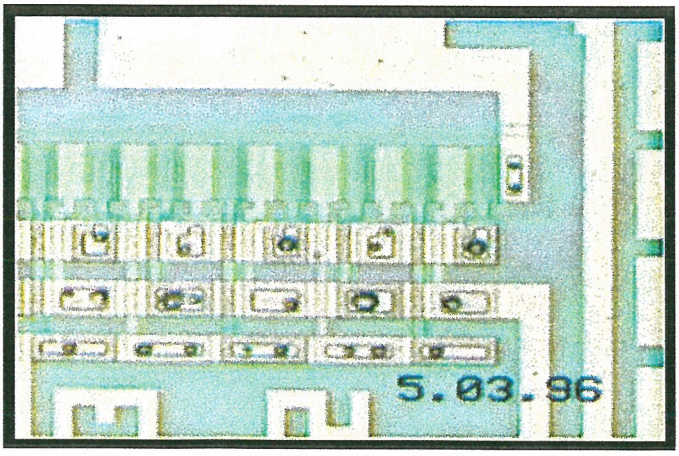

Figure 5. Completed 8-pixel linear array

IV. Conclusion

Charge-coupled devices were fabricated in the RIT factory. Working test structures include transistors and VanderPauws. An 8-pixel linear array CCD which was tested was shown to act as a transistor, but not ideally as a CCD. The design needs to be refined to bring the channel stop region under the electrodes.

Acknowledgments

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