

# DESIGN AND FABRICATION OF A LATERAL BIPOLAR PNP TRANSISTOR COMPATIBLE WITH RIT'S DOUBLE DIFFUSED PROCESS

James A. Will II  
Senior Microelectronic Engineering Student  
Rochester Institute of Technology

## ABSTRACT

A chip was designed containing lateral bipolar PNP devices with base widths ranging from four to ten microns. Vertical NPN devices were included in the designs. The transistors were fabricated using a double diffused process employing solid sources. Two different boron collector/emitter predepositions were performed in order to study the effects of the p-type diffusion sheet resistance on both lateral PNP and vertical NPN devices. Testing of the lateral PNP devices shows very small Early voltages for the five and six micron designs, while the four micron design exhibits punchthrough.

## INTRODUCTION

The standard process for the fabrication of a vertical NPN device, shown in Figure 1, begins on a P type substrate. The substrate is implanted with an N type dopant such as arsenic in areas where the NPN devices will be fabricated. This implant is referred to as a "buried layer", as the next step is an epitaxial growth of N type silicon. The sheet resistance of the buried layer is held much lower than that of the epitaxial layer. An isolation diffusion is performed with a P type dopant such as boron. This creates electrically isolated "islands" of N type material surrounded by the P type isolation. It is these N type areas which serve as the collector for the lateral NPN device. Directly underneath these areas will lie the buried layer previously discussed. The buried layer serves to reduce the collector resistance by creating a low resistance path for current flow. This is needed to produce desired electrical device characteristics. Into the N type island is diffused a P type boron base. The emitter is formed when an N type dopant such as phosphorous is diffused into the base. The vertical NPN structure is now evident.

Lateral PNP devices may be fabricated using the previously mentioned process. The boron base diffusion is utilized to form the P type collector and emitter. The epitaxial layer serves as the N type base. The phosphorous emitter diffusion will serve to form an ohmic contact to the N type base. The N type buried layer is not utilized. This is because the desired base of any

bipolar structure requires that the sheet resistance be sufficiently high. The N type buried layer may reduce the sheet resistance in the N type base, especially if the epitaxial layer is not very thick. Figure 2 represents a cross-section of a typical lateral PNP device.

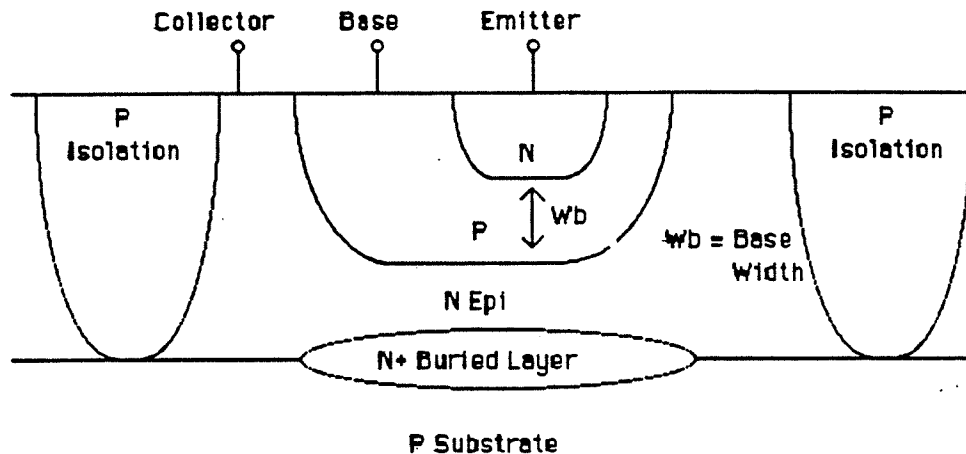


Figure 1: Cross-section of typical vertical NPN transistor.

Control of the transistor gain is critical in bipolar fabrication. The gain is related to the base width and doping of the emitter, collector, and base. The transistor gain will increase for decreasing base width and constant base doping. Thus, by controlling the base width, a desired gain may be achieved for a given base doping.

In vertical NPN fabrication, the emitter drive is what determines the base width and is the critical step in the process. A longer drive produces a narrower base width which leads to higher gain. If the emitter drive is too long the emitter will diffuse through the base and into the collector producing punchthrough, or is a short between emitter and collector. The I-V characteristics exhibited by punchthrough are very similar to those of a resistor.

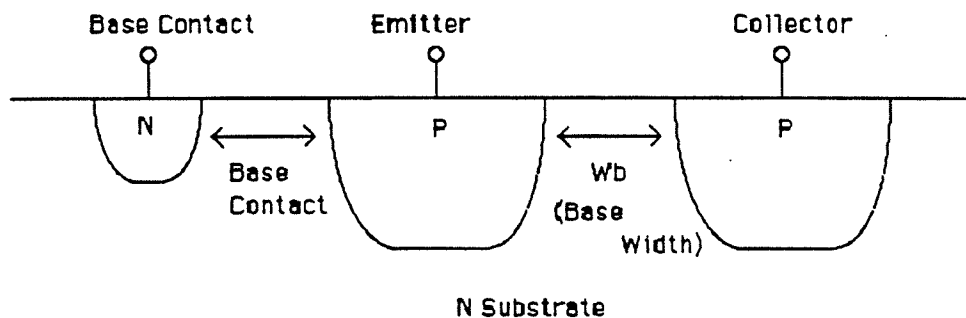


Figure 2: Cross-section of typical lateral PNP transistor.

The double diffused process at RIT is modified to lessen the fabrication time. The N buried layer and N epitaxial layer are omitted and replaced by an N type substrate. Isolation of the devices is not possible. Solid sources are utilized for both boron and phosphorous diffusions. The substrate serves as the base for the lateral PNP and the collector for the vertical NPN devices. Figure 3 represents a typical vertical NPN and lateral PNP device fabricated at RIT. Four masking levels exist: Base (P type diffusion), Emitter (N type diffusion), Contact Cut, and Metallization. The names correspond to the vertical NPN fabrication. The base serves as the P type collector/emitter for the lateral PNP device. Masking oxides are needed for both diffusions and the contact cut. The drive for the base serves as the masking step for the emitter while the emitter drive serves as the masking step for the contact cuts.

The double diffused process at RIT has progressed to a level where vertical NPN devices can be fabricated routinely with good electrical characteristics. The critical step in controlling gain on lateral PNP transistors fabricated using the same process is the mask spacing. Previous lateral PNP designs at RIT were completed using ten micron design rules. Accounting for the lateral diffusion, actual base widths were on the order of six to eight microns. This is very large and measured gains were no better than ten. Fabrication of such devices in industry targets lateral PNP base widths of one micron or less. The design, fabrication, and testing of lateral PNP transistors are the subjects of this paper.

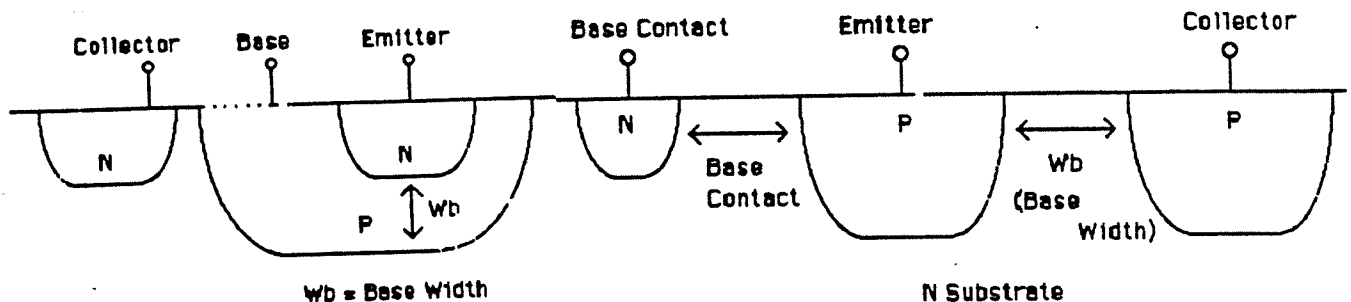


Figure 3: Vertical NPN and lateral PNP devices at RIT.

## EXPERIMENT

A chip was designed containing lateral PNP devices with base widths ranging from 4-10 $\mu$ m. The N<sup>+</sup> base contact, which is wrapped around the device, was designed at both 5-10 $\mu$ m spacings from the collector. Vertical NPN designs were included in the designs to act as monitors to verify acceptable gain. Van Der Pau structures were included on chip for sheet resistance testing.

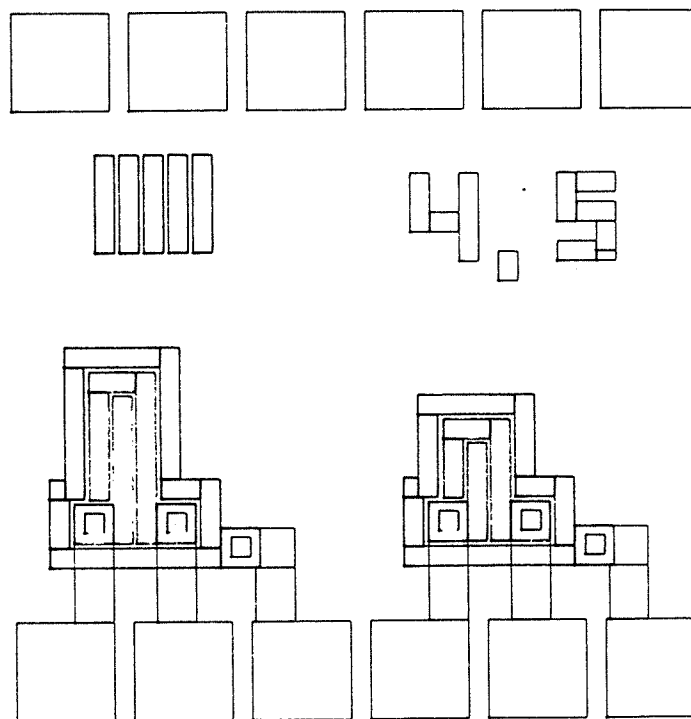


Figure 4: Sample layout containing four micron base width and 5 micron base contact wrap.

Ten N type ,<111>, 5-15 ohm-cm were scribed, RCA cleaned, and oxidized at 1100 C for 35 minutes in wet O<sub>2</sub>. The first mask was completed using the pattern generator and repeater. Lithography was completed using KT1820 resist coated on a GCA wafertrac and exposed with a Kasper contact aligner. The oxide was patterned and the resist stripped in a Tegal O<sub>2</sub> plasma. The P-type boron predeposition was completed using Carborundum BN975 solid sources with the wafers split into two groups. One group was predeposited for 30 minutes, while the other saw 40 minutes, both at 975C. The boron drive was done at 1050C with 30 minutes of N<sub>2</sub> and 30 minutes of wet O<sub>2</sub>. Second level lithography was completed for the N-type phosphorous predeposition. The N-type phosphorous predeposition was completed using Carborundum PH1025 solid sources at 1000C for 15 minutes. The drive was done at 1000C for 20 minutes in wet O<sub>2</sub>. Contact lithography, oxide etch, and resist strip were completed. Aluminum deposition was done in the evaporator. Hot phosphoric acid was used as the aluminum etchant. The resist was stripped and sinter completed at 450 C for 20 minutes in forming gas. Testing was completed on the HP4145 parameter analyzer.

## RESULTS/DISCUSSION

Process data is located in Table 1. The 10 minute difference in boron predeposition time resulted in a 56 ohm/sq difference in sheet resistance for the lateral PNP collector/emitter. Assuming that the base lateral diffusion is roughly 75 percent of the final junction depth, the total lateral diffusion from collector to emitter is 4.05 microns. This produced punchthrough on the devices designed with a four micron base width which was evident in testing. The base width of the five micron designs is less than one micron.

First Masking Oxide:  $T_{ox}=2963 \text{ \AA}$   
 Boron Predep #1:  $P_s=55.6 \text{ o/sq}$   $X_j=0.3 \text{ microns}$   
                   #2:  $P_s=35.5 \text{ o/sq}$   $X_j=0.3 \text{ microns}$   
 Boron Drive #1:  $T_{ox}=2785 \text{ \AA}$   $P_s=148.2 \text{ o/sq}$   $X_j=2.1 \text{ microns}$   
                   #2:  $T_{ox}=2932 \text{ \AA}$   $P_s=98.8 \text{ o/sq}$   $X_j=2.4 \text{ microns}$   
 Phos Predep :  $P_s=6.21 \text{ \AA}$   $X_j=0.6 \text{ microns}$  (substrate control)  
 Phos Drive #1:  $P_s=6.48 \text{ o/sq}$   $X_{jn}=1.5 \text{ microns}$   $X_{jp}=2.7 \text{ microns}$   
                   #2:  $P_s=6.99 \text{ o/sq}$   $X_{jn}=1.5 \text{ microns}$   $X_{jp}=2.7 \text{ microns}$

Table 1: Process data.

P Collector/Emitter Drive #1 $P_s = 148.2 \text{ \AA/D}$			
Base Width, Contact ( $\mu\text{m}$ )	Gain	Early V.	Characteristic
5 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	N.A.	50.8 mV	Terrible
6 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	3.78	2.10 V	Poor
7 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	2.98	5.48 V	O.K.
8 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	2.48	7.96 V	O.K. / Good
9 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	1.72	10.2 V	Good
10 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	1.78	12.2 V	Good
Test NPN	400	-100 V	Good
Base Width, Contact ( $\mu\text{m}$ )	Gain	Early V.	Characteristic
5 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	N.A.	51.7 mV	Terrible
6 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	3.40	1.32 V	Poor
7 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	3.07	5.21 V	O.K.
8 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	2.32	9.14 V	O.K.
9 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	1.82	11.4 V	Good
10 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	1.75	12.5 V	Good

Collector - Emitter Breakdown

V <sub>ceo</sub>		
Base Width	Long	Short
5 $\mu\text{m}$	-0	-0
6 $\mu\text{m}$	-5.10 V	-4.40 V
7 $\mu\text{m}$	-6.02 V	-7.22 V
8 $\mu\text{m}$	-6.81 V	-6.89 V
9 $\mu\text{m}$	-7.73 V	-6.94 V
10 $\mu\text{m}$	-7.72 V	-7.65 V

Table 2: Testing data for P-type drive #1.

P Collector/Emitter Drive #2 $P_s = 98.8 \text{ \AA/D}$			
Base Width, Contact ( $\mu\text{m}$ )	Gain	Early V.	Characteristic
5 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	N.A.	64.1 mV	Terrible
6 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	3.85	1.70 V	Poor
7 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	2.70	5.61 V	O.K.
8 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	2.22	7.02 V	O.K.
9 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	1.73	11.1 V	Good
10 $\mu\text{m}$ , 10 $\mu\text{m}$ Long	1.76	13.3 V	Good
Test NPN	38.8	-158 V	Good
Base Width, Contact ( $\mu\text{m}$ )	Gain	Early V.	Characteristic
5 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	N.A.	37.3 mV	Terrible
6 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	3.82	1.446 V	Poor
7 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	3.31	4.93 V	O.K.
8 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	2.69	8.38 V	O.K.
9 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	1.77	11.3 V	Good
10 $\mu\text{m}$ , 5 $\mu\text{m}$ Long	1.83	12.6 V	Good

Collector - Emitter Breakdown

V <sub>ceo</sub>		
Base Width	Long	Short
5 $\mu\text{m}$	-0	-0
6 $\mu\text{m}$	-4.24 V	-2.70 V
7 $\mu\text{m}$	-7.27 V	-7.99 V
8 $\mu\text{m}$	-12.0 V	-11.5 V
9 $\mu\text{m}$	-13.1 V	-12.8 V
10 $\mu\text{m}$	-12.8 V	-13.0 V

Table 3: Testing data for P-type drive #2.

Table 2 represents the testing results obtained from the devices created with the 30 minute P-type boron predeposition (Drive 1). Table 3 represents the results obtained from the 40 minute P-type boron predeposition (Drive 2).

As previously mentioned, the lateral diffusion from the P-type collector/emitter was sufficient to produce a short across the base in the four micron base width designed devices. The five micron base width designs were nearly shorted across the base, thus gain measurements could not be obtained from these two devices. The six micron base width devices had gains less than four. The gain did decrease as the designed base width increased with the ten micron base width devices possessing the lowest gain.

The Early voltages for the smaller base width devices were very poor. This was the result of the base width modulation created by the depletion region between the collector/base P-N junction. The collector to emitter breakdown voltages were also poor for the narrow base width designs. This also results from the same effect. The C-E breakdown did increase with increasing

designed base width as expected. The C-E breakdown voltage was higher for the devices created with the lower collector/emitter sheet resistance (Drive 2). This was because the built in potential across the collector-base junction was larger (for Drive 2) which in turn produced a larger depletion region. Thus there was a smaller base distance to break down.

The base contact wrap distance on the lateral PNP devices did not make a difference on device characteristics. This might play a role when the base doping is optimized. The vertical NPN devices had a higher gain for P-type drive 1 because of the higher sheet resistance. A higher sheet resistance in the base of these devices will produce a higher gain when the base width is kept constant. The vertical NPN gain produced by both drives was respectable.

In future processing the lateral PNP devices would operate more efficiently if they were fabricated using a lower sheet resistance base. This may be accomplished by using a lower resistivity substrate or by building the devices in a Nwell such as that used in RIT's CMOS process. The Nwell doping could be optimized, thus both the base and collector/emitter sheet resistance could be controlled by process variations. Optimization of the base and collector/emitter may be accomplished through the use of a two dimensional process simulator such as SUPREM 4. The two dimensional simulator could simulate the lateral diffusion distances and depletion region across the C-B junction.

## CONCLUSIONS

Lateral PNP bipolar transistors were fabricated having designed base widths which varied between four and ten microns. The base contact distance was designed at five and ten microns. Two sheet resistances were created for the P-type collector emitter. Gain was not improved on the lateral devices. This was because the doping of the base was too low thus producing large modulations and poor characteristics. Future lateral PNP fabrication should be done in an N-well or on a lower resistivity substrate and simulated on SUPREM 4.

## ACKNOWLEDGMENTS

I would like to thank Mike Jackson, Dr. Fuller, Rob Pearson, and Scott Blondell for their assistance on the lateral PNP project.