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A Thesis Submitted
In Partial Fulfillment
of the Requirements for the Degree of
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in
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RIT | Kate Gleason College of Engineering

Department of Electrical and Microelectronic Engineering

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ABSTRACT

In this work, an empirical off-state model was developed for amorphous IGZO TFTs with the purpose of creating a compact model in conjunction with an existing on-state model. The implementation of the compact model was done in Verilog-A to assess the impact of parasitc elements such as source/drain series resistance, and source/drain-to-gate overlap capacitances in a 2T1C pixel circuit. A novel region of operation was presented defined as a bridge between the subthreshold and the on-state regions. Two approaches were followed to solve for the fitting parameters inside this bridge region; an analytical and an empirical approach.

The analytical solution provided the insight that there is a point where the derivatives of the on-state and the bridge region are equal. However, this solution showed non-physical behavior at some V_{DS} bias. Therefore, an empirical approach was followed where experimental data was used to find the V_{DS} dependence and eliminate the non-physical behavior. Ultimately, the compact model provided a remarkable R^2 in relation to experimental data and allowed for convergence during circuit simulation.

The parasitic element assessment was carried out and two different phenomenon were described as they relate to these elements. Charge sharing and rise and fall time were the characteristics that were present with the introduction of parasitic elements. A capacitance ratio of $\frac{C_{ST}}{C_{ov}} = \frac{10.6pF}{265.07fF} \approx 40$ was used to diminish the former. However, the large capacitances associated in the input of the driver transistor caused the falling transient to be unable to provide full voltage swing. Therefore, proper circuit functionality was not achieved based on the presented design rules. Further work is being done to diminish overlap capacitances such as self-aligned devices.

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Term	Description	Units
μ_0	Field-independent free carrier mobility	$\frac{cm^2}{V \cdot s}$
C_{ox}	Gate oxide capacitance per unit area	$\frac{F}{cm^2}$
W	Channel width	μm
L	Channel length	μm
V_T	Threshold voltage	V
λ	Channel length modulation term	V^{-1}
SS	Subthreshold swing	$\frac{mV}{dec}$
V_{GS}	Gate-to-source voltage	V
V_{DS}	Drain-to-source voltage	V
$V_{DS_{SAT}}$	Boundary condition for the linear-to-saturation transition	V
$I_{DS_{LIN}}$	Drain-to-source current in the triode region of operation	A
$I_{DS_{SAT}}$	Drain-to-source current in the saturation region of operation	A
α_{SCE}	Short-channel effect coefficient. Adapted from SPICE level 2 model.	NA
η_G	Gate-impressed free charge ratio. Gate bias influence of band-tail states on the free charge that is available in the channel	NA
η_D	Drain-impressed free charge ratio. Drain bias influence of band-tail states on the free charge that is available in the channel	NA
θ_{BTS}	Fitting parameter that models the contribution of band-tail states trapping of free charge while the gate-to-source voltage increases	V^{-1}
Z	Fitting parameter that models the contribution of band-tail states trapping of free charge while the gate-to-source voltage is zero.	NA
V_{BTS}	Fitting parameter that models the contribution of band-tail states de-trapping of free charge as the drain-to-source voltage increases	V
V_{ON}	Boundary between the bridge region and the on-state model. Defined when the transconductance becomes unrealistically high.	V

V_{OFF}	Boundary between the subthreshold model and the bridge region. Defined when the relationship between the current and the gate-to-source voltage is no longer exponential	V
A	Fitting parameter for the bridge region.	$\frac{A}{V^{\beta}}$
V_X	Fitting parameter for the bridge region.	V
β	Fitting parameter for the bridge region	NA
A_S	Fitting parameter for the subthreshold region. Defined as the current ratio taken at the V_{OFF} boundary	A
$\Delta V_{TABL/DIBL}$	Linear interpolation function done to accommodate the fact that transfer characteristics between low drain bias and high drain bias have a separation. This is more commonly known as DIBL	V
V_{DD}	Supply voltage	V
$V_{DS_{LIN}}$	Low drain bias used to assess linear/triode behavior in MOSFETs.	V
sA	Smoothing parameter used to eliminate discontinuities at the V_{ON} boundary using the empirical approach	V
$V_{DS_{LK}}$	Drain-to-source voltage value that is used as a cutoff to avoid non-physical behavior when modeling leakage	V

Chapter 1. INTRODUCTION

There has been an increased interest in the Flat-Panel Display (FPD) industry to research and develop new material systems that can accommodate the ever-increasing demand for higher performance due to the increase in resolution, refresh rate, and size of modern FPDs. The need is further amplified when considering the current driving mechanisms that are used to control light emitting devices such as Liquid Crystal Displays (LCDs), μ-LEDs and OLEDs. Since active matrix arrays show higher control over the light emitting device than passive matrix arrays, the former are preferred. However, this comes at the expense of higher refresh rates due to the added circuitry. This increases the demand on the TFTs as these would have to respond to faster control signals.

1.1 μ-LED AND LCD FLAT-PANEL DISPLAYS

As shown in, LCDs consist of two polarizing layers, a twisted-nematic liquid crystal layer, a color filter, and a backlight that is used to illuminate the display. The way these displays work. The backlight gets polarized by the first polarizing layer, then it goes into the liquid crystal layer where the light gets rotated as a function of the applied voltage, which in turn is controlled by the pixel circuit composed of TFTs.This rotated light is then filtered by color and passes through the second polarizing layer, which is oriented 90° with respect to the first polarizer.

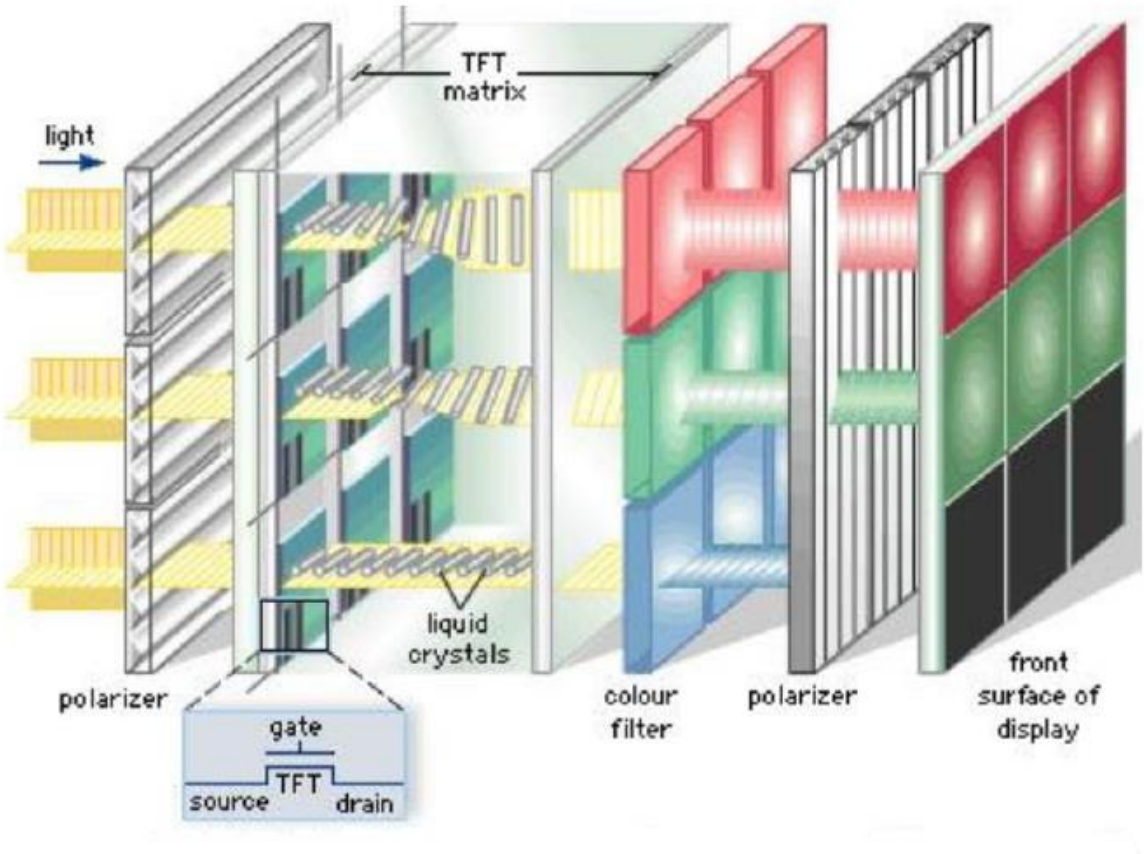


Figure 1.1 LCD schematic with TFT backplane [1].

The issue with LCD is that light polarization is sensitive to viewing angle. This means that color can degrade as a function of the angle the display is viewed upon. One of the possible solutions is to use an emissive display technology. That is, a display that is able to emit light in the RGB spectrum without the need for a light polarizer. This would get rid of the viewing angle issue, and increase image quality. For this reason, OLEDs have received positive feedback as it relates to image quality. However, OLED technology present reliability issues due to the organic material that is needed for its design [2, 3]. Like OLEDs, µ-LEDs can emit light in the RGB spectrum without the need of a polarizer. Furthermore, µ-LEDs do not require organic compounds for their design like OLEDs do. This eliminates the reliability issues that are related to the organic

compound in OLEDs. Therefore, µ-LEDs would be the preferred technology as it provides the image quality advantages of an emissive display without the reliability concern that OLEDs present.

However note that different applications may require different technologies. OLED displays have a lower manufacturing cost because these can be manufactured monolithically alongside the electronics needed for driving it. This makes this technology to be the better candidate for home applications such as monitors and TV's. µ-LED displays provide higher levels of brightness than their OLED counterparts. For this reason, when there are high levels of ambient light, µ-LED displays are preferred. The display brightness will overcome the ambient light, which will make the display viewable under these conditions. Therefore, µ-LED displays are better suited for applications where a display is going to be shown outdoors.

1.2 PIXEL ADDRESSING MECHANISMS

There are two types of addressing mechanisms when driving light emitting devices in FPDs, passive and active matrix arrays as shown by Figure 1.2. The passive matrix array consists of the light emitting device being connected by two levels of metals where one layer is used to wire up the column or data signal and runs horizontally, and the other level is used as a scan or row signal and runs vertically. There is no such thing as a controlling device in this scheme. Therefore, the isolation in between adjacent pixels can be quite poor as it is extremely sensitive to crosstalk. The active matrix array is similar to the passive matrix array in the way that is wired up. However, the main difference is the existence of an intermediate TFT circuit that handles the voltage signals that seek to control the light emitting device. This intermediate circuit takes care of the isolation in between adjacent pixels, which greatly reduces the sensitivity to crosstalk in between metal levels.

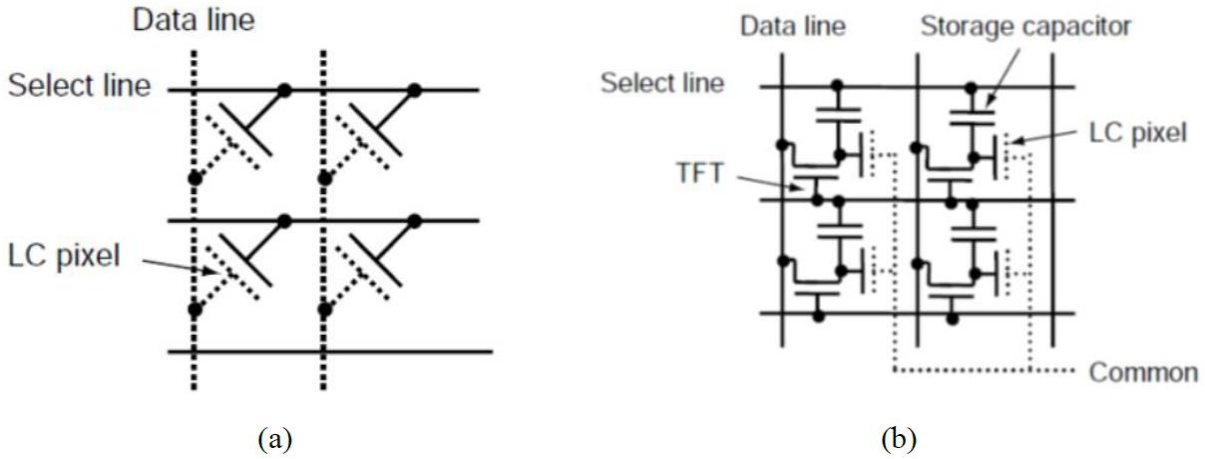


Figure 1.2. Examples of (a) a passive matrix array, and (b) an active matrix array.

1.3 TFT CHANNEL MATERIAL

Recent demand for larger FPD have driven the substrate size to increase substantially [4]. As shown by Figure 1.3, Gen10 glass substrate shows a remarkable increase in size from the previous generation. This causes design constrains in the TFT channel material that needs to be used as electrical uniformity becomes a primary concern.

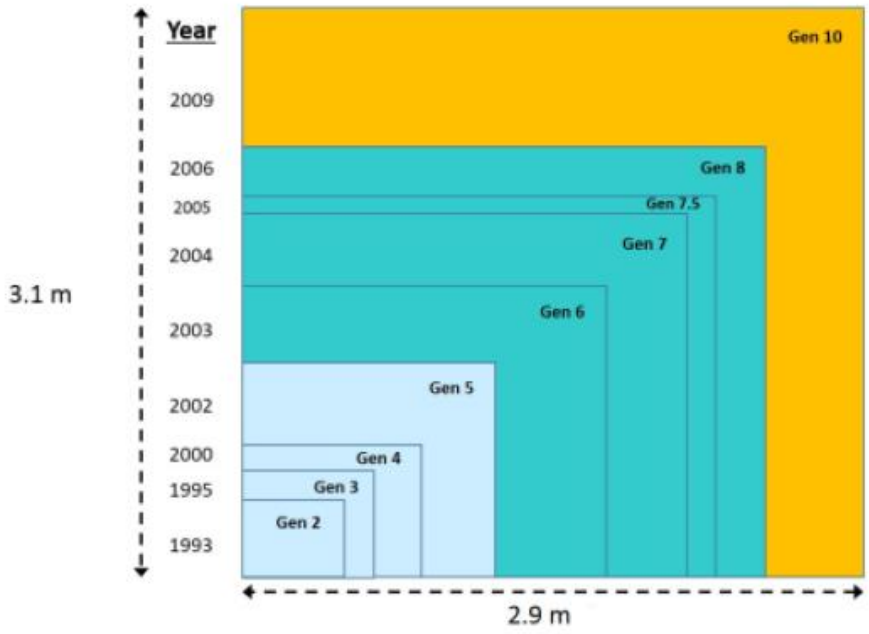


Figure 1.3 Glass substrate technology generations [5].

The different materials that are currently used to manufacture TFT backplanes for FPDs are shown in Table 1.1 along with their respective field mobility. As previously discussed, electrical uniformity is a primary concern going forward as larger substrates allow for the manufacturing of multiple FPD in a single production run. Therefore, the TFT channel material should provide two essential characteristics, high channel mobility and good uniformity. The former is required due to the increase in resolution/size, and the latter due to the substrate size increment.

Table 1.1 TFT Channel Material Properties Comparison [6, 7]

Channel Material	**Mobility (μ_{FE}) $cm^2/(Vs)$**	**Uniformity at Large Scales**	**Transistor Technology**
a-Si:H	<1	Good	NMOS
LTPS	>100	Poor	CMOS
a-IGZO	10-20	Good	NMOS

Low Temperature Polycrystalline Silicon (LTPS) may provide a higher field-effect mobility than IGZO. However, due to the grain boundaries, electrical uniformity in LTPS is not achievable at the same degree that an amorphous material such as IGZO is able to provide. Thus, the increase in uniformity, and higher mobility than the one present in hydrogenated amorphous silicon (a-Si:H) makes IGZO a theoretically better candidate for the TFT channel material going forward.

IGZO MATERIAL PROPERTIES

1.4 It has been established that IGZO is the material that fulfills many of the needs of the FPD industry going forward. Characteristics such as higher electrical uniformity due to its amorphous nature, and higher carrier mobility make it the perfect candidate to succeed a-Si:H in manufacturing on large area substrates such as Gen10 glass. For this reason, it is important to discuss the material properties of IGZO to understand why this material system offers such advantages over a-Si:H.

The difference in electron mobility in amorphous IGZO versus a-Si:H is due to fundamental differences in the electronic structure. As shown by Figure 1.4, amorphous IGZO shows a higher degree of s-orbital overlap caused by the metallic ions present in the material. This causes the electron transport mechanism to be dominated by band conduction instead of electron hopping, which is the transport mechanism that dominates in a-Si:H. The reason why this occurs is because a-Si:H has highly directional hybridized sp3 orbitals which are influenced by defect states in the lattice, causing degradation in the orbitals' overlap. This theory was proposed and validated by Hosono *et al* back in 2004 [6], when the publication directed the scientific community's attention towards amorphous oxide semiconductors as the path going forward for TFTs.

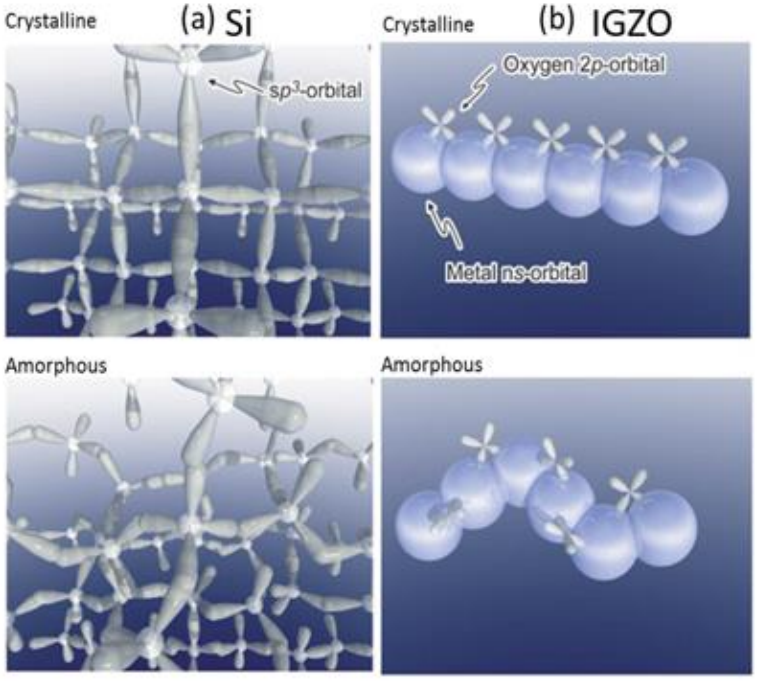


Figure 1.4 Interpretation of higher carrier mobility present in amorphous IGZO material [6].

1.5 GOAL & OBJECTIVES

The goal of this work is to create and implement an accurate compact model for IGZO TFTs in Verilog-A to assess the impact of parasitic elements, i.e. resistances and capacitances, that are inherently present in device and pixel designs. This will provide insight on the behavior of IGZO TFTs and the influence on the light emitting device operation during active matrix addressing protocol. The objectives are described as follows:

1. Obtain the mathematical foundation for an off-state model that is derived from the existing on-state model [8]. This would allow the accuracy of the on-state model to be extended to the subthreshold region.
2. Generate an empirical model based on the mathematical insight gained from objective 1.

3. Create an algorithm to perform a parameter extraction routine to find the parameters that best describe a given device.
4. Generate and validate the Verilog-A code for the compact model.
5. Perform transient simulations using the Verilog-A compact model through a proposed pixel circuit for μ-LED applications to assess the impact of parasitic elements such as source/drain overlap capacitance, and source/drain and interconnect series resistances.

1.6 DOCUMENT OUTLINE

Chapter 1 has described recent developments in the display industry, and provided motivation behind the use of IGZO as a channel material going forward. A brief description of μ-LED technology was provided along with its advantages over recent LCD display technology. Furthermore, the goal and objectives for this work have been presented.

Chapter 2 discusses the current approaches that are used for generating a compact model throughout recent literature. The shortcomings and the advantages for each approach are described while providing the motivation for this work. Lastly, the rationale behind the proposed circuit for this work is presented in this chapter.

Chapter 3 provides the mathematical foundation that was laid out for the subsequent empirical model that was used. Emphasis is given to the discovery of the mathematical form that becomes the groundwork for the off-state model. The algorithm that was created to perform the parameter extraction for the off-state region is also explained in detail.

Chapter 4 describes the proposed circuit topology that is used to validate the compact model through transient simulation. Timing analysis as it relates to row/column scan is discussed, and

the impact of parasitic elements such as source/drain overlap capacitance and source/drain series resistance is assessed through transient simulation. Emphasis is given to phenomena such as charge sharing and propagation delay.

Chapter 5 provides a summary of the key findings of the model development and the most relevant results from transient simulation analysis. Discoveries that concern the evaluation of parasitic elements to assess proper circuit functionality are included as well.

Chapter 2. COMPACT MODELS AND PIXEL CIRCUITS

Recent literature shows that there are two major approaches when generating a compact model. The first one is an analytical model based on first-principles where the solution is found by solving Poisson's equation and arriving at an expression that provides the surface potential for a given gate-to-source, and drain-to-source voltages. The second approach entails a mathematical approximation which takes advantage of the foundation established by SPICE models. Both of these approaches have their shortcomings and advantages, which will be discussed extensively. Different pixel circuits will be presented and a discussion will follow about the approach that will be taken when choosing a circuit topology for the purpose of this work.

2.1 COMPACT MODELS REVIEW

The reviewed models are presented in this section. It is worth mentioning that the device structure (i.e. electrode configuration) that was used for modeling purposes can change with each author's approach. However, it is known that the electrostatics for dual gate configurations are similar to single gate devices [9]. This means that models and their accuracy can be compared irrespective of the chosen device structure.

Analytical models are intricate and a closed form solution may not be available. Thus, approximations based on the mathematical insight are made. Complicated equations pose challenges to the logic of compact modeling languages such as Verilog-A. For instance, the

Lambert function is used regularly to find a closed-form solution of Poisson's equation when the carrier concentration is a function of deep and tail states. However, this function is not available in Verilog-A. Therefore, the approximation that needs to be made in order to code this solution can diminish from the accuracy of a physical model. Furthermore, circuit simulators benefit from using charge-based models as they present less demands for convergence [10].

2.1.1 Analytical Models

Analytical models present a similar derivation in the sense that they all base their analysis on solving Poisson's equation to find the surface potential, which provides the concentration of inversion/accumulated charge in the channel. This, in turn, will dictate the amount of current that is available for flowing into the drain given that there is a positive potential in the drain region, *i.e.* $V_{DS} > 0$. For this reason, only two different models will be presented in this section as a representative sample of the different researched models [11, 12, 13, 14, 15, 16].

2.1.1.1 Approach by Qin et al.

The structure that was used for modeling by Qin *et al* is shown in Figure 2.1. The complete derivation of the surface potential model is included in [15]. This shows the mathematical expressions that will be used during the drain current derivation. These will only be referenced and not derived during the drain current model development presented in this review.

The drain current model shown by Qin *et al* presents a mobility model that takes into account the sub-gap DOS present in a-IGZO-TFTs, where the effective mobility is described by Equation 2.1. The DOS function shows that band-tail states exist in a-IGZO TFTs. Therefore, when these band-tail states begin filling up due to an increase in V_{GS}, the apparent free carrier mobility increases as less states need filling and extra free charge is available to contribute to the drain

current. Once all of the available trap states are filled, the mobility saturates and no longer increases; this corresponds to the value of μ_{BAND}. Lastly, *m* is a fitting parameter for the mobility-gate-to-source voltage curve.

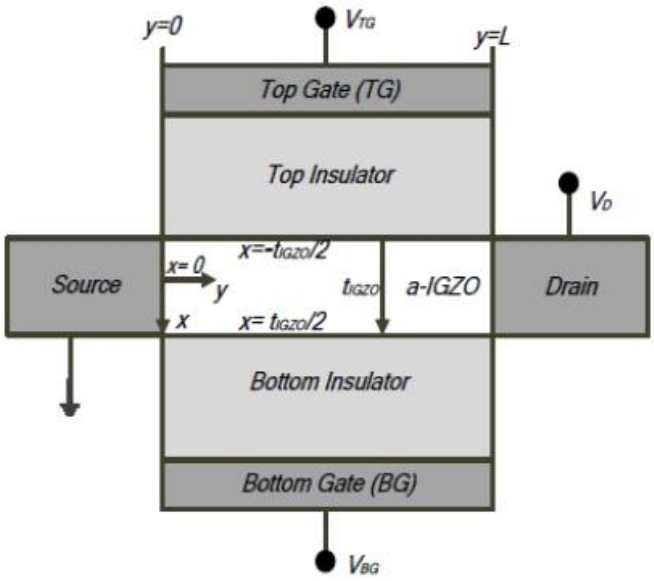


Figure 2.1 Device structure that was used for modeling purposes by Qin et al [15].

$$\mu_{eff} = \mu_{BAND} \cdot \exp\left(\frac{-m}{V_{GS} - V_{FB}}\right) \qquad 2.1$$

Because of the symmetric structure, the electric field at $x = t_{IGZO}/2$ is zero. However, the potential at this point cannot be ignored. Thus, a coupling coefficient is defined by Equation 2.2, where β is defined by Equation 2.3. The purpose of α is to represent the interaction between the top and bottom gate.

$$\beta = \frac{q}{kT_{eff}} \qquad 2.2$$

$$\alpha = -\frac{2N_{eff}kT_{eff}}{\epsilon_{IGZO}} \exp[\beta(\phi_0 - V_{ch} - \phi_{F0})] \qquad 2.3$$

where N_{eff} is the effective carrier density, kT_{eff} is the characteristic energy, ϵ_{IGZO} is the permittivity of IGZO, ϕ_0 is the potential in the middle of the film, V_{ch} is the channel potential in the y-axis, and ϕ_{F0} is the fermi potential. The electric field is derived from the Poisson's equation and it is shown in the surface potential derivation. The mathematical description for the electric field is presented in Equation 2.4. This mathematical relationship can be rearranged using Equation 2.3, leading to Equation 2.5.

$$E = -\sqrt{\frac{2N_{eff}kT_{eff}}{\epsilon_{IGZO}}}\sqrt{\exp[\beta(\phi_s - V_{ch} - \phi_{F0})] - \exp[\beta(\phi_0 - V_{ch} - \phi_{F0})]} \quad 2.4$$

$$E = -\sqrt{\frac{2N_{eff}kT_{eff}}{\epsilon_{IGZO}}\exp[\beta(\phi - V_{ch} - \phi_{F0})] + \alpha} \quad 2.5$$

The partial derivative of the electric field with respect to the channel potential is shown by Equation 2.6.

$$\frac{\partial E}{\partial V_{ch}} = \frac{1}{2E}\frac{d\alpha}{dV_{ch}} - \frac{1}{E}\frac{qN_{eff}}{\epsilon_{IGZO}}\exp[\beta(\phi - V_{ch} - \phi_{F0})] \quad 2.6$$

Due to the fact that $n_{eff} = N_{eff}\exp[\beta(\phi - V_{ch} - \phi_{F0})]$, Equation 2.6 can be rearranged as shown in Equation 2.7.

$$\frac{qn_{eff}}{E} = \epsilon_{IGZO}\left(\frac{1}{2E}\frac{d\alpha}{dV_{ch}} - \frac{\partial E}{\partial V_{ch}}\right) \quad 2.7$$

Authors use Pao-Sah formula shown in Equation 2.8 to derive the drain current.

$$I_{DS} = 2\frac{W}{L}\int_0^{V_{DS}}\int_{\phi_0}^{\phi_s}\mu_{eff}\frac{qn_{eff}}{E}d\phi dV_{ch} \quad 2.8$$

Substituting Equations 2.7 and 2.1 in Equation 2.8 provides the working expression for the drain current in IGZO TFTs as shown by Equation 2.9.

$$I_{DS} = 2\frac{W}{L}\mu_{BAND}\epsilon_{IGZO}\int_0^{V_{DS}}\int_{\phi_0}^{\phi_s}\exp\left(-\frac{m}{V_{GS}-V_{FB}}\right)\left(\frac{1}{2E}\frac{d\alpha}{dV_{ch}}-\frac{\partial E}{\partial V_{ch}}\right)d\phi dV_{ch} \qquad 2.9$$

Recall that the drain-to-source current can be divided into the diffusion and drift current components such as $I_{DS} = I_1 - I_2$, where I_1 and I_2 is the diffusion and drift current, respectively. Therefore, I_1 and I_2 are defined by Equations 2.10 and 2.11, respectively.

$$I_1 = 2\frac{W}{L}\,\mu_{BAND}\epsilon_{IGZO}\int_0^{V_{DS}}\int_{\phi_0}^{\phi_s}\exp\left(-\frac{m}{V_{GS}-V_{FB}}\right)\left(\frac{1}{2E}\frac{d\alpha}{dV_{ch}}\right)d\phi dV_{ch} \qquad 2.10$$

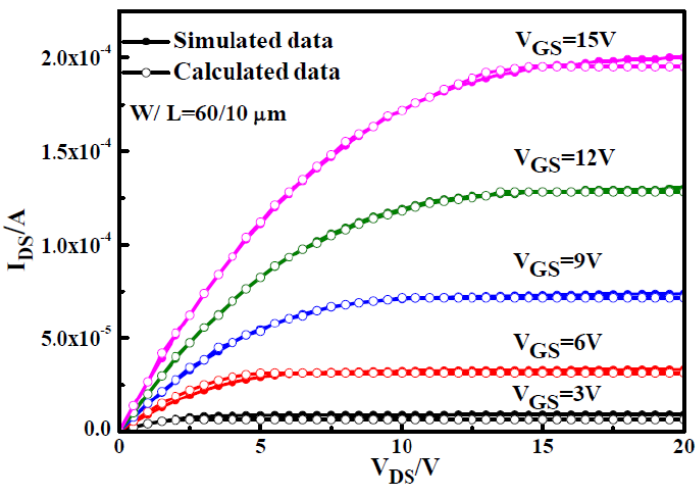
$$I_2 = 2\frac{W}{L}\mu_{BAND}\epsilon_{IGZO}\int_0^{V_{DS}}\int_{\phi_0}^{\phi_s}\exp\left(-\frac{m}{V_{GS}-V_{FB}}\right)\left(\frac{\partial E}{\partial V_{ch}}\right)d\phi dV_{ch} \qquad 2.11$$

Solving the integrals present in Equations 2.10 and 2.11 and substituting the solutions in Equation 2.9 provides the comprehensive solution for the drain current expression as shown by Equation 2.12.

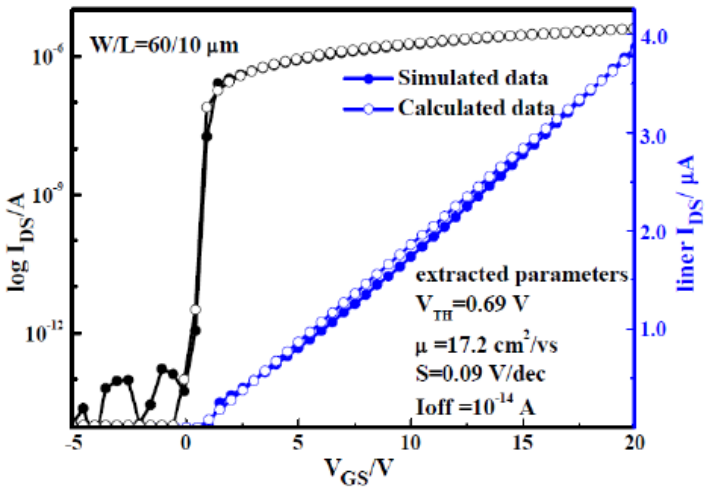
Results in the form of output and transfer characteristics that this model provides are shown in Figure 2.2. While an error measuring technique was not used by the authors, a qualitative assessment of the presented data can be made to perform a comparison between the reviewed models. Devices presented in this study are fairly long channel, $L = 10\ \mu m$ for the shortest device presented. Therefore, it is not possible to deduct the compact model ability to predict short channel behavior. Furthermore, the model's ability to predict small V_{GS} bias values is not disclosed either as the smallest value used in Figure 2.2 is 3V. Thus, it is not possible to assess the model's

capabilities in the full swing range of operation that is needed for properly functioning digital circuits.

$$
\begin{aligned}
I_{DS} = {} & \frac{W}{L}\mu_{BAND}\exp\left(\frac{-m}{V_{GS}-V_{FB}}\right)t_{IGZO}kT_{eff}N_{eff}\{\exp[\beta(\phi_{00}-\phi_{F0})] \\
& -\exp[\beta(\phi_{0L}-V_{DS}-\phi_{F0})]\} \\
& +\frac{W}{L}2C_{OX}\mu_{BAND}\left[(V_{GS}-V_{FB})\left(\phi_{SL}-\phi_{SO}-\frac{1}{2}(\phi_{SL}^2-\phi_{SO}^2)\right)\right] \\
& +\frac{4}{\beta}\sqrt{2N_{eff}kT_{eff}\epsilon_{IGZO}}\exp\left(-\frac{\beta}{2}\phi_{F0}\right) \\
& \cdot\left[\sqrt{\exp(\beta\phi_{SO})-\exp(\beta\phi_{OO})}\right. \\
& \left.-\exp\left(\frac{\beta\phi_{00}}{2}\right)\arctan\left\{\sqrt{exp\big(\beta(\phi_{S0}-\phi_{00})\big)-1}\right\}\right] \\
& -\frac{4}{\beta}\sqrt{2N_{eff}kT_{eff}\epsilon_{IGZO}} \\
& \cdot\exp\left[-\frac{\beta}{2}(V_{DS}-\phi_{F0})\left[\sqrt{\exp(\beta\phi_{SL})-\exp(\beta\phi_{0L})}\right.\right. \\
& \left.\left.-\exp\left(\frac{\beta\phi_{0L}}{2}\right)\arctan\left\{\sqrt{exp[\beta(\phi_{SL}-\phi_{0L})]-1}\right\}\right]\right]
\end{aligned}
\qquad 2.12
$$



(a)



(b)

Figure 2.2. Experimental output (a) and transfer characteristics (b) of a $\frac{w}{L}=\frac{60\mu m}{10\mu m}$ *device (markers) compared to the model generated by Qin et al (solid line) [15].*

2.1.1.2 Approach by Deng et al.

The same approach taken by Qin *et al* is taken by Deng *et al*, where Poisson's equation is solved in order to obtain the surface potential as a function of the applied voltages. This provides the charge concentration in the channel, which then provides the amount of charge that is available to flow into the drain. The most notable differences between these two studies are the mobility model, and the device structure which is a bottom gate device instead of a dual gate as shown previously in the work done by Qin *et al*. Deng *et al.* use a power-law model to fit for the mobility as shown by Equation 2.13, where μ_0 and *m* are fitting parameters. The drain current derivation details are reviewed in this work. Details of the preceding calculations such as electric field and accumulation charge are found in [16] and the references therein. The drain current equation used in this study is shown by Equation 2.14, where both drift and diffusion components are combined

$$\mu_{eff} = \mu_0 (V_{GS} - V_{FB})^m \tag{2.13}$$

$$I_{DS_0} = \frac{qW\mu_{eff}}{L} \int_{\phi_{ss}}^{\phi_{SL}} \frac{N_i(\phi_s)}{d\phi_s / d\phi_n} d\phi_s \tag{2.14}$$

where $N_i(\phi_s)$ represents the accumulation charge in the channel and is defined by Equation 2.15, ϕ_s is the surface potential, ϕ_n is the quasi-fermi potential, and μ_{eff} is the effective mobility.

$$N_i(\phi_s) = \alpha \left(\frac{V_{GS} - V_{FB} - \phi_s}{\beta} \right)^{\frac{2\phi_{eff}}{\phi_t} - 1} \tag{2.15}$$

where $\alpha = \frac{2n_0 \phi_{eff} \phi_t}{A(2\phi_{eff} - \phi_t)}$, $\beta = A \frac{\epsilon_{IGZO}}{C_{OX}}$ and $A = \sqrt{\frac{2qn_{eff}}{\epsilon_{IGZO}}}$. The derivation for $N_i(\phi_s)$ comes from solving Poisson's equation and making an approximation on the charge density. Instead of using

the analytical solution where the band-tail states contribution to the accumulated charge is taken into consideration, an effective charge density approximation is made to enable a closed-form solution for Poisson's equation.

By substituting Equation 2.15 in Equation 2.14, the solution that results is shown by Equation 2.16.

$$I_{DS_0} = -\frac{qW\mu_{eff}\alpha}{L\beta^{\left(\frac{2\phi_{eff}}{\phi_t}-1\right)}}[f(\phi_{SL}) - f(\phi_{ss})] \qquad 2.16$$

where ϕ_{SL} and ϕ_{SS} are the surface potential values at the drain and source end, respectively, and $f(\phi_s)$ is given by Equation 2.17.

$$f(\phi_s) = \frac{2\phi_{eff}\phi_t}{2\phi_{eff} - \phi_t}(V_{GS} - V_{FB} - \phi_s)^{\frac{2\phi_{eff}}{\phi_t}-1} + \frac{\phi_t}{2\phi_{eff}}(V_{GS} - V_{FB} - \phi_s)^{\frac{2\phi_{eff}}{\phi_t}} \qquad 2.17$$

Note that the drain current shown in Equations 2.16 and 2.12 is a complex function of the applied gate-to-source and drain-to-source voltages and their effect on the surface potential. This will cause extra calculations to be done during simulations, which will reduce the compact model performance. Thus, it is of interest to avoid this level of complexity when circuit simulation is the ultimate goal of a given model. Therefore, these types of models are best suited for device design rather than circuit design.

Results from the work done by Deng *et al.* are shown in Figure 2.3. Because of the mobility model used in this work, V_{GS} cannot be smaller than V_{FB} as $V_{GS} - V_{FB} < 0$. This would cause the model to provide a negative value for the mobility which is non-physical. This means that information that pertains to the leakage region is inaccessible by this model. In the context of pixel circuit simulation, leakage information is extremely important as it is the biggest factor that can

cause the storage capacitor to lose its charge over time. Therefore, this model lacks the necessary information to provide an accurate transient simulation in this context.

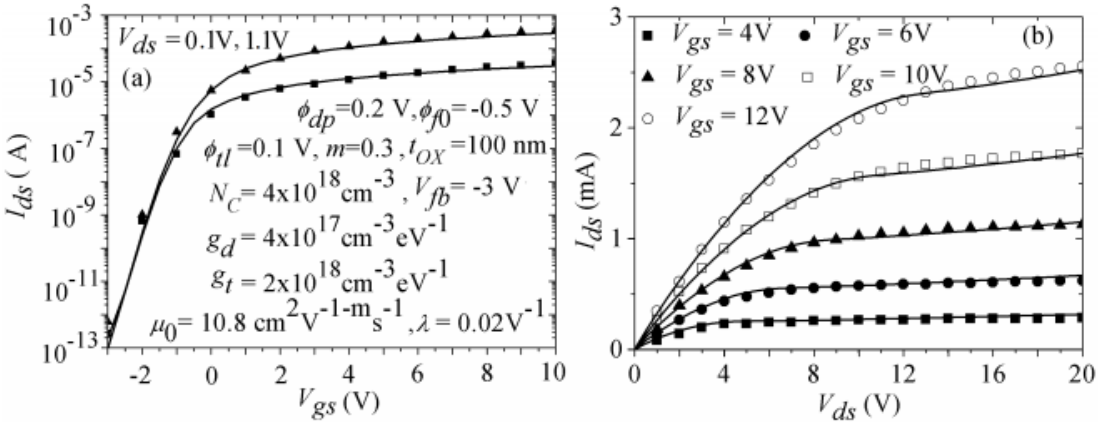


Figure 2.3. Experimental (markers) and modeled (solid lines) data in both transfer (a) and output (b) characteristics [16].

2.1.2 Semi-empirical Models

Semi-empirical models take advantage of the mathematical foundation that has been established in SPICE, with model adjustments to accommodate the defect states dominated behavior of IGZO. These models are easier to implement as the foundational work has been done. However, because IGZO shows a fundamentally different behavior than silicon, misrepresentations can cause substantial discrepancies between the model's predictions and the experimental data that it tries to model. Therefore, it is important to make these adjustments properly to have an accurate representation of what is being modeled.

2.1.2.1 Approach by Perumal et al.

The cross-section of the modeled device is shown in Figure 2.4 and it corresponds to a bottom gate device.

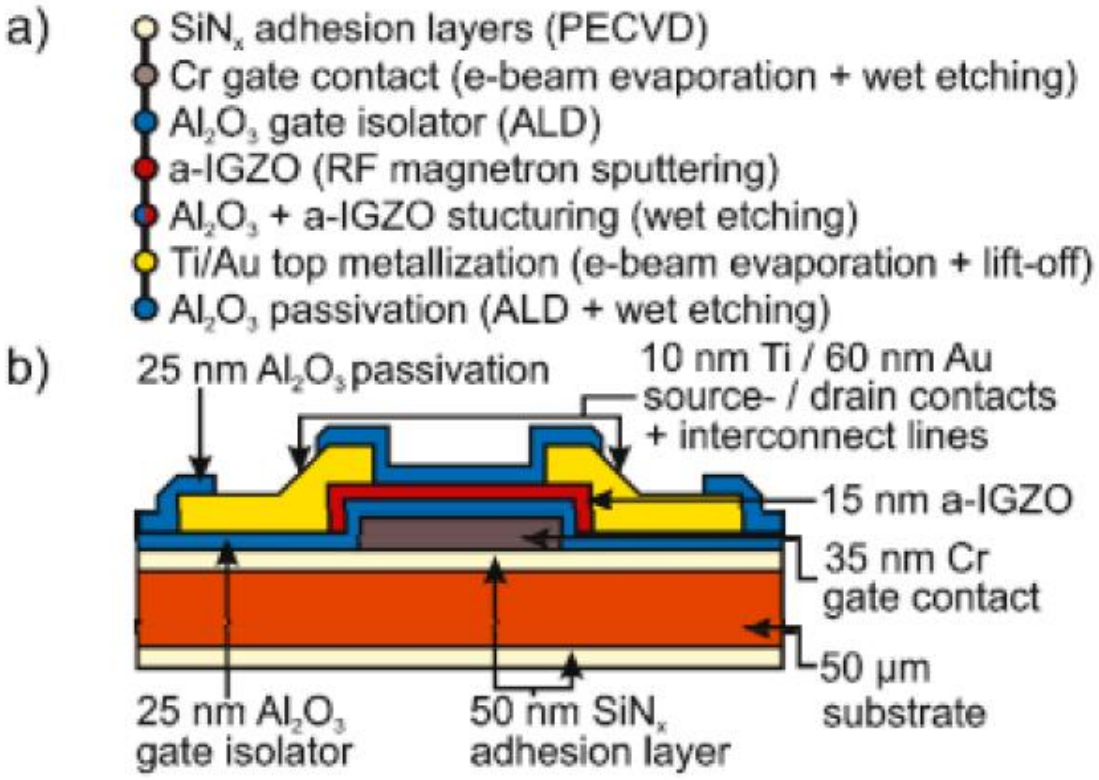


Figure 2.4. Cross-section of the device modeled by Perumal et al (b) with its layer code (a) [17, 18].

The work done by Perumal *et al* presents devices which channel lengths range from 50 μm to 3.6 μm [18, 17]. Claims are made that this model is accurate at smaller channel length. However, parameter tweaking is required to obtain better accuracy. This model uses a modified SPICE level 3 model in order to accommodate for the differences in physical characteristics between IGZO and silicon. As such, the model is a collection of constant that is presented in Table 2.1, where all the quantities correspond to SPICE level 3 parameters.

Table 2.1. Modified SPICE level 3 model for IGZO TFTs as proposed by Perumal et al [18, 17].

Key Parameters	Value	Remarks
Fast Surface State Density (NFS)	$1.538x10^{20}\ cm^{-2}$	Process Given
Al_2O_3 Relative Permittivity (ε_r)	9.5	Process Given
Physical Oxide Thickness	25 nm	Process Given
Drain-Source Shunt Resistance	0.6 Ω	Fitted for DC
Mobility (U0)	$22\ {cm^2}/{V \cdot s}$	Fitted for DC
Static Feedback (ETA)	12	Fitted for DC
Drain/Source Resistance (RD/RS)	$500\ \Omega$	Fitted for DC
Mobility Modulation (THETA)	$0.012\ V^{-1}$	Fitted for DC
Lateral Diffusion (LD)	$5\ \mu m$	Fitted for AC
SiO_2 Equivalent Oxide Thickness (TOX)	$10.26\ nm$	Fitted for AC
G-S Overlap Capacitance (CGSO)	$12\ {nF}/{m}$	Fitted for AC
G-D Overlap Capacitance (CGDO)	$12\ {nF}/{m}$	Fitted for AC

While simplistic, this model tries to circumvent the modeling efforts by trying to accommodate a released SPICE model for a-IGZO-TFTs. Note that the physics of silicon devices differs in comparison to IGZO devices; the main reason for this being the defect states interpretation. Thus a large discrepancy between the drain current values predicted by this model and the experimental data is not surprising. Results from this model are shown in Figure 2.5, and Figure 2.6. Output and

transfer characteristics generated by this model are the focal point of interest. Moreover, a short channel device is showcased in Figure 2.6. While claims were made that the model can be accurate below $L = 3\ \mu m$, this figure shows substantial difference between measured and simulated curves.

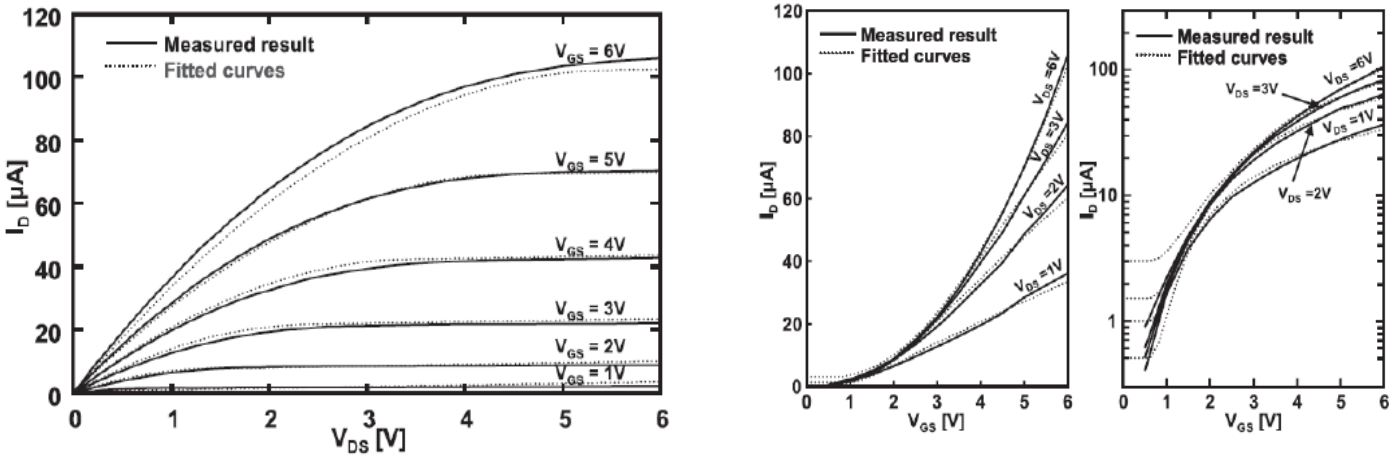


Figure 2.5. Measured and simulated output (a) and transfer (b) characteristics for a $\frac{L}{W} = \frac{50\ \mu m}{50\ \mu m}$ device [17].

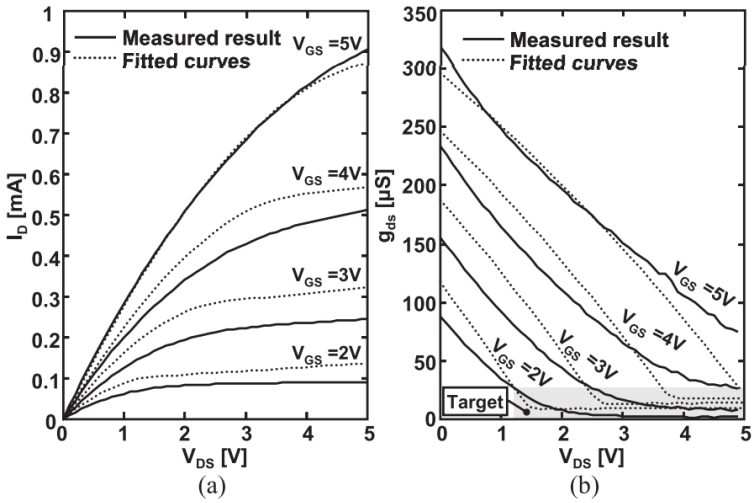


Figure 2.6. Output characteristics (a), and transconductance as a function of V_{DS} (b) of a short chanel device where $L = 2.5\ \mu m$ [17].

2.1.2.2 Approach by Hirschman et al.

In the work done by Hirschman *et al*, a bottom gate structure was used to model the electrical behavior of IGZO TFTs as shown in Figure 2.7 [8, 19, 20].

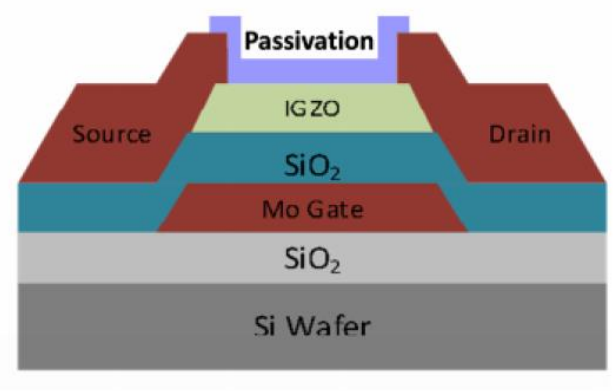


Figure 2.7. Cross-section of the device used during modeling activities by Hirschman et al. [19].

The derivation shown in this work is based on the SPICE level 2 model. The drain current in the triode region of operation is shown in Equation 2.18,

$$I_{DS} = \frac{W}{L} C_{OX} \mu_{eff} \left[(V_{GS} - V_T) V_{DS} - \frac{1 - \alpha_{SCE}}{2} V_{DS}^2 \right] \qquad 2.18$$

where W and L are the transistor's width and length, respectively, C_{OX} is the gate oxide capacitance per area, μ_{eff} represents the electron channel mobility, V_{GS} is the gate-to-source voltage, V_{DS} is the drain-to-source voltage, V_T is the threshold voltage, and α_{SCE} considers short-channel behavior.

The electrical behavior of IGZO TFTs is dominated by defect states. As such, the influence of both the drain and the gate on these defect states should be accounted for. Hirschman *et al*. call this phenomena the gate-impressed charge ratio, and the drain-impressed charge ratio models for the gate and the drain bias are shown by Equations 2.19 and 2.20, respectively.

$$\frac{Q_{free(1D)}}{Q_{total}} \approx \eta_G = \frac{1}{Z - \theta_{BTS}(V_{GS} - V_T)} \qquad 2.19$$

$$\frac{Q_{free(2D)}}{Q_{total}} \approx \eta_D = \frac{1}{1 + {V_{DS}}/{V_{BTS}}} \qquad 2.20$$

The channel generation in IGZO TFTs is caused by charge accumulation in the vicinity of the gate dielectric as caused by the gate potential. The inclusion of trap states in this scheme causes differences in the charge density that gets accumulated in the channel. As the gate bias increases, the trap states start to ionize, which decreases the overall concentration of trap states. Therefore, as the gate bias increases, the free charge density increases as well. This is denoted by the negative sign of θ_{BTS} in η_G. Furthermore, the drain causes the ionized trap states to become de-ionized, which increases the concentration of trap states thereby reducing the free charge density. Applying these two models to the drain current results in Equation 2.21.

$$I_{DS} = \frac{W}{L} C_{OX} \mu_0 \eta_D \eta_G \left[(V_{GS} - V_T) V_{DS} - \frac{1 - \alpha_{SCE}}{2} V_{DS}^2 \right] \qquad 2.21$$

where μ_0 is the field-independent free carrier mobility, and α_{SCE} represents the short channel effect coefficient, where $\alpha_{SCE} \approx 0$ for long channel devices. The field-independent mobility μ_0 is established using TCAD simulation, with a set value of 12.7 $cm^2/(Vs)$ showing good agreement with experimental data [8, 20]. A field-independent mobility is required because of the interpretation of band-tail states ionization. As band-tail states ionize, the transconductance keeps increasing due to the increase in charge density. Therefore, a field-dependent mobility will create a confounding effect with this phenomenon causing challenges in the model interpretation. The derivative of Equation 2.21 with respect to V_{DS} is set to zero in order to find $V_{DS_{SAT}}$ and the saturation current. $V_{DS_{SAT}}$ and $I_{DS_{SAT}}$ are shown by Equations 2.22 and 2.23, respectively.

$$V_{DS_{SAT}} = \sqrt{V_{BTS}^2 + \frac{2}{1 - \alpha_{SCE}} V_{BTS}(V_{GS} - V_T)} - V_{BTS} \quad 2.22$$

$$I_{DS_{SAT}} = \frac{W}{L} C_{OX} \mu_0 \eta_{D_{SAT}} \eta_G \left[(V_{GS} - V_T) V_{DS_{SAT}} - \frac{1 - \alpha_{SCE}}{2} V_{DS_{SAT}}^2 \right] \quad 2.23$$

$$\eta_{D_{SAT}} = \frac{1}{1 + {V_{DS_{SAT}}}/{V_{BTS}}} \quad 2.24$$

Results provided by this model are shown in Figure 2.8, with goodness-of-fit statistics shown in Table 2.2. As showcased by Figure 2.8 and Table 2.2, Hirschman *et al* model provides an excellent representation of the on-state electrical behavior of IGZO TFTs, even at remarkably small channel lengths ($L = 1\ \mu m$). Because of its accuracy and simplicity, this model can provide an excellent baseline for the development of an off-state model that is able to represent the entire range of gate and drain bias.

Table 2.2. Goodnes-of-fit statistics for devices with different lengths provided by Hirschman et al model [8].

Length μm	**21**	**9**	**6**	**3**	**2**	**1**
R^2	0.99993	0.99992	0.99992	0.99989	0.99971	0.99851

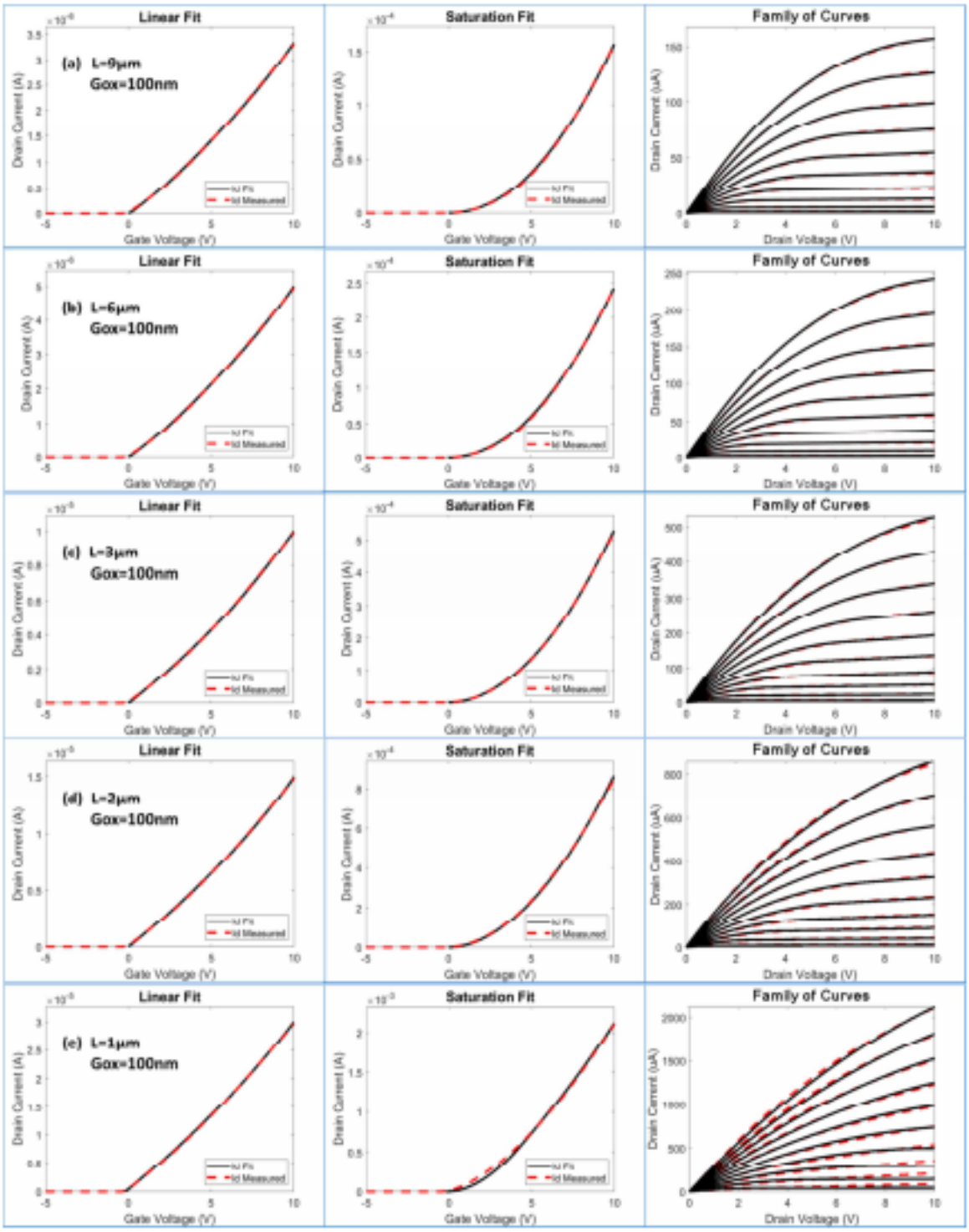
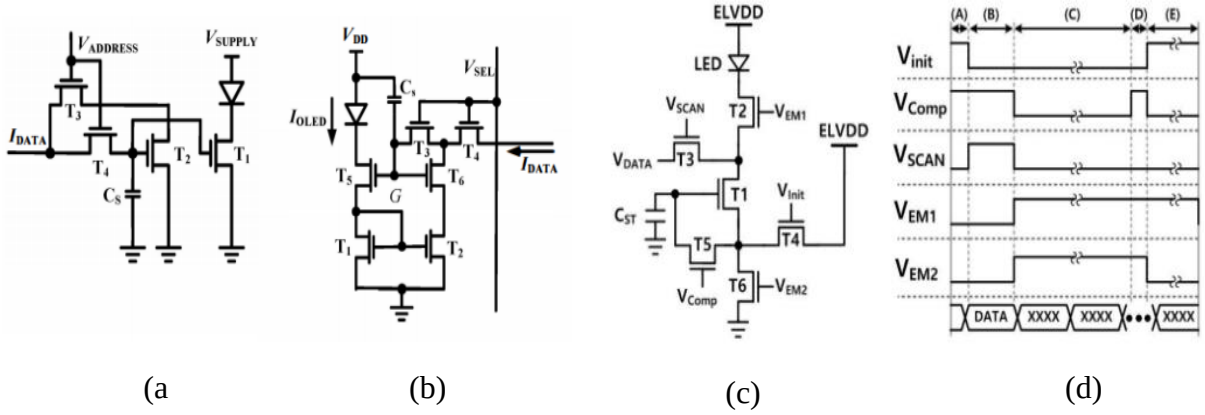


Figure 2.8. TCAD simulation (red dashed line) and model (black lines) I-V curves showing characteristics of devices of the following lengths: (a) 9 *μm, (b)* 6 *μm, (c)* 3 *μm, (d)* 2 *μm, (e)* 1 *μm [8].*

2.2 PIXEL CIRCUITS REVIEW

Recent literature shows several pixel circuits implementation using IGZO TFTs. The intention of the bulk of these reports is to try and design for non-idealities in the fabrication process such as threshold voltage variation [21, 22] and stress-related effects that degrade I-V characteristics in IGZO [23].



(a) (b) (c) (d)

Figure 2.9. A current programmed pixel circuit (a) and an improved version of this topology (b) as proposed by Liu et al [21], and a pixel circuit (c) with its waveform opeartion (d) that consists of multiple phases with the goal of compensating threshold voltage variation and annealing any damage related to photon bombardment due to illumination in IGZO TFTs [23].

Examples of each of these different topologies are shown in Figure 2.9. As discussed, the primary function on these circuits is to address issues related to uniformity in the threshold voltage, and stress-related effects in IGZO TFTs I-V curves. The former is accomplished in Figure 2.9.a and Figure 2.9.b by setting the current that goes into the light-emitting device through current mirrors, such that I_{DATA} is replicated in the driver transistor. The latter is accomplished in Figure 2.9.c by a multi-phase pixel circuit where the compensation phase puts the transistor that handles

the driving operation (T1) in reverse bias to anneal the damage caused by photon bombardment (NBIS).

The caveat of these topologies is the need for extra devices in order to accomplish the networks' purpose. The objective of this work is to generate and validate a compact model through experimental data. Therefore, adding an unwanted level of complexity to the network can cause misinterpretation on model's limitations. There needs to be a clear and concise interpretation on the models ability to predict the outcome of the transient simulation such that any shortcomings can be explained thoroughly. Therefore, the simple case of a pixel circuit shown in Figure 2.10 is proposed for the purpose of this work.

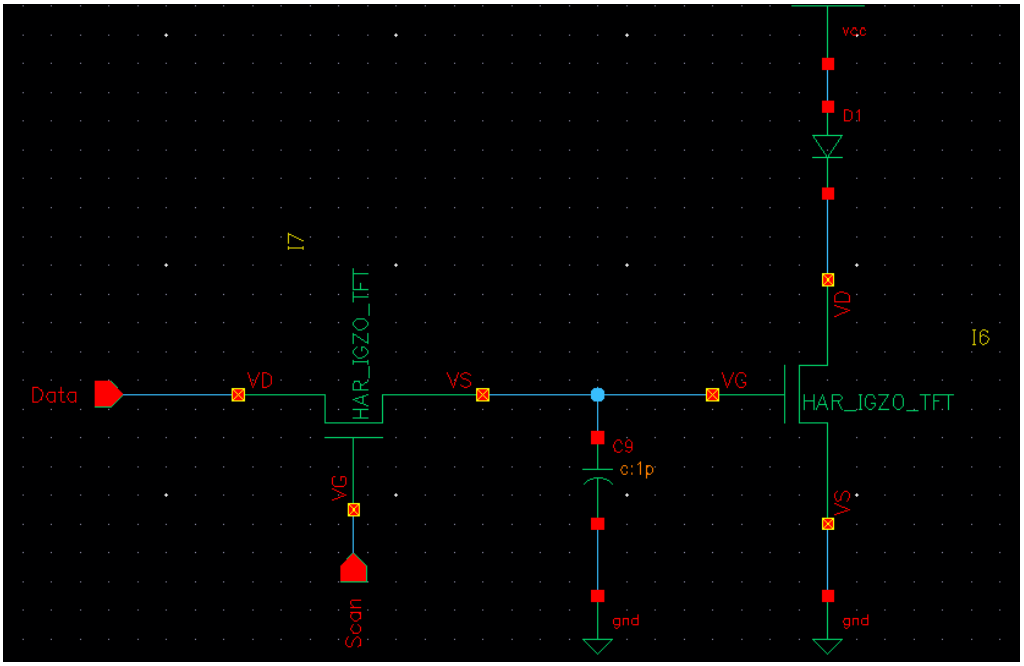


Figure 2.10. Ideal case of a 2T1C pixel circuit.

2.3 SUMMARY

All of the reviewed analytical models provide a fairly accurate description of the electrical characteristics of IGZO TFTs. However, the intricate nature of these models make it challenging to implement into a comprehensive compact model. Languages such as Verilog-A require a streamlined simplicity to avoid convergence issues during circuit simulation. While other languages can be used to work around this challenge, circuit integration can be streamlined by the usage of hardware description language (HDL). Thus, if a mathematical model is easier to implement in a HDL, it will provide far more benefits than one that cannot be implemented into a HDL. This is true even if the accuracy of said mathematical model is less than ideal. However, as shown by Figure 2.6, too little mathematical rigor can cause a substantial discrepancy between what is being modeled and what the experimental data is showing. Thus, a balance shall be found to avoid situations where simplicity overcomes accuracy.

In relation to this simplicity-accuracy trade off, it is arguable that the first-principle analytical models do not provide enough accuracy and, in the case of Deng *et al*, sufficient information to circumvent the issues around convergence in circuit simulators. Thus, these models are more suited for device engineering than circuit design. As such, the model presented by Hirschman *et al.* shows the adequate balance between simplicity and accuracy, given that the model is relatively simple and the accuracy is remarkable; $R^2 > 0.99$ for all of the shown devices, including those with pronounced short-channel behavior. The caveat is that this model lacks the off-state information. Therefore, this is the focus of this work.

Different pixel circuits were presented where multiple functions were accomplished such as threshold voltage compensation networks, current compensation techniques through current

mirrors, multi-phase pixel networks, etc. However, these circuits can detract from the goals of this work as the pixel circuit will only be used to validate the compact model in transient simulations. Furthermore, the light emitting device that will be used in this application is a μ-LED. Thus, there is a negligible need to control the voltage/current that will be used to power up the LED. This is because a driving transistor can accomplish this by itself given a supply electrode. Therefore, the simplest case of a 2T1C circuit is the proposed topology for this work.

Chapter 3. MODEL DEVELOPMENT

As described in the previous chapter, the compact model's accuracy-simplicity tradeoff presents a challenge. It is important for a model to be just complex enough such that it is accurate. However, given too much complexity can degrade the physical interpretation of said model. Furthermore, its implementation in a HDL can become cumbersome and provide convergence challenges when performing circuit simulation. For this reason, Hirschman *et al.* model is taken as the baseline model for a comprehensive compact model. In this chapter the model development will be focused on the off-state region of operation, and the on-state to off-state transition.

3.1 ON-STATE MODEL

The drain current equations for the on-state model provided by Hirschman *et al* [8] are shown in Equations 3.1, 3.2, 3.3, 3.4, 3.5, and 3.6, where $I_{DS_{LIN}}$ and $I_{DS_{SAT}}$ correspond to drain current in the triode and the saturation regions of operation, respectively, η_G is the gate-impressed charge ratio, η_D is the drain-impressed charge ratio, α_{SCE} represents the short-channel effect coefficient analog to the one used in level 2 SPICE, and C'_{OX}, μ_0, W, L, V_{GS}, V_T, V_{DS} have the same meaning as conventional MOSFET theory. Fitting parameters Z, θ_{BTS} and V_{BTS} describe the defect states dominated behavior of IGZO TFTs.

$$I_{DS_{LIN}} = \frac{W}{L}\mu_0 C'_{OX}\eta_G\eta_D\left[V_{GS} - V_T - \left(\frac{1-\alpha_{SCE}}{2}\right)V_{DS}\right]V_{DS} \qquad 3.1$$

$$\eta_G = \frac{1}{Z - \theta_{BTS}(V_{GS} - V_T)} \tag{3.2}$$

$$\eta_D = \frac{1}{1 + \frac{V_{DS}}{V_{BTS}}} \tag{3.3}$$

$$I_{DS_{SAT}} = \frac{W}{L}\mu_0 C'_{OX}\eta_G\eta_{D\,SAT}\left[(V_{GS} - V_T)V_{DS_{SAT}} - \left(\frac{1 - \alpha_{SCE}}{2}\right)V_{DS_{SAT}}^2\right](1 - \lambda V_{DS})^{-1} \tag{3.4}$$

$$V_{DS_{SAT}} = \sqrt{V_{BTS}^2 + \frac{2}{1 - \alpha_{SCE}}V_{BTS}(V_{GS} - V_T)} - V_{BTS} \tag{3.5}$$

$$\eta_{D\,SAT} = \frac{1}{1 + \frac{V_{DS_{SAT}}}{V_{BTS}}} \tag{3.6}$$

As mentioned before, the I-V characteristics of IGZO TFTs are dominated by defect states and their association with trap states near the conduction band edge. This behavior is described by both η_G and η_D, where η_G shows that as V_{GS} increases, the charge concentration in the channel increases as band-tail states will become ionized. Meanwhile, η_D shows that as V_{DS} increases, the charge concentration in the channel is reduced as the drain bias causes de-ionization of these trap states. The contribution of η_G is apparent in the transfer characteristics as the I-V behavior shows a concave up behavior. Moreover, the contribution of η_D will manifest in 'stretched' out output characteristics where $V_{DS_{SAT}}$ will be a higher number due to the contribution of V_{BTS}. An example of both of these cases is shown in Figure 2.8.

The main limitation of this model is that it is without consideration of the off-state. Evaluating Equations 3.1 and 3.4 at $V_{GS} = V_T$ shows that the drain current will go to zero. This is non-physical behavior as MOSFETs present a positive derivative across both output and transfer characteristics.

Therefore, it is known that at some point $V_{GS} > V_T$ the on-state model is no longer accurate, as depicted in the semi-log plot shown in Figure 3.1.

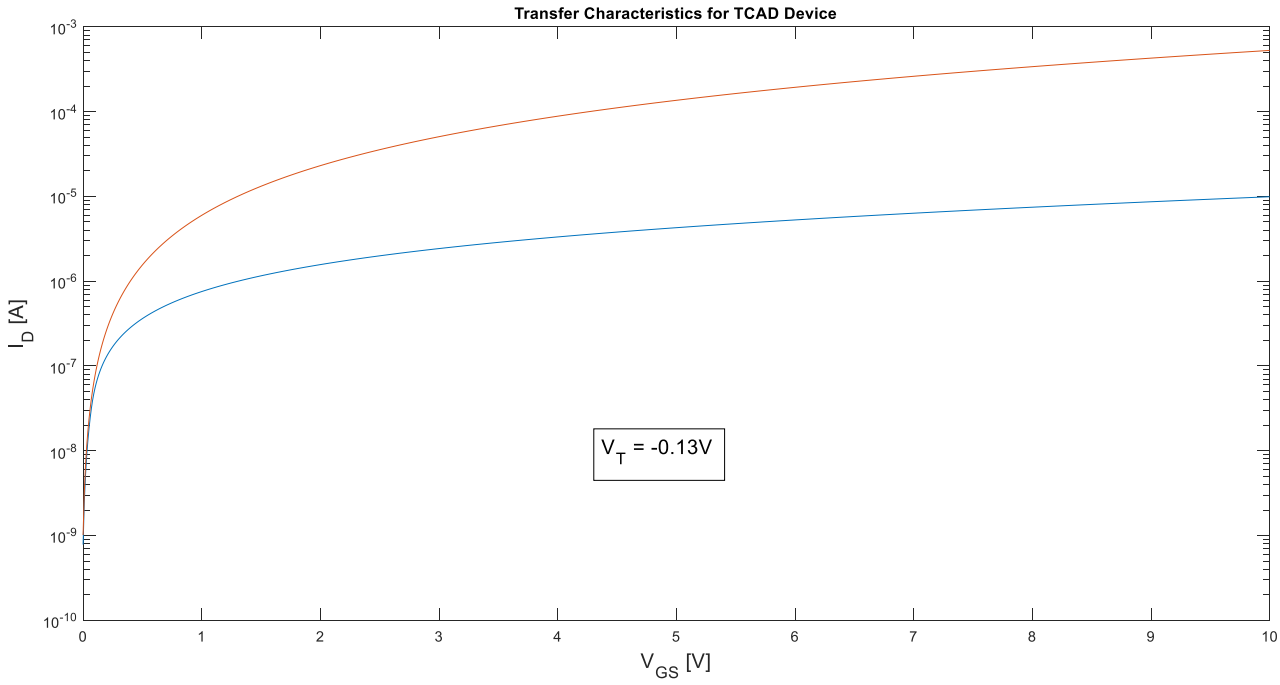


Figure 3.1. Transfer characteristics with $V_{DS} = 0.1V$ (blue line) and $V_{DS} = 10V$ (red line) for a TCAD simulated bottom-gate device with $50\,nm$ of oxide thickness and $\frac{W}{L} = \frac{100\ \mu m}{3\ \mu m}$ and extracted $V_T = -0.13\,V$. As V_{GS} approaches V_T the transconductance becomes unreasonably high, thus the on-state model is not accurate in this region of operation.

3.2

BRIDGE REGION

As mentioned, the on-state model becomes inaccurate at some point $V_{GS} > V_T$. For this reason, a region of operation needs to be defined where the drain current behavior cannot be modeled by an exponential behavior such as the subthreshold region nor the established on-state model. A bridge region is conceptually defined in Equation 3.7 where the drain current in the bridge is a function of the applied voltages V_{DS}, and V_{GS}.

$$I_{D_B} = f(V_{GS}, V_{DS}), \qquad V_{OFF} \leq V_{GS} \leq V_{ON} \tag{3.7}$$

where V_{OFF} is the gate voltage where the subthreshold region begins, V_{ON} is the gate voltage where the on-state model becomes accurate, and $f(V_{GS}, V_{DS})$ is the unknown functional form that describes the bridge region of operation.

A TCAD device where the BTS were neglected as shown in Figure 3.2 was used to investigate the functional form of the bridge region. Neglecting BTS allows for the ideal case to be looked, where 2D effects can be dismissed. This, in turn, will help uncover the contribution of oxygen vacancies in device electrostatics. Finding a functional form for the bridge is done numerically because there is a lack of an analytical solution near the flatband condition. Thus, the functional form was assessed such that data was matched inside the aforementioned V_{GS} conditions.

As shown by Figure 3.2, the functional form presented in Equation 3.8 provides an excellent fit ($R^2 \approx 0.9958$) to the simulated TCAD data. This provides motivation to pursue the use of this functional form as the potential candidate for the drain current in the bridge region.

$$I_{DS_B} = A \cdot (V_{GS} - V_X)^{\beta} \tag{3.8}$$

where A, V_X, and β are fitting parameters.

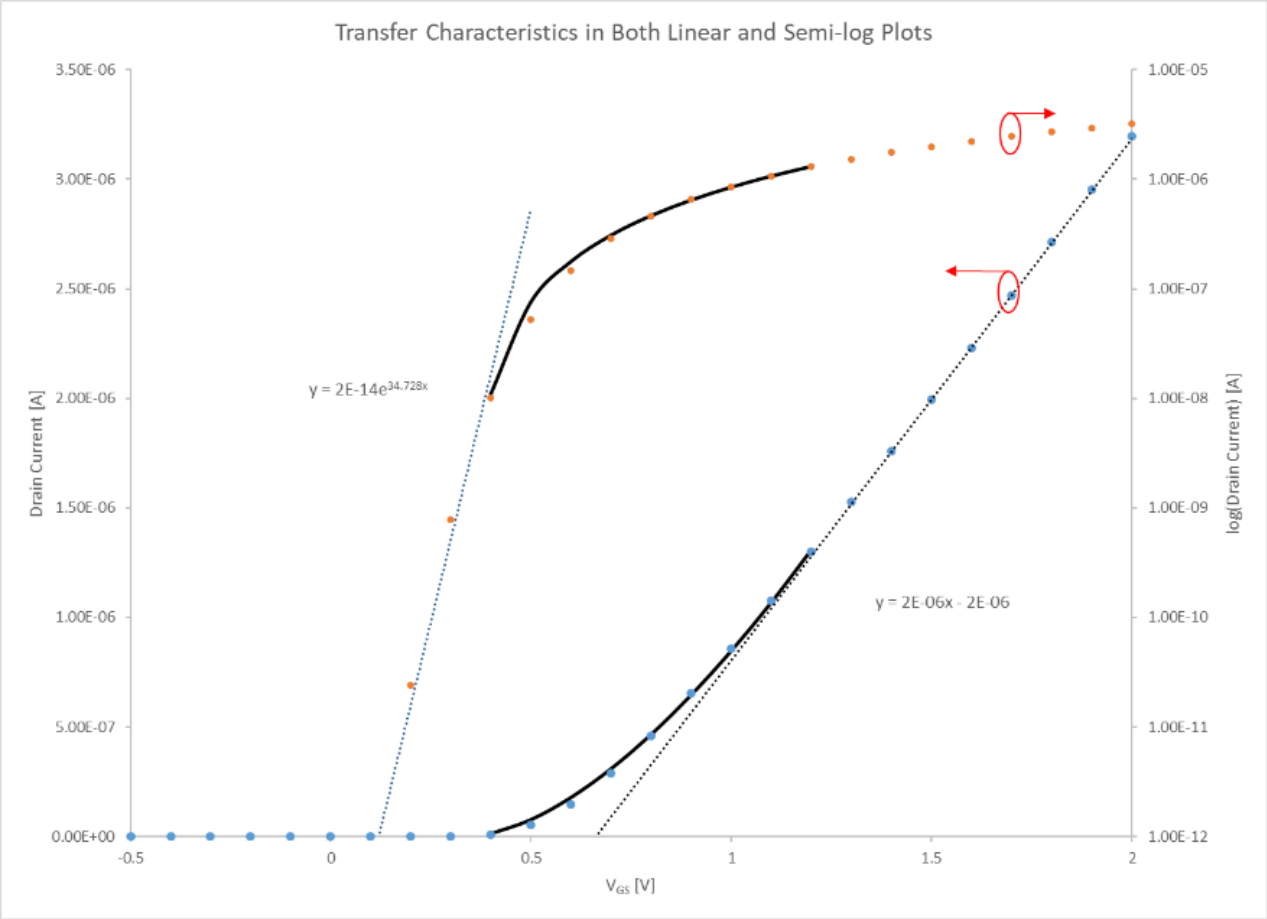


Figure 3.2. Transfer characteristic of a TCAD $\frac{W}{L} = \frac{24\mu m}{4\mu m}$ *device without BTS where* $V_{DS} = 0.1V$*. Bridge region is found to be between 0.4V and 1.3V as the linear and exponential fits show deviation at these two points in the semi-log and linear plots, respectively. Bridge region parameters found for this specific device were* $A = 1.72x10^{-6}\frac{A}{V^{1.7}}$ *,* $V_X = 0.357V, \beta = 1.61$.

3.3 SUBTHRESHOLD REGION & LEAKAGE

With the knowledge gathered thus far, the behavior of the drain current is known at $V_{GS} \geq V_{OFF}$. However, the current behavior has not been discussed below V_{OFF} or the subthreshold region of operation. It is known that the drain current in the subthreshold region of operation shows an exponential behavior. Therefore

$$I_{DS_{SS}} = \mathrm{A_S} \cdot \exp\left(ln(10) \cdot \frac{V_{GS}}{SS}\right) \quad 3.9$$

where SS and A_S are fitting parameter and correspond to the subthreshold swing and the current magnitude at V_{OFF}, respectively. Therefore, to calculate A_S, the current ratio between the bridge region and the subthreshold region needs to be taken at $V_{GS} = V_{OFF}$ such as

$$A_S = \frac{\mathrm{I_{DS_B}}\big|_{V_{GS}=V_{OFF}}}{\exp\left(ln(10) \cdot \frac{V_{OFF}}{SS}\right)} \quad 3.10$$

The exponential relationship provides the functional form for the subthreshold region. However, this functional form does not continue as $V_{GS} \ll V_{OFF}$, as leakage current eventually starts to dominate the I-V relationship. It is also known that leakage is a function of V_{DS}, thus the drain current in the subthreshold region is modeled by Equation 3.11.

$$I_{DS_{SS}} = A_S \cdot \exp\left(ln(10) \cdot \frac{V_{GS}}{SS}\right) + I_{LK}(V_{DS}) \quad 3.11$$

where $I_{LK}(V_{DS})$ corresponds to the leakage current as function of V_{DS}. An empirical model was defined to extract $I_{LK}(V_{DS})$; further details can be found in Chapter 3.4.2.

The final component of the subthreshold model that must be considered is Drain-Induced Barrier Lowering (DIBL). As known, in short enough channels, the drain potential can seep into the source causing the source-to-body potential barrier to become smaller, thus allowing extra current flow into the drain. This effect is also present in IGZO TFTs, however an additional mechanism is operative [24]. In IGZO TFTs, DIBL can be present in short channel devices. However, in long channel devices, a DIBL-like behavior can be present as well. This is not due to

drain-induced barrier lowering as the drain end of the channel is far enough from the source end of the channel to induce field related effects.

In IGZO, trap states play a significant role in the I-V characteristics. IGZO does not present a depletion layer that can provide a potential barrier between source and body. Instead, the lack of space charge provides a perfectly insulated source-to-body connection. Therefore, DIBL-like behavior is caused by the trap states contribution to drain current. The trap states contribution is understood by looking at the contribution of interface traps. Interface traps can be passivated through the manufacturing process. However, coalescence of the traps during the passivation process causes 'passivation islands' to form between the source and drain regions. These 'islands' are regions of perfectly passivated IGZO material, where all the oxygen vacancies have been occupied. This means that the drain bias can cause the potential barrier between these 'islands' to decrease. Therefore, there is an associated increase in drain current due to an increase in drain bias in the subthreshold region. This is referred to as Trap-Associated Barrier Lowering (TABL) [24].

The functional form that was used to model DIBL, and DIBL-like behavior, is a slightly modified version of the one presented by Tsividis [25], and it is shown in Equation 3.12

$$\Delta V_{TABL} = \frac{\Delta V}{\left(1 - \frac{V_{DD}}{V_{DS_{LIN}}}\right)} \cdot \left(-\frac{V_{DS}}{V_{DS_{LIN}}} + 1\right) \qquad 3.12$$

where ΔV is a fitting parameter and its used to fit for the TABL, $V_{DS_{LIN}}$ is the V_{DS} bias used in the triode condition, and V_{DD} is the supply voltage. Thus, the final model for the subthreshold region is given by Equation 3.13

$$I_{DS_{SS}} = A_S \cdot \exp\left(ln(10) \cdot \frac{V_{GS}}{SS} + \Delta V_{TABL}\right) + I_{LK}(V_{DS}) \qquad 3.13$$

DRAIN CURRENT MODEL DEVELOPMENT

Since the drain current model has been broken up into three different regions, the comprehensive piecewise definition of the drain current equation is given by Equation 3.14.

3.4

$$I_{DS} = \begin{cases} I_{DS_{SS}}, & V_{GS} \leq V_{OFF} \\ I_{DS_B}, & V_{OFF} < V_{GS} \leq V_{ON} \\ I_{DS_{ON}}, & V_{GS} > V_{ON} \end{cases} \quad 3.14$$

where

$$I_{DS_{ON}} = \begin{cases} I_{DS_{LIN}}, & V_{DS} < V_{DS_{SAT}} \\ I_{DS_{SAT}}, & V_{DS} \geq V_{DS_{SAT}} \end{cases} \quad 3.15$$

From this point, there are two different approaches that can be followed when solving for I_{DS_B}, an analytical and an empirical approach. For the analytical approach, the accuracy of the on-state model is carried out to the bridge region via its derivative. This is accomplished by solving for the fitting parameters in the boundary conditions V_{OFF} and V_{ON}. For the empirical model, the fitting parameters on the bridge are extracted from measured or simulated data.

3.4.1 Analytical Approach

Given that the accuracy of the on-state model has been validated as shown by Table 2.2, its derivative can provide insight on the prediction of gate-to-source voltage values that are smaller than the described V_{ON} boundary. Therefore, the derivative with respect to the gate-to-source voltage of the bridge model shown in Equation 3.8 can be matched to the derivative with respect to the gate-to-source voltage of the on-state model when the gate-to-source voltage is equal to V_{ON}, which will provide continuity at this point. Moreover, the same can be said for the V_{OFF} boundary and the previously defined subthreshold region current depicted by Equation 3.13. Therefore,

Equations 3.16 and 3.17 show the system of differential equations that need to be solved to find an analytical solution for V_X, and β.

$$\left.\frac{\partial \log_{10}(I_{DS_B})}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} = \left.\frac{\partial \log_{10}(I_{DS_{ON}})}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} \quad 3.16$$

$$\left.\frac{\partial \log_{10}(I_{DS_B})}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} = \left.\frac{\partial \log_{10}(I_{DS_{SS}})}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} \quad 3.17$$

Solving this equation system will allow for continuity when going from one region of operation to the next. However, there is an important distinction that needs to be made. Recall that $I_{DS_{ON}}$ is a piecewise-defined function as shown by Equation 3.15. This will modify Equations 3.16 and 3.17 as the fitting parameters will be different if the gate-to-source voltage value causes the transistor to be in the saturation or the triode region at V_{ON}. Therefore, implementing this modification yields two different equation systems that can be solved in parallel. One for when the drain current converges into the triode region of operation, and another one for then the drain current converges into the saturation region of operation at $V_{GS} = V_{ON}$. These two equation systems are represented by Equations 3.18, 3.19, 3.20, and 3.21.

$$\left.\frac{\partial \log_{10}(f(V_{GS}, V_{DS}))}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} = \left.\frac{\partial \log_{10}(I_{DS_{LIN}})}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} \quad 3.18$$

$$\left.\frac{\partial \log_{10}(f(V_{GS}, V_{DS}))}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} = \left.\frac{\partial \log_{10}(I_{DS_{SS}})}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} \quad 3.19$$

$$\left.\frac{\partial \log_{10}(h(V_{GS}))}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} = \left.\frac{\partial \log_{10}(I_{DS_{SAT}})}{\partial V_{GS}}\right|_{V_{GS}=V_{ON}} \quad 3.20$$

$$\left.\frac{\partial \log_{10}\left(h(V_{GS})\right)}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} = \left.\frac{\partial \log_{10}(I_{DS_{SS}})}{\partial V_{GS}}\right|_{V_{GS}=V_{OFF}} \quad 3.21$$

where Equations 3.18 and 3.19 correspond to the triode region of operation, and Equations 3.20 and 3.21 correspond to the saturation region of operation. This has modified the bridge region such that it now becomes a piecewise-defined function as shown by Equation 3.22.

$$I_{DS_B} = \begin{cases} f(V_{GS}, V_{DS}), & V_{DS} < V_{DS_{SAT}}\big|_{V_{GS}=V_{ON}} \\ h(V_{GS}), & V_{DS} \geq V_{DS_{SAT}}\big|_{V_{GS}=V_{ON}} \end{cases} \quad 3.22$$

where $h(V_{GS})$ and $f(V_{GS}, V_{DS})$ correspond to the functional forms when the bridge converges into saturation, and triode regions, respectively. This is further evidenced by the condition shown in this equation as $V_{DS_{SAT}}$ will be evaluated when $V_{GS} = V_{ON}$ in order to assess the region of operation that the transistor will be on. While the current in the bridge region has been redefined, the functional form will remain the same. This means that the fitting parameters present in Equation 3.8 are changing in response to these new definitions. Therefore, the current in the bridge region becomes redefined as shown by Equation 3.23.

$$I_{DS_B} = \begin{cases} A(V_{DS}) \cdot \left(V_{GS} - V_{X(V_{DS})}\right)^{\beta(V_{DS})}, & V_{DS} < V_{DS_{SAT}}\big|_{V_{GS}=V_{ON}} \\ A_{SAT} \cdot \left(V_{GS} - V_{X_{SAT}}\right)^{\beta_{SAT}}, & V_{DS} \geq V_{DS_{SAT}}\big|_{V_{GS}=V_{ON}} \end{cases} \quad 3.23$$

where $V_X(V_{DS})$, $\beta(V_{DS})$, $V_{X_{SAT}}$, and β_{SAT} are the functional forms to be found at the boundaries V_{OFF}, and V_{ON}, and $A(V_{DS})$ and A_{SAT} are defined by current ratio taken at the V_{ON} boundary as shown by Equations 3.24 and 3.25.

$$A(V_{DS}) = \frac{I_{DS_{LIN}}\big|_{V_{GS}=V_{ON}}}{\left(V_{ON} - V_X(V_{ON}, V_{DS})\right)^{\beta(V_{ON},V_{DS})}} \quad 3.24$$

$$A_{SAT}(V_{GS}) = \frac{I_{DS_{SAT}}\big|_{V_{GS}=V_{ON}}}{\left(V_{ON} - V_{X_{SAT}}(V_{ON})\right)^{\beta_{SAT}(V_{ON})}} \quad 3.25$$

Due to the complexity of the derivative of $I_{DS_{ON}}$, a MATLAB script was defined to provide the solution for V_X, β, $V_{X_{SAT}}$, and β_{SAT}. Details of the script are provided in Chapter 6.1. Transfer and output characteristics generated by the analytical solution are found in Figure 3.3.

The ability of the model to provide a remarkable match to experimental data as is shown by the transfer characteristics. However, as evidenced by the output characteristics, this solution provided non-physical behavior at certain V_{DS} values. This is caused by the V_{DS} dependence of V_X and β as the transistor is still in the triode region when this behavior occurs. While a V_{DS} functional dependence can be attached to I_{DS_B} to ensure that $\frac{\partial I_{DS_B}}{\partial V_{DS}} > 0$ at all times, there are infinite variations of functional forms that could accomplish this. Therefore, finding the V_{DS} dependence instead of using an arbitrary function is a better approach. For this reason, the V_{DS} dependence of V_X and β is found empirically using experimental data in order to find the values that provide the least mean square error fit to the transfer characteristics per V_{DS} basis.

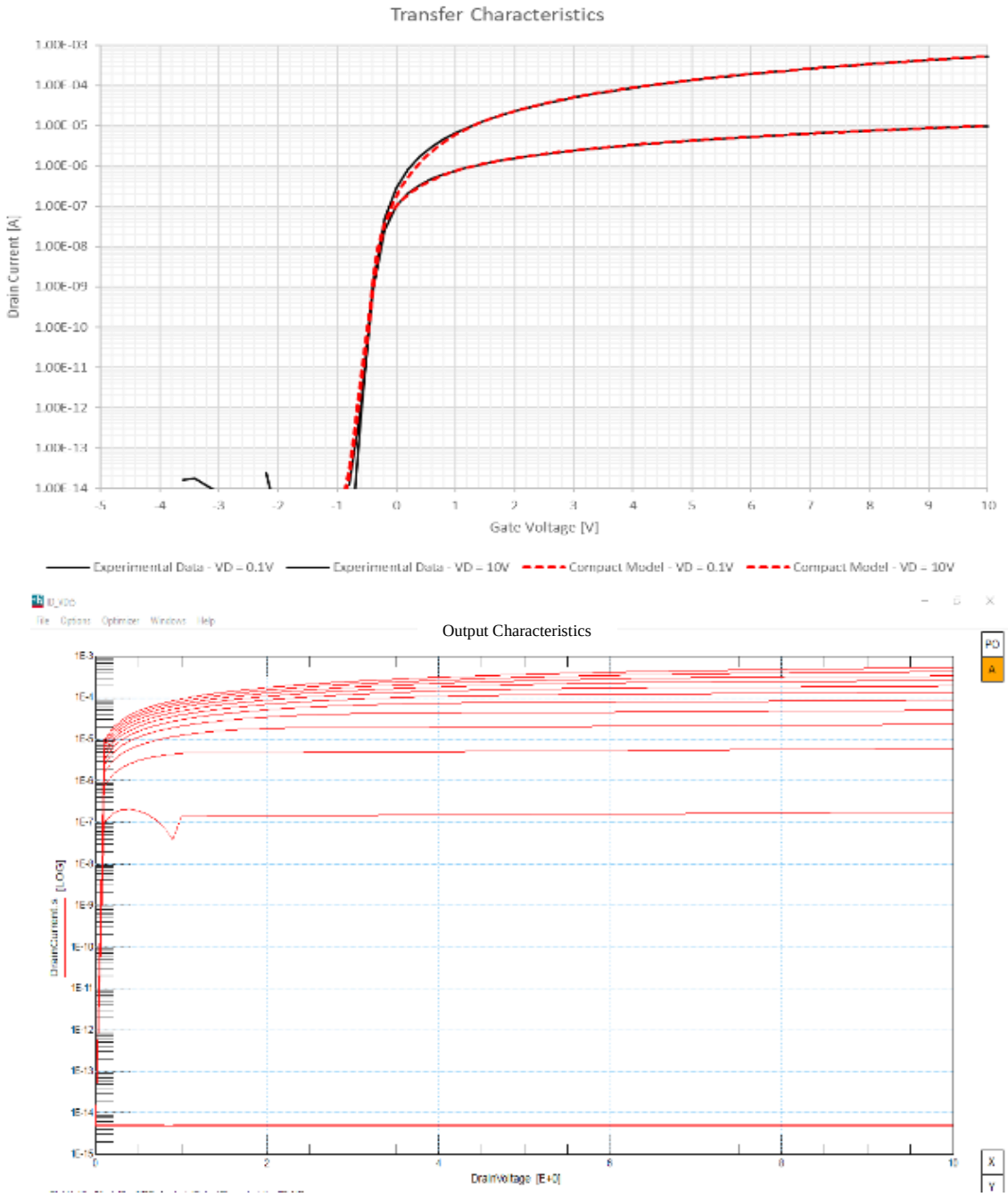


Figure 3.3. Transfer ($V_{DS} = 0.1V$ and $V_{DS} = 10V$) and output characteristics in a semilog plot provided by the closed-form solution for V_X and β (dashed lines in (a) and solid lines in (b)) compared with experimental data (solid lines in (a), not presented in (b)) for a TCAD simulated bottom-gate device with 50 nm of oxide thickness and $\frac{W}{L} = \frac{100\ [\mu m]}{3\ [\mu m]}$ with $V_{ON} = 800\ [mV]$ and $V_{OFF} = -350\ [mV]$. Transfer curves show R^2>0.999.

3.4.2 Empirical Approach

Because of the limitations of the analytical model presented in Chapter 3.4.1, an empirical approach was pursued to find the V_{DS} functional form that describes the fitting parameters A, V_X, and β. Parameter A was decoupled from its original definition shown in Equations 3.24 and 3.25 due to the need of an ever-increasing V_{ON} value to correct for error in the on-state model. However while numerically reasonable, such a high V_{ON} value detracts from the physical significance on-state model. Thus, having A as a degree of freedom in combination with smoothing at the V_{ON} boundary was used to establish the final V_{ON} value.

Due to the nature of empirical models, a parameter extraction algorithm needs to be defined to streamline the process of finding the best values that best describe a given device. Therefore, a MATLAB script was developed to extract these parameters. Details of the parameter extraction algorithm are presented in this chapter, along with any physical interpretation that mathematical analysis is able to provide.

3.4.2.1 V_{ON} & V_{OFF} Extraction

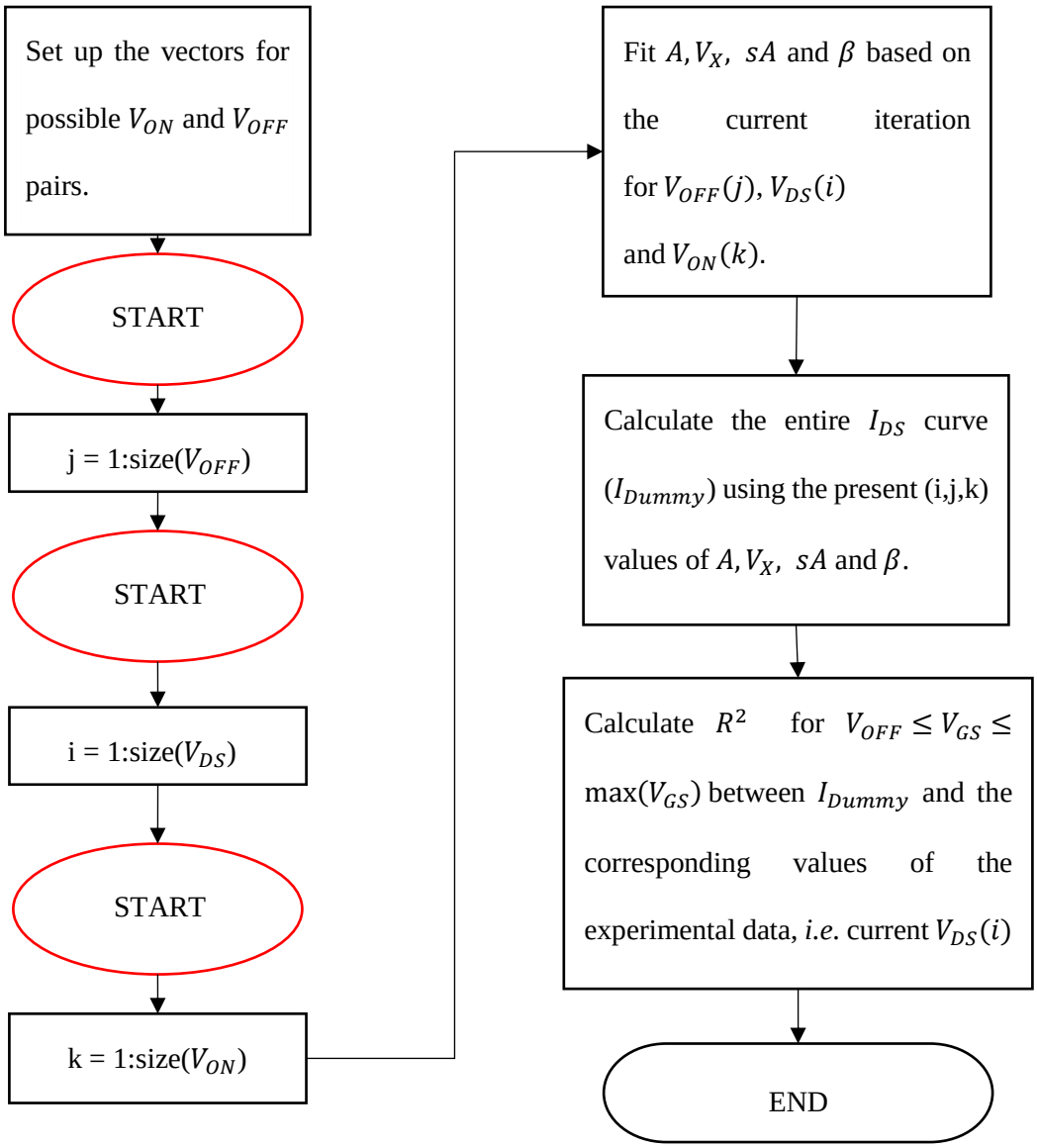


Figure 3.4. Algorithm flowchart for the extraction of the best possible values for V_{ON} and V_{OFF} . Here, three 'for' loops are set up such that all the transfer characteristics that are present in the experimental data are scanned for all the possible (V_{ON}, V_{OFF}) combinations. Three layers are present such that the innermost one is the V_{ON} scan, the middle one is the V_{DS} scan, and the outermost one is the V_{OFF} scan. This allows to search for a V_{ON} value that is consistent at each V_{DS} bias, while keeping V_{OFF} independent of V_{DS} Lastly, sA is a smoothing parameter that is used in a hyperbolic tangent function to serve the purpose of fixing any possible discontinuity at the V_{ON} boundary.

For this model, the fitting parameters are found empirically. Thus, there needs to be a systematic way of obtaining the boundaries such that V_{OFF} and V_{ON} fulfill their respective purpose. This means that V_{OFF} should provide a value such that the subthreshold swing region is matched in the x-axis, and the on-state model stops being used at a value where the derivative is still reasonable, *i.e.* $V_{ON} > V_T$. To accomplish this, an algorithm based on least mean square error was generated as shown in Figure 3.4. The full MATLAB code is disclosed in Chapter 6.2.1.

As depicted by Figure 3.4, the first step is to define the vectors that comprise the possible V_{OFF} and V_{ON} values. Taking V_T as reference, it should be evident that both of the boundaries must be in the vicinity of the threshold voltage. Therefore, these vectors are set as shown by Equations 3.26 and 3.27.

$$V_{OFF} = \langle (V_T - 5 \cdot \Delta V_{GS}),\ (V_T - 4 \cdot \Delta V_{GS}),\ (V_T - 3 \cdot \Delta V_{GS}), \dots, (V_T - \Delta V_{GS}) \rangle \qquad 3.26$$

$$V_{ON} = \langle (V_T + \Delta V_{GS}),\ (V_T + 2 \cdot \Delta V_{GS}),\ (V_T + 3 \cdot \Delta V_{GS}), \dots, (\max(V_{GS})) \rangle \qquad 3.27$$

where ΔV_{GS} is the gate-to-source voltage resolution of the experimental data, and $\max(V_{GS})$ represents the maximum value for the gate-to-source voltage of the experimental data.

For the second step, three nested 'for' cycles are initialized to scan through the V_{OFF}, V_{ON} and V_{DS} vectors. The purpose of this is to fit for the parameters of the bridge region (A, V_X, β, and sA) at each possible linear combination of these values. Here, V_{ON} is considered a function of V_{DS} while V_{OFF} is not. This is expected because the on-state drain current equation can provide a different V_{ON} value as a function of the saturation condition. However, in well-behaved devices, the subthreshold swing occurs at similar gate-to-source voltage values with a negligible drain-to-source voltage influence, sans TABL.

While the introduction of smoothing (sA) has not been discussed in detail, it is necessary to implement when allowing A to become a degree of freedom. A was the parameter that ensured continuity in the V_{ON} boundary as its value was defined as the current ratio between the on-state and the bridge region models. By releasing this constraint, the current equation becomes discontinuous at the aforementioned boundary as shown in Figure 3.5. Note that V_{ON} is still a relatively high value when compared to V_T. This is because this plot was generated without smoothing being accounted when fitting for A, V_X and β.

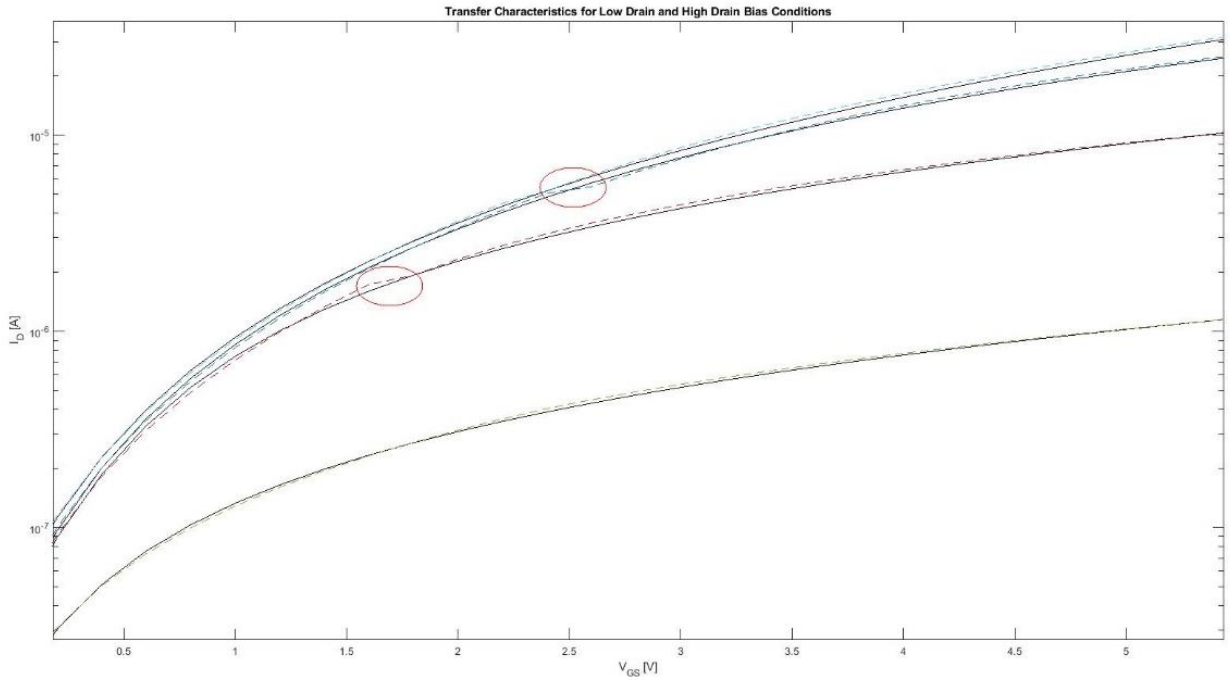


Figure 3.5. Zoomed-in view of the transfer characteristics for a $\frac{W}{L} = \frac{100\mu m}{9\mu m}$ *bottom-gate device with 100nm of gate oxide where* $V_{DS} = 0.1V, 1V, 3.4V$ *and* $10V$. *The discontinuity at the boundary at* V_{ON} *is shown. The bridge region overestimates the current as it approaches the boundary from the left, while the on-state model underestimates the current as it approaches the boundary from the right.*

Smoothing was accomplished by using a hyperbolic tangent function described in Equation 3.28.

$$S_F = \frac{1}{2}\left(1 + \tanh\left(\frac{(V_{GS} - V_{ON})}{sA}\right)\right) \qquad 3.28$$

where S_F is the smoothing function and sA is the smoothing parameter. When considering smoothing while fitting for the three degrees of freedoms in the bridge region, the combination of the on-state and bridge region models are taken into account in order to replicate the experimental data above V_{OFF}. The on-state model always underestimates the current when approaching the V_{ON} boundary from the right, while the bridge model always overestimates the current when approaching the same boundary from the left. Therefore, the linear combination of these two functions allows for a smaller V_{ON} value while still matching the experimental data with a high R^2 value as shown by Figure 3.6.

The third and fourth steps involve calculating the R^2 value for the transfer characteristic at a given V_{DS} bias. The third step looks at the R^2 given by the present (V_{ON}, V_{DS}) pair, *i.e.* the two innermost layers in the design of experiments flowchart. This provides a comprehensive R^2 value that is calculated at each possible (V_{ON}, V_{DS}) pair, which will then be used to establish the specific (V_{ON}, V_{DS}) curve that maximizes R^2. Likewise, the fourth step involves the R^2 calculation throughout the highest drain bias available, *i.e.* the outermost layer in the design of experiments flowchart. The purpose of this assessment is to look at the V_{OFF} values that maximizes this R^2 curve. Note that, for V_{ON}, R^2 is both a function of V_{DS} and V_{ON}. However, for V_{OFF}, R^2 is just a function of V_{OFF} as its assessment is done at the highest drain-to-source voltage available. This avoids floor error measurements in experimental data to meddle with the actual result.

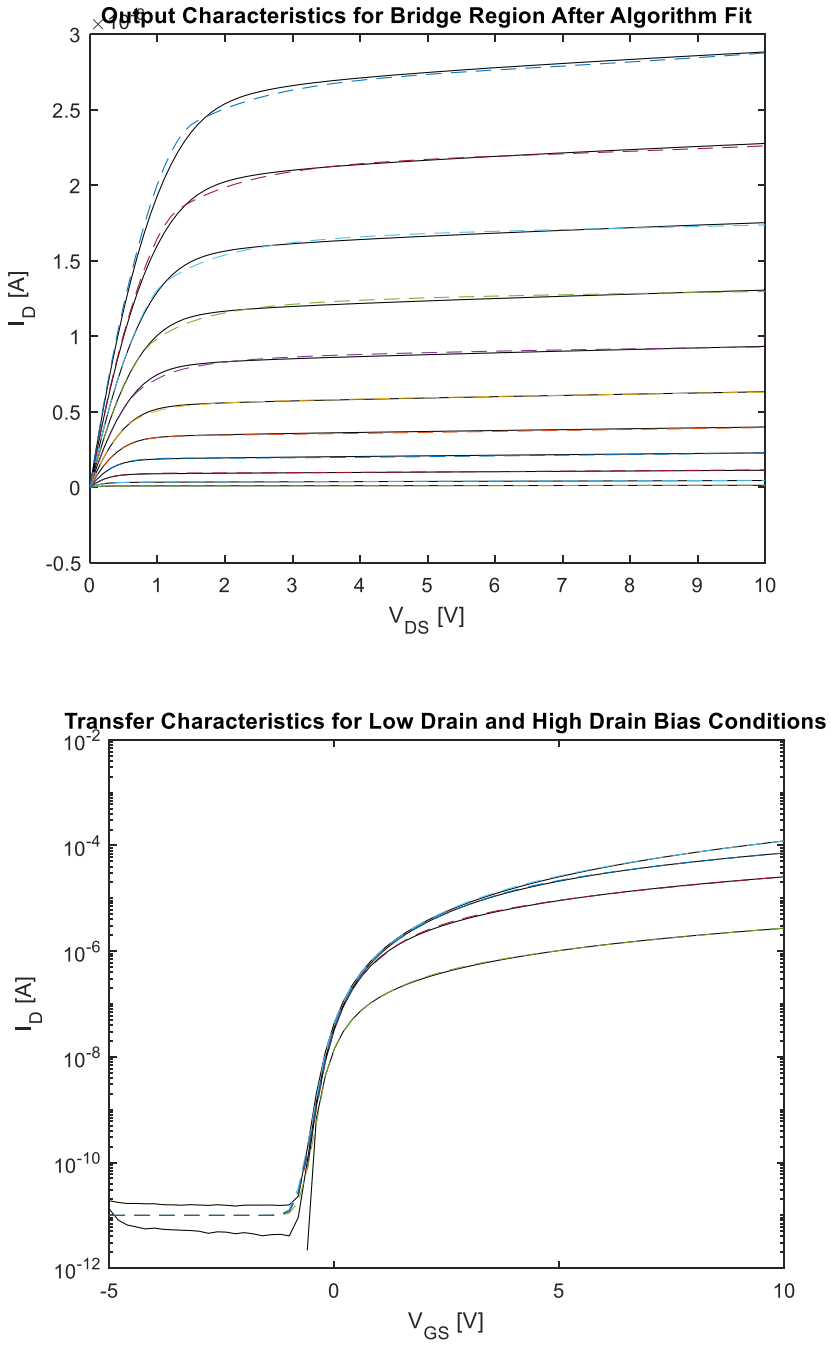


Figure 3.6. Transfer and output charateristics of simulated data (dashed lines) and experimental data (solid lines) showing the values of $V_{DS} = 0.1V, 1V, 3.4V$ *and* $10V$*, and* $V_{GS} = -0.2V, 0.2V, 0.6V,$ *and* $1V$*, respectively. Extracted* V_{OFF} *is* $-0.2V$*. The mean value of* V_{ON} *across* V_{DS} *is* $0.829V$*. This is extracted for a bottom-gate device with* 100 *nm of oxide thickness and dimensions of* $\frac{W}{L} = \frac{100\mu m}{9\ \mu m}$.

Figure 3.6 shows the transfer and output characteristics using a lookup table model that provides the exact values for A, V_X, β, and sA. This fit is the best match that can be provided by the bridge model as each individual transfer curve was fitted as a function of V_{DS} yielding the functional dependence of the bridge fitting parameters. Modeling this functional form is of interest as it could uncover physics that are related with the moderate accumulation region in IGZO TFTs. Therefore, the next steps in the empirical model development are to find the functional forms that describe A, V_X, β, and sA.

3.4.2.2 Bridge V_{DS} Functional Dependence

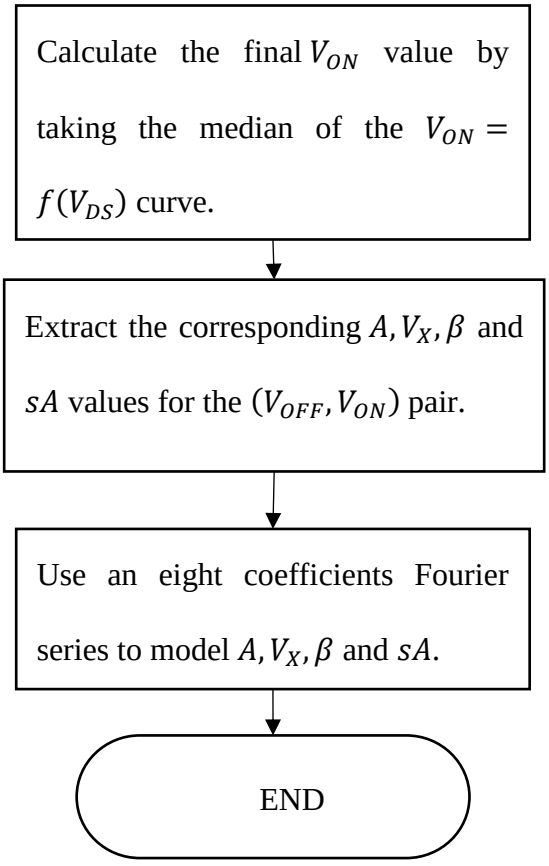


Figure 3.7. Algorithm flowchart for modeling of A, V_X, β and sA.

The first step in the algorithm is to set a constant value of V_{ON} across V_{DS}. The reason why this is needed is to avoid confounding two-dimensional effects when modeling A, V_X, β and sA. Since R^2 for V_{ON} is a function of both V_{DS} and V_{ON}, a systematic way of extracting the $V_{ON} = f(V_{DS})$ curve was designed. As shown by Figure 3.8, there is a point in the curves where the R^2 rate of change is diminished substantially. Therefore, the x-axis value where $\frac{\partial R^2}{\partial V_{ON}} \rightarrow 0$ will provide the V_{ON} at each specific drain-to-source voltage, *i.e.* evaluating the derivative and finding the first value when it approaches at each curve zero will construct the $V_{ON} = f(V_{DS})$ curve.

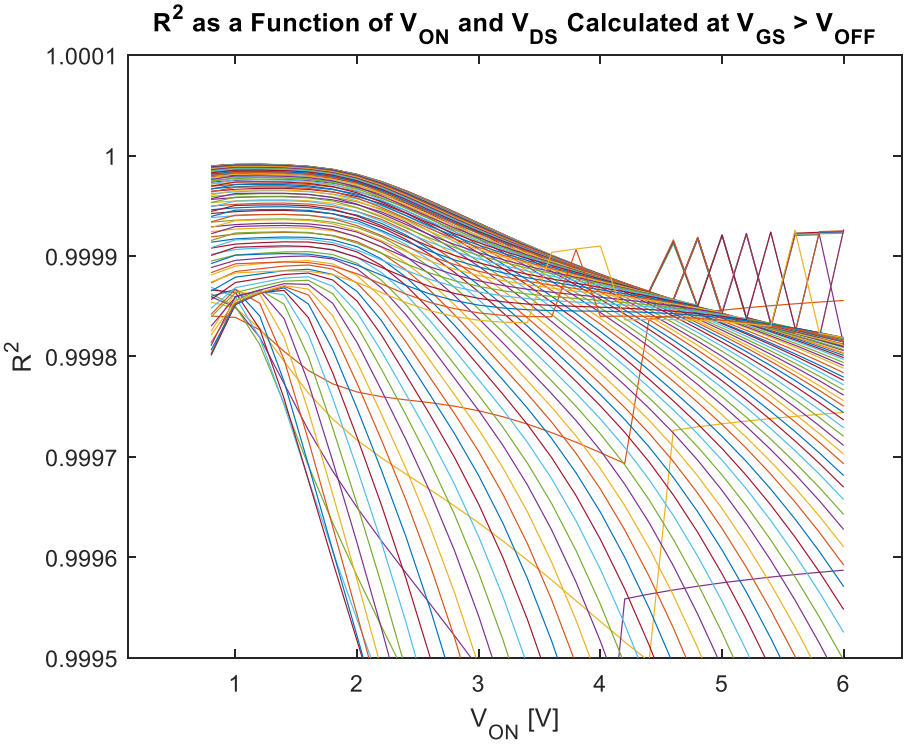


Figure 3.8. R^2 as a function of V_{ON} and V_{DS}, where each curve represents a different V_{DS} value and $0.1 \leq V_{DS} \leq 10V$.

The plot for $V_{ON} = f(V_{DS})$ generated by the aforementioned algorithm is shown in Figure 3.9**Error! Reference source not found.**. To generate a constant value, the mean of this curve is taken. Thus, the value that will be used for V_{ON} from this point is shown in Equation 3.29.

$$V_{ON} = mean\big(V_{ON}(V_{DS})\big) \tag{3.29}$$

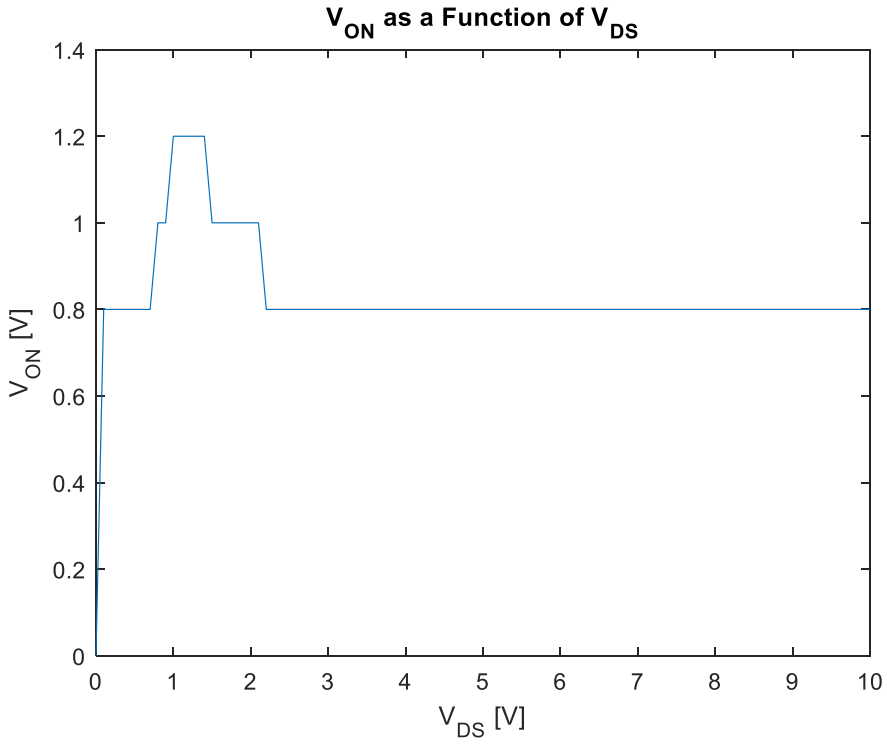


Figure 3.9. V_{ON} as a function of V_{DS} after fitting for the smoothing and the bridge region fitting parameters for a bottom-gate device with 100 nm of oxide thickness and dimensions of W/L=100μm/9μm.

Once the V_{ON} value has been defined, the next step is to extract the data of the fitting parameters from the algorithm that extracts V_{OFF}, and V_{ON}. By taking the outcome of Equation 3.29, the fitting parameters are then extracted at this specific (V_{OFF}, V_{ON}) pair providing the V_{DS} dependence on these two. After extraction, the four fitting parameters are modeled using an eight coefficient

Fourier series to replicate the functional forms that arose from finding V_{OFF}, and V_{ON}. Results from the extraction and the fitting are shown Figure 3.10.

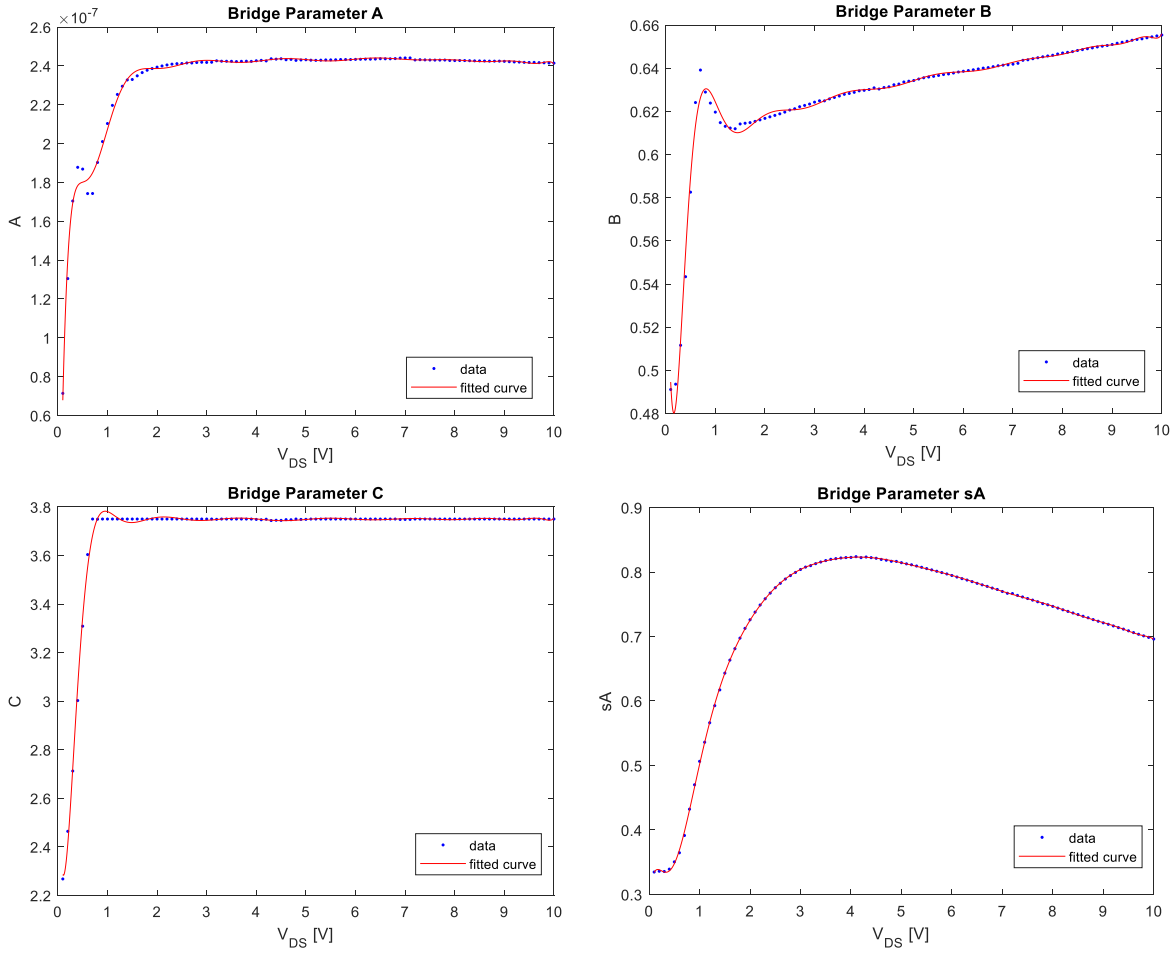


Figure 3.10. Modeling of A(a), V_X(b), β(c) and sA(d) with $V_{ON} = 0.829V$ and $V_{OFF} = -0.2V$ generated by their respective model (solid lines) and experimental data (markers). This is extracted for a bottom-gate device with 100 *nm of oxide thickness and dimensions of* $\frac{W}{L} = \frac{100\mu m}{9\,\mu m}$.

The need for the Fourier series expansion arises from the fact that the functional forms for the fitting parameters are unknown. Therefore, the algorithm should be equipped to handle different variations of these functional forms. For instance, a $\frac{24\mu m}{2\mu m}$ device with 50 nm of gate oxide was

also modeled and the outcome is shown in Figure 3.11. Note that, while the process technology is the same, the different transistor dimensions show a considerable difference in these functional forms.

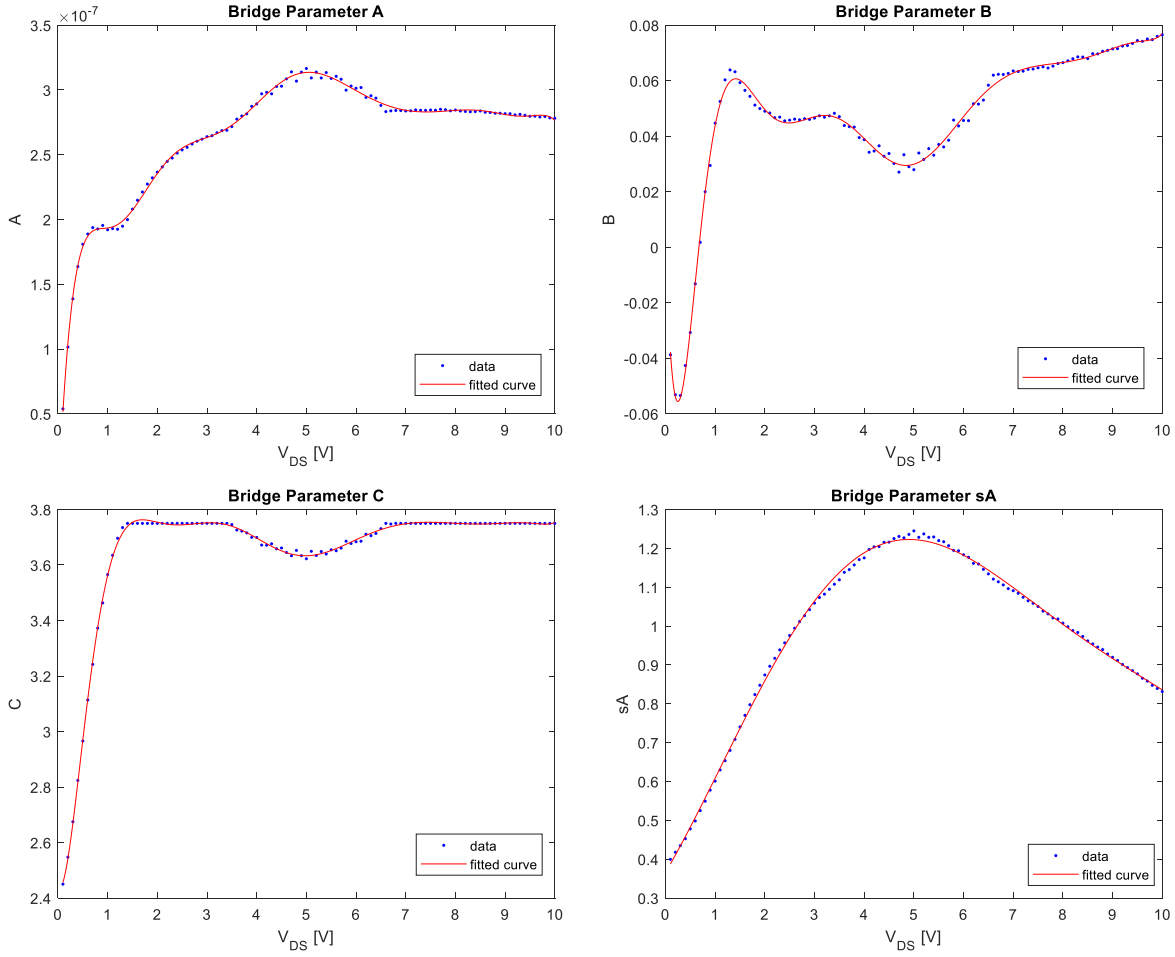


Figure 3.11. Modeling of A(a), V_X(b), β(c) and sA(d) with $V_{ON} = 1.788V$ and $V_{OFF} = 0.4V$ generated by their respective model (solid lines) and experimental data (markers). This is extracted for a bottom-gate device with 50 *nm of oxide thickness and dimensions of* $\frac{W}{L} = \frac{24\mu m}{2\ \mu m}$.

3.4.2.3 Off-state Model & Leakage

The purpose of the off-state model is to be able to model two different phenomena. The first one is related to the leakage current, and the second one is related to DIBL/TABL as it was exposed in Chapter 3.3. The algorithm that was designed to extract the parameters that describe these two mechanisms is shown in Figure 3.12.

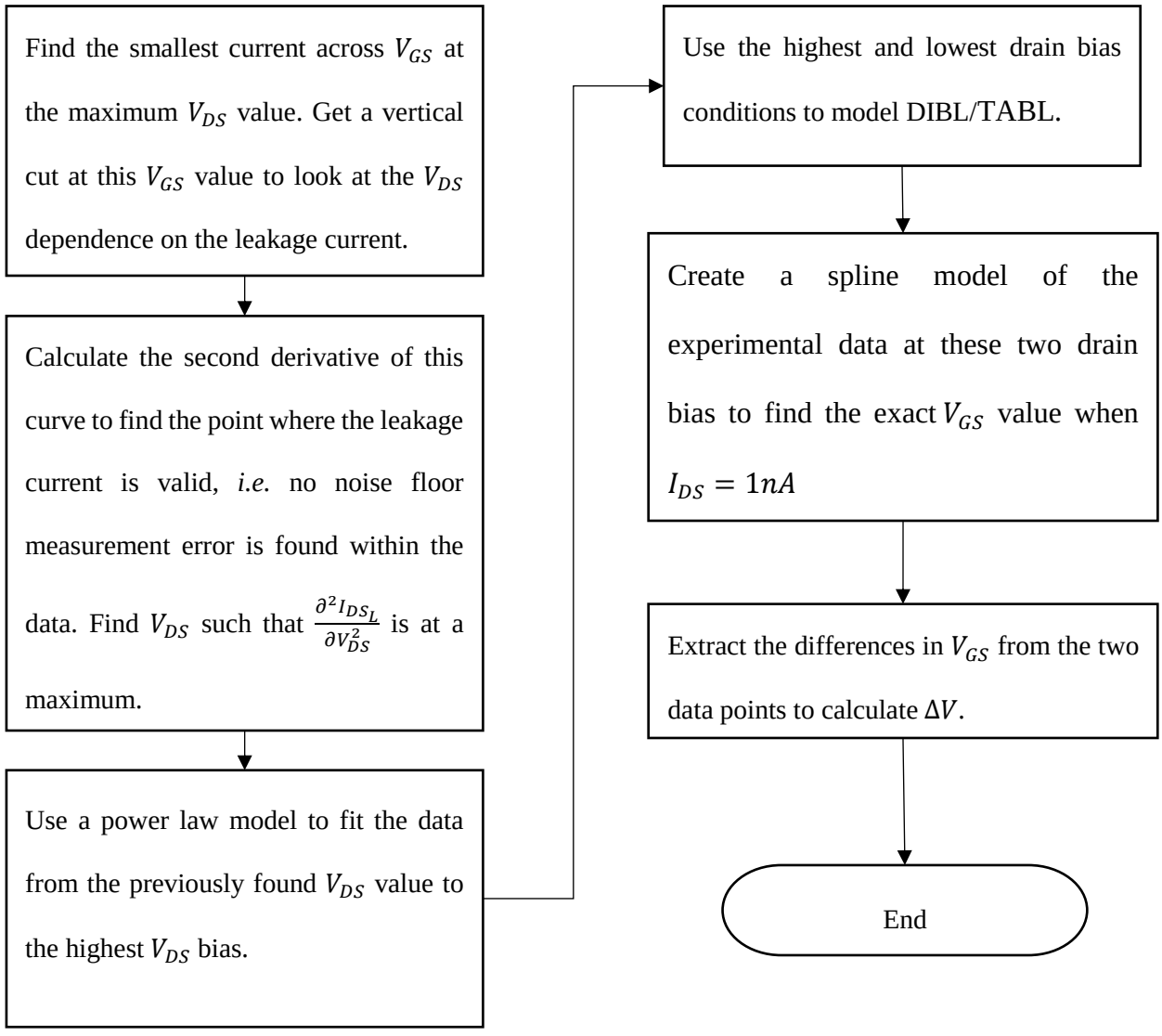


Figure 3.12. Algorithm flowchart for the parameter extraction of the leakage & off-state models

The first step in the algorithm for modeling leakage is to find the transversal cut into the transfer characteristics that will be used to model it, *i.e.* the V_{GS} bias where the drain current is at a minimum in order to avoid confounding effects such as GIDL to contribute into the leakage current. This is shown in Figure 3.13. Since the current cannot increase as V_{DS} decreases, the part of the plot that shows the current magnitude increasing as VDS is decreasing is due to the noise floor of the parameter analyzer used to gather the experimental data.

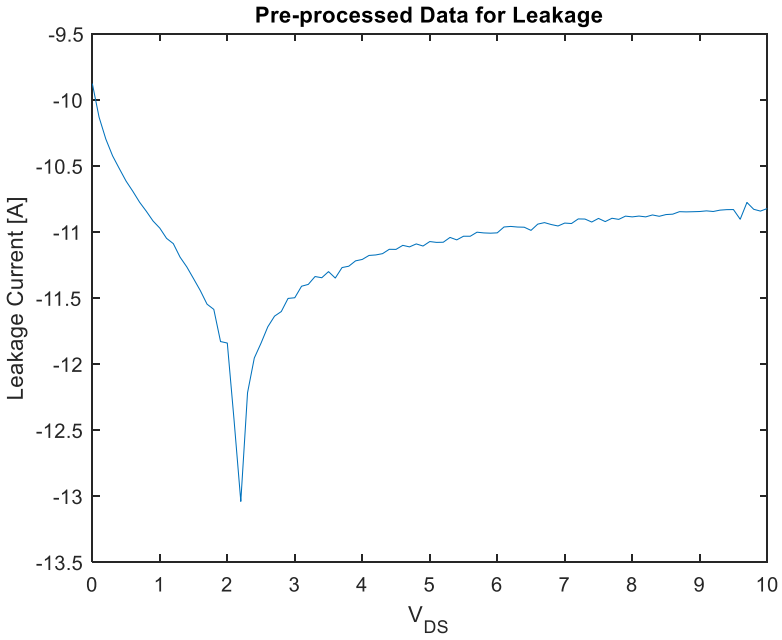


Figure 3.13. Semi-log plot of the absolute value of leakage as a function of V_{DS} where V_{GS} is found by looking at the minimum drain current value in the transfer characteristics for a bottom-gate device with 100 *nm of oxide thickness and* $\frac{W}{L} = \frac{100\mu m}{9\ \mu m}$.

Because of the non-physical behavior, the second step is to find the V_{DS} value $\left(V_{DS_{LK}}\right)$ where the maximum value of $\frac{\partial^2 I_{DS}}{\partial V_{DS}^2}$ occurs at the previously specified V_{GS} value to avoid any floor measurement error during modeling activities. The next step is to define the functional form that is used for the leakage model. This model is defined by Equation 3.30.

$$I_{LK}(V_{DS}) = \begin{cases} L_1 \cdot (V_{DS})^{L_2} + L_3, & V_{DS} \geq V_{DS_{LK}} \\ L_1 \cdot \left(V_{DS_{LK}}\right)^{L_2} + L_3, & V_{DS} < V_{DS_{LK}} \end{cases} \quad 3.30$$

where L_n are fitting parameters. After all of the $V_{DS} < V_{DS_{LK}}$ data is discarded, the model is then fitted for all of the remaining data points as shown by Figure 3.14.

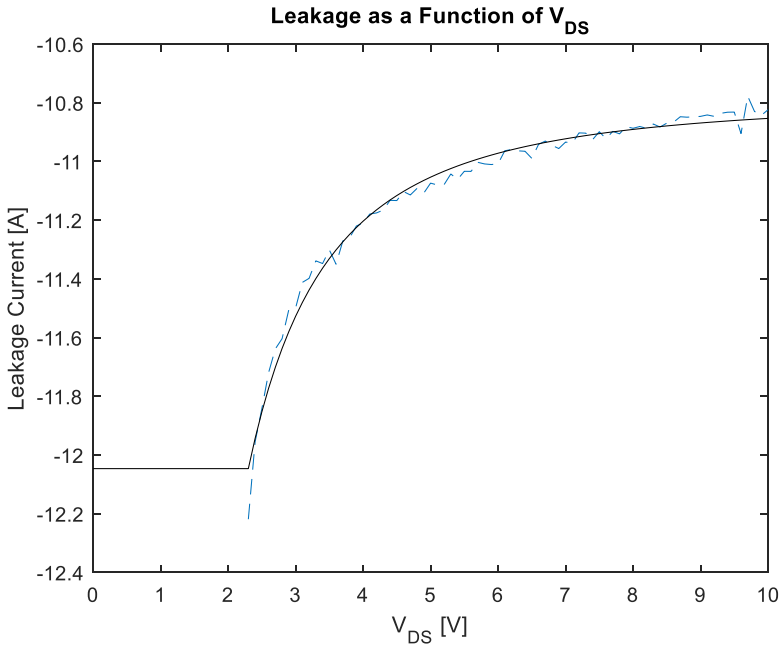


Figure 3.14. Comparison of experimental data (dashed line) with the fitted leakage model (solid line) for a bottom-gate device with 100 nm of oxide thickness and W/L=100μm/9μm.

The need for modeling DIBL/TABL is then presented by looking at a zoomed-in view of the transfer curves shown in Figure 3.15. The simulated subthreshold region shows a diminished separation in between different V_{DS} bias that the experimental data shows, where the highest simulated V_{DS} curve is not able to meet the experimental curve. This is because V_{OFF} was not modeled to be a function of V_{DS}. The reasoning behind this is that a V_{DS} dependent V_{OFF} will have

a confounding mechanism with DIBL/TABL. Thus, to match the experimental data at the highest drain bias in the subthreshold region, DIBL/TABL needs to be modeled.

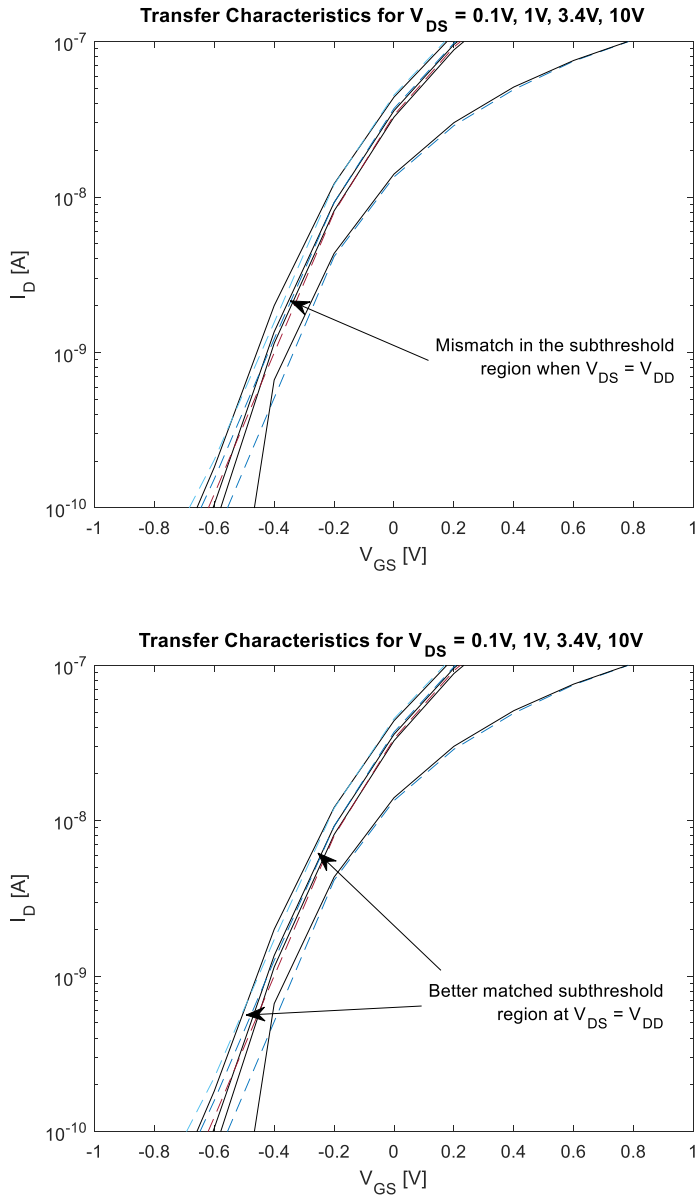


Figure 3.15. Comparison of a zoomed-in view of transfer characteristics where no TABL was modeled (a) and when it was introduced (b) with ΔV=95mV for a bottom-gate device with 100 nm of oxide thickness and W/L=100μm/9 μm.

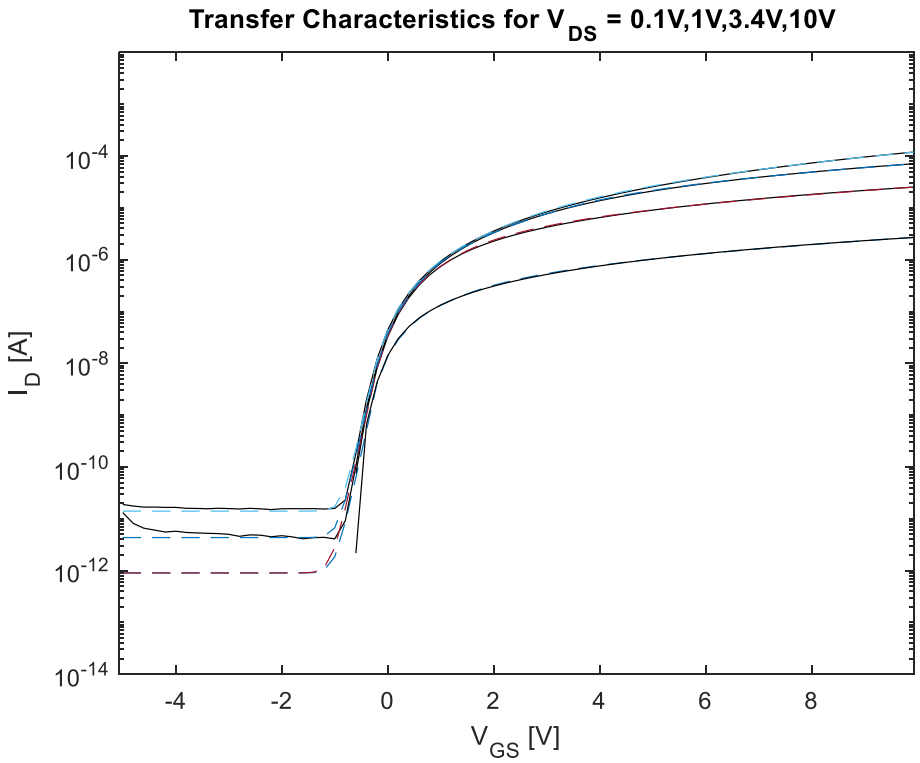


Figure 3.16. Comparison of simulated (dashed lines) and experimental (solid lines) transfer characteristics showing the values of $V_{DS} = 0.1V, 1V, 3.4V$ *and* $10V$ *after leakage and TABL modeling for a bottom-gate device with* 100 *nm of* ***oxi****de thickness and* $\frac{W}{L} = \frac{100\mu m}{9\ \mu m}$.

It is worth noting that most of the aforementioned analysis was done in a single device. However, said device was carefully chosen such that non-ideal characteristics are present. Mechanisms such as TABL, a threshold voltage that approaches zero, compromised on-state where the on-state boundary is much higher than the threshold voltage, and a shallow subthreshold are a few of the characteristics that were present such that the model becomes generalized. The reason is that well-behaved devices will not present these challenges; thus there will be no need for the added degrees of freedom which accounts for these effects. Subsequently, these degrees of freedom will approach zero when going through the routine for these types of devices. Thus, the

empirical model is able to handle better behaved devices through the generalization of modeling a non-ideal device as the one presented throughout this chapter. However, the model is still limited by sound mathematical interpretation of the device physics. The model is not going to be able to provide a reasonable fit for a device that presents large amounts of distortion due to deviations in the manufacturing process,

EMPIRICAL COMPACT MODEL IN VERILOG-A

3.5 Once all of the aforementioned challenges were overcome, a compact model that contains all the different models that were presented throughout Chapter 3.4.2 was coded in Verilog-A. Said code is presented here with all of the parameters that were extracted for a $\frac{W}{L} = \frac{100\mu m}{9\ \mu m}$ bottom-gate device with 100 nm of gate dielectric.

Note that, while MATLAB was able to use the Fourier series expansion for modeling the fitting parameters inside the bridge function, Verilog-A provided a different result when using the same coefficients. This happened because MATLAB and Verilog-A use different resolutions when doing calculations; MATLAB uses 16-bit resolution while Verilog-A uses 32-bit. This discrepancy caused the result of the Fourier series expansion to be entirely different in Verilog-A, and thus invalid. Therefore, a lookup table model was used in Verilog-A with the actual values of the fitting parameters found through MATLAB; without using their functional forms. Note that a different functional form may be found which accurately describes the fitting parameters and maintains consistency between MATLAB and Verilog-A; an example of this is presented in chapter 6, section 6.2.2.

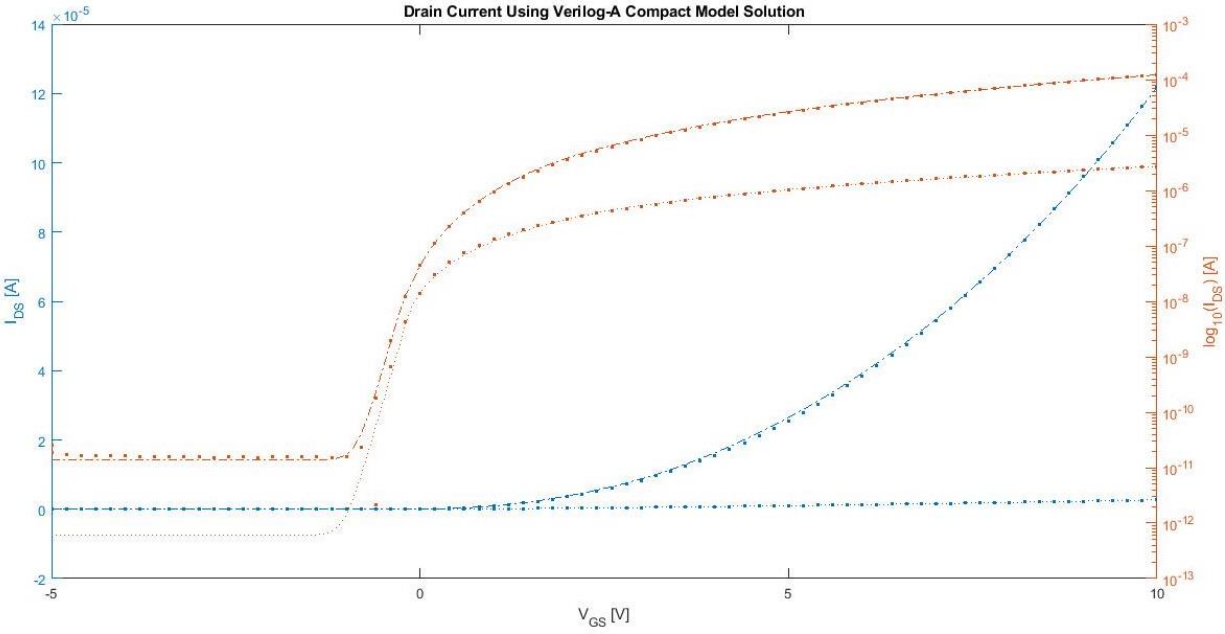
```
// VerilogA for hr8392_har_lib, HAR_IGZO_TFT, veriloga
```

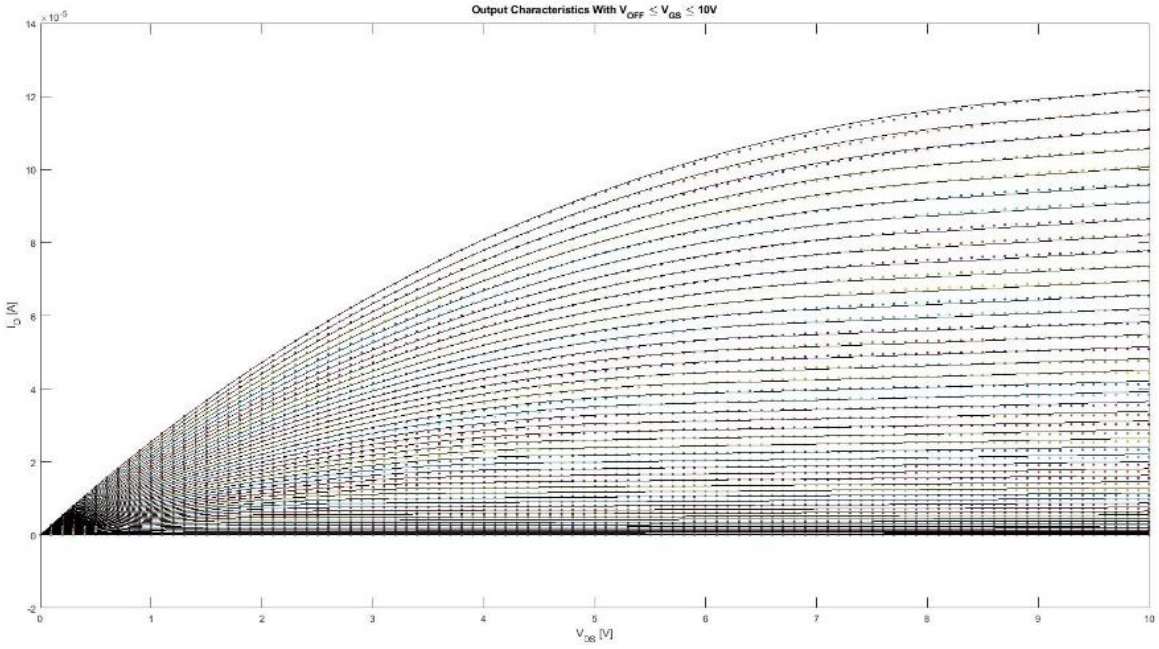
```
`include "constants.vams"
`include "disciplines.vams"

module IGZO_TFT(VS,VD,VG);
         inout                VS,VD,VG;
         electrical           VS,VD,VG;
////////////////////////////////////////////////////////////
// Fitting Parameters for Compact Model
////////////////////////////////////////////////////////////

////////////////////////////////////////////////////////////
// On-state Parameter Definition
////////////////////////////////////////////////////////////
          parameter real Z = 2.538605e+00;
          parameter real THETA_BTS = 9.147266e-02;
          parameter real VT = 3.324605e-01;
          parameter real VBTS = 2.054150e+01;
          parameter real ALPHASCE = 9.610855e-02;
          parameter real LAMBDA = 1.791571e-02;
          parameter real u0 = 1.230000e+01;
          parameter real W = 100;
          parameter real L = 9;
          parameter real TOX = 100;
////////////////////////////////////////////////////////////
// Bridge Parameter Definition
////////////////////////////////////////////////////////////
          parameter real VON = 2.400000e+00;
          parameter real VOFF = -2.000000e-01;
////////////////////////////////////////////////////////////
// Off-state Parameter Definition
////////////////////////////////////////////////////////////
          parameter real VDS_iL = 2.300000e+00;
          parameter real fL_a = -6.652587e+00;
          parameter real fL_b = -1.997697e+00;
          parameter real fL_c = -1.078668e+01;
          parameter real SS = 2.193534e-01;
          parameter real DV = 9.500000e-02;
////////////////////////////////////////////////////////////
// Declaring the VGS and VDS branches
////////////////////////////////////////////////////////////
          branch (VG,VS) VGS_B;
          branch (VD,VS) VDS_B;
          branch (VS,VD) VSD_B;
////////////////////////////////////////////////////////////
```

```
 // Declaring intermediate constants for calculations
 ////////////////////////////////////////////////////////////
           real VGS, VDS, VSD;
           real IOFF, I_B, ID_ON, Leakage;
           real ION, sA, S_F, ChangedSDRegionFlag, A1;
           real A, B, C;
           real DebugFlag;
 ////////////////////////////////////////////////////////////
 // Leakage model
 ////////////////////////////////////////////////////////////
           analog function real LeakCurrent;
                     input VDS, VDS_iL, fL_a, fL_b, fL_c;
                     real VDS, VDS_iL, fL_a, fL_b, fL_c;
                     begin
                               if(VDS >= VDS_iL) begin
                                         LeakCurrent = fL_a*pow(VDS,fL_b) +
fL_c;
                               end else begin
                                         LeakCurrent = fL_a*pow(VDS_iL,fL_b)
+ fL_c;
                               end
                     end
           endfunction
 ////////////////////////////////////////////////////////////
 // On-state drain current model
 ////////////////////////////////////////////////////////////
           analog function real on_state_drain_current;
                     input VDS, VGS, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT,
W, L, TOX, u0;
                     real VDS, VGS, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT,
W, L, TOX, u0;
                     real COX, ETAG, ETAD, VDSAT, ETADSAT, ID_LIN, ID_SAT;
                     begin
                               COX     = (3.9*8.85e-14)/(TOX*1e-7);
                               ETAG    = 1/(Z - THETA_BTS*(VGS - VT));
                               ETAD    = 1/(1 + VDS/VBTS);
                               VDSAT   = sqrt(pow(VBTS,2) + (2/(1 -
ALPHASCE))*(VBTS)*(VGS - VT)) - VBTS;
                               ETADSAT = 1/(1 + VDSAT/VBTS);
                               ID_LIN  = ((W/L)*(COX)*(u0)*(ETAG)*(ETAD)*((VGS
- VT)*VDS - ((1 - ALPHASCE)/2)*pow(VDS,2)))/(1 - LAMBDA*VDS);
                               ID_SAT  =
((W/L)*(COX)*(u0)*(ETAG)*(ETADSAT)*((VGS - VT)*VDSAT - ((1 -
ALPHASCE)/2)*pow(VDSAT,2)))/(1 - LAMBDA*VDS);
                               if(VGS <= VT) begin
```

```
                                        on_state_drain_current = 0;
                                end else if(VDS >= VDSAT) begin
                                        on_state_drain_current = ID_SAT;
                                end else begin
                                        on_state_drain_current = ID_LIN;
                                end
                        end
            endfunction
 ////////////////////////////////////////////////////////////
 // Calculations start
 ////////////////////////////////////////////////////////////
            analog begin
                        DebugFlag = 1;
 // Set the values of VGS and VDS via the access functions
 // Running routine for intercheangable drain/source regions
                        VGS = V(VGS_B);
                        VDS = V(VDS_B);
                        VSD = V(VSD_B);
                        if(VSD>VDS) begin
                                VDS = VSD;
                                ChangedSDRegionFlag = 1;
                        end else begin
                                ChangedSDRegionFlag = 0;
                        end
 //Leakage model calculation by using the analog function LeakCurrent
                        Leakage = limexp(LeakCurrent(VDS, VDS_iL, fL_a, fL_b,
fL_c)*ln(10));
 //Setting the special case of VDS<=0 for leakage definition
                        if(VDS <= 0) begin
                                IOFF  = Leakage;
                                I_B   = Leakage;
                                ID_ON = Leakage;
                                sA    = 1.0;
                        end else begin
 //Bridge model
 // A, B, and C calculations
                                A = $table_model(VDS, "A_data.tbl", "3LC");
                                B = $table_model(VDS, "B_data.tbl", "3LC");
                                C = $table_model(VDS, "C_data.tbl", "3LC");
                                sA = $table_model(VDS, "sA_data.tbl", "3LC");
 // A1 calculation
                                A1     = A*limexp(C*ln(VOFF +
B))/(exp(ln(10)*(VOFF/SS)));
 // Bridge current calculation
                                I_B    = A*limexp(C*ln(VGS + B));
```

```
 //Off-state model
                                IOFF   = A1*limexp(ln(10)*(VGS/SS) +
(10/99)*DV*VDS - DV/99) + Leakage;
 //On-state model
                                ID_ON  = on_state_drain_current(VDS, VGS, Z,
ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0);
                        end
                        S_F = 0.5 + 0.5*tanh((VGS - VON)/sA);
                        ION = (1.0 - S_F)*I_B + S_F*ID_ON;
                        if(VGS<=VOFF) begin
                                if(ChangedSDRegionFlag) begin
                                        I(VS,VD) <+ IOFF;
                                end else begin
                                        I(VD,VS) <+ IOFF;
                                end
                        end else begin
                                if(ChangedSDRegionFlag) begin
                                        I(VS,VD) <+ ION;
                                end else begin
                                        I(VD,VS) <+ ION;
                                end
                        end
            end
 endmodule
```


Drain Current Using Verilog-A Compact Model Solution
$\times 10^{-5}$
I_{DS} [A]
$\log_{10}(I_{DS})$ [A]
V_{GS} [V]


Output Characteristics With $V_{OFF} \leq V_{GS} \leq 10V$
$\times 10^{-5}$
I_D [A]
V_{DS} [V]

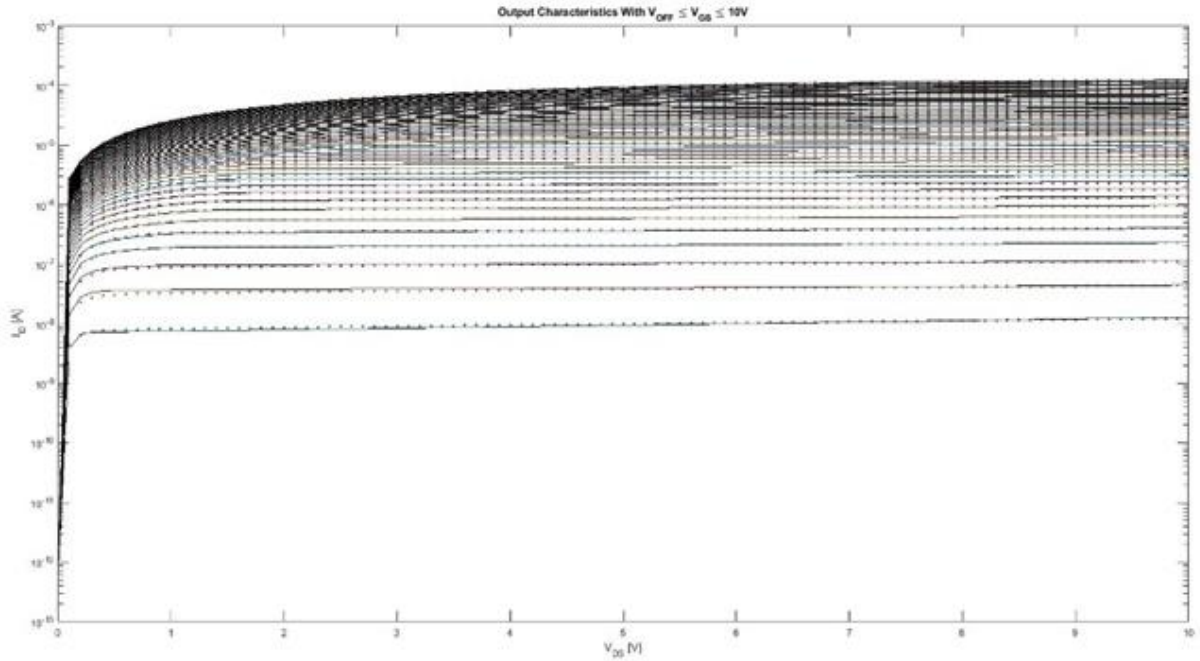


Figure 3.17. Compact model outcome showing (a) transfer characteristics with $V_{DS} = 0.1V$ *and* $V_{DS} = 10V$*, output characteristics with* $V_{OFF} \leq V_{GS} \leq 10V$*, in both linear (b) and semi-log (c) plots where markers represent the experimental data and the solid lines represent the simulated data for a bottom-gate device with* 100 *nm of oxide thickness and* $\frac{W}{L} = \frac{100\mu m}{9\ \mu m}$.

The Verilog-A model was then simulated using Cadence Virtuoso, and the outcome is presented in both transfer and output characteristics as shown by **Error! Reference source not found.**. The empirical model's ability to provide a match to the experimental data in both output and transfer characteristics is remarkable. Non-physical behavior is not present which greatly enhances convergence in circuit simulations. Moreover, the developed model does not present the need for an iterative solution of the system's equations like certain analytical models rely upon, which improves computational performance. Therefore, this is an added advantage which can greatly shorten the simulation duration.

3.6 SUMMARY

The development of a compact model and the introduction of a new definition for a region of operation in IGZO TFTs was presented in this chapter. Two different approaches were carried out when solving for the fitting parameters of the newly defined bridge region of operation. The first entailed an analytical solution where the derivatives with respect to the gate-to-source voltage of the on-state and subthreshold regions of operation were matched to that of the bridge region. The second approach consisted in an empirical model where the fitting parameters are extracted based on experimental data.

The analytical approach revealed that the solution exists such that the derivatives can be equal at the defined boundaries. However, this solution presented non-physical behavior for certain drain-to-source voltage values. This meant that, while the solution exists, it was not appropriate for modeling field-effect transistors. Moreover, finding the correct drain-to-source voltage dependence of the bridge region was an insurmountable task due to the sheer amount of variations that can present the desired behavior. Therefore, an empirical model was developed supported by the insight that the chosen functional form of the bridge can provide continuity at the boundaries.

The empirical approach consisted of different algorithms with the purpose of finding the parameters that best describe a given device in each region of operation: on-state, bridge, and subthreshold. This represented the correct drain-to-source voltage dependence for the fitting parameters in the bridge region without the non-physical behavior issues. However, because the fitting was done in a piece-wise manner, the on-state boundary presented a discontinuity. For this reason, the hyperbolic tangent function was used as a smoothing function in order to overcome

this challenge. Ultimately, the resulting compact model revealed an excellent agreement with experimental data as shown by **Error! Reference source not found.**.

Chapter 4. PIXEL CIRCUIT SIMULATION

As discussed in Chapter 2, the proposed pixel circuit for this work is one that uses a pass transistor to respond to the control signals and provide an output into the driver transistor, where the latter handles the current driving into the light emitting device. This type of topology is known as 2T1C because it uses 2 transistors, and a storage capacitor to keep the gate voltage of the driver transistor at the desired value while the controller is while the controller is addressing other pixels. In this chapter, control signal definition is carried out and the rationale behind the timing constraints is provided. Moreover, the parasitic elements impact on transient simulation is examined to assess the limitations of the current manufacturing process.

4.1 PRINCIPLE OF OPERATION

Ideally, the pixel circuit allows the LED to be turned on when the scan line (addressed as row from this point on) is being addressed and the data line (addressed as column from this point on) is set to a voltage high. If the column is set to a voltage low, the row signal will pass this over to the pixel which would not turn on the light emitting device. However, there are various timing considerations that need to be made to account for the active matrix array scheme. Characteristics such as the number of rows, columns and the intended refresh rate are important factors that play into the operation of the pixel circuit. Equations 4.1 and 4.2 are used to calculate the frequency at which the row and column scans need to occur

$$f_R = \dot{R} \cdot N_R \cdot C_{BR} \tag{4.1}$$

$$f_C = RGB \cdot N_C \cdot f_R \qquad 4.2$$

where f_R is the row frequency, f_C is the column frequency, $\dot{R}$ is the display's refresh rate, N_R is the number of rows, C_{BR} is the color bit rate, N_C is the number of columns, and *RGB* stands for the monochrome or full color display where *RGB = 1* for monochrome and *RGB = 3* for full color. The column frequency is a function of the row frequency because an entire row's data needs to be latched before scanning the next row. Therefore, the column scan needs to be that much faster than the row scan. Note that Equation 4.2 considers that the column data is arriving serially through one data register, and can be relaxed if managed with serial/parallel combinations.

The targeted display size for the purpose of this project is a *380x380* full color display with a *4*-bit color bit rate, *i.e. 16* levels of brightness to accommodate different colors. Taking the case of *60 Hz* of refresh rate, $f_R \approx 365\,KHz$ and $f_C \approx 416\,MHz$. The column frequency becomes prohibitive because of the available off-the-shelf operation frequency of silicon chips. Therefore, a scheme was designed in order to minimize the requirements.

The scheme consists of dividing the entire data vector into smaller vectors that correspond to a 16-bit serial-input-parallel-output shift register. This accomplishes a massive reduction in the column's frequency requirements because smaller 16-bit vectors are addressed simultaneously to fill the entire row's data vector. Thus, the new relationship that describes the requirements for the column's frequency is shown by Equation 4.3.

$$f_C = RGB \cdot 16 \cdot f_R \qquad 4.3$$

where the number '*16*' corresponds to the 16-bit shift registers that are addressed simultaneously. In the specific case of this work, the column frequency requirement is reduced from $f_C \approx 416MHz$ to $f_C \approx 17.6\,MHz$ with the use of *24* 16-bit shift registers to address the 380-bit vector

that comprises the data. The added circuitry allows for a smaller frequency which in turn makes this project achievable using off-the-shelf silicon chips.

The frequency provides information on the timing requirements that IGZO TFTs need to meet to drive a display of the aforementioned specifications. Furthermore, it sheds insight on adequate timings to validate the pixel design through simulation. It is important to look at the behavior that the ideal pixel circuit shows while being driven with signals that resemble real-life operation conditions such as the ones discussed previously. A sample waveform that describes the addressing operation was generated and is shown in Figure 4.1.

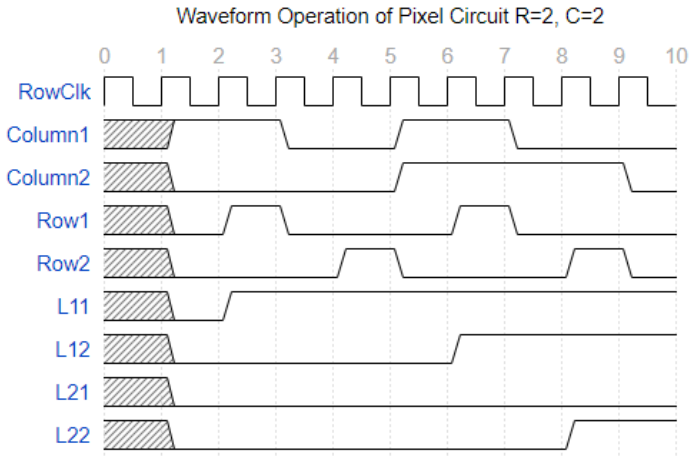


Figure 4.1. Waveform sample of a display with 2 rows and columns where all the columns are latched one clock cycle before the rows are scanned. Signals are described as follows: RowClk is the clock that corresponds to the row driver circuitry, Column1 and Column2 is the data for the first column and second column, respectively; Row1 and Row2 is the output of the first and second row drivers, respectively; L11 corresponds to the LED for the first row and first column, L12 corresponds to the LED for the first row and second column, L21 corresponds to the LED for the second row and first column, and L22 corresponds to the LED for the second row and second column.

It is desirable that all transient effects are related to the row switching. Therefore, the column should always be latched a full clock cycle before the current row is latched. This will diminish any transient related effects that the column switching may have. Furthermore, this allows all the

charge to be readily available to be transferred into the storage capacitor. This, in turn, diminishes transient effects such as propagation delay. The pixel circuit with all of the parasitic elements is shown in Figure 4.2. For the specific case of the ideal simulation, all these parasitic elements were set to zero such as $R_E = C_{ov} = 0$.

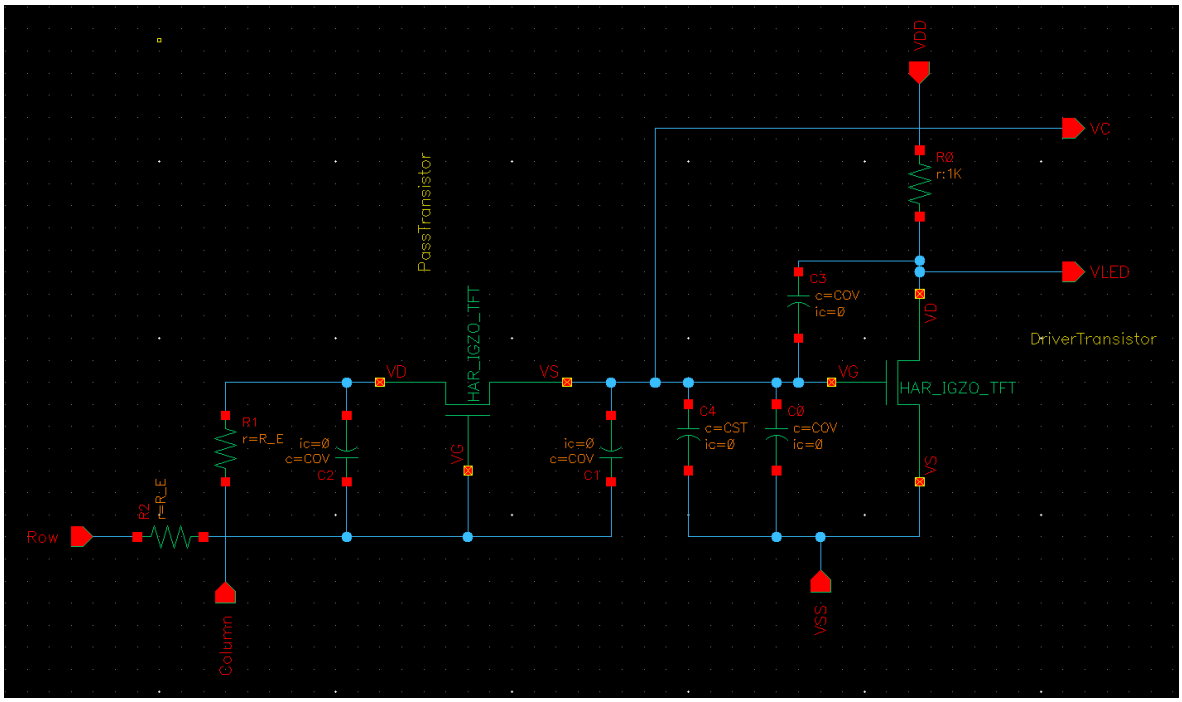


Figure 4.2. Pixel circuit considering parasitic elements such as wire resistances (R_E), and S/D-to-gate overlap capacitances (C_{ov}). The µ-LED is being modeled as a 1kΩ resistor in this case.

The IGZO TFT that is used for this application in both the pass and driver transistor cases is a $\frac{24\mu m}{2\mu m}$ bottom-gate device with *50nm* of gate dielectric; where its *I-V* characteristics (simulated and measured) are shown in Figure 4.3 and Figure 4..

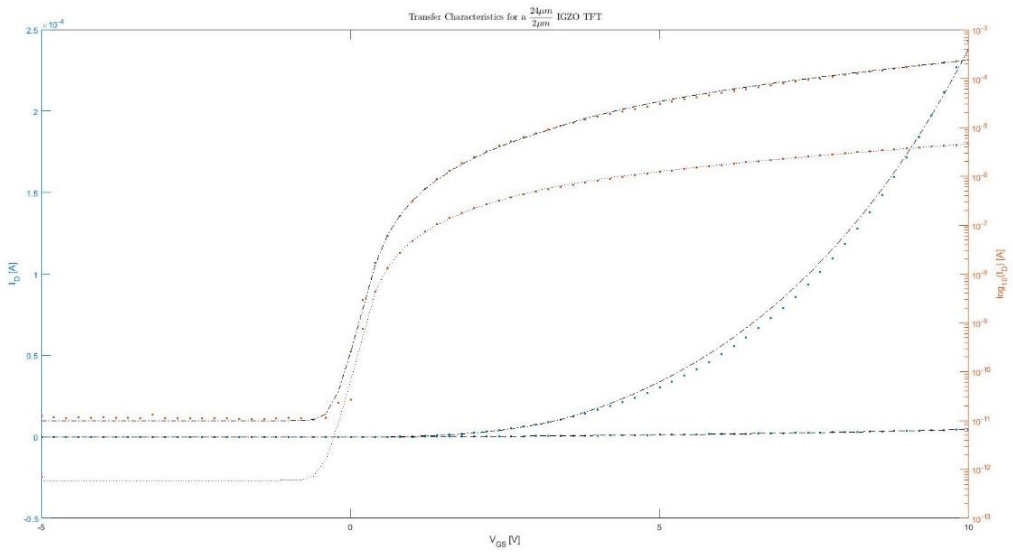


Figure 4.3. Transfer characteristics in both linear and semi-log plots showing both modeled (black lines) and measured data (markers) for a $\frac{24\mu m}{2\mu m}$ *device with 50nm of gate oxide.*

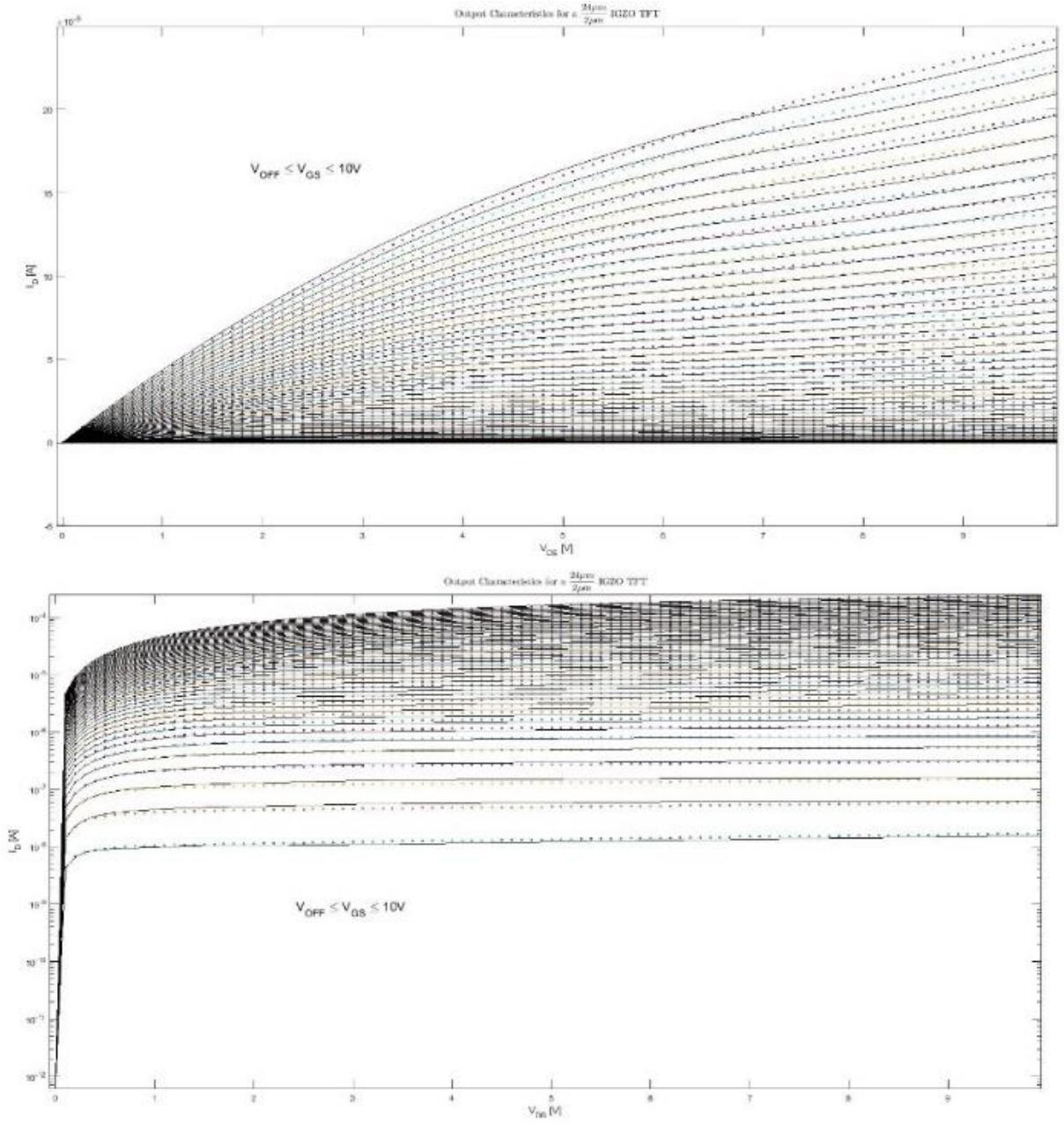


Figure 4.4. Output characteristics in both linear (a) and semi-log (b) plots showing modeled (black lines) and measured (markers) data for a $\frac{24\mu m}{2\mu m}$ *device with 50nm of gate oxide.*

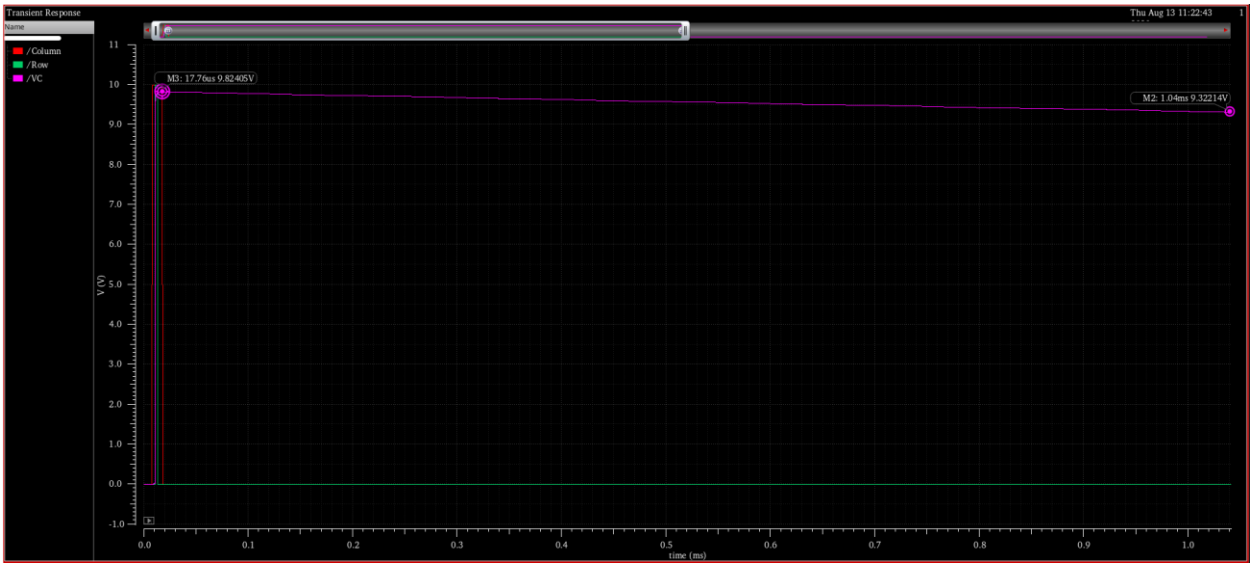


Figure 4.5. Transient simulation of the pixel circuit with parasitic elements set to zero showing the row (green), column (red) and gate of the driver (purple) waveforms. $C_{ST} = 20fF$ for this particular simulation, and ΔV at the end of the row scan is measured at $\approx$0.5V.

As shown by Figure 4.5, the *VC* node, which corresponds to the gate voltage on the driver transistor, responds to the row switching and it transfers the charge that is available in the column into the storage capacitor. This, in turn, allows for the charge to continuously drive the driving transistor even if the row goes to ground. This is the mechanism that will keep the light emitting device, which is modeled as a resistor in this specific case, to keep drawing current even if the row is not being addressed at the time. Thus, the light emitting device will keep emitting light if the column was set at a digital *'high'*. Furthermore, the timing requirements for a complete row scan cycle can be obtained by the row scan frequency: $t_{SCAN} = \frac{1}{f_R} \cdot 380 = 1.041ms$. Over this time period it must be ensured that leakage current doesn't bleed much charge off the *VC* node and subsequently reduce the amount of current drawn by the LED.

4.2 IMPACT OF PARASITIC ELEMENTS

Everything that has been discussed thus far has been related to the ideal case of the pixel circuit where parasitic elements are non-existent. However, in real-world applications, parasitic elements play an important role in any network that needs to be manufactured monolithically. Therefore, in this chapter, the addition of parasitic elements into the network will be done systematically and an assessment on the impact of each element will be discussed.

4.2.1 Charge Sharing

By setting $C_{ov} > 0$ as shown in Figure 4.2, the effect of source/drain-to-gate overlap capacitance can be investigated. However, the exact number needs to be discussed as it presents a distinctive behavior when this capacitance is introduced into the network. For this process technology, $10\mu m$ S/D-to-gate overlaps are used to accommodate for process bias. This translates into a parallel plate capacitor with an area of $10\mu m \cdot 44\mu m (24\mu m + 20\mu m$ overlap) and a dielectric in between composed of a silicon dioxide layer of 50nm. Thus, the capacitance is given by

$$C_{ov} = \epsilon_{si} \cdot \frac{A}{t} = (11.7) \cdot \left(8.85x10^{-14}\frac{F}{cm}\right) \cdot \frac{(10x10^{-4}cm) \cdot (44x10^{-4}cm)}{50x10^{-7}cm} = \ 911.196fF$$

therefore, C_{ov} needs to be set at this value to assess the impact on the pixel simulation. Furthermore, C_{ST} needs to be modified accordingly to ensure proper circuit functionality. Since it is unknown what a proper value for the storage capacitor is, it is set to $C_{ST} = C_{ov}$ to assess the impact of the introduction of overlap capacitance.

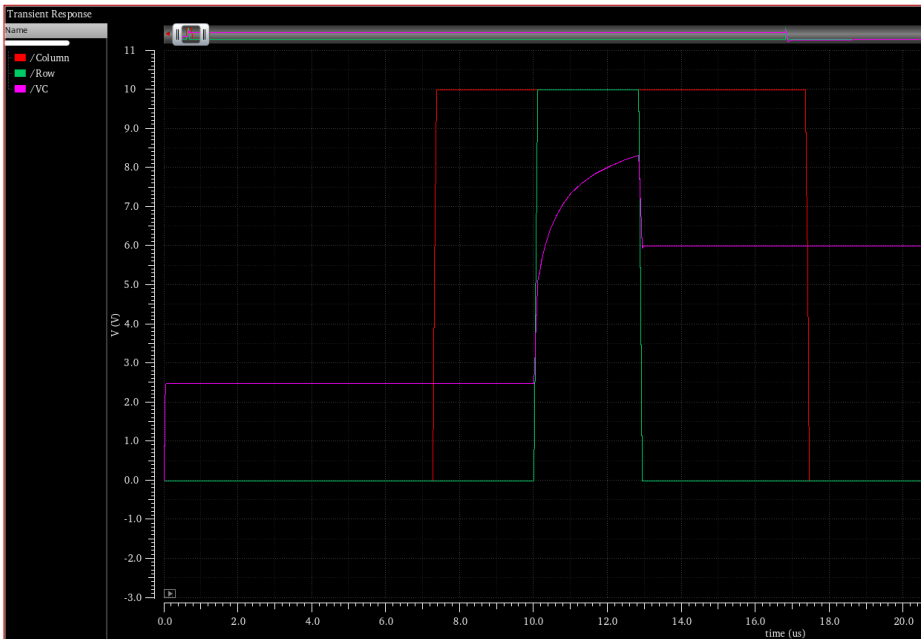


Figure 4.4. Transient simulation of pixel circuit considering overlap capacitances ($C_{ST} = C_{ov} = 911.196\ fF$) and keeping the series resistance at zero ($R_E = 0$). The waveforms correspond to the column (green), row(purple), and the gate of the driver(cyan).

As shown by Figure 4.4, the introduction of overlap capacitances causes two different mechanisms. The first occurs when both the row and column signals at are zero volts at the start of the simulation. This occurs because of a voltage divider that occurs between the VLED and *VC* nodes as showcased in Figure 4.2. This means that increasing the capacitance ratio $\left(\frac{C_{ST}}{C_{ov}}\right)$ would diminish this effect. The second mechanism is due to the row switching. When the row is at zero, the row node is now at ground, which subsequently connects the output capacitance of the pass transistor with the input capacitance of the driver transistor in parallel. Therefore, as soon as the row reaches zero volts, the charge that was accumulated in the gate of the driver gets shared in between these two capacitances. Thus, the input capacitance of the driver transistor needs to be maximized to ensure that the charge stays in the *VC* node. However, too large of a capacitance will increase the R-C delay beyond the transient time requirement.

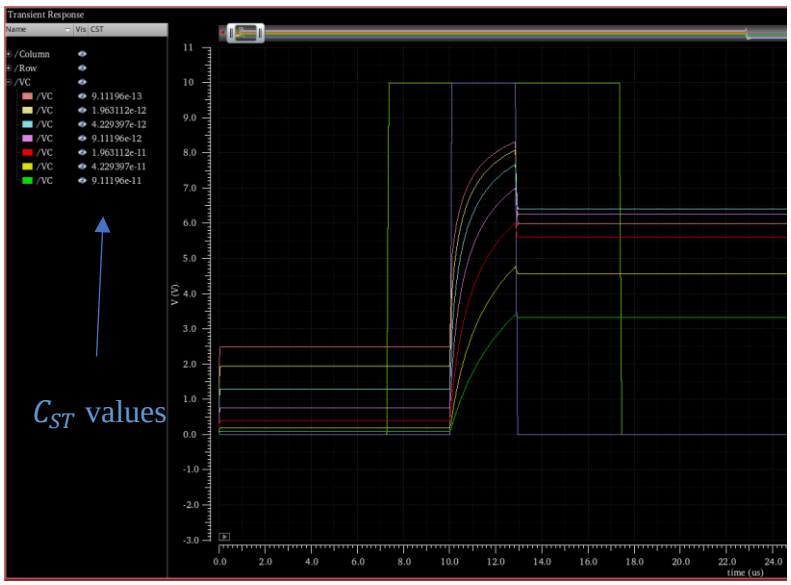


Figure 4.5. Pixel circuit transient simulation showing the response of the gate of the driver transistor when $911.196fF \leq C_{ST} \leq 91.119pF$*. The waveforms correspond to the column (yellow), row (blue), and the gate of the driver (multiple colors, each represent a different storage capacitor value).*

As shown by Figure 4.5, the input capacitance of the driver was then varied as $911.196fF \leq C_{ST} \leq 91.119pF$ to find the best capacitance ratio for circuit functionality. It must be appreciated that the overlap capacitance is the limiting factor in this scenario. The storage capacitor gets to such a high value that it can limit the voltage increase due to the VLED and *VC* voltage divider. However, at this point, the capacitance that is tied to *VC* is so large that it prevents the full voltage swing from occuring. Therefore, the overlap capacitance needs to be decreased to accomplish full voltage swing. Thus, the overlap capacitance is then modified to a $4\mu m$ by $32\mu m$ overlap. The resulting capacitance from this change is then calculated as

$$C_{ov} = \epsilon_{si} \cdot \frac{A}{t} = (11.7) \cdot \left(8.85x10^{-14}\frac{F}{cm}\right) \cdot \frac{(4x10^{-4}cm) \cdot (32x10^{-4}cm)}{50x10^{-7}cm} = 265.07fF$$

which results in 70.9% reduction in the overlap capacitance. This requires aggressive design rules such as the aforementioned $4\mu m$ overlap capacitance. This process bias is required due to the lithography process, and reducing it further may provide detrimental effects to the ohmic behavior of the source/drain connection with IGZO. The circuit was simulated again using the condition $C_{ST} = C_{ov} = 265.07fF$ and the outcome is shown in Figure 4.6.

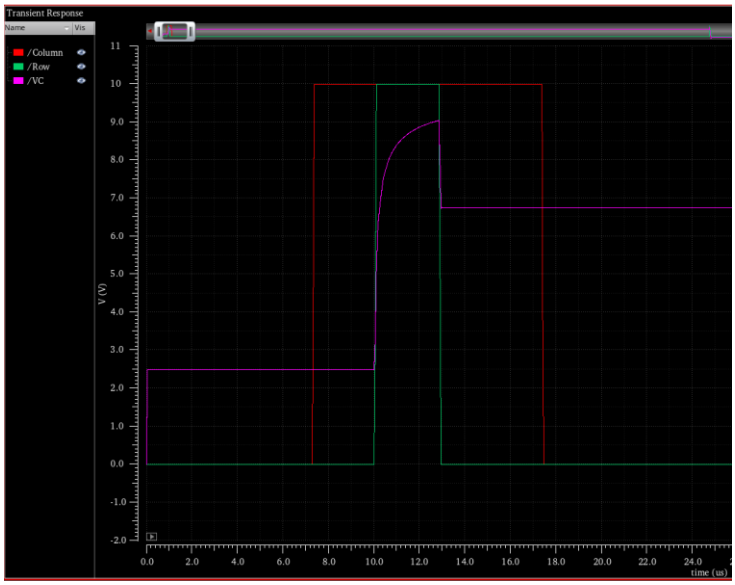


Figure 4.6. Pixel circuit transient simulation considering an overlap capacitance given by a $4\mu m$ *by* $4\ \mu m$ *overlap, and considering the storage capacitor as* $C_{ST} = C_{ov} = 265.07fF$.

The similarities between Figure 4.6 and Figure 4.4 provides further support that the capacitance ratio is driving the circuit behavior. Therefore, the experiment that was done for Figure 4.5 was repeated. However, for this case, the storage capacitor was varied such as $265.07fF \leq C_{ST} \leq 26.507pF$ and the resulting family of waveforms is shown in Figure 4.7. In contrast with Figure 4.5, Figure 4.7 shows that the highest capacitance ratio does not limit the charging of the *VC* node. However, it can be appreciated that smaller capacitance ratios suffer from a higher voltage loss

due to charge sharing. Thus, as previously stated, it is important to establish the best capacitance ratio that diminishes this charge sharing phenomenon.

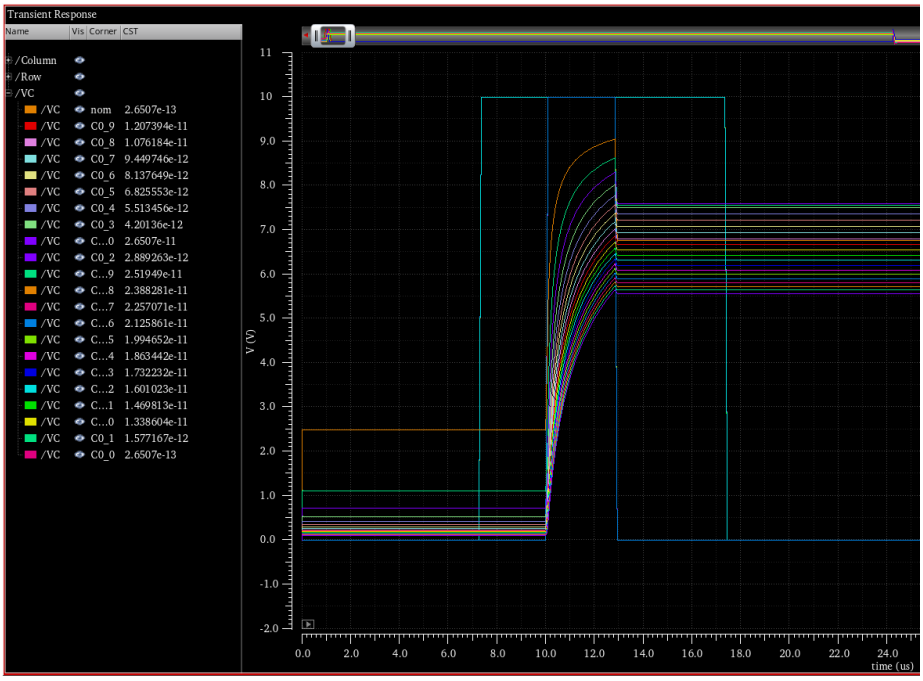


Figure 4.7. Pixel circuit transient simulation showing the response of the gate of the driver transistor when $265.07fF \leq C_{ST} \leq 26.507pF$*. The waveforms correspond to the column (yellow), row (purple), and the gate of the driver (multiple colors, each represent a different storage capacitor value).*

The voltage waveform family was measured at three different points to assess what is the best capacitance ratio that diminishes the charge sharing and the voltage divider phenomena. The first measurement was done at the start of the simulation where both row and column are at zero when $t = 4\mu s$. The second measurement was done right before the row falls to zero, *i.e.* at the end of the transient when $t = 12.84\mu s$. The third measurement was done right after charge sharing has happened when $t = 15\mu s$. As shown by Figure 4.8, the best capacitance ratio is ≈ 40, which diminishes the voltage loss due to charge sharing and the voltage increase due to the voltage divider to $223mV$. Moreover, it shows a higher charge retention than a capacitance ratio of ≈ 50 due to

an overall smaller capacitance. Therefore, it is concluded that a $4\mu m$ by $32\mu m$ overlap capacitance (i.e. 265.07fF) with a storage capacitor value of $10.6pF$ is the preferred process technology for the specific application of a *380* by *380* full color display with a refresh rate of *60Hz*.

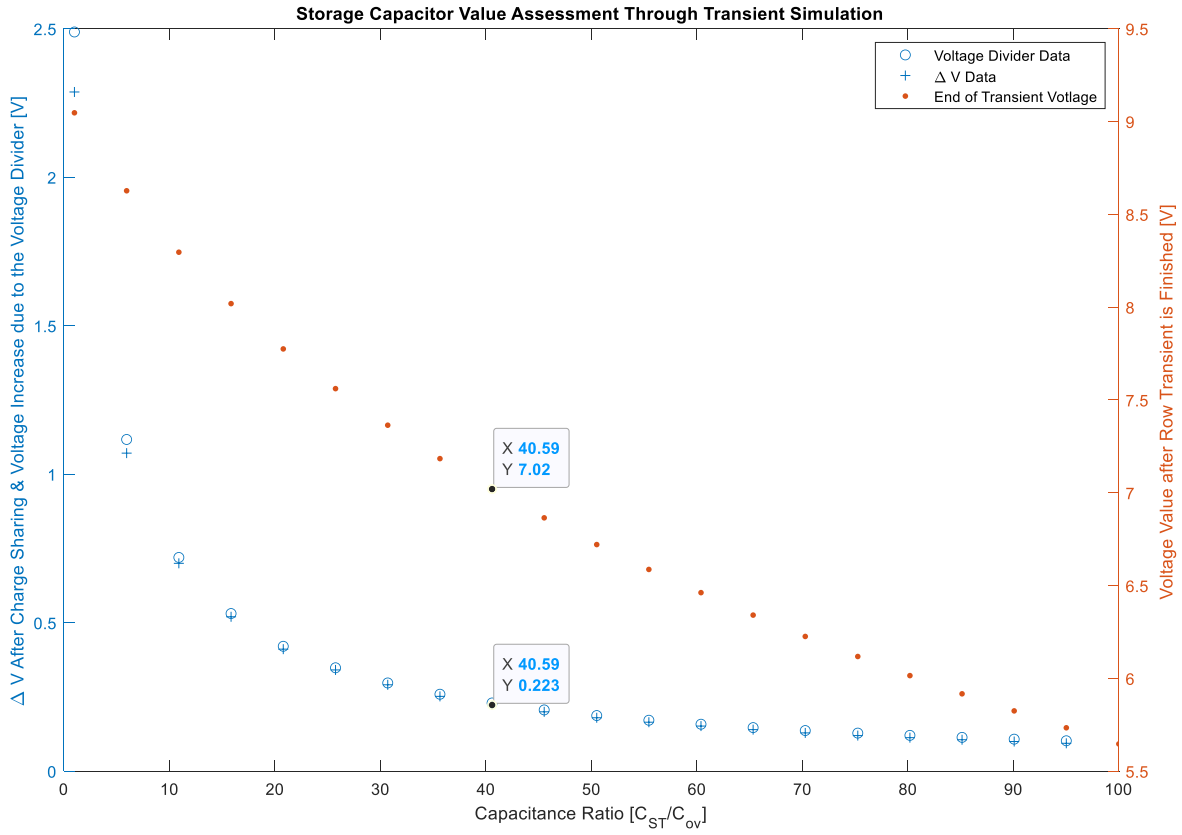


Figure 4.8. Transient simulation measurements for storage capacitor value assessment. The voltage loss due to charge sharing ("+" markers in y1-axis), the voltage increase due to charge sharing ("O" markers in y1-axis), and the final voltage after the row transient is done (orange markers in y-2 axis) are presented.

4.2.2 Rise and Fall Time

On top of considering overlap capacitances, the source/drain series resistances can cause adverse effects on the pixel circuit response. Setting $R_E > 0$ allows for this effect to be investigated. Since it is important to have a baseline operation assessment before the introduction of series resistances, the pixel circuit was simulated with the specifications that were obtained in the previous section. This simulation is shown in Figure 4.9, and it represents the transient simulation of the pixel circuit with $C_{ST} = 10.6pF$, $C_{ov} = 265.07fF$ and $R_E = 0$. Two important measurements were done from this waveform. The first one corresponds to the voltage that the gate of the driver converges to once the row transient is done, and was measured at *6.8V*. The second one corresponds to the rise time, *i.e.* the time it takes for the *VC* signal to swing from 20 to 80 percent of its final value, and it was measured at *971.1ns*.

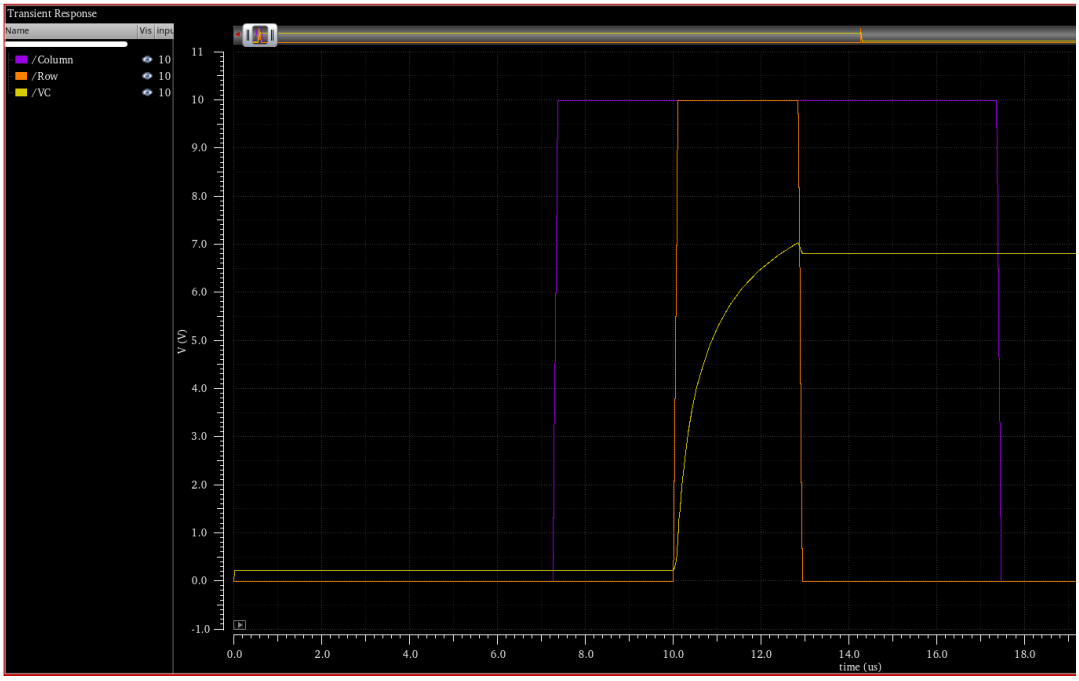


Figure 4.9. Pixel circuit transient simulation showcasing the rise time at 971.1ns with $C_{ST} = 10.6pF$, $C_{ov} = 265.07fF$, *and* $R_E = 0$.

Furthermore, the fall time was also benchmarked using the same specifications shown in Figure 4.9, and the result is shown in Figure 4.10. Fall time with $R_E = 0$ was measured at *1.13µs* with a final voltage value of *1V*. Note that the falling transient is unable to provide a full voltage swing, *i.e.* the *VC* node does not fall all the way to zero. This is due to the large capacitances associated with the *VC* node. However, design rules are already aggressive as presiously stated. Further work is needed to design devices where overlap capacitances can be diminished such as self-aligned devices. Likewise, increasing the voltage supply could also aid in circumventing these issues. For the purpose of assessing the introduction of series resistances, the zero for the falling transient will be taken as *1V* in this work. This is non-ideal, and thus it is known that proper circuit functionality is not achieved. A parameter sweep was done where R_E was changed from 1Ω to $1M\Omega$ to find the series resistance value that has an impact on the transient. The outcome of the experiment is shown in the waveforms presented in Figure 4.11.

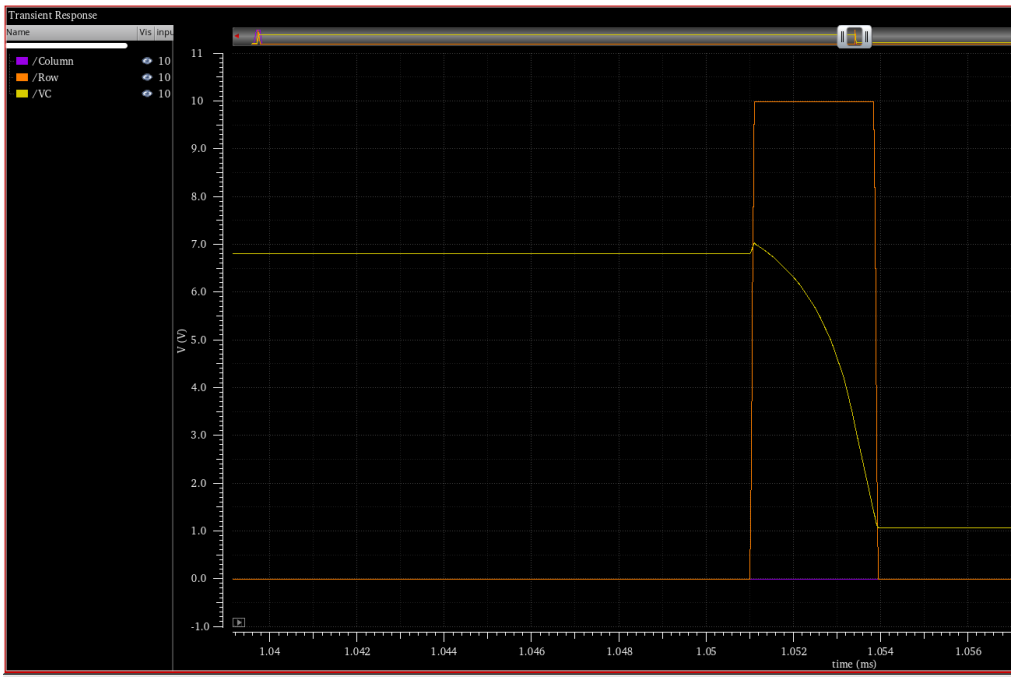


Figure 4.10. Pixel circuit transient simulation showcasing the fall time at 1.13µs with $C_{ST} =$

$10.6pF$, $C_{ov} = 265.07fF$, *and* $R_E = 0$.

Waveform measurements were done to assess the value at which the resistance starts affecting the transient of the gate of the driver. Rise and fall times, voltage values at the end of the falling and rising transients were measured to assess the upper limit on the series resistance. These measurements are shown in Figure 4.12 for the rising related measurements and Figure 4.13 for the falling related parameters. As shown by these figures, the limiting behavior is given by the falling of the *VC* node as it becomes more affected by the R_E introduction. A higher resistance value causes the *VC* node to float when the falling transient is done. Therefore, it is imperative to reduce this effect to avoid driving the LED when it is undesirable to do so. The increase in resistance causes the node to float so high that the measurement cannot be made due to the signal never reaching the 20% cutoff point, which can is being used to define the upper limit case. Note that this is all done while considering a voltage of *1V* as the signal 'low' for the falling transient due to the aforementioned constraints. Decreasing the overlap capacitance, and in consequence the storage capacitance, would allow for proper circuit functionality.

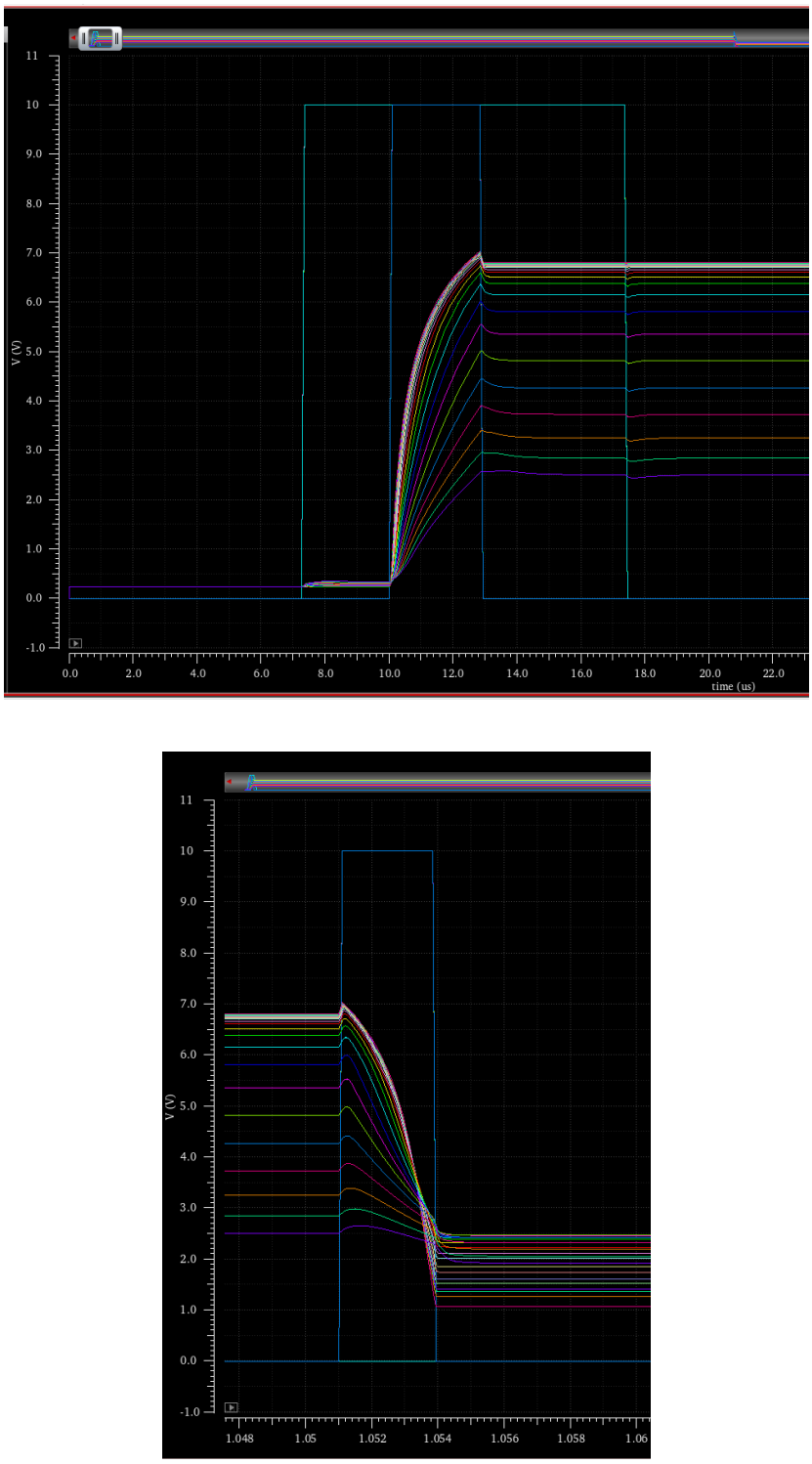


Figure 4.11. Pixel circuit transient simulation where $0\Omega \leq R_E \leq 1M\Omega$*, showcasing the rising(a) and falling(b) cases.*

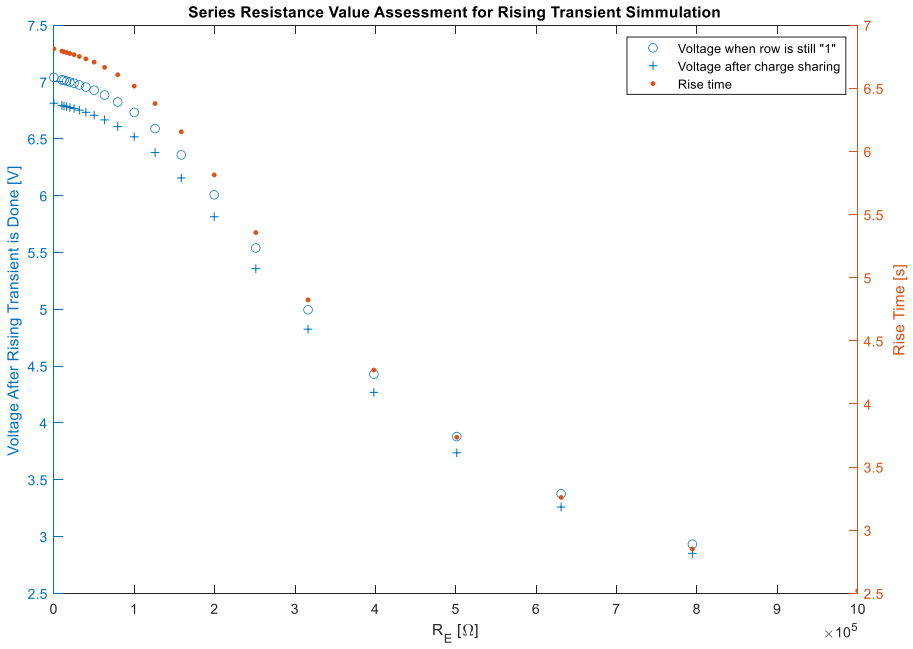


Figure 4.12. Series resistance impact on the rising transient simulation where $0\Omega \leq R_E \leq 1M\Omega$*, showcasing the voltage after the transient simulation is done and row is still high ("O" markers, y1-axis), the voltage after charge sharing has occurred ("+" markers, y1-axis), and the rise time (orange markers, y2-axis).*

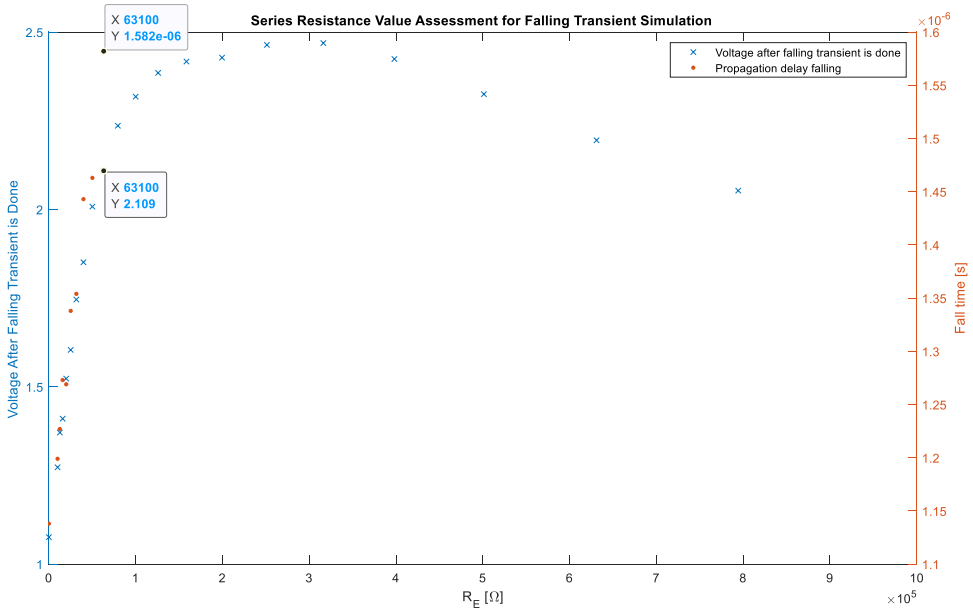


Figure 4.13. Series resistance impact on the falling transient simulation where $0\Omega \leq R_E \leq 1M\Omega$*, showing the voltage after the transient simulation is done and row is at ground ("x" markers), and the fall time (orange markers).*

4.3 SUMMARY

A pixel circuit simulation was presented with the purpose of validating the compact model that was developed in this work, and to design for the values of the passive elements needed for proper circuit functionality. This was accomplished by looking at different parasitic elements that are found in the IGZO TFT process technology. The impact on the transient simulation of elements such as S/D-to-gate overlap capacitances and series resistances was assessed to provide specifications for these.

Two different dimensions for overlap capacitances were assessed in this chapter. The first one was a $10\mu m$ by $44\mu m$ overlap, which provided a capacitance value of $911.196fF$, and the second one was a $4\mu m$ by $32\mu m$ overlap, which provided a capacitance value of $265.07fF$. The introduction of these overlap capacitances introduced two different mechanisms that were not present when the ideal case was simulated. The first one entailed a voltage divider present at the steady-state condition $Row = Column = 0$ due to *VDD* being present at the drain of the driver. The second one was related to the *Row* switching to ground after the pass transistor has accumulated charge in the gate of the driver. This caused the input capacitance of the driver to become connected in parallel with the output capacitance of the pass transistor, which effectively shared the charge that was previously accumulated between these two capacitances.

An experiment was carried out to assess which would be the ideal case that diminished these undesirable effects which consisted in changing the storage capacitor value to a range of values in order to find the one that diminished these effects. Both capacitance cases were deemed too high in order to achieve proper circuit functionality. However, Further assessment was done with the purpose of characterizing the circuit. The case of $265.07fF$ was investigated as it had the potential

for proper circuit functionality. The best capacitance ratio was found to be ≈ 40 ($C_{ST} = 10.6pF$), which diminished the floating voltage due to the voltage divider and the voltage loss due to charge sharing to *223mV*. Moreover, the voltage at the end of the row transient was measured at *6.8V*.

The series resistance experiment was carried out just like the capacitor experiment. However, it was important to determine the benchmark values of the circuit first. This would provide a baseline which would then be deteriorated by the introduction of series resistances. The benchmark values were *6.8V* for the voltage at the end of the row transient when rising, a rise time of *971.1ns*, *1V* for the voltage at the end of the row transient when falling, and a fall time of 1µ*s*. The series resistance was then varied from 0Ω to $1M\Omega$ in $50k\Omega$ steps, and it was found that $63k\Omega$ provides the upper limit for this parasitic element. This is because the falling transient becomes even more compromised due to the introduction of series resistance as it allows the gate of the driver to float to a voltage value.

A resistance below $63k\Omega$ restricts the gate of the driver to float to no more than *2.1V*. This value does not allow for proper circuit functionality as the behavior is limited by the overlap capacitance. The rise and fall times of the upper spec limit for the resistance are *1.11µs* and *1.58µs*, respectively. Results from both assessments are summarized in Table 4.1. This should be thought of as a design constraint when considering a worst-case scenerio such as the row-line resistance of the pixel in the last column of a row. Unfortunately in this specific case, the timing requirements for the desired application are not satisfied under even the best case conditions ($4\mu m$ overlaps, no series resistance). Further work is needed to design devices where the overlap capacitance is diminished such as the case of a self-aligned device. Likewise and perhaps more practical, an increase in the supply voltage could aid in circumventing these issues.

Table 4.1. Summary of the measured characteristics during the assessment of parasitic elements in the pixel circuit simulation.

Measurement	**Ideal case – no series resistance, no overlap capacitance**	**No series resistance – overlap capacitance considered ($C_{OV} = 265.07fF$)**	**Upper series resistance limit ($63k\Omega$)**
DC Voltage level when Row and Column are 'low'	*0V*	*223mV*	*234mV*
Voltage 'high' after charge sharing	*9.82V*	*6.8V*	*6.6V*
Voltage 'low' after falling transient	*0V*	*1V*	*2.1V*
Rise time	-	*971.1ns*	*1.11µs*
Fall time	-	*1µs*	*1.58 µs*

Chapter 5. CONCLUSION

The goal of this work was to create and implement an accurate compact model for IGZO TFTs in Verilog-A to assess the impact of parasitic elements, *i.e.* resistances and capacitances, that are inherently present in device and pixel designs. This was accomplished by the introduction of a novel bridge region of operation that served the purpose of 'connecting' the subthreshold region with the on-state model presented by Hirschman *et al.* [8], providing a full-range operational model for circuit simulation.

Three different regions of operation that compose the entirety of the drain current were introduced: subthreshold, bridge, and on-state. Two V_{GS} data points (V_{OFF}, V_{ON}) were defined such that the bridge region was constrained in-between these points. The rationale behind these two boundaries was introduced in Chapter 3.2, which then paved the way for two different approaches to solve for the parameters inside the bridge region; an analytical and an empirical approach.

The analytical approach allowed for the discovery that there is such point where the derivatives of the bridge and the on-state model are equal as the solution to Equations 3.18-3.21 existed. However, non-physical behavior present in output characteristics showed that the V_{DS} dependence was invalid. This encouraged a numerical solution where experimental or TCAD simulated data was used as the basis for finding this V_{DS} dependence to avoid non-physical behavior. Ultimately, the empirical model showed excellent agreement with experimental data of the modeled $\frac{24\mu m}{4\mu m}$ and $\frac{24\mu m}{2\mu m}$ devices.

The empirical compact model was coded in Verilog-A to perform circuit simulation with the purpose of assessing the impact of parasitic elements, and validating that the compact model promotes convergence within circuit simulation. These two objectives were accomplished and design constraints as they relate to the proposed 2T1C circuit topology were addressed. A $10\mu m$ overlap capacitance was deemed too large for the purpose of this application and there is a need for its reduction to $4\mu m$ due to the pass transistor incapability of providing enough current for such a high capacitance. Phenomena such as charge sharing and propagation delay that occurred within the circuit are studied extensively as well.

The output capacitance of the pass transistor and the input capacitance of the driver transistor are connected in parallel once the row falls to ground. This causes the charge on the gate of the driver to share between these two capacitances, which reduces the total charge available in said node. This, in turn, reduces the current that the driver transistor is able to provide. Therefore, the light emitting load suffers a reduction in current from this effect. It was found that an increasing $\frac{C_{ST}}{C_{ov}}$ capacitance ratio dimished this effect. As such, the values that provided proper circuit functionality were found to be $C_{ST} = 10.6pF$ and $C_{ov} = 265.07fF$, *i.e.* $\frac{C_{ST}}{C_{ov}} \approx 40$.

Rise and fall times were assessed by looking at the source/drain series resistances that are tied to the pass transistor. These are more important as these have the most impact in transient response of the circuit. The pixel circuit was assessed first when $R_E = 0$ with the aforementioned capacitance values, and rise and fall times were measured at 971.1*ns* and *1µs*, respectively. Introduction of series resistances showed that the falling transient becomes even more compromised as RC delay becomes larger due to the fact that the pass transistor is not able to drain the charge from the gate of the driver. This causes the driver to be driven when the intended

operation was to shut it off. Thus, an upper spec limit was addressed where the highest series resistance value that can be tolerated is $63k\Omega$. This resistance value resulted in rise and fall time values of $1.11\mu s$ and $1.58\mu s$, respectively, which do not allow for proper circuit functionality. Unfortunately in this specific case, the timing requirements for the desired application are not satisfied under even the best case conditions ($4\mu m$ overlaps, no series resistance).

An increase in the supply voltage could aid in circumventing these issues, and would perhaps be the most practical approach towards meeting this application specifications. However, the potential disadvantages of increasing the voltage supply would be stress-related degradation effects on both the TFTs and the interconnects. Further work can be made to achieve smaller parasitic capacitances in the fabrication of IGZO TFTs to accomplish proper circuit functionality. Devices where the channel is defined by a self-aligned process would provide smaller parasitic capacitances; this could provide a solution going forward for TFT manufacturing. In relation to pixel simulations, note that all of the series resistances were assessed using a lumped resistance model. Additional R-C delay must be need to be considered to account for the row signal propagation spanning over dozens of gate capacitances. Thus, it is important to assess the impact of these networks on the overall operation of the circuit.

Chapter 6. MODEL DEVELOPMENT ALGORITHMS

ANALYTICAL SOLUTION ALGORITHM

6.1 The following MATLAB script was generated to find the closed-form solution proposed in Chapter 3.4.1. The Symbolic Math Toolbox was used to get the expressions that were used to generate the curves shown in Figure 3.3. The script and its output are shown below.

```
%Clearing workspace variables
clear variables;

%Defining on-state model variable
syms W L COX U0 THETA_BTS Z THETA VBTS ALPHASCE VT;
%Defining input voltages
syms VGS VDS;
%Defining the boundaries
syms VON VOFF;
%Defining off-state variables
syms SS;
%Defining bridge region variables
syms VX BETA VXSAT BETASAT;

%Setting up assumptions on the values that the fitting parameters can take
assume([W L COX U0 THETA_BTS Z VBTS ALPHASCE VT SS VON VOFF], 'real');
assume([W L COX U0 THETA_BTS Z VBTS SS VON] > 0);
assume((0<=ALPHASCE) & (ALPHASCE<=1));
assume([VX BETA VXSAT BETASAT], 'real');
assume([BETA BETASAT] > 0);
assume([VGS VDS], 'real')
assume(VON>VT)

%On-state model
VDSAT = sqrt(VBTS^2 + (2/(1 - ALPHASCE))*(VBTS)*(VGS - VT)) - VBTS;
```

```
assume(VDSAT, 'real');
assume(VDSAT >= 0);
ETAG    = 1/(Z - THETA_BTS*(VGS - VT));
ETAD    = 1/(1 + VDS/VBTS);
ETADSAT = subs(ETAD, VDS, VDSAT);
IDLIN   = (W/L)*COX*U0*ETAG*ETAD*((VGS - VT)*VDS - ((1 - ALPHASCE)/2)*VDS^2);
IDSAT   = subs(subs(IDLIN, ETAD, ETADSAT), VDS, VDSAT);

%Off-state model
IOFF = exp(VGS/SS);

%Bridge model
IBRIDGELIN = (VGS - VX)^BETA;
IBRIDGESAT = (VGS - VXSAT)^(BETASAT);

%Taking the log of the drain current models
LOGIFIT1 = simplify(log10(IOFF));
LOGIFIT2 = simplify(log10(IBRIDGELIN));
LOGIFIT3 = simplify(log10(IBRIDGESAT));
LOGIDSAT = simplify(log10(IDSAT));
LOGIDLIN = simplify(log10(IDLIN));

%Equation system to solver for VX and BETA
EQN1         = simplify(subs(diff(LOGIDLIN, VGS), VGS, VON)) ==
simplify(subs(diff(LOGIFIT2, VGS),VGS, VON));
%Solving for VX to substitute in EQ2 in order to find BETA
VX_SOL       = simplify(solve(EQN1, VX));
%Setting EQ2 for VOFF boundary and solving for BETA
EQN2         = simplify(subs(diff(LOGIFIT1,VGS), VGS, VOFF)) ==
simplify(subs(subs(diff(LOGIFIT2,VGS),VGS, VOFF), VX, VX_SOL));
BETA_LIN     = simplify(solve(EQN2,BETA))
```

BETA_LIN =

$$\frac{\mathrm{VOFF}-\mathrm{VON}}{\mathrm{SS}\left(\frac{(Z-\mathrm{THETA_{BTS}}\,\mathrm{VON}+\mathrm{THETA_{BTS}}\,\mathrm{VT})\,(\mathrm{VDS}-2\,\mathrm{VON}+2\,\mathrm{VT}-\mathrm{ALPHASCE}\,\mathrm{VDS})}{\mathrm{SS}\,(2\,Z-\mathrm{THETA_{BTS}}\,\mathrm{VDS}+\mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VDS})}+1\right)}$$

```
%Substituting the beta solution into the expression for VX to find VX
VX_LIN       = simplify(subs(VX_SOL, BETA, BETA_LIN))
```

VX_LIN =

$$\mathrm{VON} + \frac{(\mathrm{VOFF} - \mathrm{VON})\,(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT})\,\sigma_1}{\mathrm{SS}\left(\frac{(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT})\,\sigma_1}{\mathrm{SS}\,\sigma_2} + 1\right)\sigma_2}$$

where

$$\sigma_1 = \mathrm{VDS} - 2\,\mathrm{VON} + 2\,\mathrm{VT} - \mathrm{ALPHASCE}\,\mathrm{VDS}$$

$$\sigma_2 = 2\,Z - \mathrm{THETA_{BTS}}\,\mathrm{VDS} + \mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VDS}$$

```
%Equation system to solve for VX_SAT and BETA_SAT; this is done in the same
%way as the first equation system was solved
EQN3         = simplify(subs(diff(LOGIDSAT, VGS), VGS, VON)) ==
simplify(subs(diff(LOGIFIT3, VGS),VGS, VON));
BETA_SOL     = simplify(solve(EQN3,BETASAT));
EQN4         = simplify(subs(diff(LOGIFIT1, VGS), VGS, VOFF) ==
simplify(subs(subs(diff(LOGIFIT3, VGS),VGS, VOFF), BETASAT, BETA_SOL)));
VX_SAT       = simplify(solve(EQN4,VXSAT))
```

VX_SAT =

$$\frac{\mathrm{VOFF}\,\left(2\,(\mathrm{VBTS} - \sigma_2)\,(\mathrm{VON} - \mathrm{VT}) - (\mathrm{VBTS} - \sigma_2)^2\,(\mathrm{ALPHASCE} - 1)\right)(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT}) - 2\,\mathrm{SS}\,\mathrm{VON}\,\sigma_1}{\left(2\,(\mathrm{VBTS} - \sigma_2)\,(\mathrm{VON} - \mathrm{VT}) - (\mathrm{VBTS} - \sigma_2)^2\,(\mathrm{ALPHASCE} - 1)\right)(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT}) - 2\,\mathrm{SS}\,\sigma_1}$$

where

$$\sigma_1 = \mathrm{VBTS}\,Z + \mathrm{THETA_{BTS}}\,\mathrm{VBTS}^2 - Z\,\sigma_2 - \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\sigma_2 + \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\mathrm{VON} - \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\mathrm{VT} - \mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VBTS}^2 + \mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\sigma_2$$

$$\sigma_2 = \sqrt{-\frac{\mathrm{VBTS}\,(\mathrm{VBTS} + 2\,\mathrm{VON} - 2\,\mathrm{VT} - \mathrm{ALPHASCE}\,\mathrm{VBTS})}{\mathrm{ALPHASCE} - 1}}$$

```
BETA_SAT     = simplify(subs(BETA_SOL, VXSAT, VX_SAT))
```

BETA_SAT =

$$\frac{2\left(\mathrm{VON} - \frac{\mathrm{VOFF}\,\sigma_3\,(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT}) - 2\,\mathrm{SS}\,\mathrm{VON}\,\sigma_1}{\sigma_2 - 2\,\mathrm{SS}\,\sigma_1}\right)\sigma_1}{\sigma_2}$$

where

$$\sigma_1 = \mathrm{VBTS}\,Z + \mathrm{THETA_{BTS}}\,\mathrm{VBTS}^2 - Z\,\sigma_4 - \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\sigma_4 + \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\mathrm{VON} - \mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\mathrm{VT} - \mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VBTS}^2 + \mathrm{ALPHASCE}\,\mathrm{THETA_{BTS}}\,\mathrm{VBTS}\,\sigma_4$$

$$\sigma_2 = \sigma_3\,(Z - \mathrm{THETA_{BTS}}\,\mathrm{VON} + \mathrm{THETA_{BTS}}\,\mathrm{VT})$$

$$\sigma_3 = 2\,(\mathrm{VBTS} - \sigma_4)\,(\mathrm{VON} - \mathrm{VT}) - (\mathrm{VBTS} - \sigma_4)^2\,(\mathrm{ALPHASCE} - 1)$$

$$\sigma_4 = \sqrt{-\frac{\mathrm{VBTS}\,(\mathrm{VBTS} + 2\,\mathrm{VON} - 2\,\mathrm{VT} - \mathrm{ALPHASCE}\,\mathrm{VBTS})}{\mathrm{ALPHASCE} - 1}}$$

6.2 EMPIRICAL SOLUTION ALGORITHMS

The different code blocks that were used to generate the parameter set for the off-state model are presented in this chapter. This chapter will be partitioned as follows: 6.2.1 includes details of the extraction of V_{OFF} and V_{ON}, 6.2.2 provides the code that accomplishes the V_{DS} modeling such as A, V_X, β and sA functional forms, and sections 6.2.3 and 6.2.4 present the code that carries out the leakage and TABL modeling, respectively.

6.2.1 V_{ON} & V_{OFF} Extraction Routine

The first step in the parameter extraction is to run the on-state model parameter extraction, which is a "legacy code" function called 'runStuff4_clean()' as shown below.

```
clear variables;
    PlotAlg = 1;  % Enables the plots relevant to the algoritm for finding
VON and VOFF
    PlotABC = 1;  % Enables the plots relevant to A,B,C modeling.
    PlotLeak = 1; % Enables the plots of relevant leakage modeling
    PlotSm = 1;   % Enables the plots relevant to the smoothing routine
%%  Calling the on-state parameter extraction routine to get the on-state
parameter subset.
    [~, ~, ~, ~, ~, parameters, totalpath] = runStuff4_clean();  %Running on-
state parameter extraction routine.
                                                                 %Inheriting
'parameters', and 'totalpath' to use same file for off-state parameter
extraction
    [vds, ids, vgs, ~] = filenom(totalpath);                     %Importing
experimental data from megafamily's excel file used in on-state extraction.
    ids = transpose(ids);
```

The next step is to run the V_{ON} and V_{OFF} extraction routine as shown below

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Declaring the VON, and VOFF vectors that will be used to scan for the
% best possible R^2
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    DELTAVGS = vgs(2) - vgs(1);
    VT       = 2*round(parameters(6)/2,1);
    VON      = (VT + 2*DELTAVGS):DELTAVGS:6+1e-6;
    VOFF     = (VT - 5*DELTAVGS):DELTAVGS:(VT - DELTAVGS);
% Creating the fit to the bridge function using the previously defined VON,
and VOFF vectors.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
% Declaring the on-state parameter subset for I-V curve generation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    Z           = parameters(1);
    ALPHASCE    = parameters(2);
    VBTS        = parameters(3);
    LAMBDA      = parameters(4);
    THETA_BTS   = parameters(5);
    VT          = parameters(6);
    W           = parameters(7);
    L           = parameters(8);
    TOX         = parameters(9);
    u0          = parameters(10);
    SS          = parameters(11)*1e-3;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Allocating variable space for the VON, VOFF scan
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    A_VDS       = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    B_VDS       = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    C_VDS       = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    sA_VDS      = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    I_DS        = zeros(size(vgs,1), size(vds,1), size(VON,2), size(VOFF,2));
    R2_VOFF     = zeros(size(VOFF,2),1);
    R2_VON_AboveVOFF = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    R2_VON_BetweenVOFF_VON = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    R2_VON_AboveVON = zeros(size(vds,1), size(VON,2), size(VOFF,2));
    I_DUMMY     = zeros(size(vgs,1), size(vds,1));
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Finding the index for VGS = VT
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    VT_idx      = 2*round(VT/2,1);
    VT_idx      = find(abs(vgs-VT_idx)<1e-6,1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% VOFF is not a function of VDS and gets evaluated at max(VDS)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    for j=1:size(VOFF,2)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% VON as a function of VDS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        for i=2:size(vds,1)
            for k=1:size(VON,2)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating the VGS vector for the bridge function such as VOFF<=VGS<=VON
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
                VGS_Bridge = VOFF(j):DELTAVGS:VON(k);
                VGS_Bridge = transpose(VGS_Bridge);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Finding the measured ids values that correspond to the VGS_Bridge values
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
                VOFF_D_Idx = find(abs(vgs - VOFF(j))<1e-1,1);
                VON_D_Idx  = find(abs(vgs - VON(k))<1e-1,1);
                ids_Bridge = ids(VOFF_D_Idx:size(vgs,1),:);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calling upon the fitting function from MATLAB's curve fitting and
% storing each value into a 4D array
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
                [FR_B, gof_B]    = createFitBridge(vds(i),
vgs(VOFF_D_Idx:size(vgs,1)), log10(ids_Bridge(:,i)), VON(k), Z, ALPHASCE,
VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0);
                A_VDS(i,k,j)     = FR_B.A;
                B_VDS(i,k,j)     = FR_B.B;
                C_VDS(i,k,j)     = FR_B.C;
                sA_VDS(i,k,j)    = FR_B.sA;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating the I-V curve using the extracted A, B, and C value for the
% present ith, kth, and jth iteration and storing each value into a 4D
% array
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
                I_DUMMY(:,i)       = IDCurve(vds(i), vgs, FR_B.A, FR_B.B,
FR_B.C, VON(k), VOFF(j), Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX,
u0, SS, FR_B.sA);
                I_DS(:,i,k,j)      = I_DUMMY(:,i);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculating R^2 for the VGS>=VT values and looking for the best possible
% case per VON case, i.e. the if case yields the VON value and its index at
% which the R^2 is maximized
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
                R2_VON_AboveVOFF(i,k,j)       =
calculateR2(log10(abs(ids(VOFF_D_Idx:size(vgs,1),i))),
log10(I_DUMMY(VOFF_D_Idx:size(vgs,1),i)));
                R2_VON_BetweenVOFF_VON(i,k,j) =
calculateR2(log10(abs(ids(VOFF_D_Idx:VON_D_Idx,i))),
log10(I_DUMMY(VOFF_D_Idx:VON_D_Idx,i)));
                R2_VON_AboveVON(i,k,j)        =
calculateR2(log10(abs(ids(VON_D_Idx:size(vgs,1),i))),
log10(I_DUMMY(VON_D_Idx:size(vgs,1),i)));
            end
        end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Evaluating for the best VOFF value at the last 'i' value, which is
% max(VDS) and finding the best case for R^2 in a per VOFF basis
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
        R2_VOFF(j,1) = calculateR2(log10(abs(ids(1:VOFF_D_Idx,i))),
log10(I_DUMMY(1:VOFF_D_Idx,i)));
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Looking at the maximum R-sq values to find the best VOFF value
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    BestVOFF_Idx    = find(abs(max(R2_VOFF) - R2_VOFF)<1e-6,1);
    BestVOFF        = VOFF(1,BestVOFF_Idx);
    VOFF_FINAL_Idx  = find(abs(vgs - BestVOFF)<1e-1,1);
    VOFF_FINAL_Idx2 = find(abs(VOFF - BestVOFF)<1e-1,1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Looking at R-sq values to find the best VON-VDS curve
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    VON_VDS = zeros(size(vds,1), 1);
    VON_VDS_idx = zeros(size(vds,1), 1);
    figure
    for i=2:size(vds,1)
        [xdataVON, ydataVON] = prepareCurveData(VON,
R2_VON_AboveVOFF(i,:,VOFF_FINAL_Idx2));
        [fVON, gofVON] = fit(xdataVON, ydataVON, 'cubicspline');
        fVON_der = fnder(fVON.p);
```

```
        VON_fnd  = fnval(fVON_der, VON);
        for j=1:size(VON_fnd,2)
            if VON_fnd(j) < 1e-4
                VON_VDS(i) = VON(j);
                VON_VDS_idx(i) = j;
                break
            end
        end
        plot(fVON, xdataVON, ydataVON)
    end
    VON_FINAL       = mean(VON_VDS, 'all');
    VON_FINAL_Idx   = find(abs(vgs - VON_FINAL)<1e-1,1);
    VON_FINAL_Idx2  = find(abs(VON - VON_FINAL)<1e-1,1);
```

Two custom defined functions are used inside this algorithm; 'createFitBridge' and 'IDCurve'. The purpose of the former is to extract the fitting parameters inside the bridge region along with the smoothing parameters for the hyperbolic tangent function. Note that this is done at the same time inside the same routine at a given drain-to-source voltage. The purpose of the second function is to generate the entire I-V curve at a given drain-to-source voltage for least mean square error assessment purposes. This curve will then be used to calculate R^2 to determine the best (V_{OFF}, V_{ON}) pair. Both of these functions are shown below.

```
function [fitresult, gof] = createFitBridge(xx, yy, zz, VON, Z, ALPHASCE,
VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0)
    VDS = xx;
    [xData, yData] = prepareCurveData(yy, zz);
    ft = fittype('BridgeIVCurve(VDS, x, A, B, C, VON, Z, ALPHASCE, VBTS,
LAMBDA, THETA_BTS, VT, W, L, TOX, u0, sA)', 'independent', 'x', 'dependent',
'y', 'coefficients', {'A', 'B', 'C', 'sA'}, ...
        'problem', {'VDS', 'VON', 'Z', 'ALPHASCE', 'VBTS', 'LAMBDA',
'THETA_BTS', 'VT', 'W', 'L', 'TOX', 'u0'});
    opts            = fitoptions('Method', 'NonlinearLeastSquares');
    opts.Display    = 'Off';
    opts.TolFun     = 1e-16;
    opts.Lower      = [1e-8 -min(yy) 1.00     0];
    opts.Upper      = [1e-6  inf     inf    inf];
    opts.StartPoint = [1e-7 0.45     2.25   0.5];
    [fitresult, gof] = fit(xData, yData, ft, opts, 'problem', {VDS, VON, Z,
ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0});
end

function I_D = IDCurve(VDS, VGS, A, B, C, VON , VOFF, Z, ALPHASCE, VBTS,
LAMBDA, THETA_BTS, VT, W, L, TOX, u0, SS, sA)
```

```
% Generates the IV curve including the off-state and on-state models
    LEAKAGE  = 1e-11;
    I_D      = zeros(size(VGS,1),1);
    for i=1:size(VGS,1)
        I_B      = A*((VGS(i) + B)^C) + LEAKAGE;
        A1       = (A*(VOFF + B)^C)/exp(log(10)*(VOFF/SS));
        IOFF     = A1*exp(log(10)*(VGS(i)/SS)) + LEAKAGE;
        ID_ON    = IDCurveOnState(VDS, VGS(i), Z, ALPHASCE, VBTS, LAMBDA,
THETA_BTS, VT, W, L, TOX, u0);
        S_F = 1/2 + 1/2*tanh((VGS(i) - VON)/sA);

        if(VGS(i) <= VOFF)
            I_D(i) = IOFF;
        else
            I_D(i) = (1 - S_F)*I_B + S_F*ID_ON;
        end
    end
end
```

6.2.2 Drain-to-Source Voltage Modeling

Once V_{ON} and V_{OFF} have been extracted, it is necessary to find the corresponding fitting parameters at every V_{DS} bias point. This is accomplished by the 'for' loop shown below, which its outcome is the V_{DS} dependence of the fitting parameter at the (V_{OFF}, V_{ON}) pair that maximizes R^2. Then, the curve fitting toolbox is used to model A, B, C, and sA which correspond to the aforementioned A, V_X, β, and sA. A ninth order polynomial is used in this case. However, this is not set in stone and bound to change due to the fact that the functional forms can change as more devices are modeled. However, because circuit simulation is of interest, a lookup table model was developed for the purpose of this work and the lookup tables are generated at the end of the attached code.

```
%% Finding the functional dependence for B and C using the BestB and BestC
variables.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Extracting the best A B C and sA cases per VON and VDS basis
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    BestA = zeros(size(vds,1), 1);
    BestB = zeros(size(vds,1), 1);
    BestC = zeros(size(vds,1), 1);
    BestsA = zeros(size(vds,1), 1);
    for i=2:size(vds,1)
```

```
        BestA(i,1) = A_VDS(i,VON_FINAL_Idx2,VOFF_FINAL_Idx2);
        BestB(i,1) = B_VDS(i,VON_FINAL_Idx2,VOFF_FINAL_Idx2);
        BestC(i,1) = C_VDS(i,VON_FINAL_Idx2,VOFF_FINAL_Idx2);
        BestsA(i,1) = sA_VDS(i, VON_FINAL_Idx2, VOFF_FINAL_Idx2);
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Fitting A as a function of VDS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    [xdataA, ydataA] = prepareCurveData(vds(2:101), BestA(2:101));
    [fA, gof_fA] = fit(xdataA, ydataA, 'poly9');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Fitting B as a function of VDS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    [xdataB, ydataB] = prepareCurveData(vds(2:101), BestB(2:101));
    [fB, gof_fB] = fit(xdataB, ydataB, 'poly9');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Fitting C as a function of VDS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    [xdataC, ydataC] = prepareCurveData(vds(2:101),BestC(2:101));
    [fC, gof_fC] = fit(xdataC, ydataC, 'poly9');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Fitting sA as a function of VDS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    [xdatasA, ydatasA] = prepareCurveData(vds(2:101),BestsA(2:101));
    [fsA, gof_fsA] = fit(xdatasA, ydatasA, 'poly9');
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating the I-V curves with A, B, and C as functions of VDS using the
parameters extracted in the previous section.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    LUTFlag = 1;
    IDPreLeak2 = IDCurvePreLeak(vds, vgs, BestA, fA, BestB, fB, BestC, fC,
BestsA, fsA, VON_FINAL, BestVOFF, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT,
W, L, TOX, u0, SS, LUTFlag);
    LUTFlag = 0;
    IDPreLeak1 = IDCurvePreLeak(vds, vgs, BestA, fA, BestB, fB, BestC, fC,
BestsA, fsA, VON_FINAL, BestVOFF, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT,
W, L, TOX, u0, SS, LUTFlag);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generating tables for the lookup table model used in VerilogA
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    mkdir FitParameterData
    dlmwrite('FitParameterData\A_data.txt', [vds BestA],'delimiter','\t')
    dlmwrite('FitParameterData\B_data.txt', [vds BestB],'delimiter','\t')
    dlmwrite('FitParameterData\C_data.txt', [vds BestC],'delimiter','\t')
    dlmwrite('FitParameterData\sA_data.txt', [vds BestsA],'delimiter','\t')
```

‘IDCurvePreLeak’ is a custom defined function used within this algorithm in order to validate the drain-to-source voltage modeling and is shown below.

```
function I_D = IDCurvePreLeak(VDS, VGS, A, fA, B, fB, C, fC, sA, fsA, VON,
VOFF, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0, SS, LUTFlag)
% Generates the IV curve including the off-state and on-state models\
    I_D      = zeros(size(VGS,1),size(VDS,1));
    LEAKAGE = 1e-11;
```

```
    for j=1:size(VDS,1)
        for i=1:size(VGS,1)
            if VDS(j) == 0
                I_B = LEAKAGE;
                IOFF = LEAKAGE;
                sA_VDS = 1;
            else
                if LUTFlag
                    A_VDS = A(j);
                    B_VDS = B(j);
                    C_VDS = C(j);
                    sA_VDS = sA(j);
                    I_B   = A_VDS*((VGS(i) + B_VDS)^C_VDS) + LEAKAGE;
                    A1    = (A_VDS*(VOFF +
B_VDS)^C_VDS)/exp(log(10)*(VOFF/SS));
                    IOFF  = OFF_state_current(VDS(j), VGS(i), A1, SS, 0) +
LEAKAGE;
                else
                    sA_VDS = fsA(VDS(j));
                    [I_B, A1]   =  Bridge_Current(VDS(j), VGS(i), VOFF, SS,
fA, fB, fC);
                    IOFF        = OFF_state_current(VDS(j), VGS(i), A1, SS,
0) + LEAKAGE;
                    I_B         = I_B + LEAKAGE;
                end
            end
            ID_ON = IDCurveOnState(VDS(j), VGS(i), Z, ALPHASCE, VBTS, LAMBDA,
THETA_BTS, VT, W, L, TOX, u0) + LEAKAGE;
            S_F = 0.5 + 0.5*tanh((VGS(i) - VON)/sA_VDS);
            if (VGS(i) <= VOFF)
                I_D(i,j) = IOFF;
            else
                I_D(i,j) = (1 - S_F)*I_B + S_F*ID_ON;
            end
        end
    end
end
```

6.2.3 Leakage Modeling

The leakage modeling algorithm is split in two parts. The first one is the written code that is described by the flowchart shown in Figure 3.12. The second part entails generating the I-V curve in order to validate that the leakage modeling was done correctly. This means that the transfer characteristics should no longer converge to the same leakage level as the drain-to-source voltage changes.

```
%% Leakage level adjustment
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Finding the index of the lowest possible current in the experimental
% data and using that index to look at VDS dependece, i.e. looking at a
% transversal cut into the transfer characteristics at the aforementioned
% index. Also, setting up the flag that enables leakage fitting
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    Leak_idx    = find(abs(ids(:,size(vds,1)) - min(ids(:,size(vds,1))))<1e-
16,1);
    didv        = diff(transpose(log10(abs(ids(Leak_idx,:))))./diff(vds);
    didv        = [0; didv];
    didv2       = diff(didv)./diff(vds);
    didv2       = [0; didv2];
    vds_idx     = find((max(didv2) - didv2)<1e-6,1);
    iL          = log10(abs(ids(Leak_idx,vds_idx)));
    VDS_iL      = vds(vds_idx);
    LeakFlag    = 1;
    LUTFlag     = 0;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Using MATLAB's curve fitting toolbox to fit the transversal cut
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   [xdataL, ydataL] = prepareCurveData(vds(vds_idx:size(vds,1)),
transpose(log10(abs(ids(Leak_idx,vds_idx:size(vds,1))))));
                fL = fit(xdataL, ydataL, 'power2');
         IDPostLeak = IDCurvePostLeak(vds, vgs, fA, fB, fC, fsA, VON_FINAL,
BestVOFF, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0, SS, fL,
VDS_iL);
```

6.2.4 TABL Modeling

Similar to the leakage model, the TABL model algorithm is partitioned into two sections. The first section handles the extraction of ΔV by using splines fit on the highest and the lowest non-zero drain bias found in the experimental data.The second section validates the extracted ΔV by generating the I-V curves.

```
%% TABL Model
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Getting the x and y data to generate the spline to find deltaV
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    VGS_spline = -5:0.001:10;
    LowDrainBias_spline = spline(vgs, ids(:,2), VGS_spline);
    HighDrainBias_spline = spline(vgs, ids(:,101), VGS_spline);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Finding the differences in the x-axis at 1nA for the high and the low
%  drain bias
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
    LowDrainCurrent_1nA = find(abs(LowDrainBias_spline - 1e-9)<1e-10,1);
    HighDrainCurrent_1nA = find(abs(HighDrainBias_spline - 1e-9)<1e-10,1);
    DV = VGS_spline(LowDrainCurrent_1nA) - VGS_spline(HighDrainCurrent_1nA);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Generating the I-V curve to validate the TABL model
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    IDPreTABLSmooth = IDCurvePostSmooth(vds, vgs, fA, fB, fC, fsA, BestVOFF,
VON_FINAL, Z, ALPHASCE, VBTS, LAMBDA, THETA_BTS, VT, W, L, TOX, u0, SS, fL,
VDS_iL, DV);
```

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