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Department of Electrical and Microelectronic Engineering

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ABSTRACT

As displays continue to increase in resolution and refresh rate, new materials for thin film transistors (TFTs) are required. Low temperature polycrystalline silicon (LTPS) formed by excimer laser annealing (ELA) has been very successful and has been implemented in small displays, but cost and scalability issues prevent it from entering larger display products. Currently LPTS TFTs are top-gate structures due to manufacturing challenges associated with crystallizing thin film silicon when a thermally conductive gate is under portions and insulating glass under others. Bottom-gate devices offer the benefit of higher breakdown voltage, better dielectric-semiconductor interface quality, and direct access to the back-channel region for interface trap passivation. The ability to fabricate bottom-gate devices would allow for different integration and design schemes and is a prerequisite for double gate structures. Flash lamp annealed (FLA) LTPS is an attractive method to expand the size of displays that use high mobility TFTs due to its scalability and parallel production nature.

In this work bottom-gate LTPS TFTs were fabricated via FLA with indium tin oxide (ITO), a transparent conductive oxide, used as the gate electrode. A p-channel TFT with 4 μm channel length crystallized with a FLA energy of 4.4 J/cm^2 for 250 μs demonstrated a low-field mobility of 190 cm^2/(Vs), a subthreshold slope of 325 mV/dec, on/off state ratio of seven orders of magnitude, and a threshold voltage of -5.4 V. A dielectric failure mechanism was identified that compromised the transistor operation under high drain bias and an alternative dopant introduction techniques were proposed to mitigate this issue. An effect due to the transduction of optical energy from the field to thermal energy under the channel via the gate was observed. Details of the FLA crystallization process, device fabrication, and electrical characteristics will be presented.

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Chapter 1. INTRODUCTION

Thin film transistors (TFTs) are an integral part of modern flat panel displays. In order to continue to push the boundaries of displays there is a constant desire to improve TFT performance. Many different transistor configurations and materials have been explored and new concepts are consistently arising. One of these schemes is bottom gate low temperature polycrystalline silicon (LTPS) devices, which has demonstrated high performance operation and benefits over other existing technologies. Flash lamp annealing (FLA) has potential for improvement in production cost reduction and ability to scale to large panel manufacturing. A material such as indium tin oxide (ITO), would be an attractive electrode option due to its high transparency and conductivity. A combination of these three presents an opportunity for new design space with innovative fabrication and integration strategies.

1.1 FLAT PANEL DISPLAY MARKET TRENDS

Like all consumer goods, there is always the push for a faster, cheaper, and better product. For the TV segment of the display industry there has been a push towards larger and larger screens. Analysis conducted by IHS and Corning Incorporated show the increase in the demand for TVs is expected to come from this large display segment, especially sixty inches and larger, as seen in figure 1.1 [1].

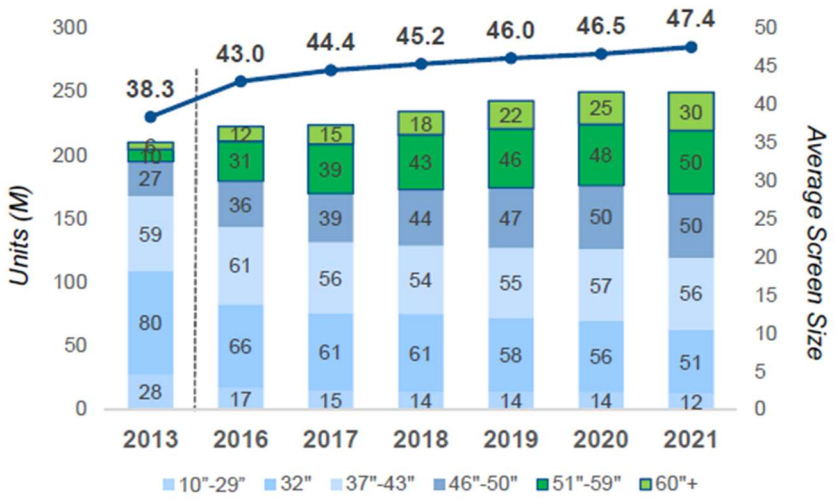

Figure 1.1 Worldwide estimated demand for TVs and average screen size [1]

To allow for the fabrication of the larger displays and higher factory capacity, manufactures have increased the size of the glass substrates. This has two main benefits; the overall size of the display can be increased, and the substrate can be utilized more efficiently. Figure 1.2 shows 75" displays on both Gen 8.5 and Gen 10.5 glass. The Gen 8.5 only allows for two displays to be fabricated on the substrate and has 56% utilization while the Gen 10.5 glass allows for six displays and is utilizing 94% of the substrate. Due to this the majority of new fabs in construction are designed to work with Gen 10.5 glass: 2940 mm by 3370 mm [2].

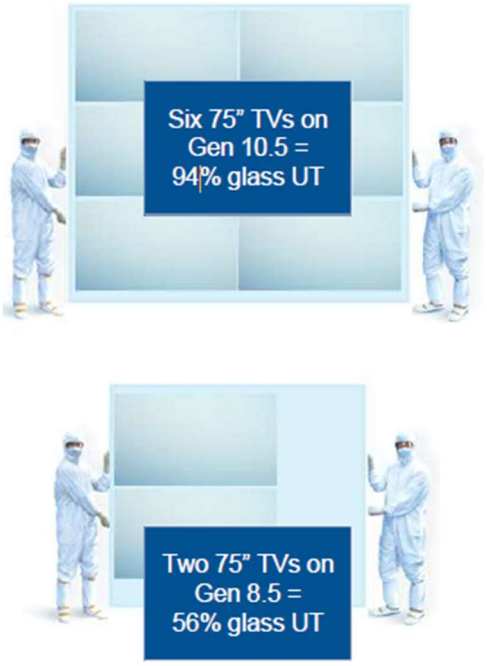

Figure 1.2 Layout and glass utilization for 75 inch TVs on Gen 8.5 and Gen 10.5 glass [1]

A major driver in the display market is the cost. As the manufacturing capacity of display fabs increase due to the larger substrates, economies of scale allow for the average unit price to come down, encouraging wider consumer adoption of larger displays.

1.2 DISPLAY PIXEL DESIGNS

There are two main types of pixels for flat panel displays; filtering and emissive. Filtering displays use electrical signal to modify light. The most common type of filtering display is the liquid crystal display (LCD). Liquid crystals are materials that have the fluidity of a liquid but the order of a crystal. Their physical properties can be manipulated by applying heat, electrical or magnetic fields. The liquid crystal display was first demonstrated by George Heilmeier from Radio Corporation of America in 1968 [3]. Common liquid crystal materials are cyanobiphenyls,

phenylcyclohexanes, and cyclohexylcyclohexanes. Liquid crystal displays are the most common display technology.

Liquid crystal displays have a liquid crystal layer that is sandwiched between two linear polarizers. When a voltage is applied across the liquid crystal it rotates, changing its optical properties. When the voltage is removed the liquid crystal relaxes to its original state, regaining its original optical properties. The two state conditions result in the light passing through the liquid crystal either maintaining its initial polarization state or rotating its polarization state 90°. If the polarization state after the liquid crystal is aligned with the second polarizer, the pixel can transmit light. If the light and second polarizer are 90° different in phase the light is blocked, and the pixel is off. Since a voltage is applied to the liquid crystal to set its state, liquid crystal-based pixels are controlled using voltage driven schemes [4]. Figure 1.3 shows an expanded view of an LCD display with the pixels at three different brightness levels. In figure 1.3 the two polarizers are crossed, meaning that if the polarization is not rotated no light is transmitted and if the polarization is rotated 90° all of the light is transmitted. For intermediate angles a fraction of the light makes it through the second polarizer and the pixel will be on but not at its maximum brightness. The top pixel in figure 1.3 is on as the liquid crystal is rotating the polarization 90°, the middle pixel's liquid crystal is at an intermediate rotation so it is on with diminished brightness, and the bottom pixel is off since there is no change in the lights polarization as it passes through the liquid crystal.

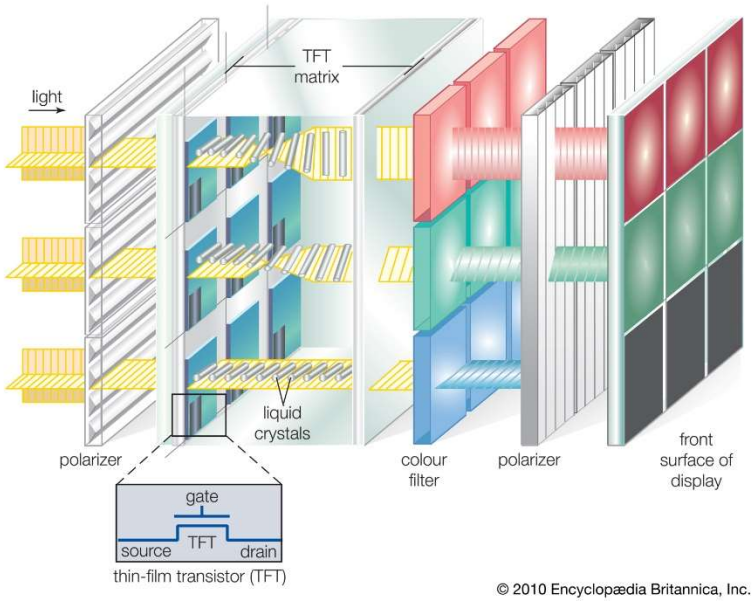

Figure 1.3 Expanded view of an active matrix LCD display [4]

Emissive displays directly convert an electrical signal to light. The two most common types of emissive displays are organic light emitting diode (OLED) and micro light emitting diode (µLED) displays. For an OLED display, each pixel is made up of organic light emitting diode (OLED) subpixels. A cut-away view of an OLED display is shown in figure 1.4. The µLED displays are made up of inorganic light emitting diodes (LEDs) that are transferred from their growth substrates onto the display. The "µ" portion of µLED comes from the fact that the transferred LEDs are tens to hundreds of microns in size. Both displays emit light when a current is passed through the diode.

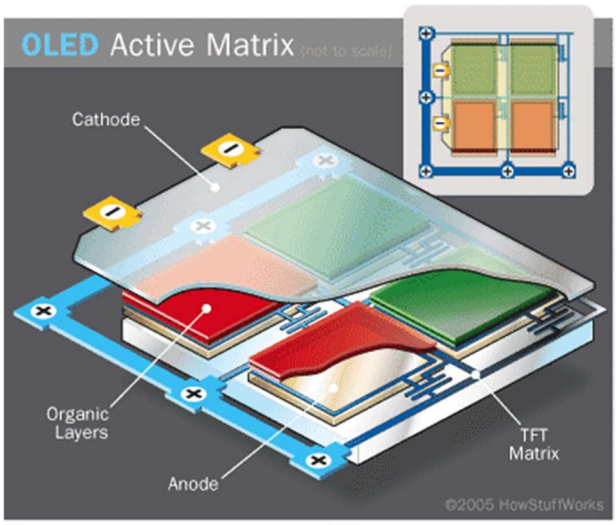

Figure 1.4 Cut-away view of an active matrix OLED display [5]

Emissive displays have the benefits of high brightness, low power consumption, fast response time, high contrast ratio, high resolution and a wide color gamut. OLED displays are currently available for purchase and are very popular for high end displays. Difficulties with processing and moisture sensitivity of the organic materials in the OLED are major areas that are restricting wider adoption. The µLED displays are seen as the next big trend in displays; they have many benefits when compared with OLED displays. They do not have the same moisture sensitivities, are more efficient, and have longer device lifetime due to their use of inorganic semiconductors [2]. The major hurdles holding them back are manufacturability and yield. Millions of µLEDs must be transferred from the growth substrate to the backplane to make a high-resolution display and any issues will lead to a dead pixel. Methods for transfer, bonding, inspection, and repair all need to be improved before µLED displays can become mainstream [2].

To drive the pixels there are two main schemes; passive matrix and active matrix. For passive matrix each pixel is connected directly to the external driver circuitry. The liquid crystal or OLED is sandwiched between two grids of electrodes, where the columns are the data lines and the rows

are the select lines, as shown in figure 1.5. The rows are selected one at a time and the columns contain the data controlling if the pixel is on or off. Since only one row can be addressed at a time, all other pixels are off. Additionally, addressing all of the pixels in a row at once leads to a large intrinsic capacitance, causing propagation delay. Due to these two factors passive matrix displays are limited in both size and resolution. Most passive displays have fifty or fewer rows and columns and are at most a few inches in size [6].

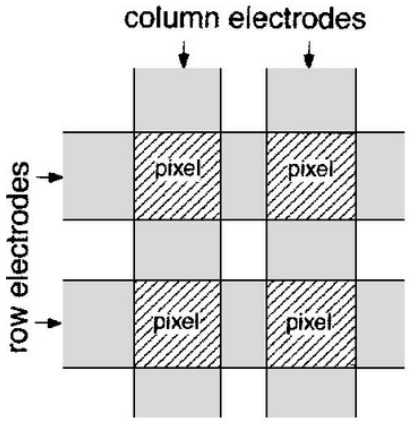

Figure 1.5 Passive matrix pixel design for LCD display [7]

For active matrix displays, each pixel is attached to thin film transistors (TFTs) and capacitors, shown in figure 1.6. This allows for charge to be stored on the capacitor, allowing for the pixel to retain its state while other pixels are being addressed. By storing the charge at each pixel, the display resolution, contrast ratio, viewing angle, and maximum size can be improved. For modern color displays each pixel is made up of at least three subpixels: one red, one blue, and one green. Due to the total number of subpixels in a display and the limitation in the quantity of pixels for passive matrix, most modern color displays are active matrix design.

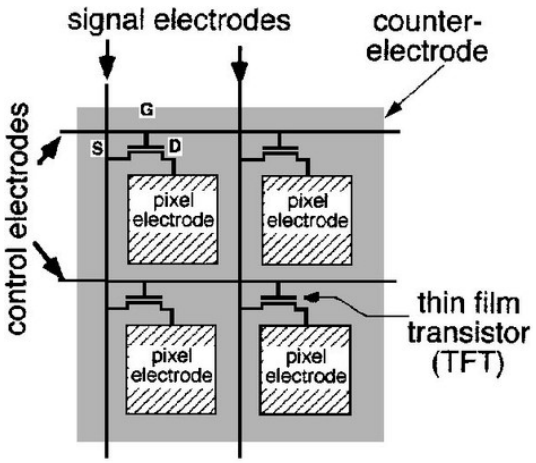

Figure 1.6 Active matrix pixel design for LCD display [7]

As the market transitions away from liquid crystal-based designs to OLED and μLED displays the control circuitry must also switch from providing a voltage to supplying a current. For applying a fixed voltage to the pixel, a simple one transistor one capacitor pixel design can be used, as seen in figure 1.7a. To supply a constant current, the simplest pixel circuit is a two transistor one capacitor design, shown in figure 1.7b. Since the intensity of light emitted by the pixel is directly related to the amount of current flowing through the diode, variation in current will cause large differences in pixel brightness. To account for variations in threshold voltage, more complicated drive circuitry designs have been proposed [8].

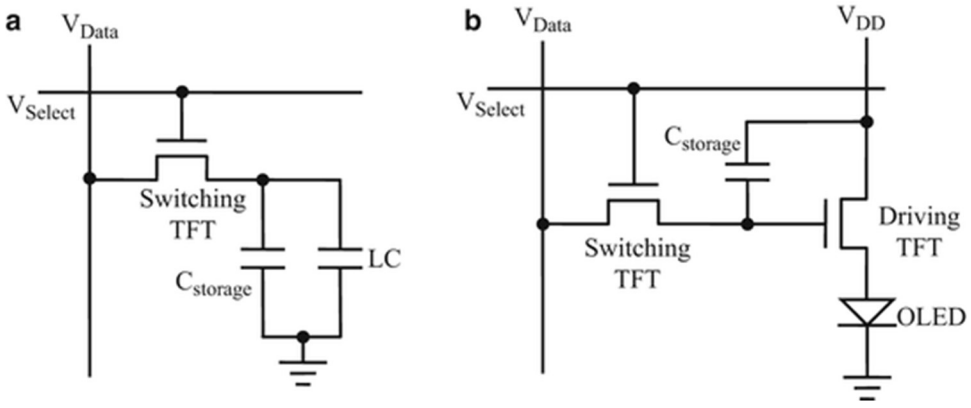

Figure 1.7 Simplest circuit for active matrix a) LCD b) OLED pixel [9]

1.3 TFT TECHNOLOGIES

There are three different TFT materials used for displays currently in production: plasma enhanced chemical vapor deposited (PECVD) hydrogenated amorphous silicon (a-Si:H), the amorphous metal oxide indium gallium zinc oxide (IGZO), and excimer laser annealed (ELA) low temperature polycrystalline silicon (LTPS). All three materials have advantages and disadvantages to their use, so the applications where they are found vary accordingly.

	a-Si:H	IGZO	ELA-LTPS
Microstructure	Amorphous	Amorphous	Polycrystalline
V_t uniformity	Good	Fair	Fair
V_t stability	Poor	Fair	Good
BTS stability	Poor	Good	Excellent
Mobility	1 cm^2/V-sec	10 cm^2/V-sec	50 – 100 cm^2/V-sec
Mobility uniformity	Good	Fair	Fair
Off current	fA	fA	pA
Device type	NMOS	NMOS	CMOS
Ambient sensitivity	Low	High	Low
Process complexity	Low	Low	High
Scalability	Gen 10.5	> Gen 8	Gen 6
Equipment cost	Low	Low	High
Main application	Price Sensitive Large Area	Large Area	Portable High Performance

1.3.1 a-Si:H

Hydrogenated amorphous silicon was one of the first materials that was used for thin film transistors and the first that was commercially manufactured. The silicon is PECVD deposited allowing for it to be scaled to large substrates. Additionally, the process itself is relatively fast, allowing for high volume manufacturing. The film is hydrogenated to passivate dangling bonds in the amorphous silicon, allowing the devices to exhibit far better transistor characteristics. The TFTs can be fabricated using a four-mask process, minimizing the number of lithography steps. The main benefits of using an a-Si:H TFT are that the fabrication process is scalable up to and even beyond the largest generation glass (Gen 10.5), exceptional uniformity across the substrate due to the amorphous structure, and the fabrication process is simple and cost-effective. The main disadvantages of a-Si:H are that the threshold voltage of the transistor drifts under bias stress and that it has extremely limited electron channel mobility, $\mu_n < 1$ cm^2/(Vs). There are many applications that are not limited by the low channel mobility and can compensate or mitigate the threshold bias drift. Currently most displays have backplanes with a-Si:H TFTs, and it is a dominant technology for large displays as well as low cost displays.

1.3.2 IGZO

Indium gallium zinc oxide is the most mature of the amorphous metal-oxide semiconductors (AOS). IGZO has many appealing properties that make it an attractive candidate to replace a-Si:H; it has a higher electron channel mobility, $\mu_n \sim 10$ cm^2/(Vs), and comparable off-state performance. One major challenge of using an amorphous metal oxide is that they are very sensitive to ambient conditions and temperature. Once the TFT backplane is completed additional processing steps are required to finish the display, some of which are hot enough to cause issues with the device

stability. IGZO is the most stable AOS and much work has gone into understanding encapsulation methods to extend usable device lifetimes and thermal stability. The IGZO is sputter deposited for manufacturing applications, which allows for both high throughput and scalability to larger substrate sizes. IGZO is currently used as the backplane in a number of tablets and TVs.

1.3.3 ELA-LTPS

Excimer laser annealed low temperature polycrystalline silicon is the primary method for fabricating high mobility TFT backplanes. The initial silicon is deposited using PECVD, similar to a-Si:H devices. The silicon is dehydrogenated and then exposed to twenty pulses or more of a XeCl laser (λ = 308 nm). This allows for the silicon film on top of the glass substrate to melt while leaving the glass below its thermal limit. This process results in a thin polycrystalline film. The channel mobility of the devices is greatly increased due to the crystallization. Unlike a-Si:H and AOS, polysilicon can be doped both n-type and p-type, thus allowing for the fabrication of CMOS circuits. Like bulk silicon devices, the mobility for electrons is higher than that of holes but it is not uncommon to see hole channel mobility $\mu_p > 100$ cm^2/(Vs).

The major disadvantage of the ELA process is the excimer laser system itself. For ELA in manufacturing the systems are designed to expose a long narrow section at a time as to maximize for uniformity and tool throughput. The system exposes half the width or the entire width with each pass. With the larger generations this becomes increasingly challenging due to the power requirements of the laser and the complexity of the laser optics. Some work has been done to extend the usable substrate sizes by using multiple laser sources and combining them into one exposure, but this leads to an expensive and complicated system. Due to the cost, complexity, and

time associated with using ELA exposure the resulting backplanes are very expensive. For these reasons, ELA-LTPS is mostly used for small high-resolution displays, such as phones.

Figure 1.8 Production Excimer Laser System [10]

1.4 TFT GATE CONFIGURATIONS

Thin film transistors can have many different configurations due to the layers being deposited. The devices can be either top gate, bottom gate, or double gate, in reference to the gate being either below or above the semiconducting layer. For a double gate device there is both a top gate and bottom gate which can either be connected or biased independently, depending on the application. Additionally, the transistors can have a coplanar or staggered configuration, in reference to the gate position relative to the source/drain metals. If the source/drain metal is on the same side of the semiconducting layer the device is coplanar. If the source/drain metal is on the opposite side of the semiconducting layer the device is staggered. An illustration showing the different top and bottom gate configurations is shown in figure 1.9. Using TFT terminology, a traditional bulk MOSFET device would be a coplanar top gate.

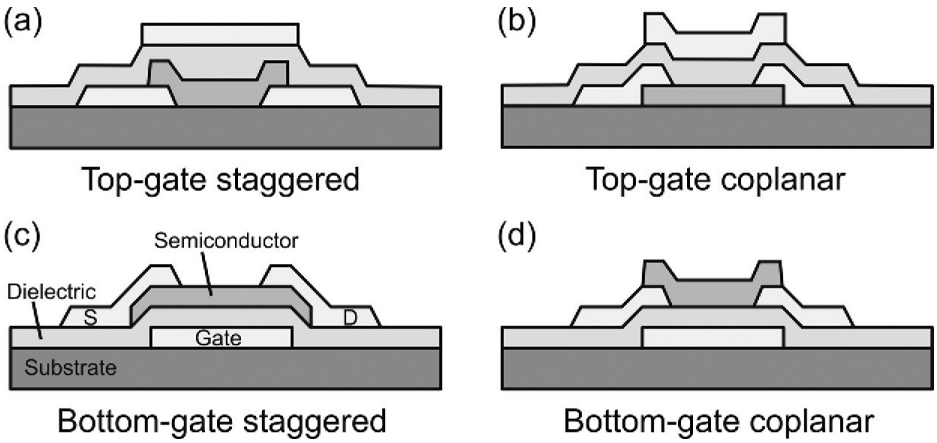

Figure 1.9 Possible TFT Configurations [11]

Chapter 2. LOW TEMPERATURE POLYCRYSTALLINE SILICON: TECHNIQUES & TRAITS

Amorphous silicon TFTs are struggling to keep up with the mobility and stability required for next generation display's pixel circuitry. While polysilicon is an attractive replacement and already used widely in the IC industry, the display industry is unable to use those methods. Thermal limitations inherent to the display glass prohibit high temperature processing. There have been many investigations to modifying the crystallization process so that it is performed at a lower temperature. These methods are collectively known as low temperature polycrystalline silicon (LTPS).

2.1 DISPLAY GLASS THERMAL LIMITS

For display glass a commonly referenced temperature is the strain point. The strain point is defined as the temperature at which the viscosity is 1014.5 poise [12]. An example of a glass viscosity curve is shown in figure 2.1. It highlights different key viscosities for different applications of glass. While the strain point is precisely defined, the maximum allowed processing temperature is more ambiguous and lower. For Corning® Lotus™ NXT display glass, the strain point is 752 °C [13] but extended processing above 630 °C for extended periods of time will cause dimensional issues.

The glass substrate imposed thermal limit is due to both the glass properties and the process by which display glass is formed. There are two main phenomena that define the glass's thermal limit: viscous sag and thermal compaction. Viscous sag is caused when the glass is heated into its viscoelastic transition range, as shown in figure 2.1, and undergoes viscous relaxation, allowing the gravitational force to deform the substrate. This can cause issues with later substrate handling, both for transportation and on vacuum chucks [14]. Thermal compaction is the permanent dimensional change of the substrate after processing at elevated temperatures. This occurs due to the glass not reaching thermal equilibrium during the formation process. Subsequent thermal processing allows the glass to relax on the atomic scale and causes a change in volume. For the temperature range used in display manufacturing this change is almost always negative, leading to the nomenclature of compaction. Unfortunately, the magnitude of this effect is influenced by the thermal history of the batch that the glass came from so it cannot be compensated for in the manufacturing process [15]. This can cause both issues with device lithographic overlay and misalignment of the TFT backplane and color filter [14,15].

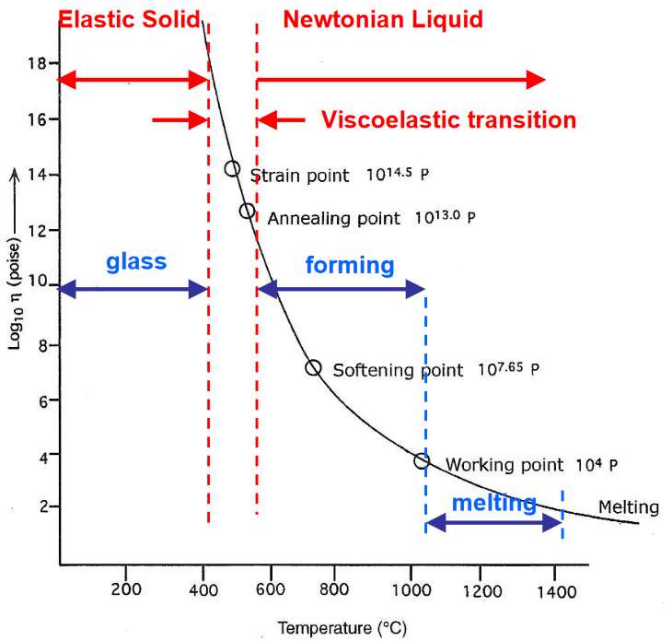

Figure 2.1 Example glass viscosity curve [16]

2.2 LOW TEMPERATURE POLYCRYSTALLINE SILICON

LTPS is an attractive material for next generation TFTs for displays. It offers a wide variety of benefits including high mobility, CMOS compatibility, similarity to the a-Si:H TFT fabrication process, and bias and environmental stability. While the name includes 'low temperature', this is a bit of a misnomer; the low temperature portion refers to the temperature that the substrate experiences. Any process in which silicon is crystallized while the substrate stays below its thermal limit is considered to be LTPS. There are two schemes for the crystallization, bulk heating and surface heating. In bulk heating, the entire stack is uniformly heated, requiring the maximum temperature of the film to remain below the thermal limit of the glass. The second technique is surface heating, where the thin silicon film is heated rapidly, potentially entering the melt phase, while the substrate remains below the thermal limit.

2.2.1 Solid Phase Crystallization

Solid phase crystallization (SPC) is the simplest of the LTPS methods. SPC is a bulk heating method where the substrate is heated up to ~ 600 °C for extended periods of time, i.e. 10 to 100 hours. The film forms nucleation sites randomly; if they are smaller than a critical radius the nuclei are not stable and dissolve back into the amorphous film. If the nucleation site is the critical radius or larger the crystallite is stable, and the grain growth phase begins. The grains will continue to grow until the crystallization front meets that of another crystallization front or an interface. If the grains are different sizes the smaller grain will start to dissolve and will be incorporated into the larger, a process known as Ostwald ripening. However, if the two grains are relatively the same size, the grain boundary is metastable, and the grain growth will no longer continue in that direction. For most SPC growth conditions the final grain size is limited to the film thickness due to a high nucleation rate relative to the growth rate.

A representative electrical characteristic for a p-channel SPC TFT is shown in figure 2.2a. The subthreshold region of the device is relatively shallow and demonstrates hysteresis, and the overall drive current is relatively low. Figure 2.2b shows an example transfer characteristics for an n-channel SPC crystallized top-gate TFT, and an as-deposited (a-Si:H) device for comparison. The SPC device exhibits a higher drive current and comparable off state leakage when compared with the as-deposited a-Si device. The subthreshold slope in the two devices are similar, with SS ~ 1 V/dec. The shallow subthreshold limits the TFT switching ability, restricting the possible applications.

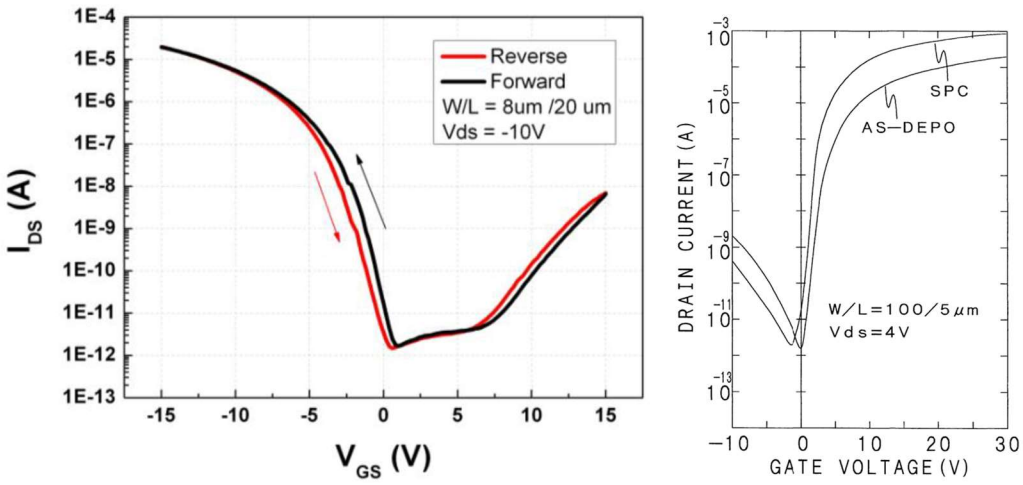

Figure 2.2 a) Hysteresis characteristics for a p-channel SPC TFT [17] b) comparison of n-channel transfer characteristics for a top gate as deposited a-Si and SPC TFT with channel thickness of 25 nm [18]

While SPC is a simple fabrication process for LTPS there are many disadvantages. One disadvantage of SPC LTPS is the size of the grains. For most TFT applications the thickness of the film is 100 nm or less, so this limits the grain size to at most 100 nm. These small grains produce numerous grain boundaries, lowering the carrier mobility. Another issue with SPC is the duration of the high temperature process. To achieve the highest crystallization rate the temperature of the processing is close to the thermal limit of the glass. The extended process time causes the substrate to compact and causes further processing issues, as discussed in section 2.1. Additionally, adding a 10 hour or longer thermal step greatly increases the fabrication time, causing a fabrication bottleneck. Due to the low mobility, substrate challenges, and processing time, SPC LTPS has not been adopted into mainstream display manufacturing.

2.2.2 Metal Induced Crystallization

Metal induced crystallization (MIC) is another bulk heating method for forming LTPS. For MIC a thin layer of metal, less than 5 nm, is deposited on an amorphous silicon film. The stack is then heated in a furnace for an extended crystallization anneal. The crystallization occurs at a lower temperature and faster than SPC crystallized films. The most common metal used is nickel, however many other metals have been investigated such as aluminum, palladium, and copper [19].

A schematic showing the mechanism of nickel induced crystallization is shown in figure 2.3. Initially the silicon and nickel form a $NiSi_2$ precipitate. A thin epitaxial layer of crystalline silicon then forms on the {111} face of the silicide due to a small lattice mismatch, 0.4%. The stable crystalline phase lowers the free energy of the silicon from the initial metastable amorphous phase. The crystallization propagates due to the $NiSi_2$ that is in contact with the a-Si being silicon rich relative to the portion in contact with the c-Si due to the relative chemical potentials of the Si and Ni. This causes Ni diffusion from the crystalline interface to the amorphous interface and the Si to diffuse in the opposite direction. The crystallization continues with the $NiSi_2$ consuming the a-Si and leaving c-Si [20].

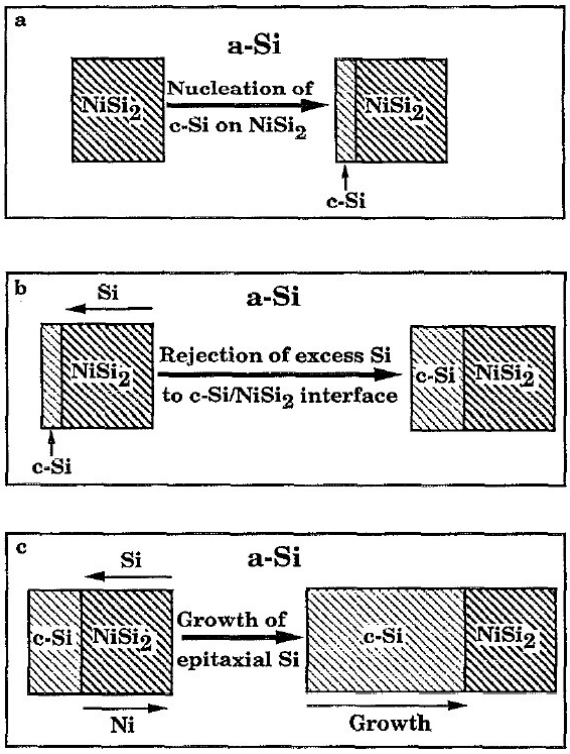

Figure 2.3 Illustration showing mechanism for nickel induced crystallization [20]

There are also two variants of MIC, metal induced lateral crystallization (MILC) and metal induced cap crystallization (MICC). MILC is similar to MIC but the metal film is patterned into islands before the crystallization to occur. This causes the crystallization to occur laterally in regions not covered by the islands. This causes the grains to have preferential crystal orientations and can result in larger grain sizes. MICC incorporates a thin nitride capping layer between the metal and film, shown in figure 2.4. The metal diffuses through the cap and into the underling silicon.

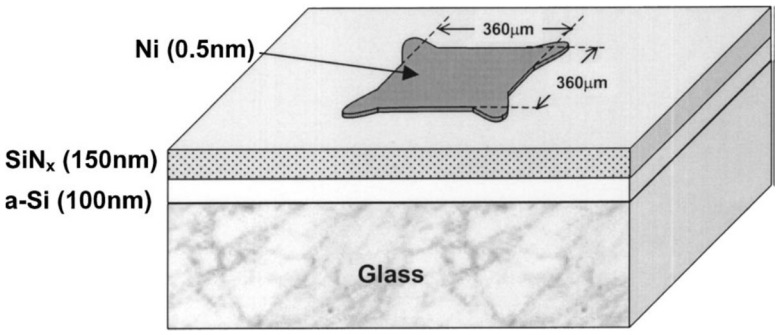

Figure 2.4 Illustration of film stack for MICC [21]

Figure 2.5 shows the transfer characteristics for a top gate MICC device. The device exhibits a good threshold, mobility, and on/off state ratio. While these results are quite good, MICC has not been widely adopted in industry. The main challenges implementing MIC for TFTs is metal contamination. The residual metal left after crystallization degrades device electrical performance. It can increase the leakage current, degrade the subthreshold slope, and cause lower channel mobility.

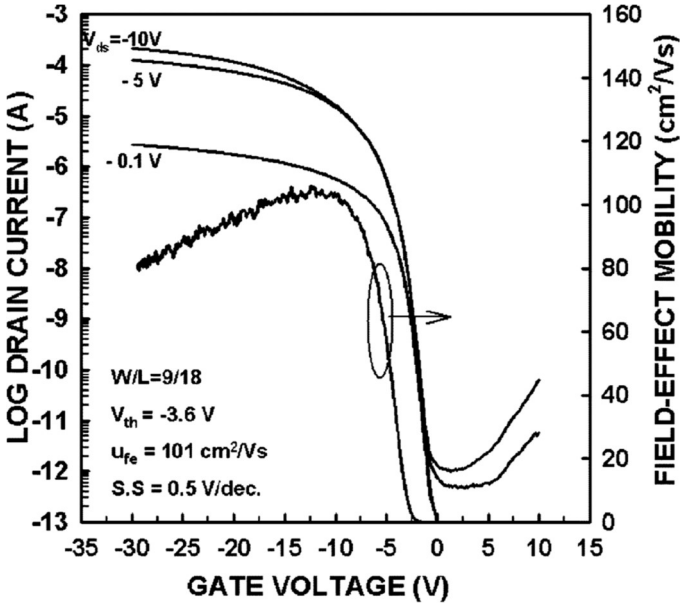

Figure 2.5 Transfer characteristics and mobility for a MICC top gate device [22]

2.2.3 Excimer Laser Annealing

Excimer laser annealing (ELA) is a surface heating LTPS method that uses an excimer laser to crystallize the amorphous silicon with repeated nanosecond-duration pulses. The most commonly used laser is XeCl based (λ = 308 nm), but some research has been done with KrF lasers (λ = 248 nm). Each section of the film is irradiated multiple times and the substrate is moved a small amount between each pulse to produce a more uniform crystallization, shown in figure 2.6. This allows for a reduction of the effects of beam non-uniformity and pulse to pulse variation [23].

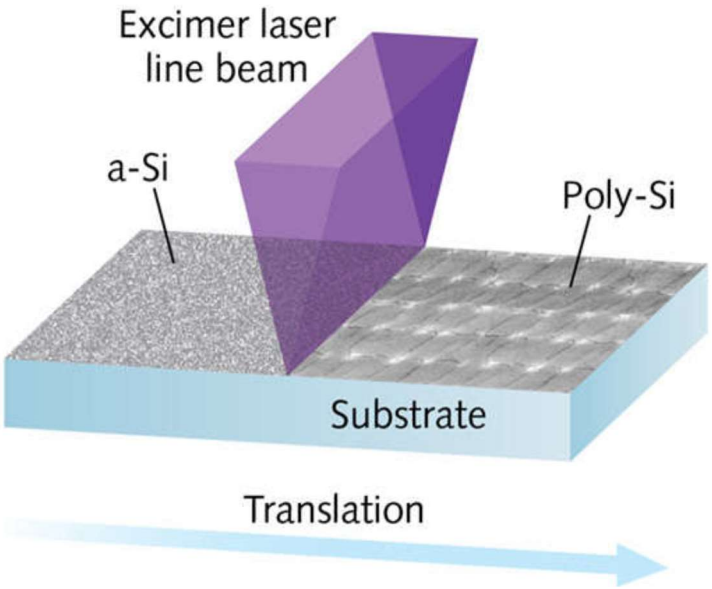

Figure 2.6 Illustration of excimer laser annealing process [24]

The absorption length for the XeCl laser is 7.6 nm in amorphous silicon which is much smaller than the typical film thickness of 50 nm [25]. This means that the majority of the energy is absorbed and almost none is transmitted, which allows the film to receive enough energy that it can enter the melt phase while the substrate remains well below its thermal limit. Additionally, since each pulse discharge takes place on the nanosecond timescale the film is rapidly heated and there is

minimal thermal conduction to the substrate. This method allows for high quality polycrystalline silicon and is currently used in manufacturing for small high-resolution displays.

ELA crystallization results in a film that has moderately sized grains with raised grain boundaries and protrusions as seen in figure 2.7. Protrusions are formed where three (or more) grains intersect. The raised topography is due to a difference in density between liquid and solid phase of silicon; when it solidifies it undergoes volume expansion. The displaced material deforms out of plane, resulting in the ridges and protrusions.

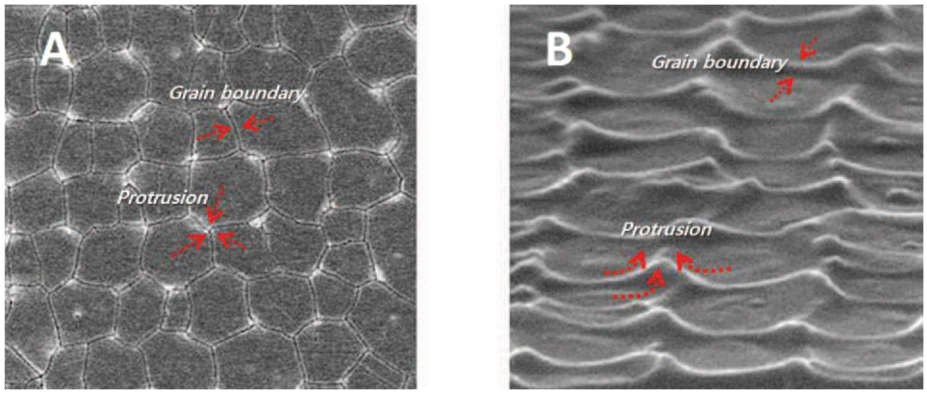

Figure 2.7 SEM micrograph of ELA crystallized polysilicon a) top-view b) tilted view [26]. Grain size approximately 300 nm

TFTs fabricated from ELA crystallized silicon can offer excellent electrical characteristics. A reprehensive transfer characteristic for a top gate ELA device is shown in figure 2.8. They have steep subthreshold, high drive current while maintaining minimal leakage current, CMOS compatibility, and are scalable to small device dimensions. One drawback in their electrical performance is their threshold voltage uniformity. Due to the large size of the grains the number of grains in the channel can vary, this results in a small variation in the mobility and has a larger impact on the threshold voltage.

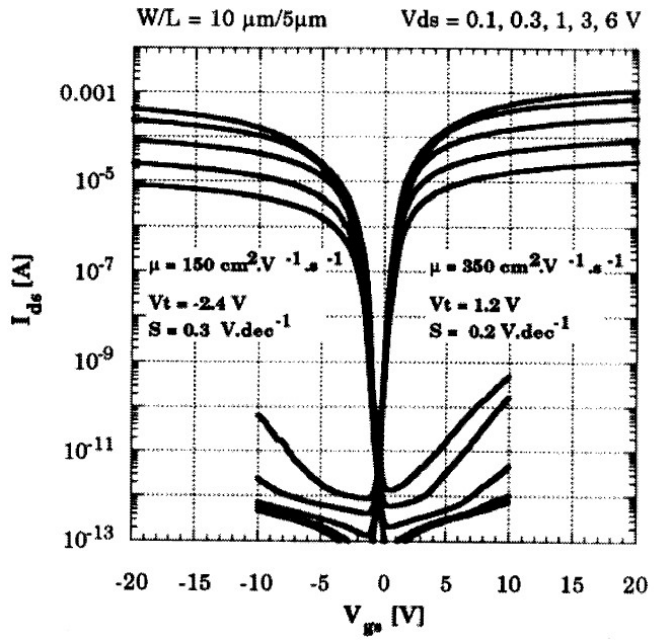

Figure 2.8 Example transfer characteristics for ELA crystallized TFTs [27]

For scaling to large display substrates, the systems become very complicated and expensive. The main issue for larger substrates is the excimer laser themselves; a proposed system is shown in figure 2.9. In order to crystallize the silicon on display glass the beam is converted into a line beam; a long narrow exposure window, allowing for better pulse to pulse repeatability and uniformity. To maximize the throughput of the tool each substrate is exposed at most twice. With panels larger than Gen 6 this becomes an issue as single lasers can no longer provide enough energy to crystallize the area required. Some companies have extended the usable range of ELA systems to Gen 8 by combining multiple lasers into a single beam [28]. This method requires a more complicated and expensive system and has not been adopted by industry.

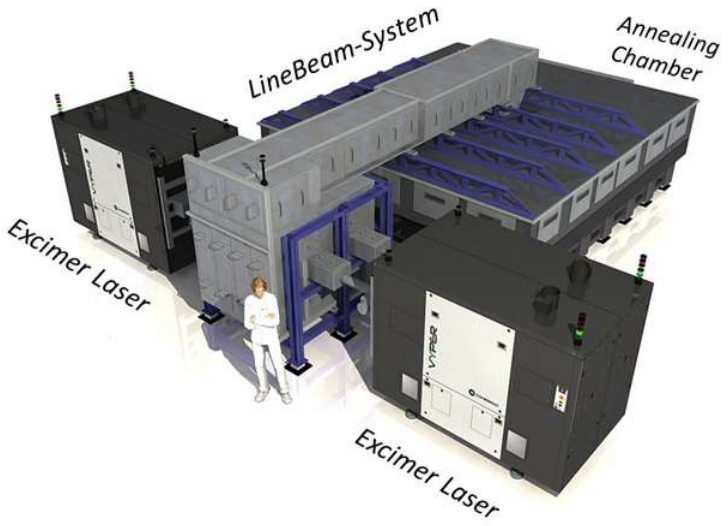

Figure 2.9 Rendering of a potential ELA system for a manufacturing setting [29]

2.2.4 Continuous Wave Laser

Continuous wave laser annealing is being investigate as a replacement for ELA. There are two main types of continuous wave laser annealing, green laser annealing (GLA) and blue laser annealing (BLA). The most common type of GLA uses a second harmonic Nd:YAG laser, which has an output wavelength of 532 nm. This method has resulted in high quality LTPS films. Unfortunately, the absorption coefficient for amorphous silicon at that wavelength is low so the process requires high laser power. This can cause damage to the glass substrate due to the penetration depth and the power required for crystallization. Due to this GLA is better suited for films that are 200 nm or thicker; much thicker than typically used for TFTs [30].

Blue laser annealing uses a GaN solid state laser. The wavelength of light used varies slightly depending on the device structure of the laser diode. The penetration depth of the light is longer than that of the excimer laser allowing for thicker films to be crystallized, but not so deep that is causes excessive heating of the glass substrate [30-32]. Additionally, the use of GaN laser diodes

allows for a much cheaper and more energy efficient system. BLA is a relatively new process and has demonstrated excellent results as seen in figure 2.10 [32]. However, many engineering challenges remain, such as an increase in beam size and reduction in cost, to overcome before it is manufacturable.

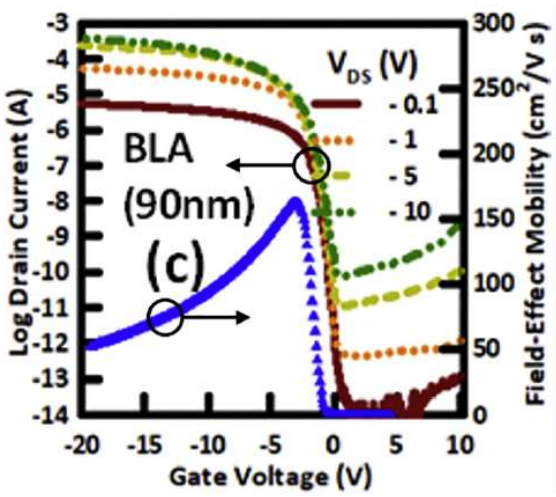

Figure 2.10 Transfer characteristics for a blue laser annealed TFT with a 90 nm thick channel [32]

2.2.5 Flash Lamp Annealing

Flash lamp annealing (FLA) crystallizes the silicon by using a microsecond-scale pulse from a xenon flash bulb. The bulb emits a broad-spectrum pulse that melts the silicon while not significantly heating the substrate. The absorption coefficient versus wavelength and the emission spectra for a Xe flash lamp is shown in figure 2.11.

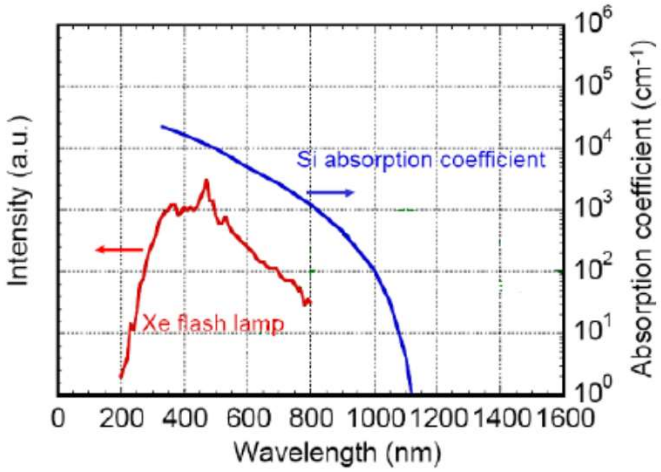

Figure 2.11 Emission spectrum for a generic Xe flash lamp and Si absorption coefficient versus wavelength [33]

The ultra-violet portion of the light is absorbed by the thin film silicon and the longer wavelengths that make it through the silicon also pass through the glass substrate. The substrate is preheated to lower the intensity of the light required to melt the film. The temperature remains below the thermal limit and the duration is short enough that the dimensional stability of the glass is maintained. Figure 2.12 shows a simplified illustration of a FLA system.

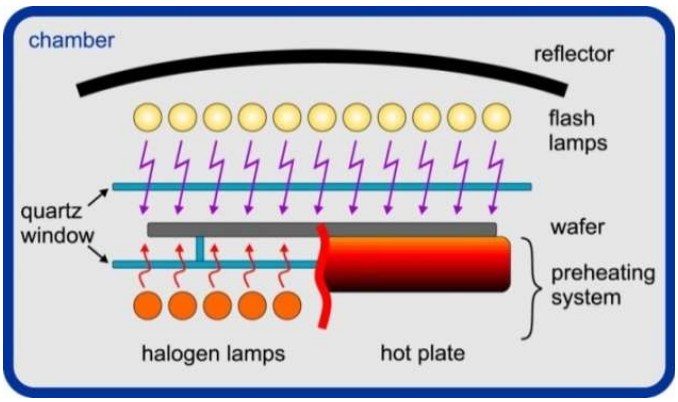

Figure 2.12 Illustration of a flash lamp annealing system with radiant or conductive heating [34]

FLA is an attractive alternative to ELA due to the fact that the exposure area is more easily scaled. A 3.8-meter-wide system is already commercially available and used for architectural glass coatings; a picture of this system is shown in figure 2.13. Due to the parallel nature of the system the crystallization window can be further enlarged by adding additional flash bulbs.

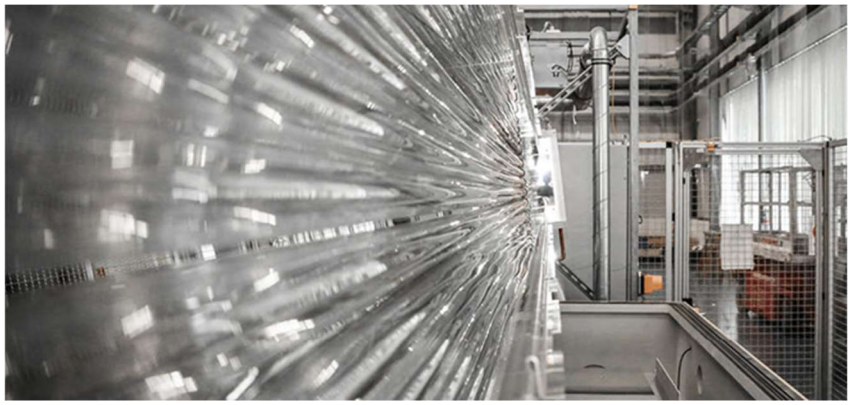

Figure 2.13 A 3.8-meter-wide flash lamp system for architectural glass coatings [35]

2.3 INITIAL FLASH LAMP ANNEALED TFTS

The first reported flash lamp annealed transistor was reported in 2010 by the group of Prof. Jing Jang from Kyung Hee University. They were able to fabricate a p-channel transistors that exhibited promising electrical characteristics. They used a multi flash crystallization of a dehydrogenated blanket undoped a-Si film. The substrate was preheated to 450 °C and crystallized with two 100 μs flashes separated by 5 minutes. The estimated energy delivered by each pulse was over 5.2 J/cm^2.

This process resulted in a polycrystalline film with grain size around 15 μm and branchlike grain boundaries. An optical micrograph of the resulting film and a cross-sectional TEM and electron diffraction pattern is shown in figure 2.14. Following crystallization, the individual transistor mesas were formed for electrical isolation and remaining processing was completed.

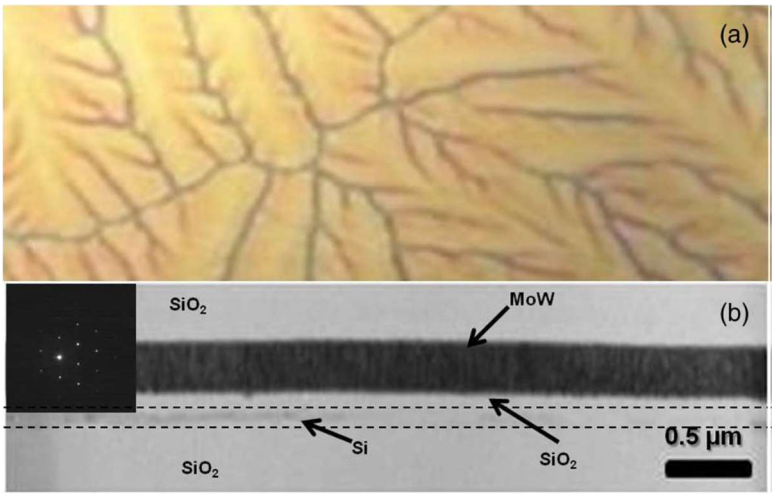

Figure 2.14 a) optical micrograph of FLA crystallized silicon showing branchlike morphology and an average grain size of 15 µm b) cross-sectional TEM micrograph of the TFT with electron diffraction pattern insert [36]

The transfer characteristics and family of curves is shown in figure 2.15. The extracted mobility was 138 $cm^2/(Vs)$, a subthreshold swing of 400 mV/dec, threshold voltage of -1.3 V, and a difference of on/off current over 8 orders of magnitude. While the transfer characteristics for the low drain bias shows excellent device performance there is no high drain bias characteristics. Additionally, for the family of curves there is an absence of the small V_{gs} values. These two exclusions are most likely an indication that the device had difficulty shutting off for high drain biases.

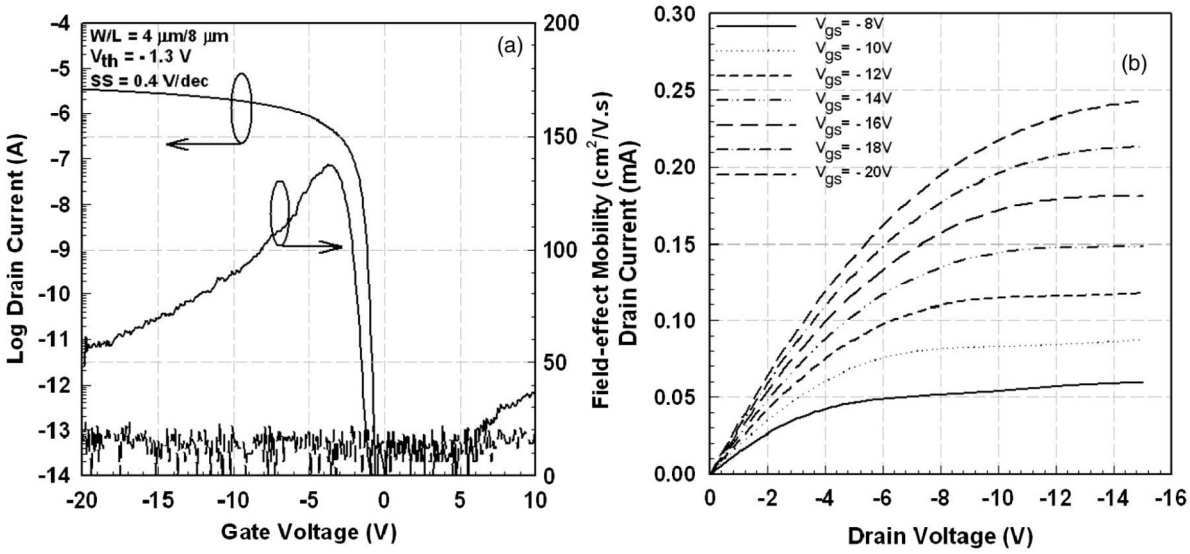

Figure 2.15 Electrical characteristics for PMOS FLA TFT L = 8 µm W = 4 µm a) transfer characteristics b) family of curves [36]

2.3.1 RIT's First Demonstration of FLA TFTs

Both a n-channel and p-channel devices were successfully fabricated on the same substrate. The amorphous silicon was patterned into mesas and the source and drain were implanted before crystallization. The substrate was preheated to 550 °C and crystallized by a single 200 µs flash with bolometer measured energy of 6 J/cm^2. A SEM micrograph and EBSD mapping of a deprocessed device is shown in figure 2.16. The resulting film was smooth with scattered voids, most likely caused by the silicon melting and dewetting from the substrate during the crystallization.

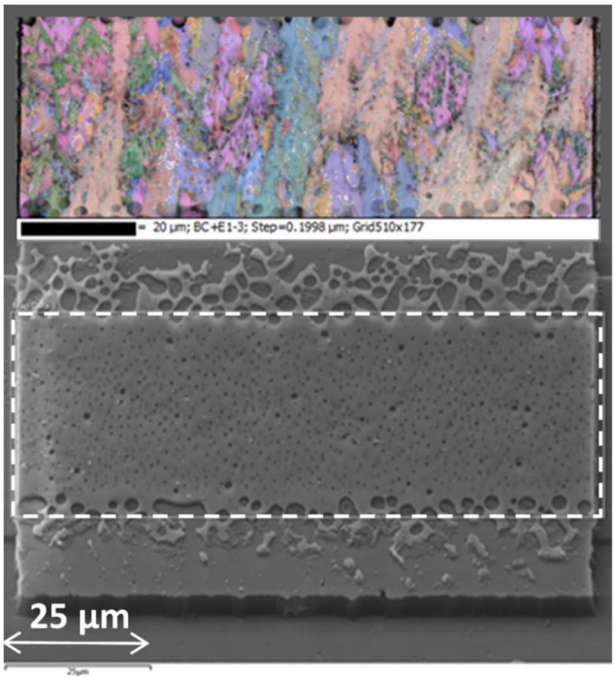

Figure 2.16 SEM micrograph and EBSD mapping of deprocessed TFT showing individual grains [37]

The best transfer characteristics for both device types are shown in both linear and log scale in figure 2.17. The best case NMOS device had a threshold voltage of 0.23 V, channel mobility of 380 $cm^2/(Vs)$, and a subthreshold slope of 120 mV/dec. The best PMOS device had a threshold voltage of -2.82 V, a channel mobility of 143 $cm^2/(Vs)$ and a subthreshold slope of 140 mV/dec.

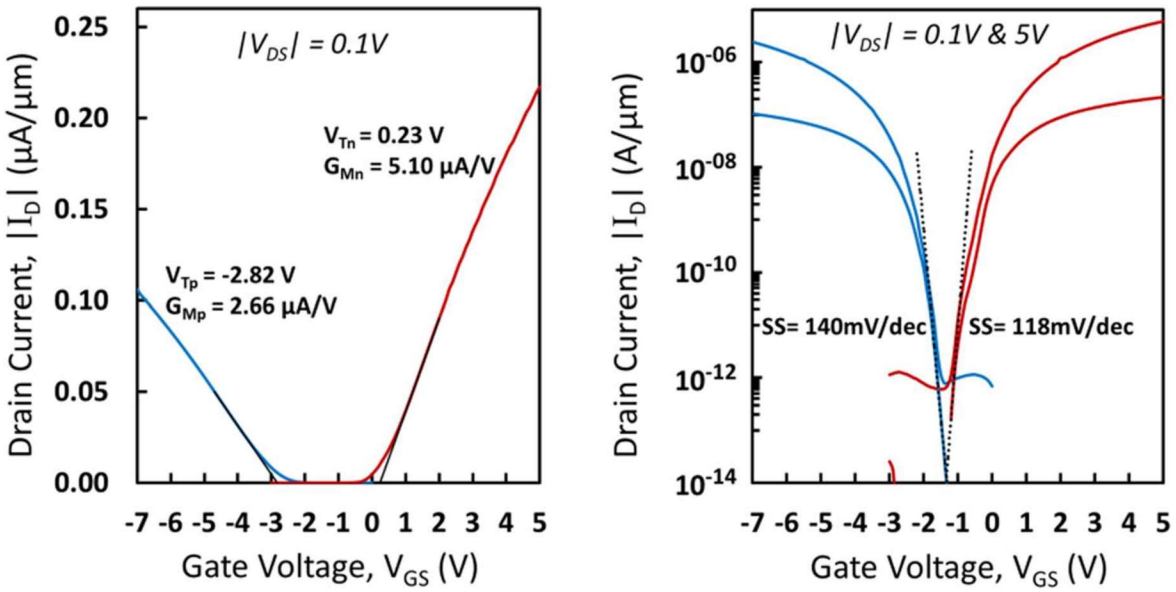

Figure 2.17 Transfer characteristics for NMOS and PMOS TFT Lmask = 32 µm W = 100 µm a) linear scale b) log scale [37]

The change in effective channel length was calculated using Terada-Muta method and were 6.3 µm for the NMOS device, and 13.4 µm for the PMOS device. This large change in effective channel length is most likely due silicon reaching melt phase during the crystallization and the dopant rapidly diffusing from the source and drain into the channel. Due to the large lateral diffusion, making scaled devices is not possible using this approach.

Chapter 3. DEVELOPMENT EFFORTS TOWARDS BOTTOM-GATE LTPS TFTS

Bottom-gate LTPS TFTs have many attractive qualities for next generation displays, however fabrication of these devices has presented many challenges. Due to these challenges, the top-gate is the predominant configuration for LTPS devices. This section will discuss the potential benefits of a bottom gate structure and describe select works that provide details on device fabrication, process integration, and electrical characteristics.

3.1 BENEFITS OF BOTTOM GATE

Bottom-gate LTPS devices have many attributes that make them attractive when compared to more traditional top-gate LTPS devices. Some of these benefits include better semiconductor interface quality, simpler channel passivation, higher gate breakdown voltage, different device integration strategies allowing a reduction in short channel effects, and ability to more aggressively scale devices.

The better interface quality is due to the ability to deposit the gate oxide and silicon in the same chamber without breaking vacuum between, minimizing contamination. Additionally, since the interface is present during crystallization a high-quality interface can be formed. Lastly, the bottom gate integration eliminates the channel interface plasma damage that can occur during gate dielectric deposition, which can occur with the top gate integration. Due to the back channel of the

device (channel region opposite the gate) being directly accessible, passivation is easier to perform either by either hydrogenation or other methods.

Higher gate breakdown voltage in bottom gate devices is due to the smooth interface between the silicon and underlying gate oxide. For ELA crystallized silicon, there are protrusions formed where grains meet. For top gate devices, any protrusions or ridges in the silicon cause deformations that extend into the gate oxide. The protrusions present sites with higher localized electric field and lower dielectric breakdown voltage. The bottom gate does not have these issues since the interface is planer, leading to the field being uniformly distributed. The protrusions still occur but are in the backside passivation layer where there is no concern of applied bias. A Tsuprem4 simulation showing the filed distribution and maximum field for a bottom and top gate device is shown in figure 3.1.

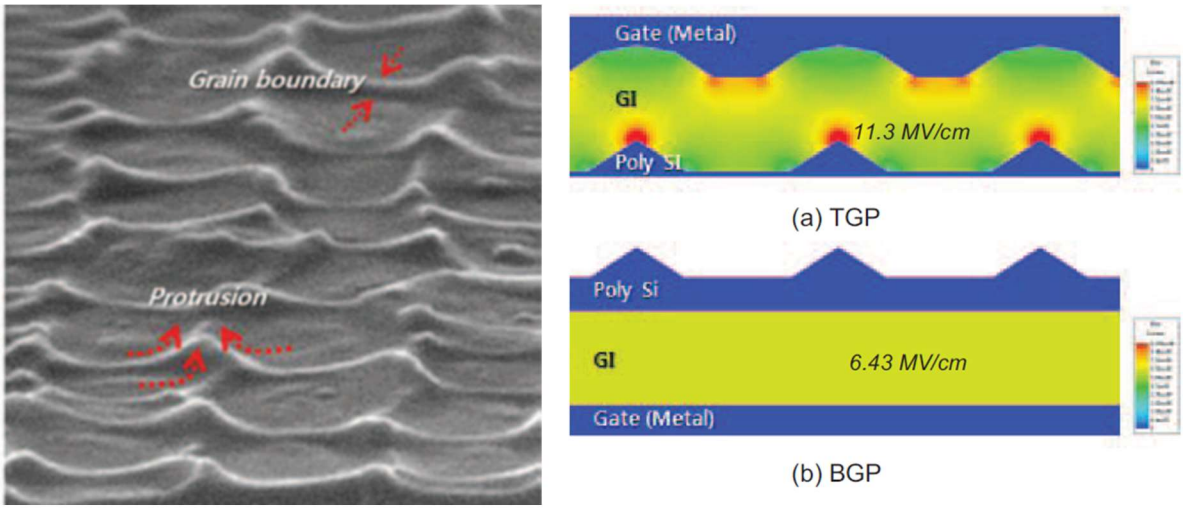

Figure 3.1 Left: SEM micrograph of ELA crystallized silicon showing topography caused by grain boundaries and protrusions (discussed in section 2.2.3) Right: Tsuprem4 simulation of electric field distribution in gate insulator for a) top gate b) bottom gate with insulator thickness 140 nm, 50 nm silicon with 45 nm tall and 140 nm wide protrusions, and V_G = 90 V [26]

The use of a bottom gate also allows for the simple integration of a gate overlapped lightly doped drains (GOLDD) structure in devices. This structure greatly reduces the devices sensitivity to short channel effects. The LDD allows for a reduction of the maximum electric field at the drain end of the device, thus decreasing impact ionization. The improved interface quality inherent to the bottom gate configuration combined with the decrease in impact ionization supports device operational stability and long-term reliability.

Bottom-gate devices also allow for more aggressive scaling since they exhibit suppressed short channel behavior for given dimensions. A reduction in oxide thickness would enable better channel control while still managing to avoid gate leakage and dielectric breakdown. Scaled bottom gates would allow for smaller pixel sizes or more complex pixel control circuitry.

3.2 BOTTOM GATE LTPS TFTS: FABRICATION & CHARACTERISTICS

There have been many previous attempts to fabricate bottom gate LTPS TFTs with various levels of success. There are three main LTPS techniques that have been used to fabricate bottom gate devices; metal induced crystallization, excimer laser annealing, and continuous-wave laser annealing.

3.2.1 Metal Induced Crystallization

The group of Jing Jang from Kyung Hee University fabricated a n-channel LTPS TFT with a MoW bottom gate and n+ a-Si:H source and drain. The channel was crystallized via MICC (see section 2.2.2). Illustrations showing the devices at various processing steps are shown in figure 3.2. A thin film of a-Si:H was deposited on the substrate on top of the gate and gate dielectric. Then the film was dehydrogenated and a 50 nm SiN_x film was deposited as the capping layer. Less

than a monolayer of Ni was sputtered onto the capping layer. The sample was then annealed at 580 °C for 10 hours to crystallize the film. The SiNx layer was then removed and the sample was annealed at 650 °C for 10 minutes in a pulsed rapid thermal annealer (PRTA) to improve the films quality and to reduce the Si/SiO_2 interface states. The TFTs mesas were then defined and etched. A n+ a-Si:H layer was deposited to form the source and drain, and chrome was used for metallization. A SiNx film was PECVD deposited as the backchannel passivation.

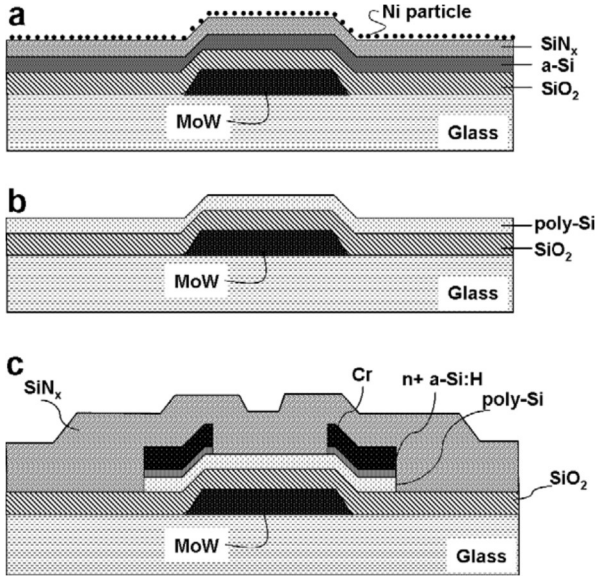

Figure 3.2 a) Device stack before crystallization b) device after crystallization and removal of cap c) completed MICC BG TFT [38]

Prior to electrical testing the devices were annealed at 200 °C. This was most likely to dehydrate the surface of the passivation nitride. Any water that had adsorbed on to the surface between device completion and testing could act a source of charge on the back channel, thus distorting the results. The transfer characteristics were measured and are shown in figure 3.3. The device had a field effect mobility of 34.8 $cm^2/(Vs)$, a subthreshold swing of 1.08 V/dec, and an off-state current of less than 1 pA/μm at a V_{DS} of 5 V. An extracted value for the threshold voltage

for the device was not given. Based on a visual interpretation of the figure the device would require an overdrive voltage to effectively turn off the device.

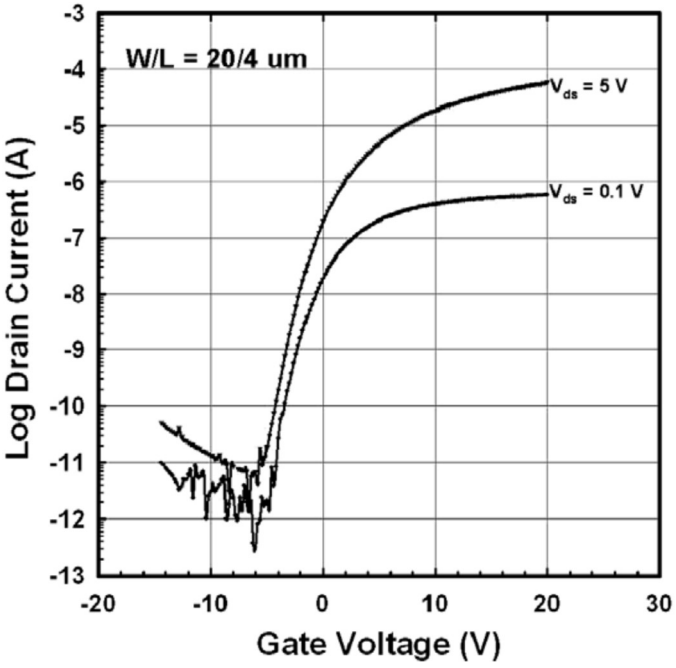

Figure 3.3 Transfer characteristics of a bottom gate n-channel LTPS TFT W = 20 µm L = 4 µm [38]

A subsequent work from the Kyung Hee University group investigated the use of a spin on glass at the gate dielectric for MICC crystallized bottom-gate p-channel TFTs. Figure 3.4 shows important steps during the TFT fabrication. After gate formation they spin coated and cured a spin on glass layer for the gate dielectric. Subsequently they PECVD deposited a 50 nm a-Si:H film followed by a 50 nm PECVD SiNx capping layer. There was no mention of a dehydrogenation process between the two depositions. Less than a monolayer of nickel was deposited on top of the nitride. The samples were then crystallized in a furnace at 590 °C for 20 hours. Post crystallization the nitride cap was removed, and the polysilicon was then etched into the final TFT mesas. The

source and drain were doped and activated. Then the source and drain electrodes were deposited and a thick SiN_x film was deposited as the passivation layer.

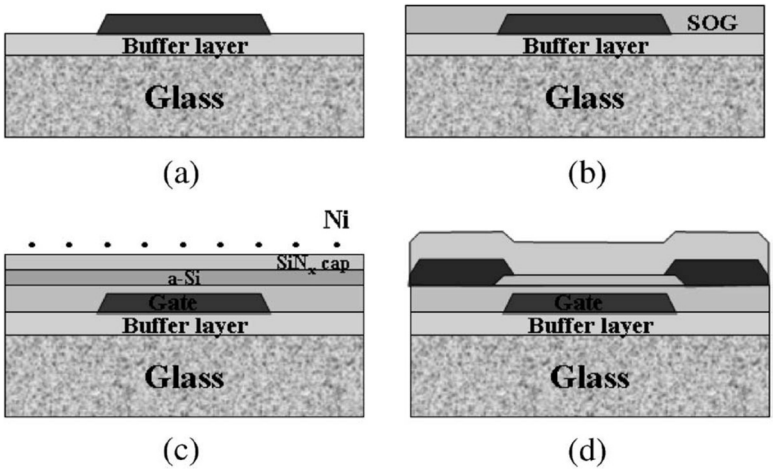

Figure 3.4 a) Formation of gate electrode b) coating of gate dielectric c) device stack before MICC d) completed device [39]

Electrical characteristics for a device were provided and are shown in figure 3.5. The device exhibited a field effect mobility of 48.2 $cm^2/(Vs)$, a threshold voltage of -4.2 V, a subthreshold swing of 1.2 V/dec, an off state current of less than 0.4 pA/μm at VDS of -0.1 V. Additionally, the device exhibited a difference in on and off state current of 6 orders of magnitude.

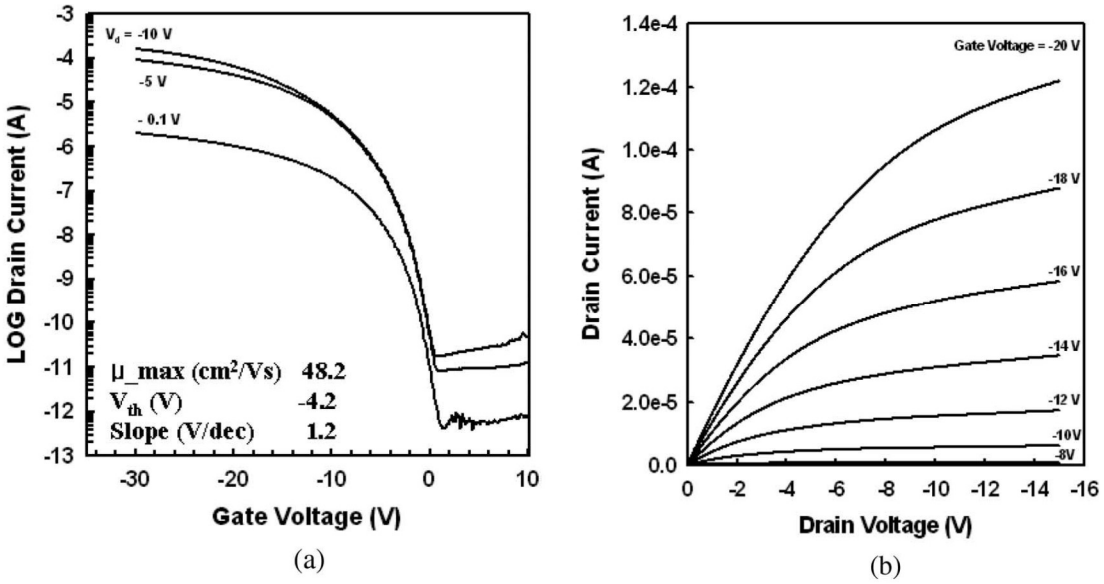

Figure 3.5 a) Transfer characteristics and b) family of curves for a p-channel (L/W) 10 µm / 10 µm BG TFT [39]

3.2.2 Excimer Laser Annealing

Tsai *et al.* [40] fabricated a double gate TFT with the channel being crystallized by ELA. Illustrations of various key steps and a cross-sectional SEM of a completed device are shown in figure 3.6. For their experiments they used a silicon wafer with a thick oxide barrier and doped polysilicon for the gate. The gate oxide was deposited followed by 100 nm of a-Si for the channel. The samples were then crystallized using a KrF laser (λ = 248 nm) with the samples in a vacuum chamber at 10^{-3} Torr and room temperature. A laser energy density of 450 mJ/cm^2 was used and the shots were overlapping 95% (20 shots per area). The polysilicon was then etched to form the device mesa. The top gate dielectric was deposited, and another polysilicon layer was deposited for the top gate. After formation of the top gate electrode the devices were implanted, doping the gate as well as the source and drain. An oxide was then deposited for passivation and the dopants were activated. The devices were sintered and underwent a plasma treatment.

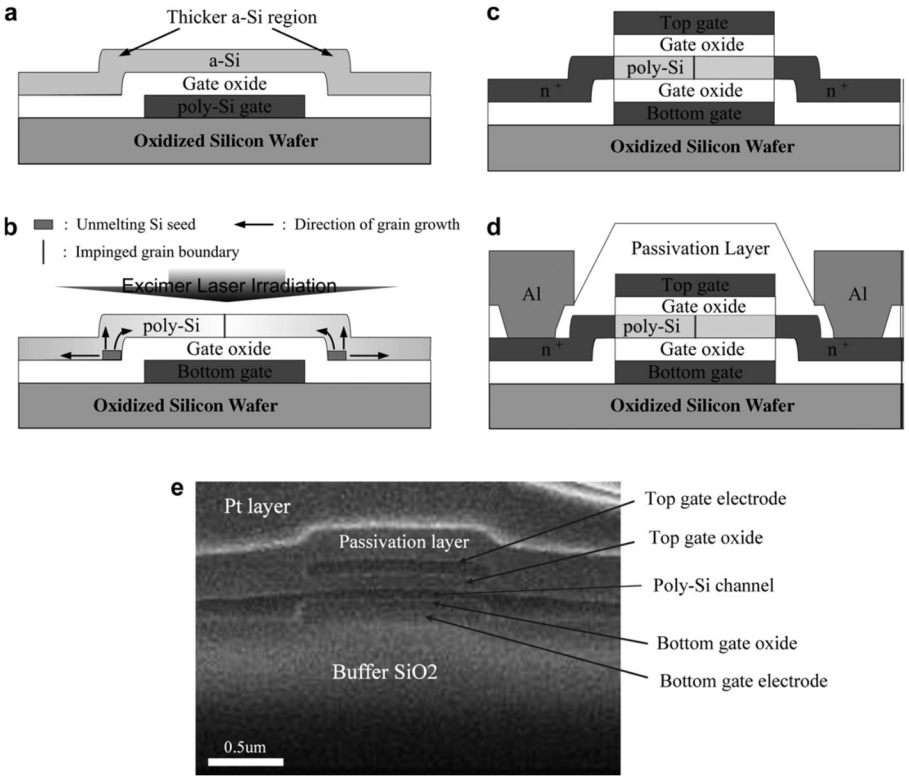

Figure 3.6 Illustration of a) film stack pre crystallization b) during crystallization indicating super lateral growth (SLG) c) TFT after doping d) completed device e) SEM micrograph of completes double gate TFT [40]

Three different devices were fabricated and compared, the ELA double-gate, a traditional ELA top-gate, and a SPC double-gate. The transfer characteristics for all three devices is shown in figure 3.7a and the family of curves is shown in figure 3.7b. The ELA double gate had a threshold voltage was -2.48 V, a field effect mobility of 396 $cm^2/(Vs)$, subthreshold swing of 335 mV/dec, and on/off current ratio greater than eight orders of magnitude.

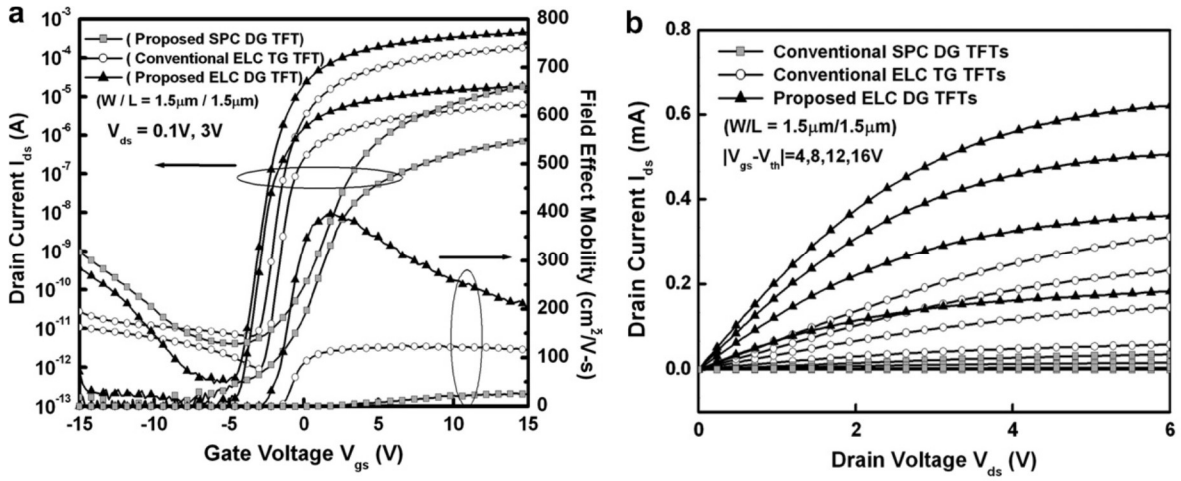

Figure 3.7 Electrical comparison between SPC double-gate, top-gate ELA, and double gate ELA TFTs a) transfer characteristics b) family of curves; all devices L = 1.5 μm W = 1.5 μm [40]

Follow up work by Wang *et al.* [23] fabricated bottom gate devices. The fabrication process used was nearly identical to that of the double gate devices and the electrical results were also comparable and are shown in figure 3.8. The bottom gate device with 50 nm of gate oxide exhibited a field effect mobility of 323 $cm^2/(Vs)$ and nearly 9 order of magnitude between the on and off state currents.

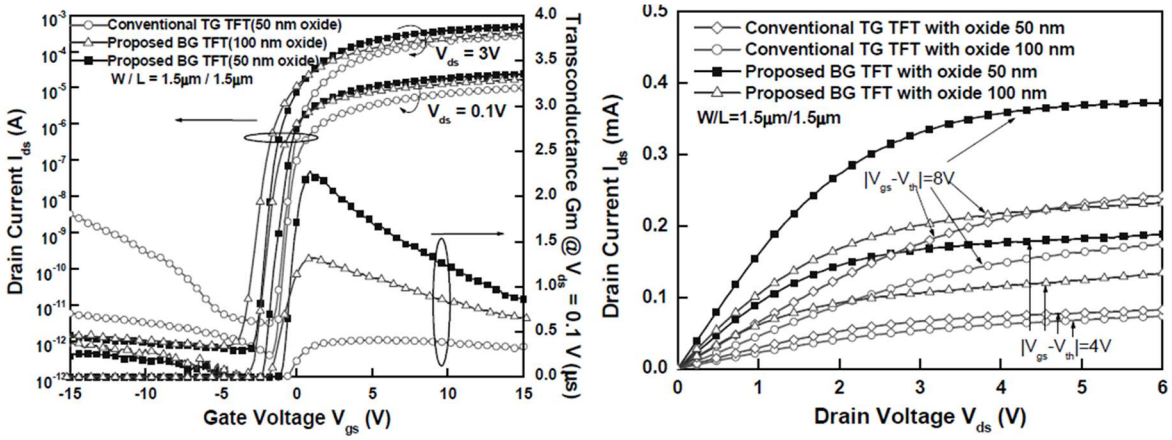

Figure 3.8 Electrical comparison between top-gate ELA with 50 nm gate dielectric, bottom gate ELA with 100 nm gate dielectric, bottom gate ELA with 50 nm gate dielectric. Left: transfer characteristics Right: family of curves; all devices L = 1.5 µm W = 1.5 µm [23]

As part of their study they fabricated transistors with various channel dimensions. The mobility of each channel dimension is shown in figure 3.9. For short channel length devices, the mobility of the bottom gate devices is much higher than the comparable top gate devices. As the channel length gets longer the top gate devices start having higher mobility than the bottom gate.

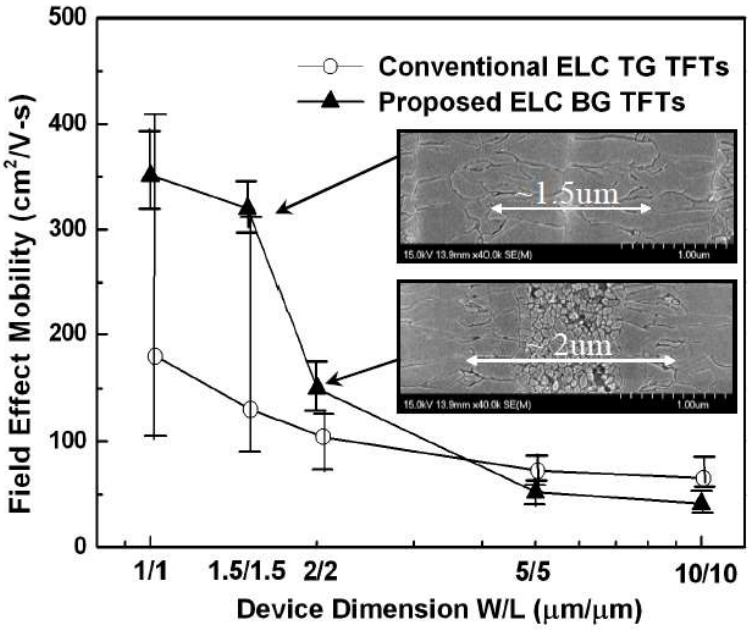

Figure 3.9 Comparison of top-gate and bottom-gate mobility as a function of device dimensions, insert showing SEM micrograph of bottom-gate devices length 1.5 μm and 2 μm [23]

This is due to the crystallization regime that is being used for the bottom gate devices, the super lateral growth (SLG) regime. An illustration showing the regime is shown in figure 3.10. This type of crystallization occurs when the laser is high enough intensity to melt the majority of the film with the exception of the thicker region caused by the topography of the gate, this thicker region then acts as a seed for the solidification of the liquid silicon. This technique allows for large grain growth, allowing for the short channel devices to have high mobility. For the longer bottom gate devices, the liquid silicon starts to randomly nucleate before the crystallization front arrives, resulting in small grains in the middle of the channel, decreasing mobility. These two cases are shown in the insert of figure 3.9. Top-gate devices are extremely difficult to tune to the SLG regime due to the lack of variation in the film thickness. They are uniformly melted resulting in random nucleation and smaller grains with low mobility.

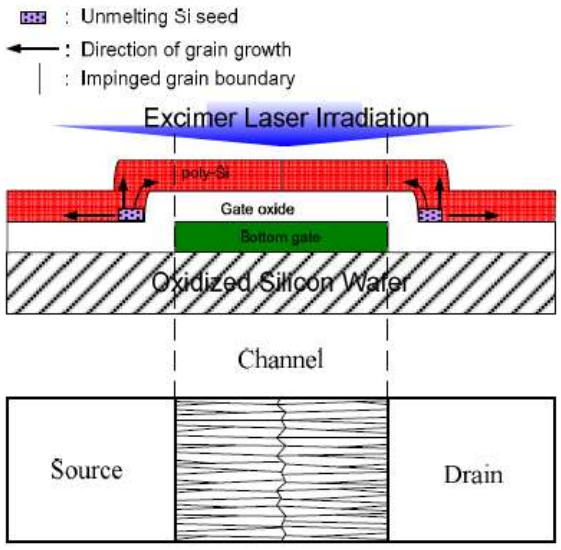

Figure 3.10 Illustration showing super lateral growth regime during pulse and final result [23]

In 1995 Hayashi *et al.*, a research group at Sony, fabricated both n-channel and p-channel bottom gate devices using ELA crystallization. Additionally, they fabricated the n-channel devices both with and without a lightly doped drain (LDD). An illustration of cross-section of a completed n-channel device with LDD is shown in figure 3.11. They patterned and etched a Mo/Ta stack to for the gate electrode. The gate was then anodized to form a thick Ta_2O_5 layer. Subsequently SiNx and SiO_2 were PECVD deposited to complete the gate dielectric stack. The channel, 30 nm a-Si, was then PECVD deposited. Prior to crystallization the a-Si was dehydrogenated. The silicon was then crystallized using a XeCl laser (λ = 308 nm) with a pulse duration of 25 ns, total energy of 360 mJ/cm^2, and a beam overlap of 90% in a nitrogen ambient at room temperature. Next SiO_2 was deposited on the silicon. Backside illumination was then used to self-align the source and drain and the oxide was etched. The doping was done using a non-mass-separated ion doping system. The dopant was activated using the same laser conditions as crystallization but with an energy of 280 mJ/cm^2. An interlayer dielectric was then deposited, and Al interconnects were

formed. A thick SiN_x layer was deposited for passivation and then the devices underwent a hydrogenation.

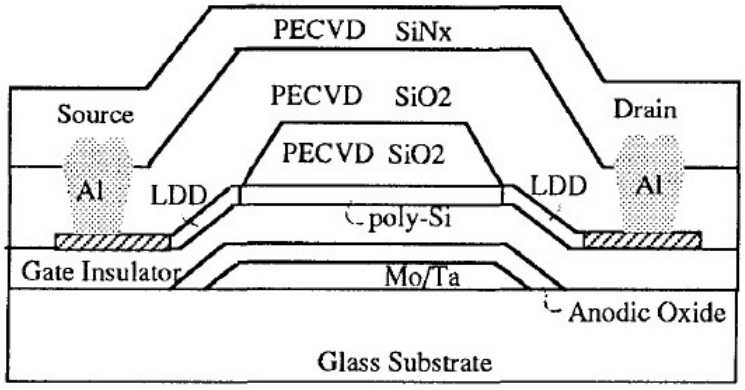

Figure 3.11 Schematic cross-section of ELA crystallized BG device [41]

Electrical transfer characteristics were measured from L = 10 µm W = 10 µm device with n-channel both with and without LDD and p-channel without the LDD. The characteristics for these three devices are shown in figure 3.12. All devices had a 7 orders of magnitude difference for on and off currents. The extracted field effect mobility was 73 $cm^2/(Vs)$ for the n-channel and 30 $cm^2/(Vs)$ for the p-channel. The subthreshold swing was 390 mV/dec for the n-channel and 570 mV/dec for the p-channel. The n-channel with LDD exhibited a leakage current of less than 1 pA/µm. By introducing the LDDs they were able to lower the leakage current of the device, but this also resulted in a reduction on the drive current due to the increased series resistance.

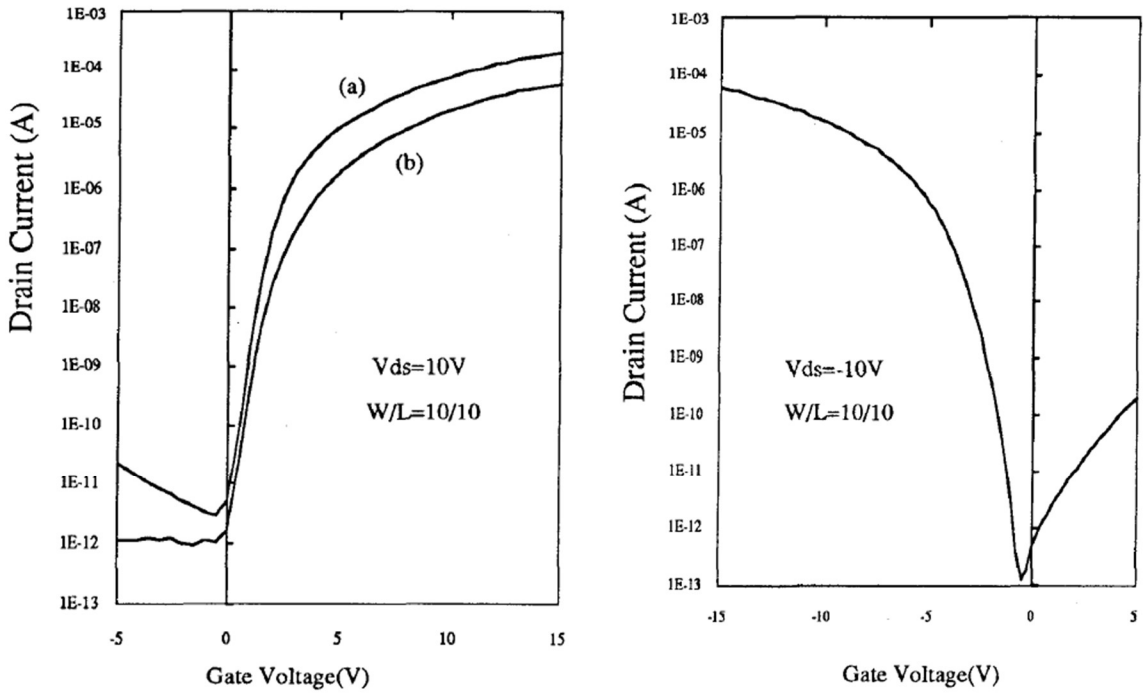

Figure 3.12 Left: transfer characteristics of a n-channel TFT a) without LDD b) with LDD; Right: transfer characteristics of p-channel TFT without LDD [41]

The research group of Oh *et al.* from LG display, fabricated a bottom gate device via ELA with a tapered metal gate to minimize the gate step height. Crystallization with a bottom gate requires a higher energy exposure to compensate for the thermal sink of the gate. With a thick gate this leads to discontinuities in the channel as the film goes over the gate edge. To eliminate this issue, they developed a dry etch process resulting in the rounding of the gate edges, thus reducing the step height. For device fabrication they started with a glass substrate with an oxide buffer layer and gate metal. Then gate was then defined and etched by the dry etch process resulting in a taper below 40°. Then the gate oxide and a 50 nm a-Si layer were PECVD deposited and subsequently dehydrogenated. A 95% overlap (20 shots) was used to crystallize the Si with multiple different energies used. They then used phosphorus implants to form the source and drain. Additionally, a

lightly doped drain region was formed. SiO_2 and SiN_x layers were deposited for the interlayer dielectric. The dopants were then activated, and the devices were then hydrogenated. Last the source and drain electrodes were formed.

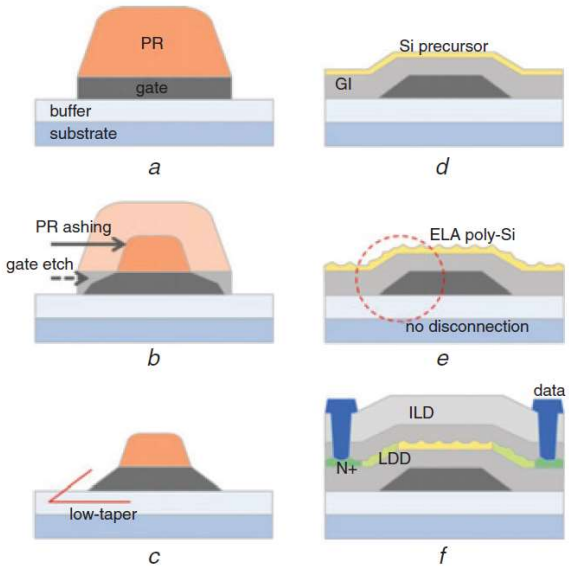

Figure 3.13 Illustration of ELA crystallized TFT at various stages a-c) gate dry etch to introduce a gate taper d) TFT stack before crystallization e) after crystallization f) completed device [42]

A transfer characteristic curve and family of curves for top-gate and bottom-gate device is shown in figure 3.14. In the log scale transfer characteristics there is negligible difference between the two gate configurations. However, for the family of curves the bottom gate configuration outperforms in drive current and greatly suppresses short channel effects. The bottom gate is able to do this due to the addition of a gate overlapped lightly doped drain (GOLDD) reducing the impact ionization at the drain end of the device, as discussed in section 3.1.

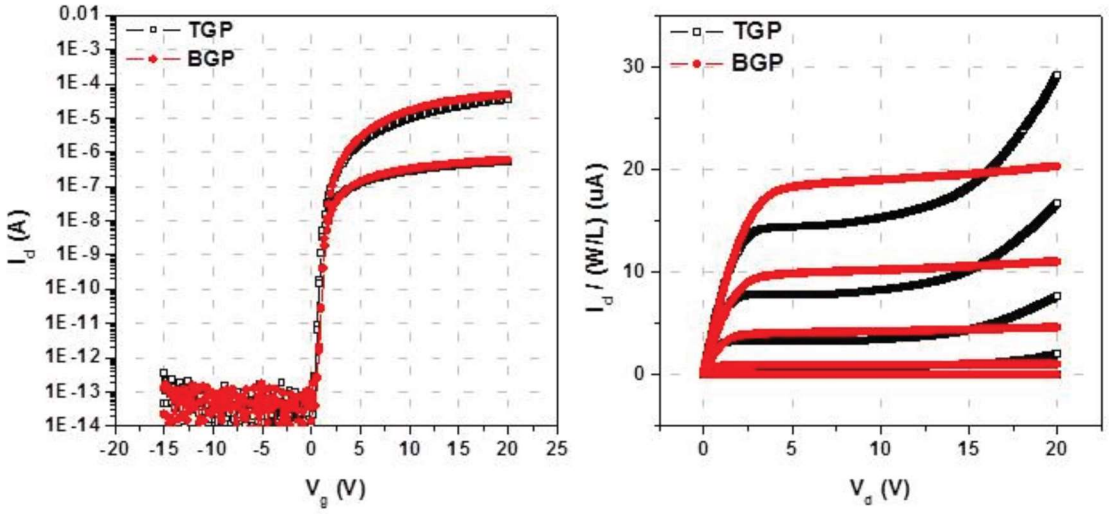

Figure 3.14 Comparison of transfer characteristics and family of curves for top gate and bottom gate ELA crystallized TFTs; L = 20 µm W = 4 µm [26]

The breakdown voltage for the top gate of 4.25-5.3 MV/cm and 7.0-8.7 MV/cm for the bottom gate. The higher breakdown voltage is partially due to the improvement in interface quality, but the major contributor is the protrusions into the gate oxide for the top gate devices. Extracted average parameters for thirty devices of dimensions W = 4 µm L = 3 µm and a 3 µm LDD were given. The average mobility was 77.8 $cm^2/(Vs)$, the average subthreshold slope was 160 mV/dec, the average threshold voltage was 0.81 V with a standard deviation of 0.30 V, and the average off state current was 0.03 pA/µm. The variation in the threshold voltage is quite significant for the magnitude of the voltage. This could limit some of the applications of the end device.

3.2.3 Continuous Wave Laser

The research group of Akito Hara from Fujitsu Laboratories [43,44] fabricated double gate continuous wave laser crystallized (CLC) devices. In the initial work [43,44], they started with a metal gate on a thick SiO_2 buffer layer. Then PECVD deposited the gate oxide and a 100 nm thick

a-Si film. Subsequently the film was dehydrogenated and formed into ribbons. The crystallization was performed using the second harmonic of a Nd:YVO_4 laser (λ = 532 nm). Following crystallization, the silicon was etched into islands and a window was etched for the bottom gate contact. They then deposited the top electrode and used backside illumination to pattern the gate. Then they etched the gate, ion implanted the source and drain, and activated the dopant. Lastly the interlayer dielectric was deposited, and source/drain metallization was performed. A cross-sectional SEM micrograph and an insert of top down optical micrograph of completed device is shown in figure 3.15.

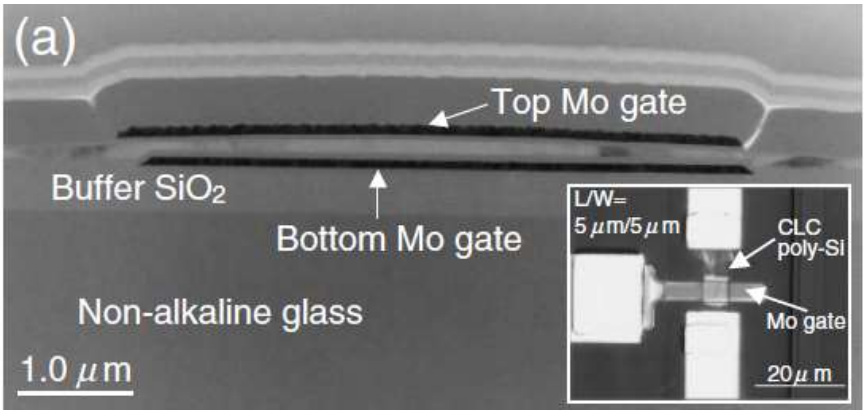

Figure 3.15 Cross sectional SEM micrograph of completed device with insert of top down optical micrograph [44]

In addition to the CLC double gate device they fabricated a CLC top gate and an ELA crystallized top gate. A comparison of the transfer characteristics for the three devices is shown in figure 3.16. The double gate device had a subthreshold slope of 89 mV/dec and a nominal field effect mobility of 950 $cm^2/(Vs)$. The mobility was calculated as if it was a single gate device with similar properties, so the actual mobility of the carriers is less than half. The double gate device also has approximately double the drive current of the top gate device, again this is expected because it has effectively double the channel width.

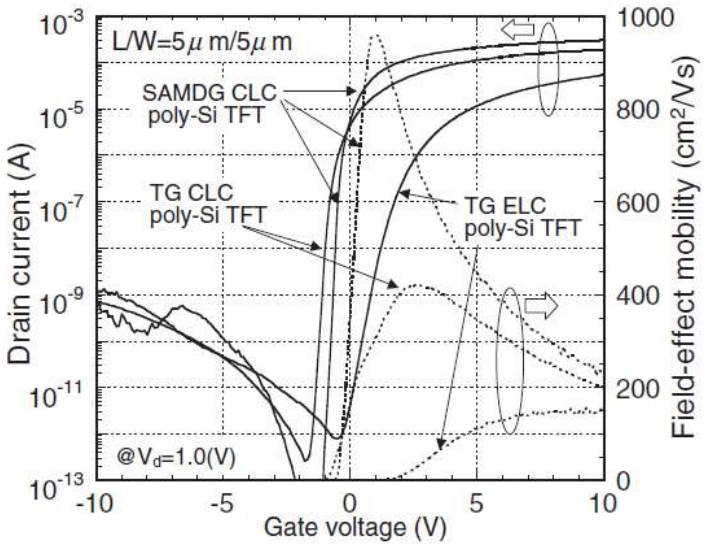

Figure 3.16 Transfer characteristics comparison for top gate ELA, top gate CLC, and double gate CLC device [44]

Later work from group of Akito Hara, now at Tohoku Gakuin University, fabricated both n-channel and p-channel devices [46]. The fabrication of the devices was similar to the previous work except the silicon layer was thinner, 90 nm. The transfer characteristics for both the device as well as top gate only devices is shown in figure 3.17. The double gate n-channel device had a subthreshold slope of 130 mV/dec and a nominal field effect mobility of 638 $cm^2/(Vs)$. The double gate p-channel device had a subthreshold slope of 120 mV/dec and a nominal field effect mobility of 156 $cm^2/(Vs)$. As with the previous work the double gate has a roughly double the effective mobility of the single gate.

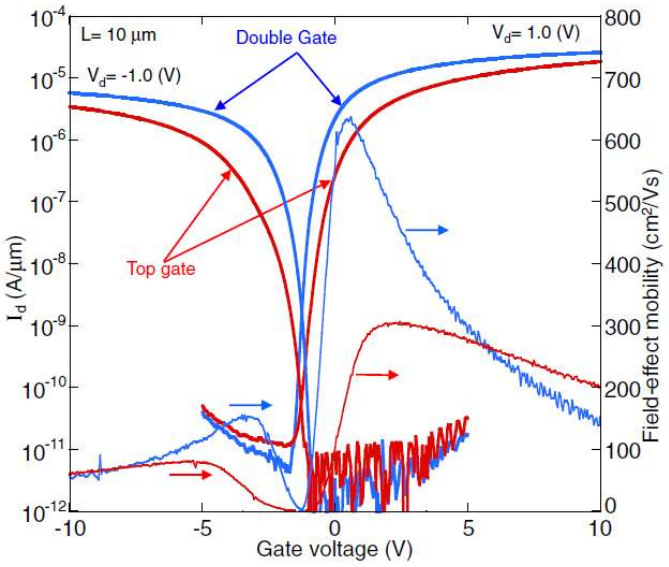

Figure 3.17 Transfer characteristics comparison for top gate and double gate CLC devices [45]

3.3 COMPARISON OF METHODS

The MICC papers show devices that exhibit good on and off states, but the subthreshold slope is quite shallow. For the SLG ELA devices exhibit high mobility and acceptable subthreshold. One major issue with the method is the strong impact of device length on device mobility. The random nucleation on larger devices limits the maximum channel length. Additionally, since all of the work was done on oxidized silicon wafers there could be compatibility issues that remain when transitioning to display glass. The ELA work from LG shows excellent results, but the process is most likely more complicated than their publication describes. For CW laser the results are very promising and are worthy of further investigation.

Chapter 4. BOTTOM GATE STRUCTURE AND FLA PROCESS INTEGRATION

The ability to fabricate bottom gate LTPS TFTs offers many attractive benefits for next generation displays. The introduction of the bottom gate causes new challenges due to its influence on optical and thermal properties. While LTPS made via ELA offers excellent device performance, the associated cost makes it prohibitively expensive to scale to larger substrates. FLA offers an attractive replacement for LTPS on large substrates due to easier scalability and reduction in cost, with the potential for comparable device performance.

4.1 INITIAL FLA BOTTOM GATE ATTEMPTS

The initial attempt for bottom-gate FLA devices at RIT used a molybdenum bottom gate. Molybdenum was chosen since it is a common gate material for TFTs, and is a refractory metal allowing for high temperature processing without melting. An optical image of a mesa after FLA crystallization is shown in figure 4.1. The portion of the mesa that is over the gate crystallized as if it was exposed to a higher energy than the portions that were not over the gate. This increased effective energy is due to two factors: the reflection and absorption of the light that passed through the mesa and the absorption of the gate causing it to heat and funnel heat under the mesa, causing the region to have reduced heat loss.

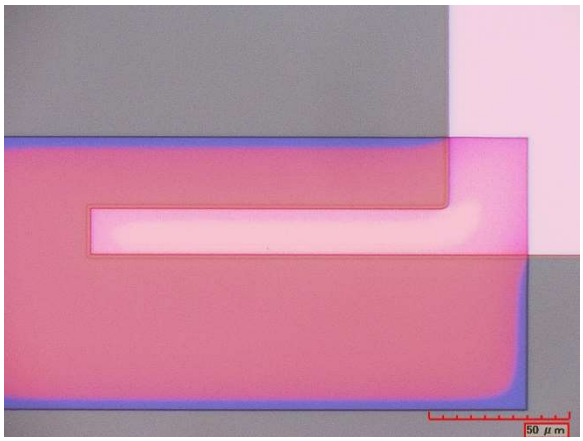

Figure 4.1 Optical image of a molybdenum bottom gate structure after FLA crystallization

In addition to the channel being crystallized during the flash the dopant was also activated. The electrical characteristics for the best device are shown in figure 4.2. The device exhibits good transfer characteristics with a good off state for the low drain bias. Due to the low yield of the process the effective channel length was not able to be extracted.

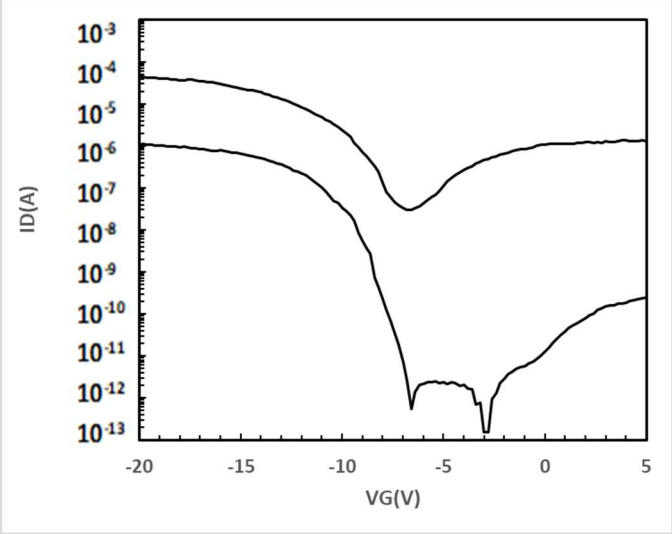

Figure 4.2 Transfer characteristics for a L = 12 µm W = 24 µm device

Due to the inclusion of the molybdenum bottom gate the required energy for crystallization of the channel is greatly reduced. Indium tin oxide (ITO) is a transparent conductive oxide that is already commonly used in display manufacturing. By using a transparent material for the gate, differences between sections over and outside the channel region should be reduced, resulting in a more uniform crystallization.

4.2 ITO PROPERTIES

ITO is a transparent conductive oxide with electrical and optical properties that depend on multiple factors including deposition and annealing conditions. A transmission, reflection, and absorption plot for a generic ITO film is shown in figure 4.3. For the visible wavelengths the transmission of the film is high. For short wavelengths the transmission of the film drops off rapidly as the absorption becomes significant.

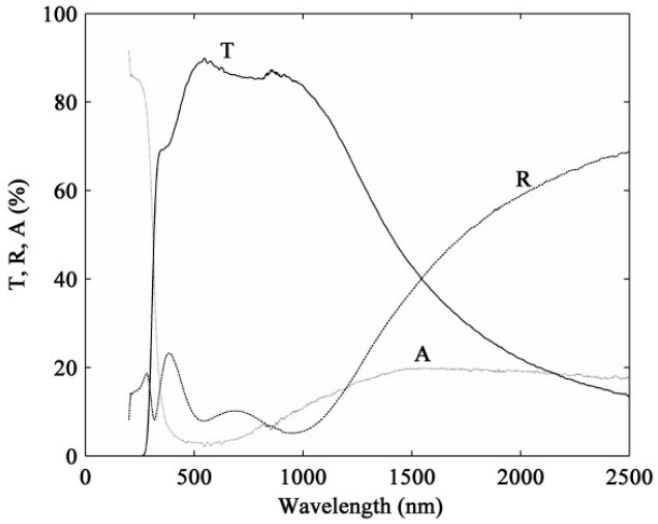

Figure 4.3 Generic transmission, absorption, and reflection plot for an ITO film [46]

A comparison between the transmission of bare Lotus NXT glass, an as deposited ITO film, and a post anneal ITO film is shown in figure 4.4. Annealing the film results in higher transmission for all wavelengths. For the ITO used in the experiment the transmission was over 75% for the visible range and the transmission drops off below 375 nm. The post anneal sheet resistance of 125 Ω/sq with standard deviation of 50 Ω/sq, measured using the four-point probe method.

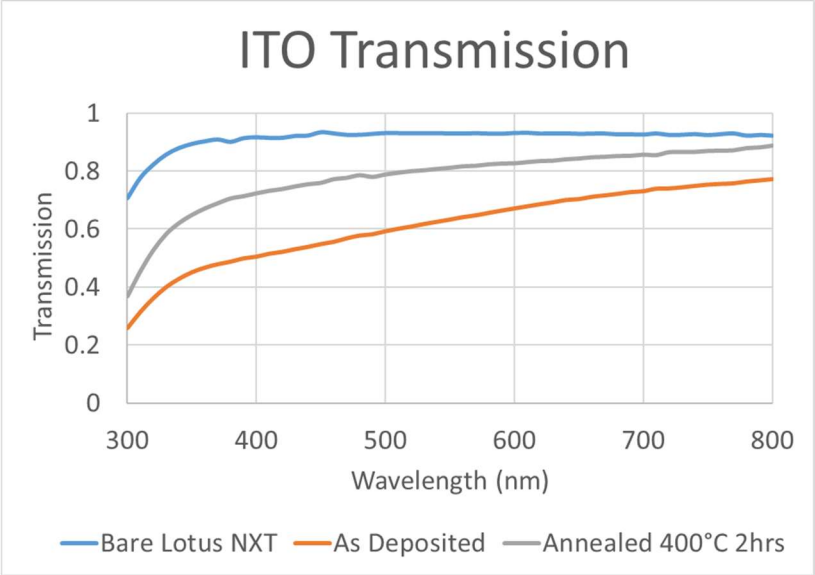

Figure 4.4 Experimental transition plots for Lotus glass, unannealed, and annealed ITO film

4.3 DEVICE FABRICATION

A 50 nm indium tin oxide (ITO) film was pulse DC sputtered on 150 mm diameter Corning Lotus NXT glass with no barrier layer. The ITO was then patterned and etched with dilute hydrochloric acid. Next the wafers were annealed at 400 °C for two hours in room air ambient. The annealing step is required to increase the transparency and decrease the resistivity of the ITO film. Additionally, the anneal increases the etch resistivity of the ITO layer in both concentrated hydrochloric and buffered oxide etch. The gate dielectric of 100 nm TEOS PECVD deposited oxide was then formed. A 60 nm thick hydrogenated amorphous silicon film was PECVD

deposited from a silane precursor. The film was then dehydrogenated at 450 °C for 2 hours in a nitrogen ambient and then patterned into mesas for crystallization. Next an additional 100 nm thick PECVD oxide film from a TEOS precursor was deposited to act as a capping/thermal barrier/antireflective layer for the silicon. The mesas were then crystallized via FLA. The crystallization was done on an open hotplate preheated to 400 °C with the flash pulse length of 250 µs. Four different pulse energies were used, 4.2, 4.3, 4.4, and 4.5 J/cm^2, measured by a blackbody bolometer.

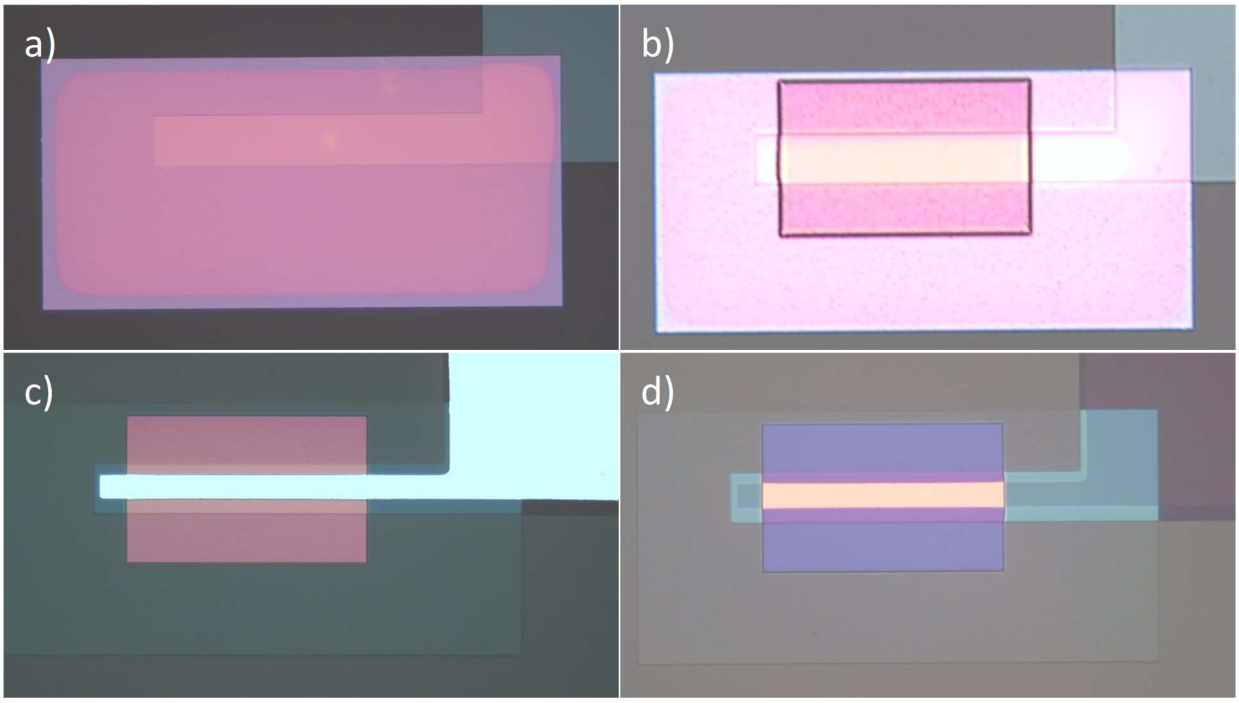

Figure 4.5 a) Super mesa post crystallization b) final mesa patterned before etching c) device with implant hard mask pre implant d) post implant before activation anneal

After a piranha clean, the capping oxide was removed, and the final mesa was defined and etched. The purpose of the final mesa is to remove the edges of the crystallization super-mesa, which is less crystallized due to proximity effects, defining the final channel width. After the final

mesa etch, a 100 nm TEOS PECVD deposited oxide is used as the capping/screen oxide. Aluminum was deposited to be used as an ion implant hard mask, allowing for a higher beam current. After the hard mask was patterned and etched the wafers were implanted with $^{11}B^{+}$ at an energy of 35 keV and a dose of 4×10^{15} cm^{-2}. After the hard mask was removed the dopant was activated using a furnace anneal at 630 °C for 12 hours in a nitrogen ambient. The source, drain, and gate contact cuts were etched with 10:1 BOE, and 500 nm of aluminum was deposited as the source and drain metal. Lastly the wafers were sintered in forming gas (5% H_2 in N_2) using a two-step process, 450 °C for 30 minutes than 300 °C for 30 minutes, to allow for both good contact formation and hydrogenation of dangling bonds within the polysilicon.

4.4 FABRICATION RESULTS

The amorphous silicon crystallizes differently over the ITO gate compared to regions over just glass; the former region behaves as if it was exposed to a higher energy pulse than the latter region, despite both receiving the same delivered FLA intensity. An example of this is shown in figure 4.6. This effect causes the silicon to begin forming voids as it dewets from the underlying oxide. The most likely cause is the uncovered portion of the gate absorbing the UV wavelengths and heating, with reduced thermal loss towards the center of the mesa.

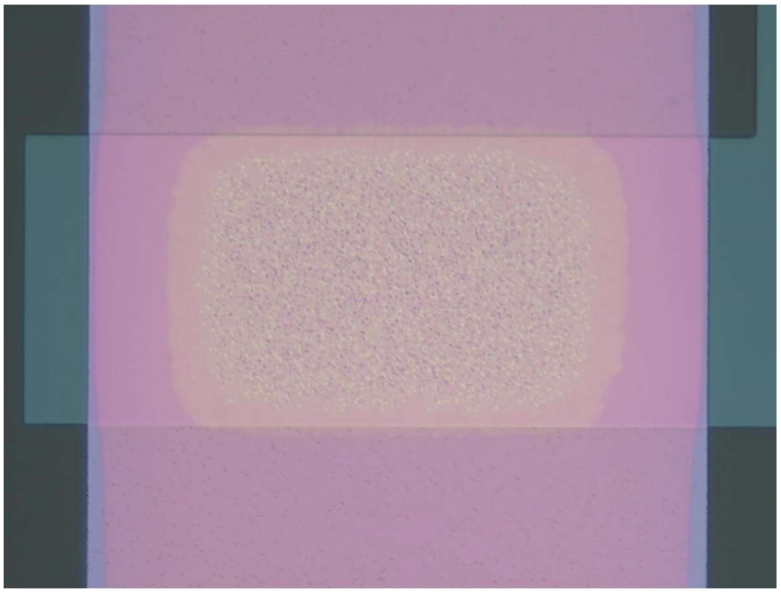

Figure 4.6 Optical image of a FLA crystalized mesa with bottom gate showing proximity effects

In the completed TFT there is an optical difference between the implanted source/drain and the channel, shown in figure 4.7. This is due to crystalline damage in of the source/drain regions due the high-dose boron implant and subsequent recrystallization during the activation anneal. The channel region remains unmodified, protected by the hard mask.

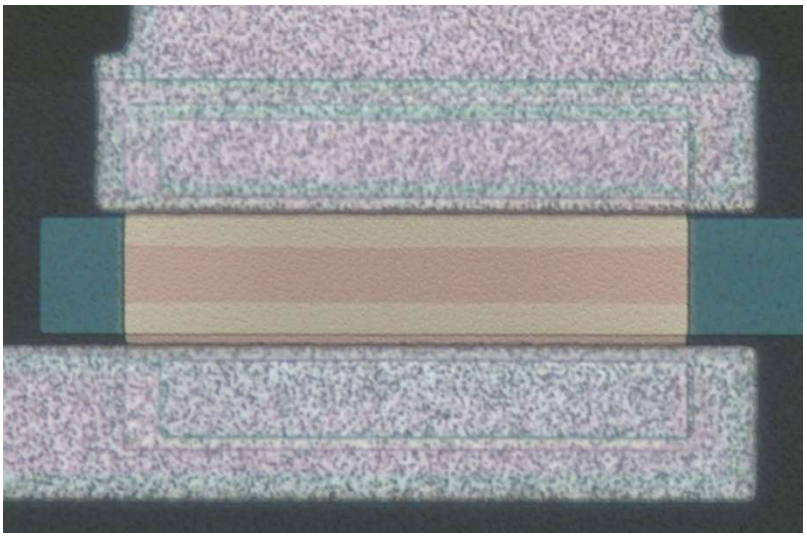

Figure 4.7 Optical image of an ITO bottom-gate FLA PMOS TFT before sinter

4.5 ELECTRICAL RESULTS

The best device transfer characteristics were obtained from a length 4 µm width 8 µm device crystallized with a nominal exposure energy of 4.4 J/cm^2 with a pulse duration of 250 µs. The transfer characteristics of this device on log and linear scale is shown in figure 4.8. The device exhibited a field effect mobility of 190 cm^2/(Vs), a subthreshold swing of 325 mV/dec, on/off ratio of more than seven orders of magnitude, and a threshold voltage of -5.4 V. In the linear characteristics, once the gate voltage increased past -10 V the drain current exhibited erratic behavior that may have been related to the bias sweep rate used during the test.

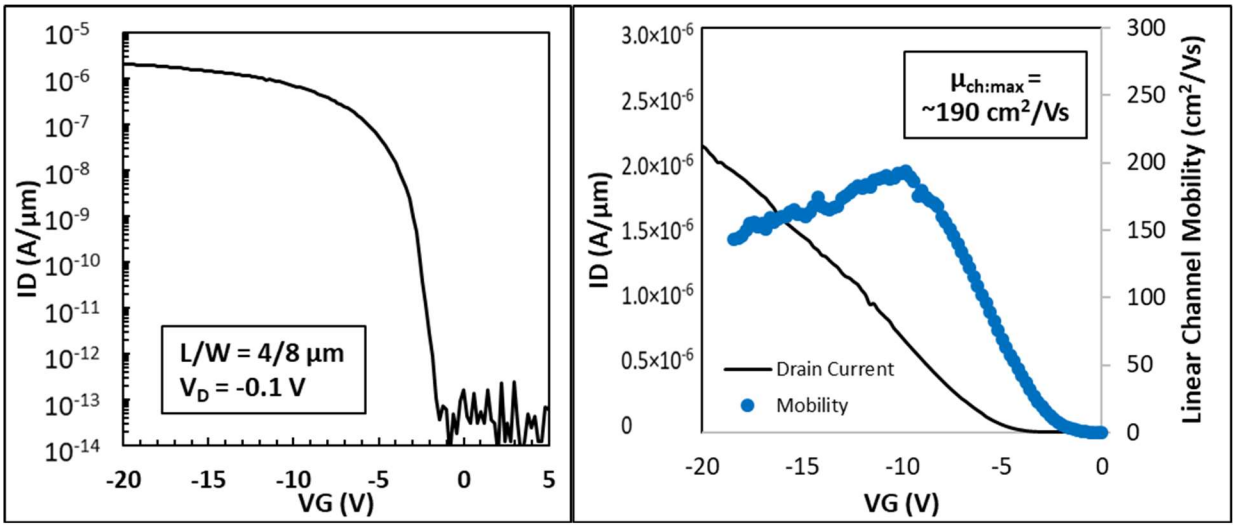

Figure 4.8 Linear and log-scale transfer characteristics of a bottom-gate PMOS TFT with L = 4 µm and W = 8 µm, crystallized via FLA intensity of 4.4 J/cm^2 over a 250 µs pulse.

Unfortunately, this device was not able to survive a high drain bias of -10 V and became an open circuit when the gate voltage was around -10 V, shown in figure 4.9. Additionally, under the high drain bias there is a significant shift in the off-state region indicating trap states. Multiple devices in the same region exhibited this behavior.

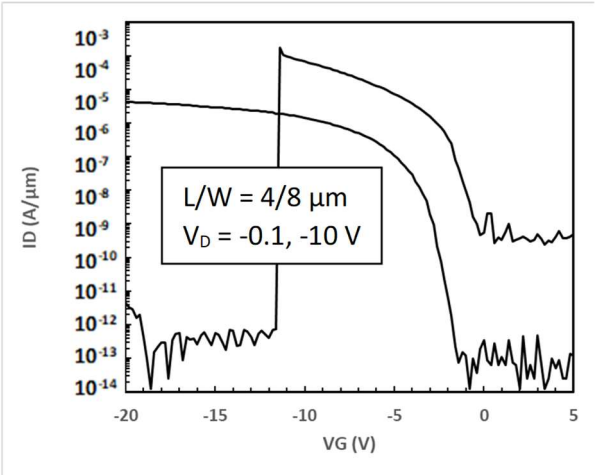

Figure 4.9 Transfer characteristics for L = 4 µm W = 8 µm showing device failing at VDS = -10 V

The most likely cause of the devices failing and becoming open circuits is a failure of the gate dielectric. During the source/drain implant a large portion of the dose goes through the channel and enters the gate dielectric underneath. This portion of the dose causes displacements and compromises the integrity of the gate oxide. Due to the devices being non-self-aligned there is a large overlap between the drain and the gate to accommodate for potential device misalignment. The compromised gate oxide fails when the high drain bias is applied across it. A SRIM simulation was performed to confirm that a large portion of the dose is entering the gate dielectric, the results are shown in figure 4.10.

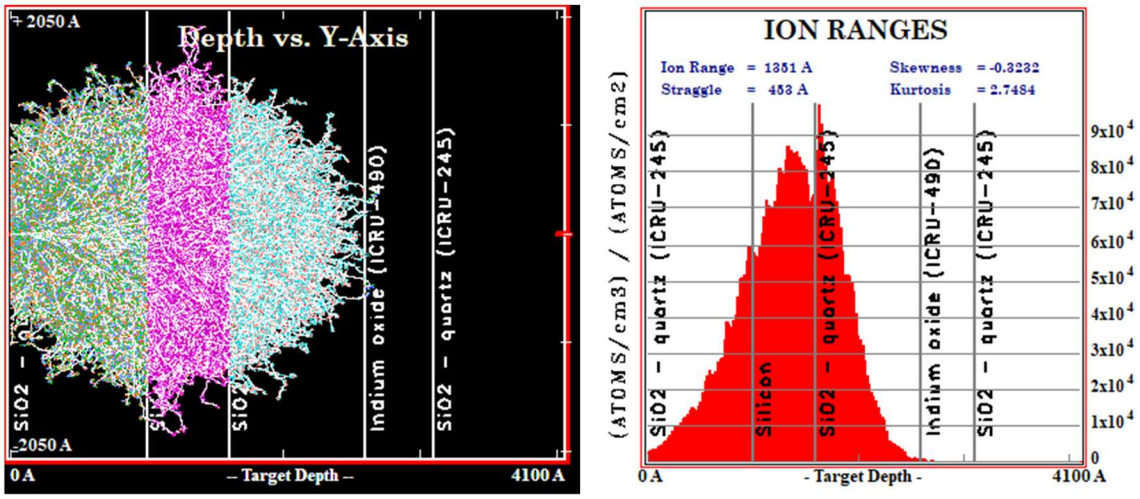

Figure 4.10 Left: SRIM collision plot showing locations of damage caused by source/drain implant Right: Concentration of B_{11}^{+} from the implant

The failure was more common in better performing devices, but some devices survived the higher bias and had good transfer characteristics. Figure 4.11 shows a L = 8 µm and W = 16 µm device that survived a high drain bias of -10 V. Like the devices that had failed, there was significant off state leakage for the high drain bias.

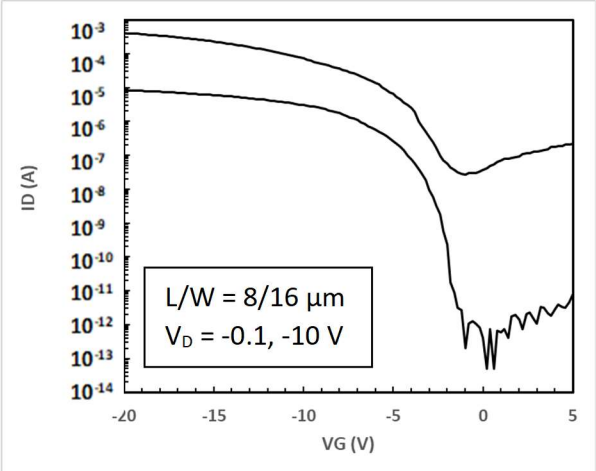

Figure 4.11 Transfer characteristic for L = 8 µm W = 16 µm device that survived drain bias of -10 V without dielectric failure.

The mobility values for both the linear and saturation modes of operation were calculated and are shown in figure 4.12. The maximum mobility in the linear mode was ~85 $cm^2/(Vs)$ and ~55 $cm^2/(Vs)$ for the saturation mode. While lower than the best device, both values are very good for p-channel LTPS TFTs.

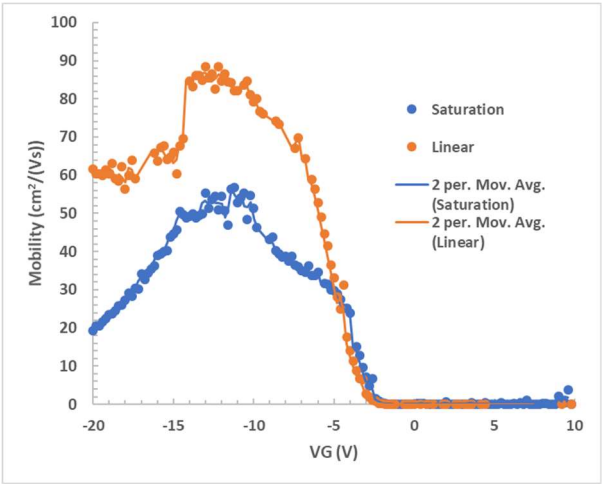

Figure 4.12 Channel mobility calculated using the transconductance method in the linear and saturation mode for L = 8 µm W = 16 µm device at V_{DS} = -0.1 V and -10 V, respectively

When the maximum gate voltage applied was reduced from -20 V to -10 V and the high drain bias was reduced from -10 V to -5 V no additional devices failed under high drain bias. The transfer characteristics for another L = 8 µm and W = 16 µm device from the same die is shown in figure 4.13. The device exhibits less off state leakage and has less separation between the low and high drain biases. Additionally, the subthreshold between the two bias states are parallel. These results show that by reducing the maximum drain bias the degradation of the device is minimized if not entirely avoided.

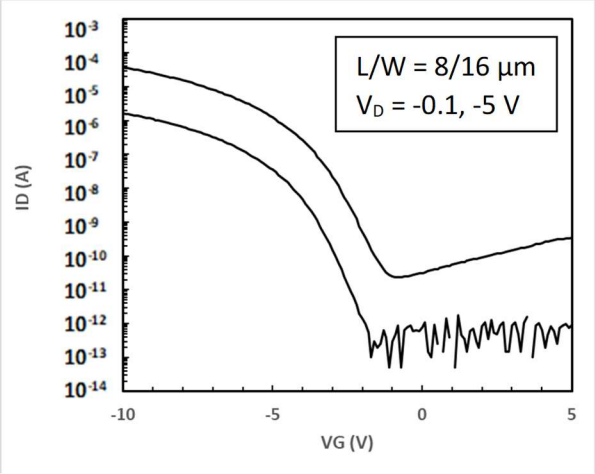

Figure 4.13 Transfer characteristic for different L = 8 µm W = 16 µm device from the same die.

Device performance across the wafer varied greatly due to nonuniformity of the flash lamp exposure. Additionally, device location within the test die influenced the device performance with devices towards the center of the die working better than those closer to the streets. Such observations are being used to obtain an understanding of exposure proximity effects and develop a qualitative model. An example of the variability caused by the nonuniformity and proximity effects is shown in figure 4.14. The device crystallized at 4.4 J/cm^2 was in the same die as the best measure devices but the characteristics were that of the lower energy exposure due to its

location near the street. Additionally, the 4.5 J/cm^2 device located near the street exhibited performance similar to the best 4.4 J/cm^2 while other 4.5 J/cm^2 devices had performance issues related to the high crystallization energy.

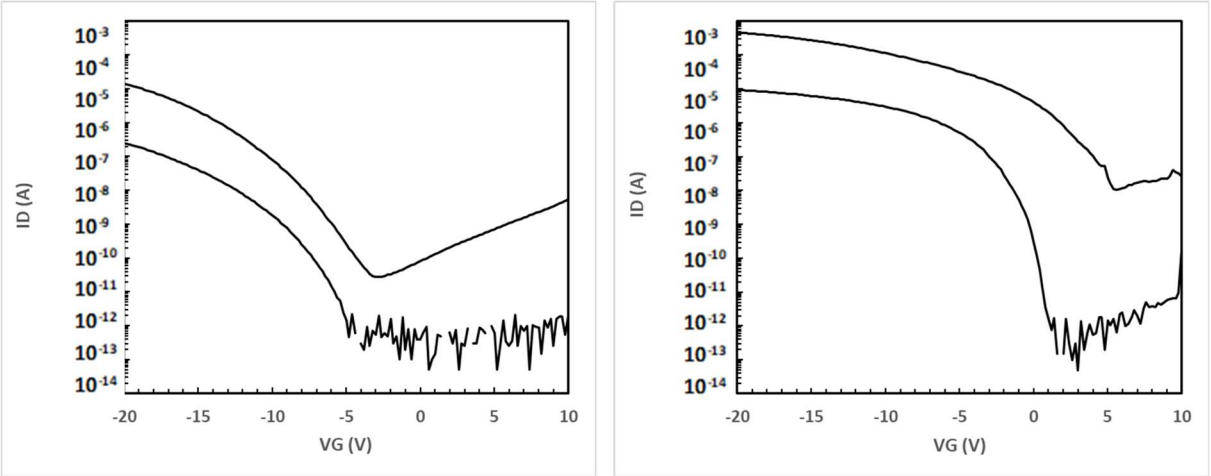

Figure 4.14 Transfer characteristics for L =12 µm W =24 µm with crystallization energies 4.4 J/cm^2 (left) and 4.5 J/cm^2 (right)

4.6 SUMMARY

A high conductivity high transparence ITO film was characterized and successfully incorporated into a FLA crystallized bottom gate TFT. The FLA exposure of 4.4 J/cm^2 for 250 µs produced the best results with high mobility, steep subthreshold, and a large on/off state difference. Under low bias the devices showed low influence of defect states, but under high drain bias the device exhibited increased leakage and failed under high gate bias. The failure mechanism is proposed to be damage to the gate dielectric as a result of dopant entering the dielectric during the source/drain implant. Reducing the high drain bias and reducing the maximum gate voltage applied

to the gate reduced the occurrence of the failure mechanism. High variability between devices was noted due to experimental equipment and processing capabilities.

Chapter 5. CONCLUSION

This thesis has presented an investigation on bottom-gate TFTs fabricated using FLA crystallization, with ITO implemented as the gate electrode material. The ITO deposition and anneal process was characterized focusing on the optical and electrical properties of the film, achieving high transparency with sheet resistance Rs ~ 125 Ω/sq. Devices that were crystallized using an FLA exposure of 4.4 J/cm^2 over 250 µs pulse duration achieved superior electrical characteristics. The best-case results were demonstrated on a TFT with L = 4 µm W = 8 µm channel dimensions, exhibiting a hole channel mobility of 190 cm^2/(Vs), a subthreshold swing of 325 mV/dec, on/off state ratio of seven orders of magnitude, and a threshold voltage of -5.4 V. For many devices, a transfer characteristic sweep at high drain voltage (-10 V) resulted in open circuit behavior due to dielectric failure. This behavior is most likely due to gate oxide damage from boron ions during the source/drain implant; the implant profile results in a large portion of the dose entering the oxide causing displacements. A reduction in the applied gate and drain voltage conditions avoided device failures.

A key finding was the observed crystallization dependence on the gate electrode region outside of the mesa polygon. This effect may be utilized to engineer transduction structures specifically to supply and manage energy transfer to the channel region.

High variability was observer across all treatment conditions due to nonuniformity in the exposure window, proximity effects within a die, and device dimensional dependence. These factors made it difficult to determine the optimum exposure conditions and required extensive device sampling. While these factors complicated initial interpretation, none are insurmountable

limitations and can be compensated for through equipment design and device design rules. The preliminary results are very encouraging and warrant further study.

5.1 FUTURE WORK

One area of further investigation is the improvement of the gate oxide integrity by reducing the source/drain implant energy. This would reduce the dose that is making it through the channel and damaging the gate oxide. The implant step could also be replaced by a plasma immersion or monolayer doping process which should have a similar effect. These techniques of dopant introduction could also offer improvements in device operation considering that they may suppress defects in the transition between the source/drain and channel regions.

Defect passivation techniques represent an additional area of interest. The addition of a NH_3 plasma process could add additional benefits to device performance. Similarly, sintering before the patterning of the source/drain metal would allow for an alternative site for monatomic hydrogen liberation, allowing for more complete hydrogenation. Subsequent patterning and etching would result in no impact on device electrostatics. Additionally, a top gate structure could be added to the device making it become a double gate device. This would improve channel electrostatics and help mitigate some of the non-ideal behavior due to interface traps.

REFERENCES

[1] J. Zhang, This is the Glass Age How glass is shaping the future of the display industry. [Online]. Available: https://www.corning.com/media/worldwide/global/documents/Zhang_SID_Presentation.pdf. [Accessed: 07-Mar-2020].

[2] S. Dash, "Display Technology – Top Trends for 2020," DisplayDaily, 16-Dec-2019. [Online]. Available: https://www.displaydaily.com/article/display-daily/display-technology-top-trends-for-2020. [Accessed: 08-Mar-2020].

[3] "History of LCD Displays." [Online]. Available: https://www.emdgroup.com/en/expertise/displays/solutions/liquid-crystals/history-of-lcd-displays.html. [Accessed: 07-Mar-2020].

[4] D. Dunmur and H. G. Walton, "Liquid crystal display," Encyclopædia Britannica, 03-Aug-2015. [Online]. Available: https://www.britannica.com/technology/liquid-crystal-display. [Accessed: 18-Apr-2020].

[5] C. Freudenrich, "How OLEDs Work," HowStuffWorks, 24-Mar-2005. [Online]. Available: https://electronics.howstuffworks.com/oled3.htm. [Accessed: 19-Apr-2020].

[6] W. den Boer, Active matrix liquid crystal displays: Amsterdam: Elsevier, 2005.

[7] T. Scheffer and J. Nehring, "Supertwisted Nematic (Stn) Liquid Crystal Displays," Annual Review of Materials Science, vol. 27, no. 1, pp. 555–583, 1997.

[8] S. Jafarabadiashtiani, "Pixel Circuits and Driving Schemes for Active-Matrix Organic Light-Emitting Diode Displays", University of Waterloo, 2007.

[9] J. Chen, Handbook of visual display technology. Cham: Springer International Publishing, 2016.

[10] R. Delmdahl, “Case Study: Excimer Laser Annealing for Brilliant AMOLED Displays.” [Online]. Available: https://www.coherent.com/assets/pdf/Case_Study_Excimer_ELA_2018_English.pdf. [Accessed: 27-Mar-2020].

[11] K. Myny, J. Genoe, and W. Dehaene, “Organic and Metal-Oxide Thin-Film Transistors,” Robust Design of Digital Circuits on Foil, pp. 9–32, Sep. 2016.

[12] A. K. Varshneya, “Properties of glass,” Encyclopædia Britannica, 10-May-2016. [Online]. Available: https://www.britannica.com/topic/glass-properties-composition-and-industrial-production-234890/Properties-of-glass#ref608326. [Accessed: 29-Apr-2020].

[13] Corning.com. [Online]. Available: https://www.corning.com/media/worldwide/cdt/documents/Lotus_NXT_Glass_PI%20-%20FINAL%20-Eng.pdf. [Accessed: 07-Aug-2020].

[14] Josef C. Lapp, “Glass substrates for AMLCD applications: properties and implications,” presented at the Proc.SPIE, Apr. 1997, vol. 3014, doi: 10.1117/12.270278.

[15] A. Ellison and I. A. Cornejo, “Glass Substrates for Liquid Crystal Displays,” International Journal of Applied Glass Science, vol. 1, no. 1, pp. 87–103, 2010, doi: 10.1111/j.2041-1294.2010.00009.x.

[16] R. K. Brow, “Physical Properties of Glass.” [Online]. Available: https://www.lehigh.edu/imi/teched/GlassProp/Slides/GlassProp_Lecture5_Brow_Part1.pdf. [Accessed: 12-Apr-2020].

[17] J.-M. Lee *et al.*, “56.3: Performance Improvement of Compensation Circuit Using p-Type SPC TFT for AMOLED Driving,” SID Symposium Digest of Technical Papers, vol. 44, no. 1, pp. 779–782, Jun. 2013, doi: 10.1002/j.2168-0159.2013.tb06331.x.

[18] T. W. Little, K. Takahara, H. Koike, T. Nakazawa, I. Yudasaka, and H. Ohshima, “Low Temperature Poly-Si TFTs Using Solid Phase Crystallization of Very Thin Films and an Electron Cyclotron Resonance Chemical Vapor Deposition Gate Insulator,” Jpn. J. Appl. Phys., vol. 30, no. Part 1, No. 12B, pp. 3724–3728, Dec. 1991, doi: 10.1143/JJAP.30.3724.

[19] W. Knaepen, C. Detavernier, R. L. Van Meirhaeghe, J. Jordan Sweet, and C. Lavoie, “In-situ X-ray Diffraction study of Metal Induced Crystallization of amorphous silicon,” Thin Solid Films, vol. 516, no. 15, pp. 4946–4952, Jun. 2008, doi: 10.1016/j.tsf.2007.09.037.

[20] C. Hayzelden and J. L. Batstone, “Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films,” Journal of Applied Physics, vol. 73, no. 12, pp. 8279–8289, Jun. 1993, doi: 10.1063/1.353446.

[21] J. H. Choi, D. Y. Kim, B. K. Choo, W. S. Sohn, and J. Jang, “Metal Induced Lateral Crystallization of Amorphous Silicon Through a Silicon Nitride Cap Layer,” Electrochem. Solid-State Lett., vol. 6, no. 1, p. G16, Nov. 2002, doi: 10.1149/1.1527411.

[22] J. C. Kim, J. H. Choi, S. S. Kim, and J. Jang, “Stable polycrystalline silicon TFT with MICC,” IEEE Electron Device Letters, vol. 25, no. 4, pp. 182–184, Apr. 2004, doi: 10.1109/LED.2004.824844.

[23] J. L. Wang, C. C. Tsai, C. C. Hwang, and T. Y. Hsieh, “Bottom-Gate Thin-Film Transistors Fabricated by Excimer Laser Annealing,” AMR, vol. 811, pp. 177–180, Sep. 2013, doi: 10.4028/www.scientific.net/AMR.811.177.

[24] R. Delmdahl, “Case Study: Excimer Laser Annealing for Brilliant AMOLED Displays.” [Online]. Available: https://www.coherent.com/assets/pdf/Case_Study_Excimer_ELA_2018_English.pdf. [Accessed: 27-Mar-2020].

[25] S. D. Brotherton, Introduction to Thin Film Transistors. Heidelberg: Springer International Publishing, 2013.

[26] K. Oh, S.-Y. Yang, J.-I. Lee, K.-S. Park, I.-B. Kang, and M. Y. Sung, “Bottom-Gate ELA Poly-Si TFT for High-Resolution AMOLED Mobile Displays,” SID Symposium Digest of Technical Papers, vol. 47, no. 1, pp. 923–926, 2016, doi: 10.1002/sdtp.10860.

[27] G. Fortunato, L. Mariucci, R. Carluccio, A. Pecora, and V. Foglietti, “Excimer laser crystallization techniques for polysilicon TFTs,” Applied Surface Science, vol. 154–155, pp. 95–104, Feb. 2000, doi: 10.1016/S0169-4332(99)00475-4.

[28] R. Paetzel and R. Delmdahl, “Testing the Limits of Excimer Lasers: Annealing for Advanced Displays,” Photonics Media, 27-Jul-2016. [Online]. Available: https://www.photonics.com/Article.aspx?AID=60931. [Accessed: 31-Mar-2020].

[29] R. Delmdahl, “Sowing the Seeds for Smarter Screens,” Opli, 20-Jun-2014. [Online]. Available: https://www.opli.net/opli_magazine/eo/2014/sowing-the-seeds-for-smarter-screens-coherent-june/. [Accessed: 31-Mar-2020].

[30] Y.-H. Choi and H.-Y. Ryu, “Formation of a Polycrystalline Silicon Thin Film by Using Blue Laser Diode Annealing,” J. Korean Phys. Soc., vol. 72, no. 8, pp. 939–942, Apr. 2018, doi: 10.3938/jkps.72.939.

[31] M. Park, Z. Vangelatos, Y. Rho, H. K. Park, J. Jang, and C. P. Grigoropoulos, “Comprehensive analysis of blue diode laser-annealing of amorphous silicon films,” Thin Solid Films, vol. 696, p. 137779, Feb. 2020, doi: 10.1016/j.tsf.2019.137779.

[32] Y. H. Jung *et al.*, “Sequential lateral crystallization of amorphous silicon on glass by blue laser annealing for high mobility thin-film transistors,” Thin Solid Films, vol. 681, pp. 93–97, Jul. 2019, doi: 10.1016/j.tsf.2019.04.023.

[33] R. Illgen, S. Flachowsky, T. Herrmann, T. Feudel, D. Thron, B. Bayha, W. Klix, M. Horstmann, and R. Stenzel, “A comparative study of non-melt laser spike annealing and flash lamp annealing in terms of transistor performance and pattern effects on SOI-CMOSFETs for the 32 nm node and below,” 2009 10th International Conference on Ultimate Integration of Silicon, 2009.

[34] Prucnal, S., Rebohle, L. and Skorupa, W. (2017). Doping by flash lamp annealing. Materials Science in Semiconductor Processing, 62, pp.115-127.

[35] “VON ARDENNE Provides Flash Lamp Annealing for Cost-Sensitive Industries,” VON ARDENNE Website. [Online]. Available: https://www.vonardenne.biz/en/company/press-events/von-ardenne-provides-flash-lamp-annealing/. [Accessed: 31-Mar-2020].

[36] S. Saxena, D. C. Kim, J. H. Park, and J. Jang, “Polycrystalline Silicon Thin-Film Transistor Using Xe Flash-Lamp Annealing,” IEEE Electron Device Letters, vol. 31, no. 11, pp. 1242–1244, Nov. 2010, doi: 10.1109/LED.2010.2064282.

[37] T. Mudgal, K. Bhadrachalam, P. Bischoff, D. Cormier, R. G. Manley, and K. D. Hirschman, “Communication—CMOS Thin-Film Transistors via Xe Flash-Lamp Crystallization of Patterned Amorphous Si,” ECS J. Solid State Sci. Technol., vol. 6, no. 12, pp. Q179–Q181, Jan. 2017, doi: 10.1149/2.0021802jss.

[38] J. H. Oh *et al.*, “Inverse staggered poly-Si thin-film transistor with non-laser crystallization of amorphous silicon,” Solid-State Electronics, vol. 52, no. 3, pp. 482–486, Mar. 2008, doi: 10.1016/j.sse.2007.10.016.

[39] J. H. Cheon, J. H. Bae, and J. Jang, “Inverted Staggered Poly-Si Thin-Film Transistor With Planarized SOG Gate Insulator,” IEEE Electron Device Letters, vol. 29, no. 3, pp. 235–237, Mar. 2008, doi: 10.1109/LED.2008.915623.

[40] C.-C. Tsai *et al.*, “High-performance top and bottom double-gate low-temperature poly-silicon thin film transistors fabricated by excimer laser crystallization,” Solid-State Electronics, vol. 52, no. 3, pp. 365–371, Mar. 2008, doi: 10.1016/j.sse.2007.10.029.

[41] H. Hayashi *et al.*, “Fabrication of low-temperature bottom-gate poly-Si TFTs on large-area substrate by linear-beam excimer laser crystallization and ion doping method,” in Proceedings of International Electron Devices Meeting, Dec. 1995, pp. 829–832, doi: 10.1109/IEDM.1995.499345.

[42] K. Oh, S. Yang, J. Lee, K. Park, and M. Y. Sung, “Poly-Si TFTs with bottom-gate structure using excimer laser crystallisation for AMOLED displays,” Electronics Letters, vol. 51, no. 24, pp. 2030–2032, 2015, doi: 10.1049/el.2015.2422.

[43] A. Hara, M. Takei, K. Yoshino, F. Takeuchi, M. Chida, and N. Sasaki, “Self-aligned top and bottom metal double gate low temperature poly-Si TFT fabricated at 550/spl deg/C on non-alkali glass substrate by using DPSS CW laser lateral crystallization method,” in IEEE International Electron Devices Meeting 2003, Dec. 2003, p. 8.6.1-8.6.4, doi: 10.1109/IEDM.2003.1269246.

[44] A. Hara, M. Takei, K. Yoshino, F. Takeuchi, and N. Sasaki, “Self-Aligned Metal Double-Gate Low-Temperature Polycrystalline Silicon Thin-Film Transistors on Non-Alkali Glass Substrate Using Diode-Pumped Solid-State Continuous Wave Laser Lateral Crystallization,” Jpn. J. Appl. Phys., vol. 43, no. No. 6B, pp. L790–L793, Jun. 2004, doi: 10.1143/JJAP.43.L790.

[45] A. Hara, T. Sato, K. Kondo, K. Hirose, and K. Kitahara, “Self-Aligned Metal Double-Gate Low-Temperature Polycrystalline Silicon Thin-Film Transistors on Glass Substrate Using Back-Surface Exposure,” Jpn. J. Appl. Phys., vol. 50, no. 2R, p. 021401, Feb. 2011, doi: 10.1143/JJAP.50.021401.

[46] H. Askari, H. Fallah, M. Askari, and M. C. Mohmmadieyh, “Electrical and optical properties of ITO thin films prepared by DC magnetron sputtering for low-emitting coatings,” p. 8.