BIPOLAR DEVICE FABRICATION USING RIT'S CMOS TECHNOLOGY TO DEVELOP A BICMOS PROCESS

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ABSTRACT

An NPN bipolar transistor process was designed and fabricated for incorporation with RIT's N well CMOS technology to develop BiCMOS devices. The only additions to the CMOS process were the base masking step, base implant, and drive. Base dose was varied to achieve current gains of 50, 100, and 200 using SUPREM-3. Unfortunately, do to an incomplete etch of the collector region, a rework had to be performed, whose added temperature steps pushed the emitter through the base.

INTRODUCTION

BiCMOS combines the qualities of CMOS and Bipolar circuits on one chip. The CMOS device qualities are higher packing densities, virtually infinite input resistance with leakage currents in the picoamp range, precision capacitors, and near ideal switches, (i.e. either on or off and have virtually instantaneous switching.) The Bipolar circuit qualities, on the other hand, are their ability for higher frequency response, higher intrinsic gain, higher drive capability, and larger output swings. This combined technology will allow for design and fabrication of analog and digital devices on the same chip. This combined technology is used to achieve optimum performance that should out perform circuits fabricated in one or the other technology.

A BiCMOS technology requires a much more involved process to fabricate than either of the other two processes alone. Other potential drawbacks were a lower yield, and the extra time required for the additional step. Therefore in this project to simplify it as much as possible, an existing CMOS process was used as the baseline and the additional required steps needed for the fabrication of the bipolar circuits were added. The existing CMOS process is shown in Figure 1. One can see the N well used in the PMOS device region and the N+ source and drain sections in the NMOS devices. The two implants for these regions were used in bipolar NPN vertical transistor for the collector and emitter regions respectively as can be see in Figure 2.

The N-type well from the CMOS process was only five microns deep and for this reason the base implant and drive were two very critical steps. TMA SUPREM-3 was used to simulate every process

step in order to achieve desired gains from the NPN bipolar transistors. The predicted junction depths for the vertical NPN transistor are shown in Figure 3. This plot was obtained from TMA SUPREM-3 and shows the net active concentrations of dopant as a function of depth into the wafer. These additional process conditions simulated in SUPREM-3 for desired gains were used in the processing of the device wafers. Appendix A has SUPREM-3 plots for the different current gains predicted, Appendix B has the TMA SUPREM-3 input file used.

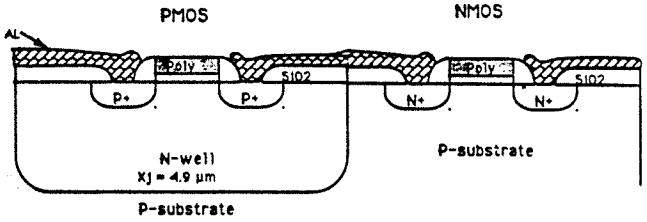

Figure 1: CMOS cross section.

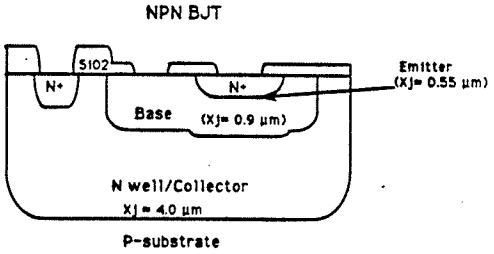

Figure 2: NPN cross section for BiCMOS.

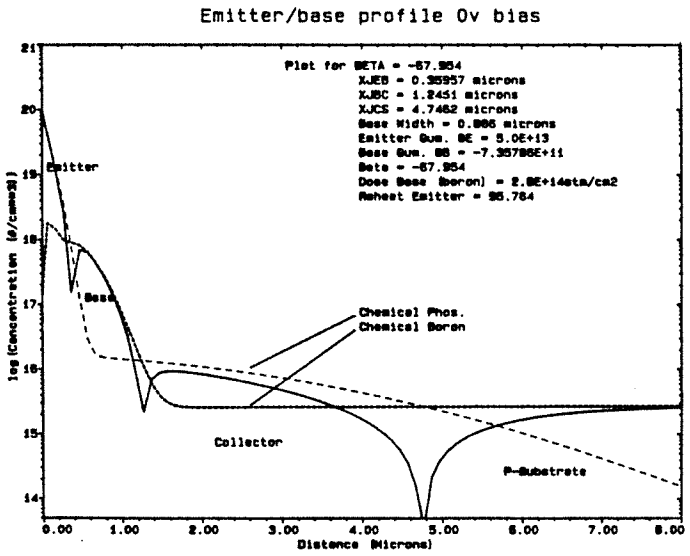

Figure 3: SUPREM-3 plot of net concentration vs. depth in wafer.

EXPERIMENT

Three inch <100> P-type wafers with a resistivity of 5 ohms-cm were used in the fabrication of bipolar devices. Four point probe measurements were taken on the wafers and 3226A of oxide grown on them for the first mask. The oxide was patterned for the well was patterned and implanted with a phosphorous dose of 6E12 atoms/cm2 at an energy of 130kev. A well drive was performed at 1150C for approximately 21 hours in nitrogen. The oxide was then all stripped off and a field oxide was grown at 950C in wet 02 for approximately six hours. This was followed by the base pattern, etch, and implant. To experiment with three different base doses predicted by TMA SUPREM-3. The doses were 9.6E13, 1.6E14 and 2.6E14 atoms/cm2 and the energy used was 40kev followed by a driven in at 1000C in wet 02 for 60 minutes. The emitter mask was used to etch through the oxide grown during the drive and the emitter region was implanted with a dose of 1E15 atoms/cm2. The open emitter regions were covered with Allied signal spin on glass and the cure of the spin on glass also served as the emitter drive in, which was 30 minutes in wet 02 at 900C. The contact cuts, metal deposition, and etch were the final steps in the process. Full details in processing can be found in Appendix C.

The masks used in processing were emulsion masks and were generated on a MANN photo repeater from a reticle that was generated on a MANN 3000 pattern generator. The MANN file for the pattern generator was generated from the CIF file created by ICE. (ICE is an in house VAX based CAD tool which stands for Integrated Circuit Editor.)

The devices that were designed were vertical NPN transistors of different sizes, Vertical PNP transistors of different sizes, lateral NPN and PNP transistors, Van der Pauw structures, Kelvin contact resistance structures etc. Appendix D contains plots of the designed cells.

All of the photolithography was performed using KTI 820 photo resists. It was patterned on Kasper Contact Aligners and developed on a GCA wafer track using a 934 spuddle develop. After exposure, the wafers were developed on a GCA wafer track using a spray/puddle develop system. Both the coat and develop programs were standard for KTI 820 positive photo resist.

RESULTS/DISCUSSION

Table 1 shows the final results of junction depth, sheet resistance and oxide thicknesses of the actual measured results and compares them to the results obtained by TMA SUPREM-3. As one can see not any of the values from TMA were right on to the actual measured values demonstrating that a lot of characterization of SUPREM-3 is needed. The base junction depths measured after drive in were really not that far off from SUPREM's value. The difference might only be due to the accuracy

of the travelling stage, which was used to make my measurements. The N well junction on the other hand was as much as 0.67 microns less than TMA's value. This demonstrated the inability to accurately produce some results with respect to RIT's clean room processes. The base sheet resistances were also not very comparable, even though they did turn out to be rather high for a P-type base region in an NPN vertical transistor. The base implant dose should be varied using higher doses than were used in future experiments in efforts to attempt to lower the sheet resistance.

After the Spin on glass cure, which doubled as the emitter drive in, a great number of changes from previous measured results, as well as discrepancies to simulated results were observed. One can see how the emitter junction depth was much less as predicted, compared to the actual measured results. A difference of 0.14 microns in the emitter junction brings about the issue of the reliability of the process or the tool, the traveling stage, used to measure the junction depth. The traveling stage was not a very accurate tool and the measurement was dependent on the individual using the tool and where they assumed the edge of the grove to be. The measurements of the base junction actually showed a decrease both in non emitter implanted regions and in emitter implanted regions, where emitter push drove the base deeper. Even after emitter push the junction was still shallower than prior to emitter implant. The junction could not have been consumed by the 15 minute, wet 02 growth at 900C prior to spin on glass coat. The only other possible explanation was that the wet 02 that was used during the cure could have penetrated through the spin on glass to grow more oxide on the surface thus consuming more silicon. This can be determined by performing an experiment with a nitrogen cure as compared to a wet 02 cure.

Implant Dose = 2.6E14 atm/cm2

SUPREM-3 RESULTS	ACTUAL RESULTS
Base Drive sup	Base Drive
Xjb = 1.18 um	Xjb = 1.04 um
Xjw = 4.79 um	Xjw = 4.12 um
RHOSB = 480 ohms/square	RHOSB = 360 ohms/square
Ox = 3409 A	Ox = 1680 A
Emitter Drive sup	Emitter Drive
Xje = 0.3596 um	Xje = 0.546 um
Xjbpush = 1.245 um	Xjbpush = 0.883 um
Xjb = 1.22 um	Xjb = 0.86 um
Xjw = 4.75 um	Xjw = 4.07 um
RHOSE = 95.8 ohms/square	RHOSE = 126 ohms/square
RHOSB = 527 ohms/square	RHOSB = 397 ohms/square
RHOSW = 1353 ohms/square	RHOSW = 1100 ohms/square
Ox/emit = 5192 A	Ox/emit = 3988 A
Ox/field = 1.396 um	Ox/field = 9500 A

TABLE 1: SUPREM-3 vs. Actual measured results.

The sheet resistance measured by four point probe from the emitter region were fairly close to that calculated by TMA, but the values for the base and N well regions were not as predicted. The values measured were less than those calculated. Again this has to be worked on to obtain predictable desired results. One thing that was noticed between both the measured and calculated before and after the emitter implant and drive, was that the sheet resistance of the base region increased. The only explanation that can be deduced at the time was that the concentration must have been depleted possibly from the growth of the oxide on the surface as was mentioned earlier. Appendix E has a more in depth table of results

Some electrical testing of Van der Pauw structures after processing of the rework revealed that the emitter sheet resistance ranged from 60 to about 140 ohms/square across a wafer. None the less, the average was around the range that was predicted by TMA and measure on the four point probe. The sheet resistance values of the well from the Van der Pauw structures were around 1.1 K ohms/square, which were also very comparable. Because of some biasing problems in testing the base Van der Pauw structures, accurate base sheet resistances were not able to be obtained.

Electrical testing right after processing indicated a flaw in the fabrication of the devices. The collector region had not been totally etched prior to implant and therefore working NPN transistors were not able to be obtained. In attempts to salvage the devices, a rework was performed which would reopen the collector regions, dope them and reconnect with metal.

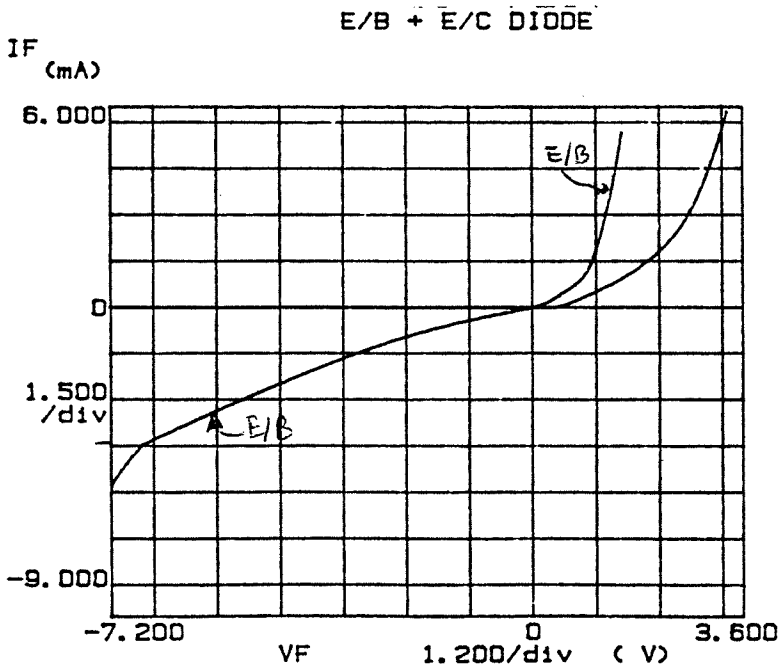

FIGURE 4: Plot of E/B and E/C diodes.

Unfortunately, these extended efforts were not enough to yield working devices. It was believed that the extra temperature steps added in attempts to salvage the devices pushed the emitter through the base. This verified that the base width was indeed small prior to the rework and that there was the likely hood that the junction measurements obtained earlier were fairly accurate. The punch through was observed electrically by the curves in Figure 4. As one can see, the emitter base diode curve had a respectable turn on voltage but had an enormous leakage current. The other curve was that of a bias across the emitter/collector contacts. This demonstrated the very low voltage that what was required to break down the emitter/collector regions. Both of these curves support the hypothesis of emitter punch through.

CONCLUSIONS

After the design and processing of this project it was observed that TMA SUPREM-3 definitely needs more characterization work performed on it. It was also observed that a number of steps have to be changed or modified to correct some of the results that were obtained. Such as using a nitride layer to eliminate the consumption of the N well during field oxide growth, increasing the base dose to decrease sheet resistance and further experimentation to correct the base junction depletion observed. Even though the devices were not functional, given the data obtained prior to rework, It was and will be possible in the future to obtain working NPN vertical bipolar junction transistors using this process or the process of the combination of the two technologies. The combination of the technologies would require minimal added steps and minimal extra time. Therefore it is a viable and cost efficient upgrade.

ACKNOWLEDGMENTS

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