POLYSILICON EMITTER BIPOLAR TRANSISTORS

Todd C. Sieger
Senior Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

Polysilicon emitter vertical NPN transistors were fabricated in an attempt to create devices with very high current gains and high forward Early voltages. TMA SUPREM-3 simulations were used to optimize the process to obtain emitter junction depths of 0.05 and 0.08um. Final emitter junction depths of 0.1um, or less, were measured. High current gains were not achieved, due to high base doping.

INTRODUCTION

Current gains of conventional emitter bipolar transistors are limited due to the effects of high emitter doping. In theory, higher gains may be obtained for conventional emitter transistors by using very small base widths and high emitter doping densities. However, increased emitter doping reduces the bandgap and increases the minority carrier recombination [1]. The result is reduced emitter injection efficiency and no real improvement in current gain [2]. Increasing emitter doping would also have the detrimental effects of reducing the emitter-base breakdown voltage (BVebo) and increasing the emitter-base junction capacitance [3]. Another problem associated with conventional emitters is with scaling. The minority-carrier diffusion length becomes larger than the emitter for emitter junction depths below 0.2 um, which, further reduces current gain [4]. The use of polysilicon as the emitter is one method for avoiding these problems.

Polysilicon emitters are formed by outdiffusion of dopant from polysilicon into the monocrystalline silicon base region. The polysilicon is either in direct contact with the monocrystalline substrate or separated from it by an interfacial oxide that is eight to fourteen Angstroms thick [5]. Current gains three to seven times higher than for conventional-emitter transistors have been reported [6]. High current gain may be traded for a lower gain and increased base doping without premature breakdown. This is particularly useful for digital circuits, because the narrower base widths which are obtained result in higher switching speeds [7].

Several models have been reported, that attempt to explain the increase in current gain over conventional-emitter transistors. Originally, it was believed that reduced bandgap narrowing due to lower emitter doping was the cause. This model failed to quantitatively account for the enhanced emitter injection efficiency [8]. Another early model was the reduced mobility, or two-layer, model [9]. This model attributes increased current gain to the increased emitter length due to the polysilicon film and a reduced minority-carrier mobility in the polysilicon, which, predicts a dependence of base saturation current on polysilicon film thickness. However, experimental results show that for polysilicon films less than or equal to 500 Angstroms the film thickness does not influence base saturation current [10]. Another related model is that of reduced carrier lifetime due to the large number of dangling bonds and recombination centers at the polysilicon grain boundaries [11].

The tunneling model [12] recognized the presence of an interfacial oxide between the polysilicon and monocrystalline silicon as a barrier to minority-carrier injection into the emitter. This model is consistent with the increased emitter resistance due to transport of majority carriers through the oxide barrier. Tunneling is believed to play a major role for oxide barriers greater than ten angstroms thick [13]. To explain the increased current gains of devices with oxide free (i.e. less than ten angstroms) interfaces, the interface dopant-segregation model was proposed [14]. This model treats the interface between the polysilicon and monocrystalline silicon as essentially a large grain boundary at which dopant atoms from the polysilicon segregate. The high dopant concentration at the interface is a potential energy barrier for holes when the emitter-base junction is forward biased.

The precise control of shallow emitter junction depth that is possible with polysilicon emitters, allows the transistors to be scaled vertically and laterally, while keeping the peripheral emitter-base junction capacitance at a reasonable value [15]. Scaling is also improved because of the possibility for self-alignment with polysilicon emitter transistors [16]. Single and double-polysilicon self-aligned transistors have been reported. With the single-polysilicon self-alignment approach, polysilicon is deposited over a lightly p-doped region and is the implanted with arsenic. The polysilicon is then patterned and oxidized. The oxidation forms a sidewall spacer. Boron is implanted everywhere, forming an extrinsic base where the emitter regions were not masking the implant. This type of process is suitable for integration into a BiCMOS process because of its similarity to LDD-CMOS processes [17]. Both vertical scaling and self-alignment result in increased packing density making polysilicon emitter devices practical for VLSI integrated circuits.

Two other advantages of polysilicon emitters owe to the fact that the polysilicon film protects the monocrystalline part of the emitter. The polysilicon is implanted, and the emitter is

formed by outdiffusion, which, results in the formation of the emitter-base junction in undamaged monocrystalline silicon [18]. Also, the polysilicon film reduces the incidence of aluminum spiking of the emitter-base junction because the emitter contact is to the polysilicon.

Polysilicon emitter transistors have previously been fabricated at RIT [19]. The process was defined with the aid of SUPREM-3. In the simulations, base and emitter implant and drive-in parameters were varied in an attempt to obtain an emitter junction depth of 0.0940 um, base junction depth of 0.4744 um, integrated emitter doping of 3.3E14 cm-2, and integrated base doping of 7.5E13 cm-2 [20]. The origin of these parameters is an example of a polysilicon emitter process from the back of the SUPREM-3 users manual. Processing was performed using the simulated implant and hot-processing parameters on wafers of lower substrate doping than that used for the simulations. In addition, the base implant dose was varied from the simulated value for several wafers. One of the wafers that was of lower doping and received a lower base implant dose, exhibited the highest gain of 359.

This project investigates the hypothesis that, by reducing the emitter drive-in time and/or temperature, higher gains should be achievable [21]. Emitter drive-in cycles were varied to achieve final emitter junction depths of 0.08 um and 0.05 um, respectively. The remainder of the process follows the previous schedule [19]. A cross-section of the device resulting from this process is represented in Figure 1.

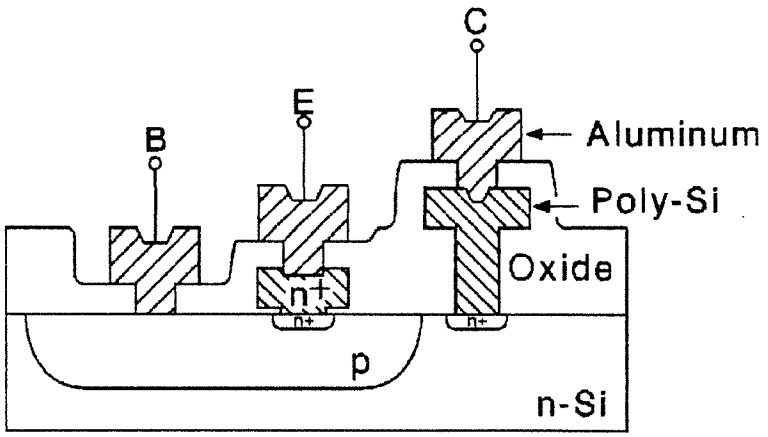

Figure 1: Polysilicon emitter transistor cross section.

EXPERIMENT

Simulations using TMA SUPREM-3 employed an optimization loop for the emitter drive-in time and temperature. Targets were defined as an oxide thickness of 2000A over poly-si, and emitter junction depths of 0.05 um and 0.08 um. The simulations resulted in emitter drive-in cycles of 875C for a total of 120 minutes, and 900C for a total of 95 minutes. The emitter drive-in of the existing process was 120 minutes at 900C.

Twelve n-type, <100>, phosphorous-doped, 5-15 ohm cm, wafers were four-point probed and then divided into two groups of six; one for devices and one for controls. The wafers were given a 10:1 HF dip, rinsed, and a field oxide of approximately 6000A was grown at 1100C using dry oxygen for ten minutes, wet oxygen for seventy-five minutes, and dry oxygen for ten minutes. Base patterning was performed using a GCA Wafertrac for coating, pre-bake, development, and post-bake. A Kasper mask aligner was used for exposure. After wet etching the oxide, all device wafers and several control wafers were implanted using a Varian model ion implanter. A dose of 1E14 ions/cm2 BF2 was implanted in each wafer at an energy of 35KeV. The resist used for masking the implant was then stripped with an oxygen plasma. All wafers were RCA cleaned. An 850C, forty minute long oxidation was performed to anneal and drive in the base implant.

Emitter regions were patterned, and the wafers received a full RCA clean. Polysilicon (0.4 um) was LPCVD deposited at 610C. All device wafers were then implanted with a phosphorous dose of 4E15 ions/cm2 at 50KeV. The polysilicon was patterned using a SF6:02 plasma in a Tegal 700 etcher. The resist was stripped with an oxygen plasma and the wafers were RCA cleaned. The wafers were split into two groups of three device wafers and one half of each control wafer. Each group was subjected to one of the two different emitter anneal/drive-in cycles described above. During these cycles, the polysilicon was partially oxidized. Processing on the wafers was completed by patterning contact cuts, RCA cleaning the wafers, depositing and patterning aluminum, and sintering the wafers in forming gas.

Working copies of the masks were made from reticles created for the previous attempt to fabricate polysilicon emitter transistors. The designed devices include: Van der Pauw structures and resistors for base, base pinch, collector, emitter, polysilicon, and metal layers; metal-to-base, metal-to-collector, and metal-to-poly Kelvin structures; and lateral PNP and vertical NPN transistors of various dimensions. Layouts are shown in the Appendix. The test structures and the control wafers were used to determine final junction depths, sheet resistances, and contact resistances for each of the two emitter drive-in cycles. Current gains were measured and Gummel plots were made on finished NPN devices. These plots of the logs of the base and collector currents versus emitter-base junction voltage aided characterization of emitter and base doping.

RESULTS/DISCUSSION

Control wafer measurements of emitter and base junction depths gave values of 0.1 um, or less, for the emitter-base junction and 0.53 and 0.61 um for the base-collector junction. The values for the base-collector junction compare very well to the values of 0.4609 and 0.4729 um, respectively, that were obtained from SUPREM3. More precise values of emitter-base junction depth could not be obtained due to accuracy limitations of the travelling stage micrometer that was used for the measurements.

Sheet resistances were obtained from four-point probe measurements on control wafers and from diffused resistors and Van der Pauw strutures on finished device wafers. These values are given in the table below; all numbers are in ohms/square.

Layer	Drive-In	4-Pt. Probe	Diff. Resistor	Van der Pauw
Base	875	1689	2051	2145
	900	1622	2113	2278
Poly Emitter	875	282	260	260
	900	201	183	204
Poly on oxide	875	295	302	301
	900	209	201	223

SUPREM-3 predicted base sheet resistances of 1561.3 and 1539.5 ohms/square for the 875C and 900C emitter-drives, respectively. Poly sheet resistances of 294.85 and 290.43 ohms/square were predicted. These values are compared to measurements because SUPREM-3 calculates separate sheet resistances for the emitter and the poly, which, produces an artificially high value of emitter sheet resistance. Measured values of emitter sheet resistance are actually the poly resistance in parallel with the emitter resistance. The result is that emitter sheet resistance is slightly less than for the polysilicon alone. Full comparisons of control wafer measurements to simulations are given in Appendix A.

Results from testing of the transistors showed that when aluminum was present directly over the active part of the emitter, there was a resistor from emitter to base. Based on control wafer data, it was obvious that the emitter-base junction existed. Measurement of emitter-collector breakdown voltages of 70 to 90 volts for these devices confirmed that, indeed, there was an emitter-base junction. Devices that did not have aluminum directly over the active emitter produced device characteristics as expected for an NPN transistor. It followed, that the aluminum had spiked through the polysilicon. One advantage of this, however, is that it supports the measurements of very shallow emitter junction depths. This problem did not occur in the processing previously performed at RIT, in which, the emitter junction depth was about 0.2 um.

Current gains of the NPN transistors were measured to be approximately 15 to 25, which, were far less than expected. From the simulation results for integrated base doping, it can be seen that the base doping was high, approximately 2E13 cm-2. The integrated dopant results from the simulations also indicate that the 900C emitter-drive should produce devices with higher gains than those produced with the lower temperature drive-in. This result was actually observed.

Measurements of emitter-base breakdown voltages in the -3 to -4 Volt range and base-collector breakdown voltages of -90 to -100 Volts support the hypothesis that the base doping is high. This is also confirmed by the data obtained from Gummel plots of the devices. Saturation currents were 1.26E-15 and 1.75E-15 Amps for the two emitter-drives.

One other transistor parameter of importance is the forward Early voltage. Fairly large values of -141 to -417 Volts were obtained, with the larger (more negative) value being for the lower temperature emitter drive-in. This indicates, as expected, that the base width was wider for this drive-in. The highly negative values for small base widths are one advantage of polysilicon emitters.

CONCLUSION

Precise control over shallow junction depths by using polysilicon as the emitter contact of a bipolar device was accomplished. However, the primary advantage of polysilicon emitters, the enhanced current gain, was not observed. It was determined that a high base doping level caused a reduction in gain. Future work with this process should involve a base implant dose lower than the 1E14 ions/cm2 dose that was used. Another change for future work would be to redesign the devices in order to eliminate any metal directly over the active emitter regions. Aluminum spiked through the polysilicon creating a resistor from emitter to base in the devices that were fabricated.

ACKNOWLEDGMENTS

I would like to thank Dr. Renan Turkman, Mike Jackson, Rob Pearson, Dr. Lynn Fuller, Dr. Richard Lane, Dave Price, Scott Blondell, and Gary Runkle for all their help throughout this project.

REFERENCES

[1] S. Wolf, Silicon Processing for the VLSI Era: Volume 2 - Process Integration (Lattice Press, Sunset Beach, 1990), 501
[2] Ibid.
[3] Ibid.
[4] T.H. Ning and R.D. Isaac, IEEE Trans. Elect. Dev., ED-27, 2051 (1980).
[5] G.R. Wolstenholme, et al, J. App. Phys., v.61, 225.
[6] T.H. Ning and R.D. Isaac, IEEE IEDM, 1979, 473.
[7] S. Wolf, ibid., 502.
[8] H. Schaber and T.F. Meister, IEEE Bipolar Ckts. and Tech. Meeting, 1989, 75.
[9] T.H. Ning and R.D. Isaac, opcit.
[10] H. Schaber and T.F. Meister, ibid., 76.
[11] H.C. Card and C.S. Yang, IEEE Trans. Elect. Dev., ED-24, 397-402 (1977).
[12] H.C. deGraff and J.G. deGroot, IEEE Trans. Elect. Dev., ED-26, 1771-1776 (1979).
[13] H. Schaber and T.F. Meister, ibid.
[14] C.C. Ng and E.S. Yang, IEEE IEDM, 1986, 32-35.
[15] S. Wolf, ibid.
[16] H. Schaber and T.F. Meister, ibid., 79.
[17] Ibid.
[18] S. Wolf, ibid.
[19] David Price, Independent Study project, 1990.
[20] Ibid.
[21] Renan Turkman, Ph.D. (private communication).