LINEAR POLY GATE CHARGE COUPLED DEVICE IMAGING ARRAYS

Lucien Randazzese
Senior Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

A five mask level process was used to fabricate single level, poly gated charge coupled devices intended for use as optical imagers. Three micron gate spacing was achieved with an emulsion mask through tight control of the lithography process. Testing revealed a short between the gates. It is hypothysized to result from insufficient poly gate etching or over diffusion of the gate.

INTRODUCTION

The inherent low voltage / low power nature of charged coupled devices, CCDs, combined with their relative ease of manufacturing, has led to a wide range of microelectronic uses including large scale memories, imaging arrays and digital signal processing components [1]. It is by exploiting the transparent nature of polysilicon thin films that CCDs can be used as solid state imaging devices.

A CCD is essentially a linear array of MOS capacitors along which charge is transferred. Consider such an array made up of polysilicon gates over a p-type substrate. When a positive voltage is applied to the gate, the holes in the silicon substrate are repelled from the semiconductor surface, creating a positively charged depletion region at the surface. If the gate bias is increased further, the number of electrons at the surace will exceed the number of holes originally present. At this point the MOS device is said to be in the inversion regime with an electron potential well under the gate.

If two MOS capacitors are spaced within three microns of one another their inversion regions will overlap when biased. If the two gates are sequentially biased with overlapping pulse signals, any charge stored in the first inversion well will be temporarily shared by both capacitors, and following that, will reside completely under the second. The origin of this charge can be from current injection or by generation of electron-hole pairs via thermal or optical means. Using a single level gate configuration, a three phase overlapping clock can be used to propagate charge along a CCD array.

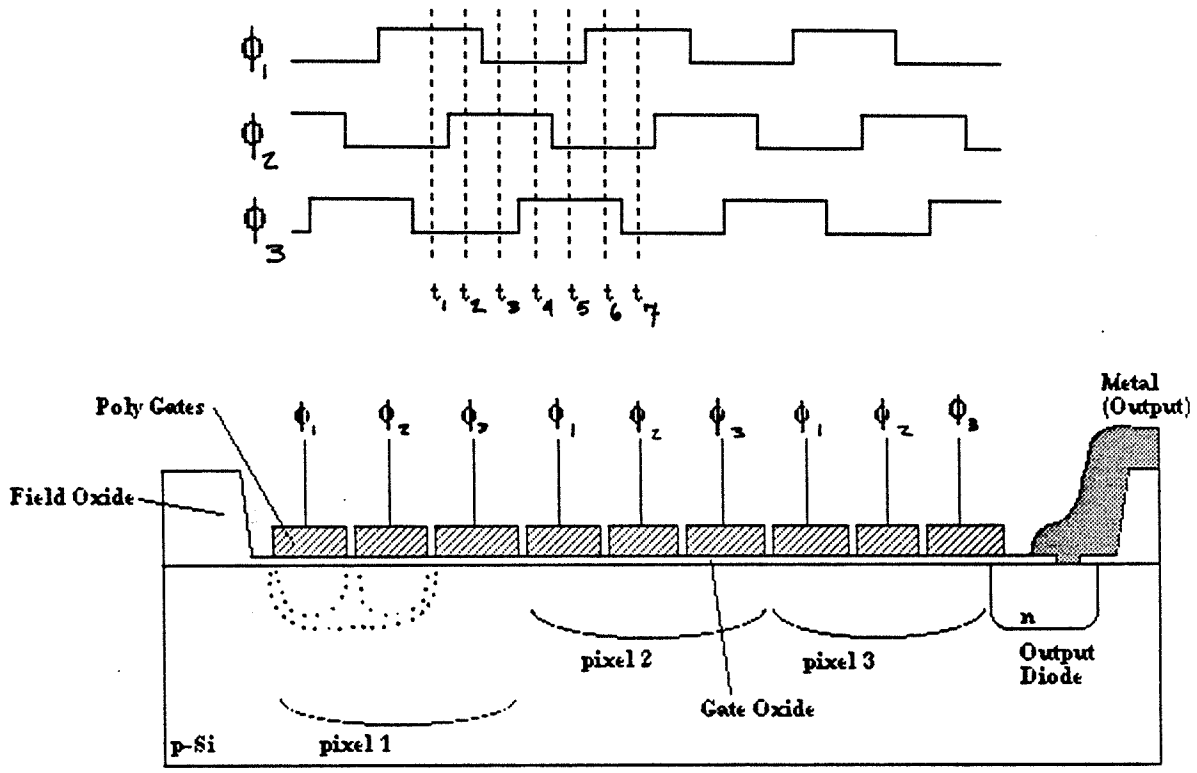

Figure 1: 3 pixel CCD array and clocking scheme.

Using Figure 1, let us examine the propagation of charge in a little more detail. Shown is a 9-gate, 3-pixel CCD array cross section employing a three phase clock scheme. At time t_1 a potential well exists under every MOS capacitor gate connected to clock ϕ_1. At time t_2 every gate connected to ϕ_2 is also biased for depletion. For a short time then when both ϕ_1 and ϕ_2 are high, the potential wells are two capacitors wide. As ϕ_1 goes low the potential well under ϕ_1 gates disappears and the charge stored under them spills completely into the potential wells under ϕ_2 gates, at time t_3. At times t_4 and t_5 the same mechanism shifts the charge from under the ϕ_2 gates to under the ϕ_3 gates. At time t_6 the charge is temporarily shared between ϕ_3 and ϕ_1 gates and finally spilled entirely into the wells under the ϕ_1 gates, t_1, mimicking the original charge storage scheme except now the free charge configuration in the silicon has been shifted 3 MOS capacitors down the CCD array [2].

The last gate of the array must overlap the output n-well to guarantee the shifted charge will be injected into the output diode. This injection can be detected as a current spike at a relatively high capacitance output terminal (the capacitance is provided off chip) [3].

Due to the transparency of polysilicon films, polysilicon gated CCD's can be used as imaging arrays. As visible light impinges on the array it travels relatively unimpeded through the poly and thin oxide to generate free charge carriers in the semiconductor. The density of these photo-generated carriers is

proportional to the intensity of incident light and the time allowed for charge accumulation, referred to as the integration time. If charge is allowed to build up indefinately it may spill over into adjacent wells. Thus a well or pixel may contain an amount of charge not proportional to the incident light intensity, jeopardizing the integrity of the stored information. The charge profile created under the array by the optical image can be continuously clocked out by means of the charge transfer mechanism described above and used to provide dynamic information on the light incident on the semiconductor device. For electronic image scanning applications the array output can be used to stitch together a digital replication of an image over which the CCD array is passed. Note that to prevent the charge from individual pixels from mixing, three gates, one for each phase of the clock, is needed for one pixel.

Gate thickness must be minimized in order to maximize charge creation. In addition, a thinner poly thickness also allows for a better poly etch due to reduced aspect ratios. These benefits of thin poly gates had to be balanced with the constraints on gate resistance. In this experiment, the design and fabrication of three phase poly gated CCDimaging arrays was implemented using a p-type substrate because the minority carriers are electrons whose greater mobility allows for better charge transfer. With this single level configuration, gate spacing plays a critical role in charge transfer efficiency [4]. It was believed that the requisit three micron gate spacing could be achieved using emulsion mask lithography with tight control of the exposure and development steps.

EXPERIMENT

CCD arrays consisting 2, 3 and 6 pixel configurations were implemented with three 60 um x 100 um doped polysilicon gates per pixel. Gate spacings of 2,3 and 4 um were designed in order to insure successful poly-gate definition during emulsion mask lithography and etching. Device fabrication included 5 masking levels: output diode and underpass diffusion, thin oxide, poly gate definition, contact cuts and metal interconnects. Six p-type ⟨100⟩ 5ohm-cm Si wafers were used to fabricate all devices. An additional 2 wafers were used as control wafers.

TMA SUPREM-3 process simulation software was used to verify that the 3264A of initial oxide was enough to mask a 35 minute, 1100C substrate diffusion (15 minutes in N2, 20 minutes in wet 02). Following this spin on phosphorous predeposit, the masking oxide and dopant glass were removed and a 20 minute, 1100C, drive-in was performed in wet 02. This resulted in a 3704A field oxide with 3131A of oxide over the phosphorous diffusion regions. A 650A gate oxide was grown at 1100C (10 minutes in dry02 followed by 10 minutes in N2) after thin oxide lithography and etch. A 1792A Polysilicon film was LPCVD deposited at 610C. Suprem3 was again used to determine the maximum poly doping

allowable without jeopardizing the thin oxide gate dielectric. After running several simulations a 950C diffusion (15 minutes in N2 followed by 5 minutes in wetO2) showed sufficient poly doping with a substantial margin of safety for protecting the gate dielectric. A spin on type boron diffusion source was used here.

The critical processing step was the polysilicon gate definition, both lithography using an emulsion mask, and etching. Optical microscopy inspection of the masks showed the 2, 3 and 4 um gate spacing features to be well defined. The wafers were intentionally underexposed by 15% (Dose = 0.85 Optimal Dose) so as to minimize the resist spacings. A 3 minute oxygen plasma ash was used to clear the residual resist scum which resulted from the intentional underexposure. Poly etching was done in a Tegal 700 plasma etcher running 3.5 sccm of O2 and 10 sccm of SF6. Each wafer was etched in 10 second intervals with optical inspections between each etch. Etching took 90 seconds to complete for all wafers.

Contact cuts and metal interconnection (aluminum was evaporated) completed the fabrication process. Note that both 450C, 20 minute sinter was done both before and after aluminum patterning. Complete process sheets and output decks for TMA SUPREM-3 simulations are provided in the appendices. Figures 2 and 3 illustrate the layout for a 9-gate 3 pixel device and the testing circuitry schematics respectively.

Testing circuitry was provided off chip via a bread board set up in an effort to minimize non CCD related failures. A oscilloscope was used to monitor the output of the arrays directly from the chip while were tested with a variable intensity white light.

RESULTS/DISCUSSION

Processing of the linear poly gated CCD arrays was successful in producing 2 testable wafers. Even with the 3 minute O2 ash of the resist, gate spacing features on all wafers for most devices designed with 2 and 3 micron spacings were scummed. The resist image for devices designed with four micron gate spacings showed gate spacings of approximately 3 microns. Many of these spacings were rough and a 6 second poly etch was done after the protective resist mask had been ashed away in an effort to clear some residual poly bridging. This process was successful for two wafers but resulted in over-etched gates for device wafers 2 through 4 and 6.

Testing showed all the gates so be shorted together through a resistive path. I-V curves generated for the electrical characteristics between each clock pad and the output pad showed linear resistive paths ranging in value from 0.5 kohm to 1.5 kohm

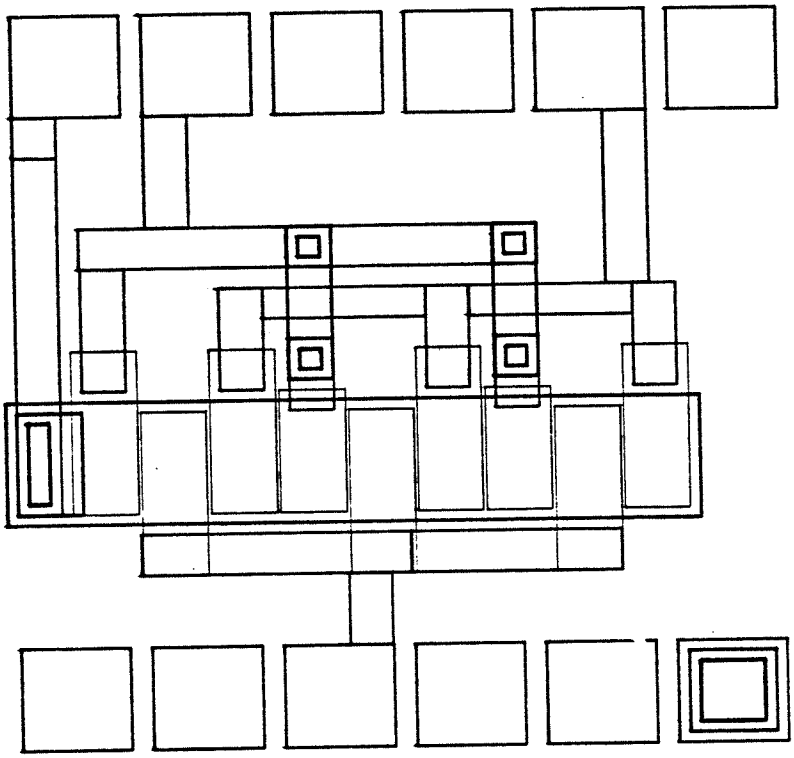

Figure 2: 9-gate, 3-pixel array layout.

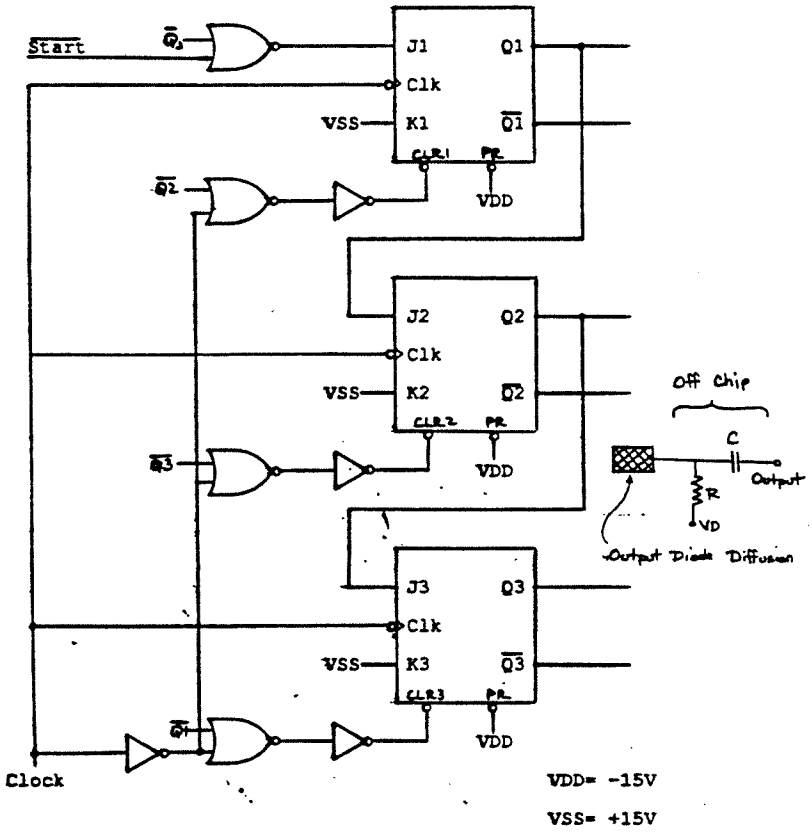

Figure 3: Clocking and output circuitry.

This wafer-wide short was most likely caused during either the poly doping or poly etching steps. If the boron polysilicon doping process was too severe the dopants may have diffused right through the thin gate oxide, shorting the gates to the substrate and washing out the n-type output diode diffusion under the last gate. This would have succeeded in effecting a resistive path between each gate and the output. SUPREM-3 simulations of the poly doping show a gate oxide penetration of only 100A and so it is unlikely that the boron actually diffused through the entire 650A of gate oxide and washed out the n-type output diode diffusion as well.

The more likely explanation of the wafer-wide shorting observed during CCD testing was an insufficient poly etch. If the gates had not been completely etched, a thin sheet of polysilicon would have been present over the entire surface of each wafer. Given the doped nature of the polysilicon and the extremely small effective square number between any closely spaced 100 um gates, the resistance values determined are not at all unrealistic.

CONCLUSIONS

Two, three and six pixel poly gated CCD imaging arrays were constructed with gate spacings of 3 um achieved with emulsion mask technology through tight control of lithography and poly etching steps. CCD functionality could not be demonstrated due to wafer-wide shorts which appeared on all device wafers. These shorts resulted either from a poly diffusion which broke through and shorted the gate oxide, or a more likely poly gate under etch.

ACKNOWLEDGMENTS

The author would like to thank the following people for their various contributions to this project: Mike Jackson, Pat Drennan and Dr. Zoran Ninkof.

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