BiCMOS VS CMOS AT RIT

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ABSTRACT

This project involved the performance comparison of the standard RIT N-well CMOS and a proposed BiCMOS processes. Device parameters were extracted from TMA SUPREM-3 simulations and used to create NPN, PMOS, and NMOS model cards for Accusim simulations. Two inverter circuits, one in CMOS and one in BiCMOS were designed to drive a 50pF load. The BiCMOS circuit was determined to be four times faster, less temperature dependent, and considerably smaller than its CMOS counterpart. These results lead to a final conclusion favoring the development and use of BiCMOS here at RIT.

INTRODUCTION

Today's IC market is dominated by CMOS technology for several important reasons: well characterized process, practically zero power consumption, a higher packing density, lower standby power, and, to a first order, infinite input impedance. CMOS lends itself to large-scale and very large-scale integration because its simple gate construction is readily scalable, more scalable than any bipolar technology. Also, any increase in circuit density does not exacerbate the power dissipation problem as severely as in bipolar technology. However, bipolar technology exhibits higher frequency response, higher transconductance per area, higher driving capability and less noise. Thus, the trend has emerged in industry to tap these advantages by incorporating bipolar and CMOS technologies into a single process dubbed BiCMOS.

The merger of the Bipolar and CMOS technologies can be utilized to implement systems with not only higher performance, but with a wider range of functions than each technology alone. The BiCMOS circuits should possess similar DC characteristics to those of CMOS circuits, but much improved AC drive characteristics, and less dependency on external conditions such as process variations and temperature. A BiCMOS circuit exhibits different power consumption properties than a CMOS circuit. In CMOS the load capacitance not only increases the gate delay, but also degrades the slew rate of the output. The degraded output characteristic causes the next driven gate to switch slower, therefore spending more time in the transition region and consuming more power. The BiCMOS gate, because of its low output

impedance provided by the bipolar transistors, does not degrade the switching performance of the driven gate and is therefore more power efficient. These are only some of the benefits of the BiCMOS technology.

RIT currently has an N-well, self-aligned, poly-gate CMOS process. A bipolar process is being developed which could eventually be integrated with the N-well CMOS process. This bipolar process will not have an epitaxial layer, instead the NPN devices will be fabricated in the N-well. A cross-section of the proposed BiCMOS process is shown in Figure 1.

In order to exploit the strengths of both technologies the MOS and Bipolar transistors in the BiCMOS process must be optimized. This investigation will not make an effort to optimize the MOS devices in the existing RIT N-Well CMOS process or the NPN device currently being developed by Luigi Ternullo Junior. The purpose of this research work is to join the two processes in order to develop a RIT BiCMOS process, compare the two processes (N-Well CMOS and BiCMOS) and determine whether the RIT BiCMOS process will yield circuits with the same enhanced AC drive characteristics and less dependency on external conditions typical of a good BiCMOS process.

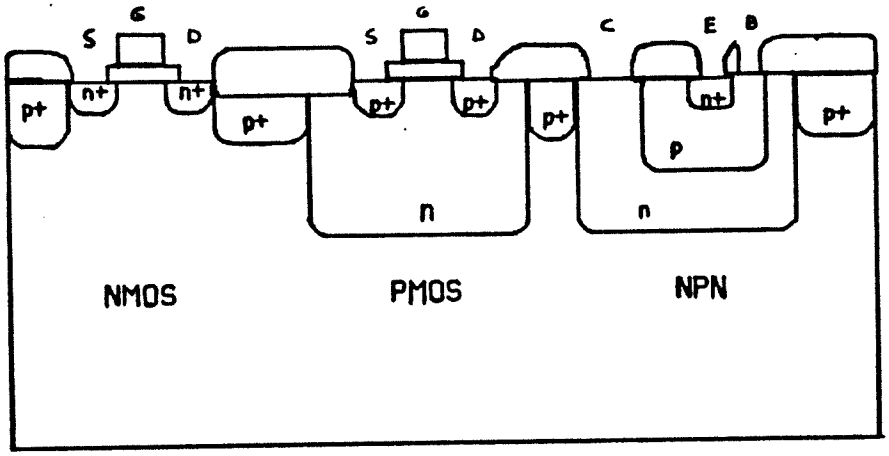

Figure 1: Complete Cross-section of the Proposed BiCMOS Process.

EXPERIMENT

The BiCMOS process was developed using the existing RIT N-Well CMOS process as the starting point. Theoretically, the only extra steps that are required are the base implant and base drive-in. These steps need to be added into the CMOS process somewhere between the N-Well drive-in and the gate oxide growth for the gates of the MOS devices. SUPREM simulation work supported this theory and a decision was made to add the base implant and drive-in immediately following the LOCOS process. The CMOS devices were identical to those of the RIT N-Well CMOS

process. The NPN bipolar transistor was designed in the N-Well using the well as the collector, the source/drain implant for the NMOS device to form the emitter and the added implant and drive-in to form the base. Figure 2 is a plot of the concentration profile through the emitter cross-section. The plot shows an emitter junction depth of 0.34 um, a base Xj of 1.24 um, and the Xj of the collector or the N-well of 4.69 um. The junction depth of the N-Well must be deep enough such that the subsequent implants for the base and emitter can't diffuse through the well into the p-substrate and effectively short out the base-collector junction thereby forming a diode instead of a transistor. The base-width of the NPN device is a very critical parameter that directly affects the device parameter Beta and therefore the performance of the device. The base width was determined by SUPREM to be 0.9 um to produce an NPN device with a Beta of 54.12.

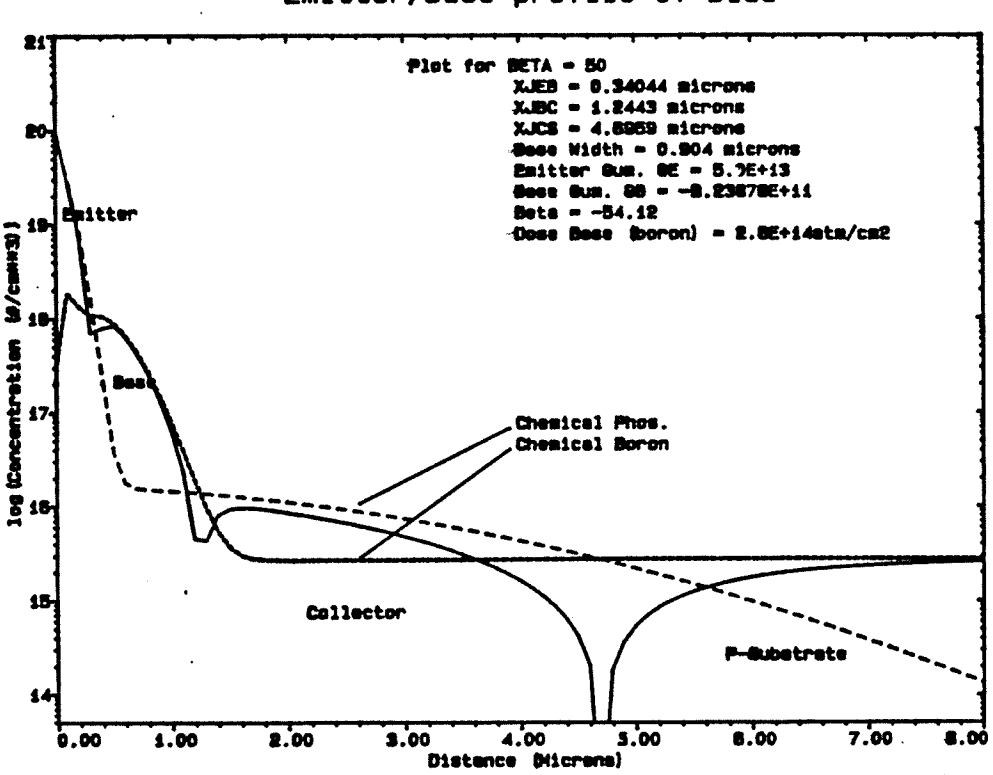

Figure 2: NPN Transistor Concentration Profile.

In order to complete the second part of this research work (comparison of the CMOS and BiCMOS technologies), device parameters that were extracted from the SUPREM simulations were used to create PMOS, NMOS, and NPN model cards for Accusim simulations. Accusim is a SPICE 2G.6 based simulator available through Mentor Graphics. The two functionally equivalent inverter circuits (one using CMOS technology and the other in BiCMOS) were designed to drive 50pF loads. Figures 3 and 4 are schematics of these circuits. More discussion of design considerations for each of these circuits is available in the Results and Discussion section of this report. The simulations that were run for both of these circuits were aimed to reveal the

benefits of the BiCMOS technology that were discussed in the Introduction. The propagation delay and static power are the most critical characteristics of a logic circuit. The propagation delay simulations were run at temperatures ranging from -40C to 125C for each circuit to determine the dependance of both circuits on external conditions.

RESULTS/DISCUSSION

The CMOS inverter shown in Figure 3 is actually a five stage inverter with a build-up ratio of 2.76. The build-up of five stages is necessary to drive the 50pF load most efficiently. The total gate width for this circuit is 32,502um, which is a relatively large inverter. The BiCMOS inverter shown in Figure 4 consists of six MOS transistors and two NPN transistors. Timing is very important in this circuit since crow-bar currents could escalate and produce a power hungry circuit. The key to minimizing power dissipation is by making sure that both NPN devices are not conducting simultaneously. The bipolar devices are capable of sourcing and sinking very large currents and if both devices are allowed to conduct at the same time, a direct path between Vcc and ground will exist and result in considerable power dissipation. A check of the current through each of the devices in the BiCMOS inverter revealed that no overlapping currents existed and therefore the static power consumption of this circuit is zero, same as the CMOS inverter.

The speed advantage of the BiCMOS circuit was very evident throughout the entire temperature range. Table 1 shows the propagation delays of both circuits at each temperature. At typical conditions (T=25C), the slowest prop delay for the BiCMOS inverter is 5.91ns as opposed to 21.03ns for the CMOS inverter. The dependance on external conditions such as temperature was determined to be less for the BiCMOS circuit. Running the simulations throughout the temperature range (-40C to 125C) the BiCMOS inverter's prop delays changed only 8.16%, where the CMOS inverter slowed down by 12.28%. Better temperature stability is typical of a good BiCMOS circuit, since at higher temperatures the performance of the MOS devices degrade in a CMOS circuit. The bipolar devices, however, speed up due to a decrease in Vbe and the input capacitance, thereby reducing the time it takes to charge and turn on the transistor. Therefore in a well designed BiCMOS circuit the degradation affect of the MOS devices is offset by the improved performance of the bipolar devices and the overall circuit performance remains nearly constant.

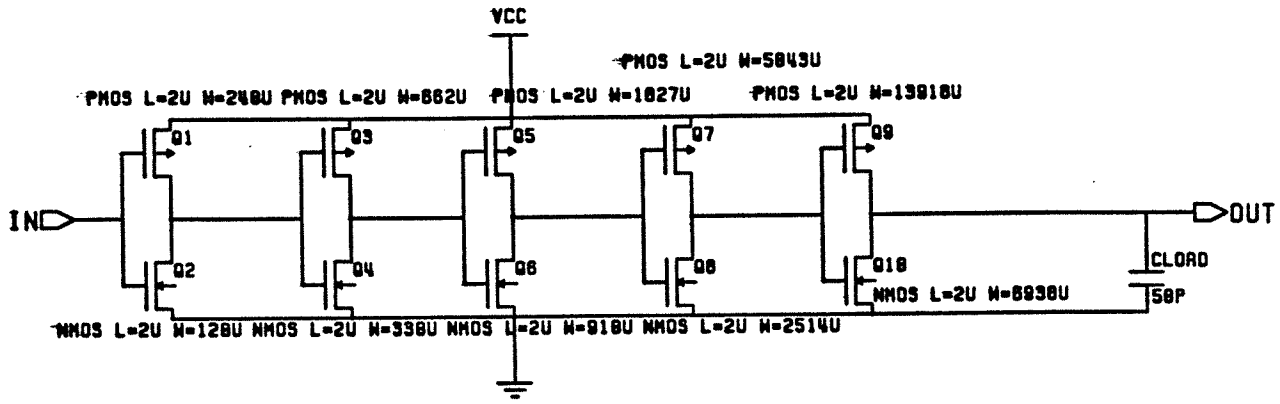

Figure 3: Schematic of CMOS Inverter.

BiCMOS INVERTER

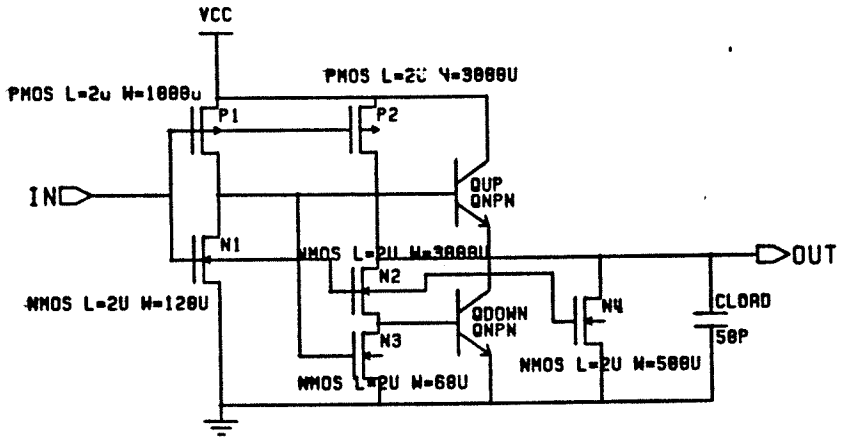

Figure 4: Schematic of BiCMOS Inverter.

BiCMOS INVERTER

	-40C	25C	85C	125C
tpHL	3.44ns	3.62ns	3.74ns	3.80ns
tpLH	5.74ns	5.91ns	6.11ns	6.25ns

CMOS INVERTER

	-40C	25C	85C	125C
tpHL	17.25ns	18.03ns	18.75ns	19.20ns
tpLH	20.00ns	21.03ns	22.05ns	22.80ns

Table 1: Propagation Delay Summary.

The total area of each circuit is another important factor which distinguishes the two technologies being evaluated here. Recall, the total gate width of the CMOS inverter is 32,502um. The total gate width of the MOS devices in the BiCMOS inverter is 7,680um and the emitter length of each of the two NPN transistors is 250um. When approximate die sizes of both inverters are compared, the CMOS circuit is found to be about twice the size of the BiCMOS circuit. Since the digital world is very much focused on producing high-density chips, the BiCMOS technology certainly will be used more widely in the future.

CONCLUSION

A BiCMOS process was designed using the RIT N-well CMOS process as the starting point. The device parameters from both processes were used to design and simulate two functionally equivalent inverter circuits (one in CMOS and one in BiCMOS). The BiCMOS inverter was found to have considerable advantages in the areas of die size, speed, and performance consistency over a wide temperature range. These results are the basis for a final conclusion of developing and using BiCMOS to design and fabricate circuits here at RIT.

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