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Millimeter-wave interconnects for intra- and inter-chip transmission and beam steering in NoC-based multi-chip systems

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Millimeter-wave interconnects for intra- and inter-chip transmission and beam steering in NoC-based multi-chip systems

by

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Technical Abstract

The primary objective of this work is to investigate the communication capabilities of short-range millimeter-wave (mm-wave) communication among Network-on-Chip (NoC) based multi-core processors integrated on a substrate board. To address the demand for high-performance multi-chip computing systems, the present work studies the transmission coefficients between the on-chip antennas system for both intra- and inter-chip communication. It addresses techniques for enhancing transmission by using antenna arrays for beamforming. It also explores new and creative solutions to minimize the adverse effects of silicon on electromagnetic wave propagation using artificial magnetic conductors (AMC). The following summarizes the work performed and future work.

Intra- and inter-chip transmission between wireless interconnects implemented as antennas on-chip (AoC), in a wire-bonded chip package are studied 30GHz and 60 GHz. The simulations are performed in ANSYS HFSS, which is based on the finite element method (FEM), to study the transmission and to analyze the electric field distribution. Simulation results have been validated with fabricated antennas at 30 GHz arranged in different orientations on silicon dies that can communicate with inter-chip transmission coefficients ranging from -45dB to -60dB while sustaining bandwidths up to 7GHz. The fabricated antennas show a shift in the resonant frequency to 25GHz. This shift is attributed to the Ground-Signal-Ground (GSG) probes used for measurement and to the Short-Open-Load (SOLT) calibration which has anomalies at millimeter-wave frequencies. Using measurements, a large-scale log-normal channel model is derived which can be used for system-level architecture design. Further, at 60 GHz densely packed multilayer copper wires in NoCs have been modeled to study their impact on the wireless transmission

between antennas for both intra- and inter-chip links and are shown to be equivalent to copper sheets. It is seen that the antenna radiation efficiency reduces in the presence of these densely packed wires placed close to the antenna elements. Using this model, the reduction of inter-chip transmission is seen to be about 20dB as compared to a system with no wires. Lastly, the transmission characteristics of the antennas resonating at 60GHz in a flip-chip packaging environment are also presented.

The transmission coefficients observed in the previous cases can be further improved by using antenna arrays to perform beamforming which can increase the overall system gain. Three types of arrays are designed with different beam angles – broadside, phased and endfire, which are considered in two scenarios that are intra-chip and inter-chip. The antenna elements are fed with a delayed-line system to create the desired progressive phase for arrays. For broadside arrays working at 60GHz, the measured transmission when the beam max is directed towards the desired array pair for untrimmed-feed for intra-chip case vary from -43 to -55dB, and for the inter-chip case, it varies from -35dB to -40dB. For phased array in the intra-chip scenario, the measured transmission between the arrays with untrimmed-feed varies from -37dB to -42dB. Lastly, the endfire array for the intra-chip case shows a good consistency between the simulation and measured results. For inter-chip scenarios, despite best alignment between the arrays, the measured results are quite lower than the simulated results. This may be due to the fabrication variation. Simulated radiation patterns and electric field density are plotted to explain beamforming for all types of designed arrays located at various locations across the chip. These radiation patterns are compared with the free space patterns. The beam of the array is distorted by the losses in the silicon substrate and diffraction effects due to the chip structure. The measured transmission coefficients would be useful to find the link budget for the system-level design.

Moreover, innovative techniques like artificial magnetic conductors (AMC) are investigated to improve the transmission between wireless interconnects such as zigzag antennas. During the study of intra- and inter-chip transmission described above, it was seen that the antenna radiation efficiency reduces with a decrease in the resistivity of silicon. Preliminary work has been done to show the enhancement of intra-chip transmission between wireless interconnects, which are implemented as antenna-on-chip (AoC), using a Jerusalem-Cross Artificial Magnetic Conductor (JC-AMC). For each quadrant, a zigzag monopole AoC above a JC-AMC surface is simulated to resonate at 30GHz with a return loss of -13dB. The enhancement is almost 3dB for two out of three antenna pairs. This enhancement has almost doubled the received power at the antenna with JC-AMC which is beneficial when designing on-chip integrated transceivers. Experimental validation through the fabrication of the zigzag antennas on JC-AMC surfaces on silicon wafer will be pursued as future work.

Outreach Abstract

Emerging technologies like the Internet of Things (IoT), artificial intelligence (AI), cloud computing requires unprecedented processing power. Generally, the customers of these technologies are using their small handheld devices for usage, but technically, all the processing occurs over the Internet at the backend servers which are located far-away in giant datacenters. Improving processing power of datacenters by decreasing the size of the transistor is not a feasible option because we have reached the atomic limits. Also, this means Moore's law, which states that the number of transistors will double in about every two years, is dead so innovative ways are needed to improve the efficiency of existing computing systems. If the computing power in datacenters is improved, this will ultimately improve the user experience in the near future.

In the industry, scientists and engineers are moving beyond their traditional approach to enhance the computing power of datacenters even further by incorporating wireless technologies inside computer chips. It is expected that the wireless will enhance the communication within and between multiple chips, and therefore improve the overall computing power of a server. Moreover, using wireless interconnects for intra-chip and inter-chip communication will decrease the power consumption involved in parallel processing.

Since the beginning of wireless communication, it has touched the lives of everyone on our connected planet. Most of the communication systems of the world depend on wireless technology for optimal performance. Many wireless technologies like MIMO systems, beam steering, etc. are yet to be implemented on a silicon chip. This creates an opportunity for researchers to investigate the ways to connect silicon chips wirelessly. Due to the small size of the chip, innovative solutions

must be designed to implement a wireless system inside the chip. This work is performed to provide a basic framework for the implementation of wireless technologies on the chip.

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Publications from current work

First authored peer-reviewed publications:

- R. S. Narde, J. Venkataraman, A. Ganguly and Ivan Puchades, "Intra- and Inter-Chip Transmission of Millimeter-Wave Interconnects in NoC-based Multi-Chip Systems," in *IEEE Access*, July 2019, DOI: 10.1109/ACCESS.2019.2931658.
- R. S. Narde, J. Venkataraman, A. Ganguly and Ivan Puchades, "Phased Array as Millimeter-Wave Interconnects in Multi-Chip Systems", *IEEE Antennas and Wireless Propagation Letters*, 2020. (under review)
- R. S. Narde, J. Venkataraman and A. Ganguly, "Disc-Loaded, Vertical Top-Hat Monopole Antenna at 225 GHz for On-Chip Wireless Communications," *2019 IEEE International Symposium on Antennas and Propag.*, Atlanta, GA, USA, 2019, pp. 1883-1884.
- R. S. Narde, J. Venkataraman, and A. Ganguly, "Enhancement of Intra-chip Transmission between Wireless Interconnects using Artificial Magnetic Conductors," in *2018 IEEE Antennas & Propag. Soc. International Symp., APS 2018 - Proceedings*, 2018, pp. 805–806.
- R. S. Narde, N. Mansoor, A. Ganguly, and J. Venkataraman, "On-Chip Antennas for Inter-Chip Wireless Interconnections: Challenges and Opportunities," in *12th European Conference on Antennas and Propagation (EuCAP 2018)*, 2018, pp. 600 (5 pp.)-600 (5 pp.).
- R. S. Narde, J. Venkataraman, and A. Ganguly, "Feasibility study of transmission between wireless interconnects in multichip multicore systems," in *2017 IEEE International Symp. on Antennas and Propagation*, 2017, pp. 1821–1822.

Second and third authored peer-reviewed publications:

- M. S. Shamim, N. Mansoor, R. S. Narde, V. Kothandapani, A. Ganguly, and J. Venkataraman, "A Wireless Interconnection Framework for Seamless Inter and Intra-Chip Communication in Multichip Systems," *IEEE Trans. Comput.*, vol. 66, no. 3, pp. 389–402, Mar. 2017.
- M. S. Shamim, R. S. Narde, J.-L. Hernandez, A. Ganguly, J. Venkataraman, and S. Kandlikar, "Evaluation of wireless network-on-chip architectures with microchannel-based cooling in 3D multicore chips," *Sustain. Comput. Informatics Syst.*, vol. 21, pp. 165–178, Mar. 2019.
- A. Ganguly *et al.*, "The Advances, Challenges and Future Possibilities of Millimeter-Wave Chip-to-Chip Interconnections for Multi-Chip Systems," *J. Low Power Electron. Appl.*, vol. 8, no. 1, p. 5, Feb. 2018.
- A. Ganguly *et al.*, "Intra-chip Wireless Interconnect: The Road Ahead," in *Proceedings of the 10th International Workshop on Network on Chip Architectures*, 2017, pp. 3:1--3:6.

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List of Abbreviations

AMC	Artificial Magnetic Conductor
ANT	Antenna
AoC	Antenna-on-Chip
AiP	Antenna-in-Package
BCB	Benzo-cyclo-Butene
BEOL	Back End of Line
BOE	Buffered Oxide Etch
CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Co-planar Waveguide
EBG	Electromagnetic Band-Gap
FCC	Federal Communications Commission
FEOL	Front End of Line
GND	Ground
GSG	Ground-Signal-Ground
HFSS	High Frequency Structure Simulator
HPC	High Performance Computing
IC	Integrated Circuit
IoE	Internet of Everything
IoT	Internet of Things
ITRS	International Technology Roadmap for Semiconductors
MCMC	Multichip Multicore
MIMO	Multiple Input Multiple Output

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NoC	Network-on-Chip
PCB	Printed Circuit Board
PEC	Perfect Electric Boundary
PMC	Perfect Magnetic Boundary
PNA	Programmable Network Analyzer
RFIC	Radio Frequency Integrated Circuit
RIT	Rochester Institute of Technology
SMFL	Semiconductor and Microelectronics Fabrication Laboratory
SOI	Silicon On Insulator
TSV	Through Silicon Via
UWB	Ultra-Wide Band
WLAN	Wireless Local Area Network
WiNoC	Wireless Network-on-Chip

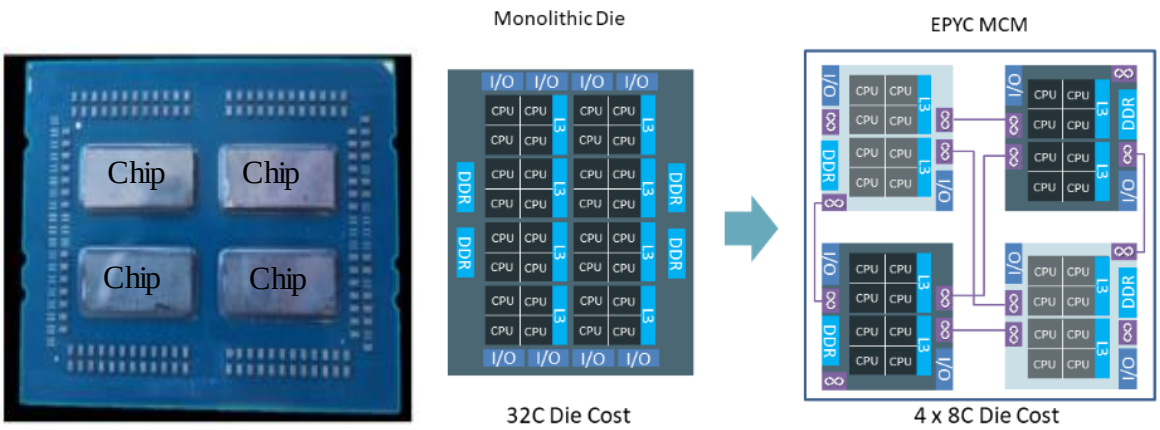
1. Introduction

Emerging technologies like the Internet of Things (IoT), artificial intelligence (AI), cloud computing requires unprecedented processing power. Generally, the customers of these technologies are using their small handheld devices for usage, but technically, all the processing occurs over the Internet at the backend servers which are located far-away in giant datacenters. These datacenters house an enormous network of multichip multicore (MCMC) processing systems to keep up with the demands of parallel processing.

1.1 Multichip multicore systems

Recently, Intel and AMD have released new processors Xeon 9200 and EPYC, respectively [1][2]. Intel Xeon 9200 is a 2-chip processor with 28 cores on each chip and AMD EPYC is a 4-chip processor with 8 cores on each chip. Xeon is based on a 14nm technology node and AMD EPYC is based on 7nm technology node. The pictures of Intel and AMD multichip multicore (MCMC) systems are shown in Figure 1-1. As a modern trend to manufacture server-side processors, a monolithic giant chip is broken into a small scalable chip which has a better economic and cost structure. This also helps to improve the manufacturing yield which is important when profit margins are taken into account. Also, it helps with uniform heat dissipation leading to longer life of the processor.

In the modern computing platform, a single chip multicore system is packaged as shown in Figure 1-2. This package design is used in Intel Xeon [3], which is generally used in high-performance servers. The silicon die/chip is flipped on top of the package substrate, also known as flip-chip technology [4]. This is done to reduce the contact between the transistors and the printed circuit board (PCB). The connection between the chip and substrate is established by using

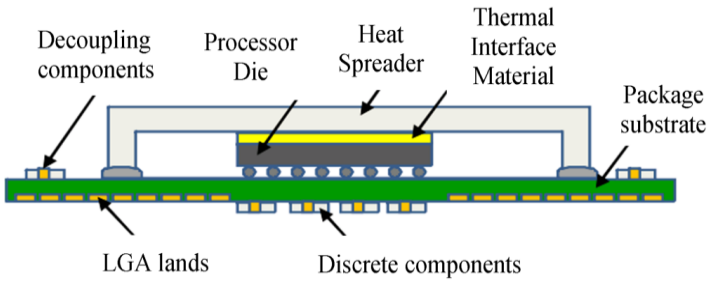


(a) (b)

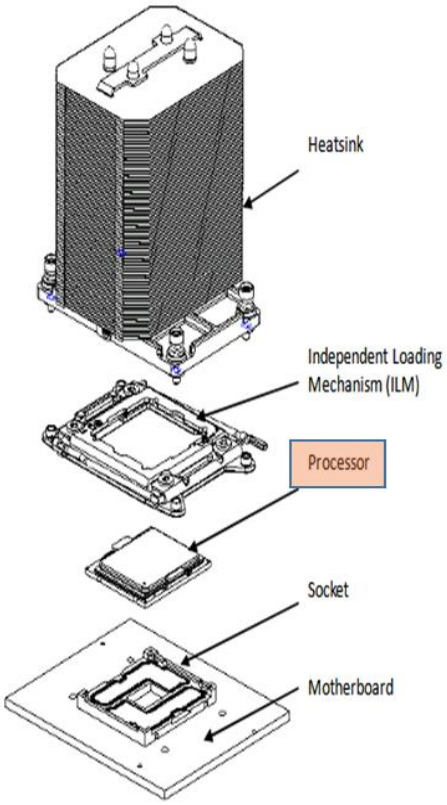
Figure 1-1: (a) AMD EPYC Multichip system, (b) EPYC Monolithic vs MCMC system [2].

solder balls. As the connection points increase the solder balls are arranged in a grid array known as ball grid array (BGA). Moreover, to uniformly spread the heat generated by the transistors on the chip, a heat spreader is placed at the top of the silicon chip. The chip and the heat spreader are attached using a thermal material to provide proper thermal connection without leaving any gaps at the surface contact.

This packaged chip, or simply a package, is placed on the printed circuit board, here labeled as a 'Motherboard'. The connection between the package and the motherboard is established using different interfaces depending on the flexibility, reusability, performance, and environment to be used. Various connections interfaces are BGA, land grid array (LGA), pin grid array (PGA). In Intel Xeon, LGA is used as shown in the picture. LGA provides the feature of reusability to the package as it can be detached from one motherboard, and then placed into another. A similar case can be stated for a PGA socket, however, the electrical performance is lower and they require thick sockets on the motherboard for the pillars to sit into the socket. BGA may provide reusability but at a higher cost of complexity and lower performance for large grid arrays.



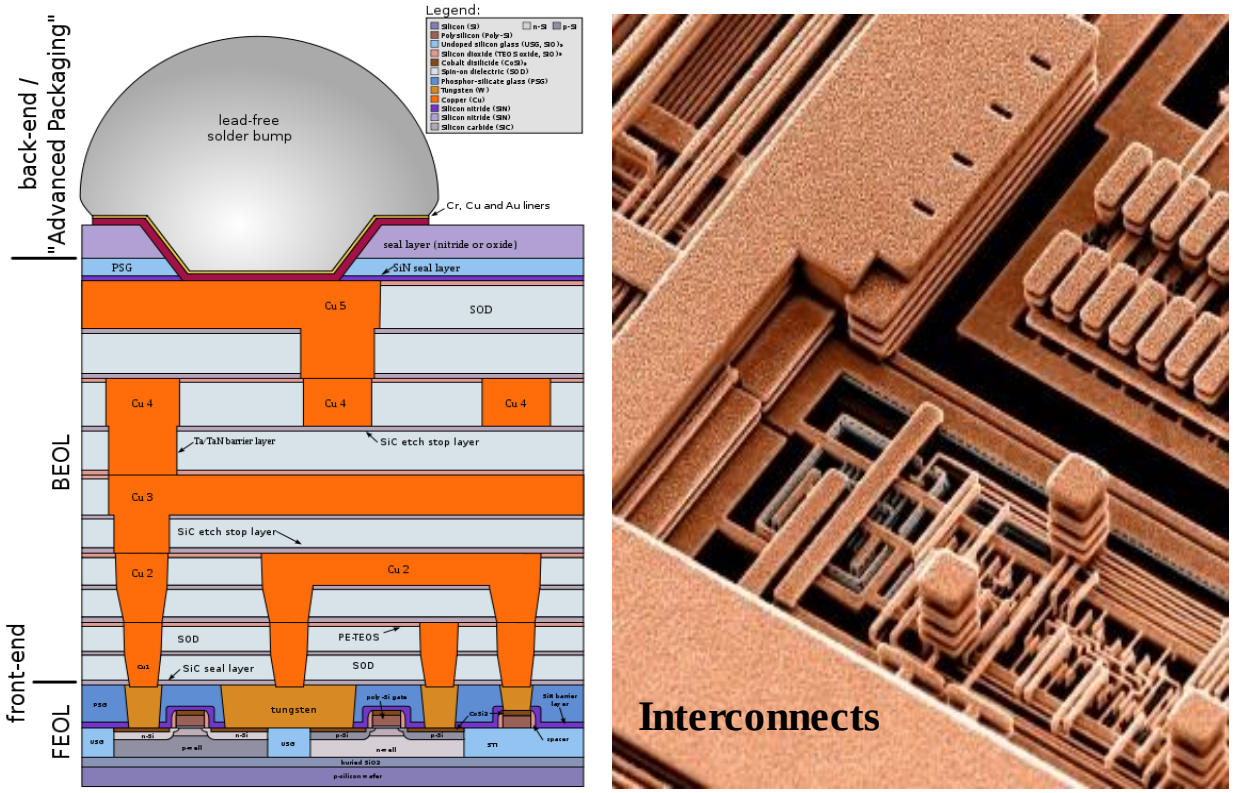
(a)



(b)

Figure 1-2: Modern Package design (a) side view of the package, (b) perspective view of the package[3].

Now, field-effect transistors (FETs) are fabricated on a silicon wafer using a variety of standard CMOS processes. The process of fabrication of transistors is generally known as Front End of Line (FEOL). The front end layer is nothing but two-dimensional placements of FETs on a silicon wafer. The front end does not include connections between different FETs. A metal wire, technically known as a metal interconnect is fabricated on top of the transistors to support the transfer of power or signal. The metal used to fabricate interconnects may be copper or aluminum.



(a) (b)

Figure 1-3: Wired interconnects. (a) View of cross-section of the chip [5]; (b) 3D view [6].

Fabrication of metal interconnect is known as Back End of Line (BEOL). The FEOL and BEOL are shown in Figure 1-3 (a). These Metal interconnect does not only provide connections between MOSFET in FEOL but also connects to the outer package pins using a solder bump. The lead solder bump can be seen in Figure 1-3 (a).

The metal wires connecting the transistors are fabricated as a back-end-of-line (BEOL) process. It involves a complicated and slow process of deposition & etching of an inter-layer dielectric (ILD) layer, usually silicon dioxide (SiO_2), and a metal layer (either copper or aluminum). There are various parameters taken into an account while depositing ILD since, the structure should be mechanically stable at the same time, the metal between ILD should form a good connection. Since, if the appropriate amount of metal is not deposited or etched, the metal wire would be unable to conduct current leading to lower yield. In modern processors, wires are

fabricated using copper, however, copper doesn't go well with SiO_2, so a special process called damascene process is used which forms an additional barrier between copper and SiO_2.

Recently the number of transistors has increased to billions per chip, consequently, the metal interconnects connecting them have increased tremendously. It has become difficult to design these metal interconnects. Also, the interconnects take space and generate heat due to conductive losses of metal. Moreover, the scaling of interconnects with smaller technology nodes is problematic [7] due to increasing power consumption [8], delay, electro-mitigation, electrical noise, and clock synchronization [9]. New methods of transferring signals are required to efficiently transfer the signal/data from one location of the chip to another. As a result, the network-on-chip (NoC) came into existence.

Considering limitations of metal interconnects, a new interconnect system was proposed in 2002 which implemented networks of interconnects based on computer networking [9]. Switches, routers, hubs and other networking devices were designed on the chip to support the network-on-chips (NoC). Moreover, different networking algorithms like mesh, bus, et al. based on large computer networks were implemented to improve the interconnect performance. Commercial and research-oriented devices based on mesh networking topology is Mellanox 72 core SoC processor [10] and a research-oriented 'kilocore' 1000 core processor [11].

As the chips like Tx72 from Mellanox are slowly getting into the mainstream since Intel and AMD are now looking to take the path to multichip many-core processors. In the future, the typical number of cores in a processor will increase to a hundred or more cores. Furthermore, recent research analyzing the system-level performance of wire-based NoC architectures has found that the network is bound to suffer congestion and packet latency or, even, loss when it comes to

the communication between farthest cores [12]. A new approach to solve the congestion and delay problems must be found to keep the improving computing power in high-performance servers.

Near-term emerging solutions to this problem are using wireless interconnects or optical interconnects for long-distance communication between cores located in intra-chip or even inter-chip. Although the interconnects based on optical waveguides have large bandwidth, the fabrication process, size, and requirement of additional heating elements for waveguides seriously limits the integration with the CMOS digital circuitry [13]. On the contrary, wireless interconnects are based on standard CMOS process technology. The metal antennas used as wireless interconnects can be designed using the standard processes. Therefore, research for wireless interconnects as AoCs is attractive.

1.2 Intra- and Inter-chip wireless communication

As the demand for processing power is driven by innovative technologies like artificial intelligence (AI), cloud computing, virtual reality (VR), and others, in near future, the high-performance systems will be required to parallel processing enormous amount of data. Since the CMOS technology node is reaching its ceiling at 5-7nm, novel technology is needed to keep up with the upcoming computational demands. Recent research has shown that wireless interconnects can serve for intra-chip (wireless network-on-chip) or inter-chip communication to improve the performance of NoC and therefore enhancing the computational power of the processor [14].

As the number of cores increases in a chip, the NoC leads to poor performance due to the congestion and delays. When several cores are processing information, the injection rate of data packets increases which affects the NoC performance for the long-destined packets. Some data packets, destined for far away core, may get into a routing loop problem due to local congestion

nearby or between routers, this leads to tremendous delay or even loss of the packet. Using network packet simulation, it has been found that if a few wireless nodes are placed in proper places as shown in Figure 1-4 as an example scenario, higher performance can be achieved [15]. Since the wired NoC works well for near-destined packet and considering the overhead cost of fabricating a wireless node (wireless interconnect and transceiver circuits), few wireless nodes are sufficient to improve the network performance significantly and reduces the congestions at even higher injection rates.

One more advantage of wireless is, obviously, it is wireless. No wired interconnect is required to transfer data from one chip to another. The fact that different data transfer protocols are used at different interfaces, so data is converted into specific blocks corresponding to interfaces which increase the delay and complexity. But with direct wireless links, complexity and delay will reduce. This will increase the performance, and save the chip space of CMOS devices.

The wireless interconnects can also be extended further to transmit to the neighboring chips as inter-chip communications. There are many purposes and applications for inter-chip communication. This communication will require a large bandwidth to support high data rates.

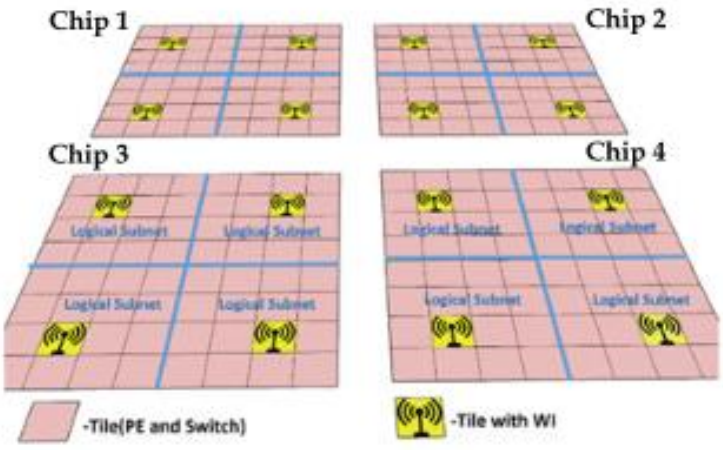


Figure 1-4. Conceptual diagram of wireless multichip system [15].

High-speed communications require a large bandwidth. Federal Communications Commission (FCC) has allocated an unlicensed 57-64GHz band [16] with greater than 100MHz band channels in the USA. This millimeter-wave (mmWave) frequency band is commonly known as 60 GHz frequency band, since it is centered around 60 GHz. This allocation made possible the realization of ultrahigh-speed communication systems. Moreover, the range of frequency helps design an antenna of very small size (of micrometer dimensions) which is feasible for fabricating antenna on the chip. In this way, small wireless interconnects for WiNoC can be implemented on semiconductor devices.

Since the transmission of 60 GHz band is used for a short distance with a maximum of 10 meters. Moreover, the 60 GHz band cannot even penetrate concrete walls. It has a high attenuation rate in the atmosphere. All the above-mentioned reasons are going to decrease the chances of spoofing (unauthorized access using wireless protocols), thereby increasing security. Another advantage is the fabrication process of AoC is compatible with existing CMOS technology. The antennas are easily fabricated using standard process technology used by the semiconductor industry today.

Many wireless technologies like MIMO systems, beam steering, etc. can be implemented to further use advanced wireless technologies. This creates an opportunity for researchers to investigate the ways to connect chips wirelessly.

1.3 Related work on antennas on a chip

The research on the antenna on-chip (AoC) is going on for more than two decades now. One of the earliest implementations was the planar microstrip antenna array [17] in 1986. It was implemented with a 95GHz oscillator circuit on a very high resistivity substrate (ρ=10kΩ-cm).

Later in 2000, AoC was implemented to demonstrate the idea of wireless clock distribution in digital integrated circuits [18].

Recently published book chapter [19] and article [20] on AoC provide good references. There has been research on the topic of antenna-on-chip (AoC). Different types of antennas are analyzed like a dipole antenna, meander, zigzag, loop, patch, Yagi, and bow-tie antennas. Kenneth K.O and his students have studied planar dipole antennas on a silicon chip [21][22]. Their research has been limited to lower than 20GHz. They have shown the operation of the antenna at microwave regime lower than 10GHz.

A form of zigzag dipole antenna shown in Figure 1-5 (b) is provided in [21]. Figure 1-6 shows the design of the dipole antenna and substrate cross-section. This antenna showed promising results for being an omnidirectional antenna at 15 GHz. Above shown dipole antenna is modified into a monopole [22] with long sleeves for ground shown in Figure 1-7. This antenna was tested at a frequency centered around 6 GHz. Despite little change in the radiation pattern of the monopole, its performance is similar to the dipole. Moreover, the monopole antenna takes less space than the dipole antenna shown above.

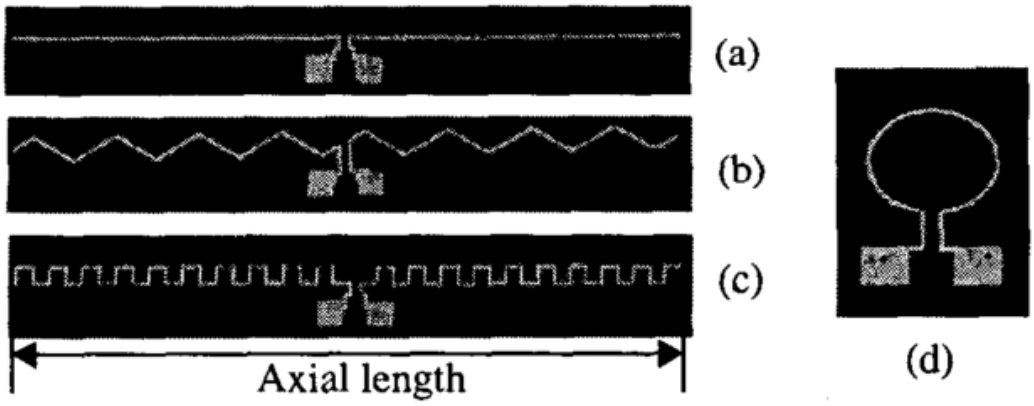


Figure 1-5. Antenna on chip [21] (a) Dipole (b) Zigzag (c) Meander (d) Loop. Axial length=2mm.

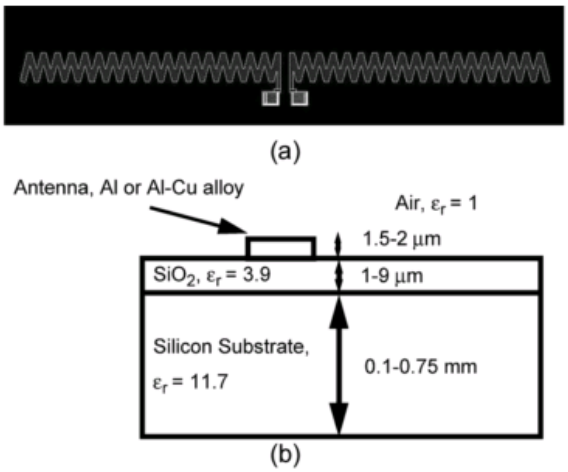


Figure 1-7. (a) Zigzag antenna on silicon wafer [22], (b) Cross-section of silicon wafer.

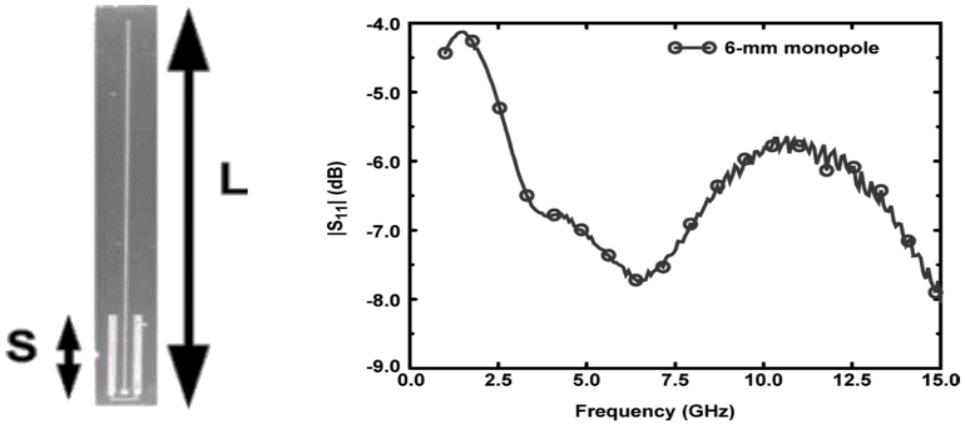


Figure 1-6. (a) Monopole antenna on chip with long sleeves [22], (b) S11 of antenna in part (a).

All aforementioned antennas do not include feed but excited by GSG probes. A zigzag antenna with coplanar waveguide (CPW) feed was designed in [22]. It is shown in Figure 1-8. The reason for choosing CPW feed is its lower loss at high frequencies. Moreover, the CPW feed can be easily fabricated on a single layer without a bottom ground plane, unlike microstrip feed. The zigzag antenna is optimized and simulated to work at 60GHz. It was simulated in ANSYS HFSS. Modified zigzag antenna is designed to excite the zigzag antenna using a CPW feed. This antenna is a monopole antenna.

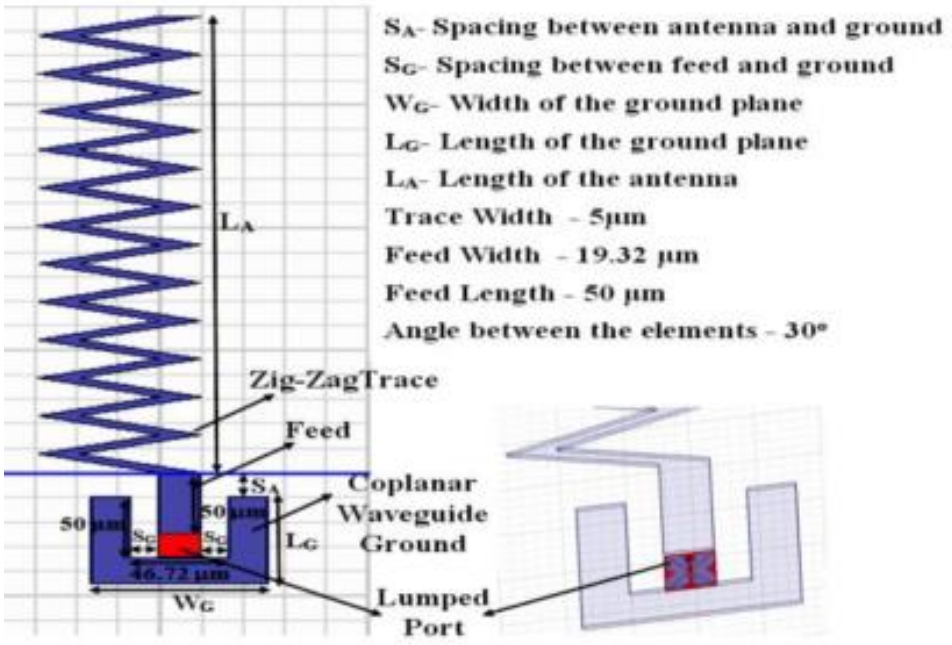
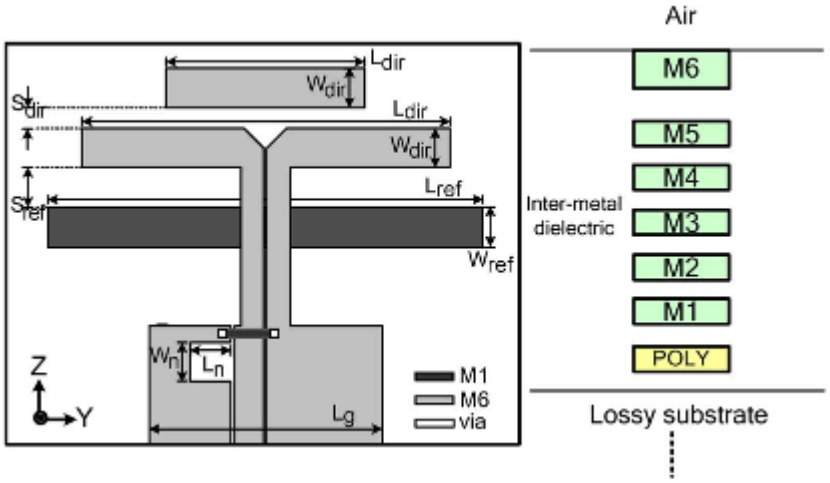
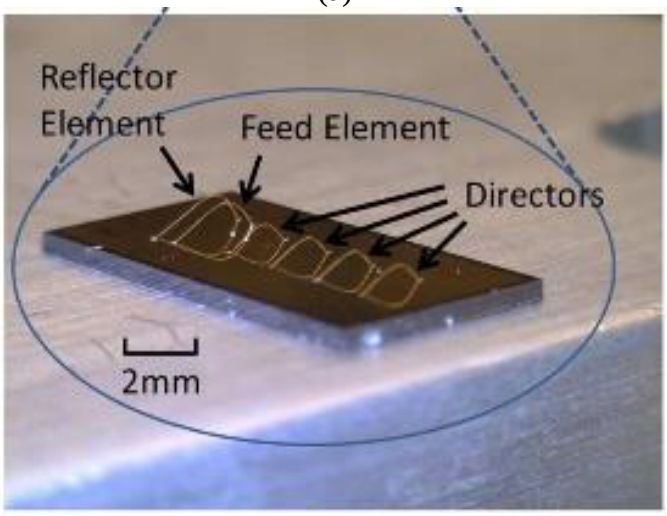


Figure 1-8: CPW-fed zigzag antenna [23].

A bow-tie antenna is also developed as AoC for high resistive silicon to increase the operating bandwidth [24]. The simulated operating frequency of the antenna is from 51GHz to 100GHz with a radiation efficiency of about 20%. Another version of a bow-tie antenna is designed for a BiCMOS process for RFID and other sensor application [25]. Moreover, Yagi antenna is analyzed for a directional radiation pattern. First, Zhang and his team have designed a planar quasi-Yagi antenna with two directors and a truncated ground plane as the reflector with operating frequency around 60GHz [26]. The resistivity of silicon selected is 10Ω-cm, therefore the radiation efficiencies are 6%. Later, Hsu, et al. have redesigned Yagi antenna in multi-BEOL layer form [27]. Antenna designed by is Hsu, et al is working around 60GHz. It can be excited by a CPW feed as shown in Figure 1-9 (a). Moreover, they have considered lossy silicon substrate, so the simulated radiation efficiency of the antenna is 10% with a front-to-back ratio of 9dB and max. gain of -8dB. A Yagi-Uda antenna [28] is also manufactured using the bond-wire connecting the PCB and the



(a)



(b)

Figure 1-9. Quasi-Yagi antenna with a CPW feed designed by Hsu, et al. [27], (b) Yagi-uda antenna made by the bond-wires for on-chip radio applications [28].

high-resistivity SiGe CMOS chip as shown in Figure 1-9 (b). The antenna is resonating at 35GHz with S_{11} below -10dB.

Various modification of the fabrication process has been implemented to improve the radiation efficiency of the on-chip antenna. Some of the modifications are:

- Use of proton implantation [29],[30] to increase the resistivity of silicon, thereby improving the radiation efficiency of AoC.

- Substrate thinning: This process involves the trimming of the substrate to reduce the losses incurring in the substrate [31].
- Using artificial magnetic conductor (AMC): Fabricating special structures which reduce the image current generated by the bottom ground plane. These special structures are artificial magnetic conductor (AMC) [32].
- Use of superstrate or dielectric resonator to improve antenna efficiency [33].
- Micromachining the antenna structures with precision [34].

Some of the modifications like substrate thinning, superstrate are not compatible with the CMOS processes. In a later chapter, preliminary work has been performed to include AMC with a zigzag antenna to analyze the improvement in transmission between the antennas.

1.4 Research objective and contribution

The objective and contribution of this work are described as follows:

A. **Intra- and inter-chip transmission between wireless interconnects in a realistic chip package consisting of on-chip wires:** The first objective is to find the transmission coefficients between on-chip antennas for intra-chip and inter-chip communication in old (wire-bonded) and modern (flip-chip) packages. This work is discussed in chapter 2. The wireless interconnects implemented using on-chip antennas are designed in HFSS and fabricated at Semiconductor and Microelectronics Fabrication Laboratory (SMFL), RIT. The intra- and inter-chip transmission between the wireless interconnects implemented as antennas on-chip are simulated and measured. Also, a channel model has been presented based on the measurements between wireless interconnects. The on-chip metallic wires in processors have been modeled and

simplified for simulation purposes. The transmission between wireless interconnect, which are implemented as on-chip antennas, in the presence of wires and other metallic structure is simulated. The transmission between wireless interconnects implemented in a flip-chip package has been simulated.

B. **Implementation of beamforming using antenna arrays on-chip:** Another objective is to design antenna arrays for beamforming using the zigzag antennas. The antenna arrays are discussed in chapter 3. The antennas arrays are designed using zigzag antennas using ANSYS HFSS. Proper feed networks are designed to provide the antenna elements with the appropriate phase for beamforming. The antenna arrays are placed at the edge of the chip as discussed in chapter 3. Fabrication of antenna arrays is performed at the RIT SMFL cleanroom. The antenna arrays on the chip are measured using the Keysight network analyzer and probe station. The results like transmission coefficients between array pairs from simulation and measurement are shown and analyzed. Moreover, the radiation pattern and electric field density are also plotted to show the beamforming in desired directions. These results would be helpful to design the link budget for a transceiver system.

C. **Transmission enhancement using artificial magnetic conductors (AMC):** The final contribution of the work is the implementation of on-chip metasurface like artificial magnetic conductors which is known in the research community to enhance antenna properties like efficiency. Artificial magnetic conductors (AMCs) are also designed and simulated to enhance the transmission between the antennas on the chip. The results are discussed in chapter 4. It is shown that the artificial magnetic conductors are enhancing the transmission coefficients between antenna pairs. Moreover, the

challenges of using the AMC for enhancing the transmission between antennas are also discussed.

1.5 Societal and technological impacts

Today the world is moving towards cloud computing, artificial intelligent systems, machine learning, and other technologies that require enormous data processing power. The data processing for these technologies occurs remotely at datacenters. These remote centers use computing technologies that are based on MCMC systems for parallel processing. This research is focused on increasing the data transfer between cores of the MCMC system using wireless node. Recent research has shown significant improvement in data throughput when using a few wireless nodes placed between cores in the MCMC system [15]. This on-chip wireless interconnect technology can be implemented as a near-term solution to improve the processing performance in parallel processing systems.

This research would help implement wireless interconnects that are needed to cope with the challenges of processing power in datacenters. By improving the capabilities of datacenters, the cloud services that use those datacenters such as web applications, scientific simulations and computations, Internet of Things, virtual reality (VR) technologies, and others would become much better. Ultimately, the general public would experience an enhanced performance of technologies like virtual reality, augmented reality, and driverless vehicles. This improvement would in turn benefit the students in the field of education, scientists who are in research, the engineers who are designing new virtual models of various machines and megastructures, mechanics who may use the virtual technology to fix and understand problems, and much more. Furthermore, it would enhance the capabilities of artificial intelligence that has found new applications in social media (fact-checking), et al.

2 Intra- and Inter-chip Transmission in NoC based multichip systems

2.1 Introduction

Network-on-chip is the solution to the problem of complex wiring between different blocks and processing cores of a processor. However, when the number of blocks and cores increases, the network-on-chip starts to get congested and causes delays to transfer the data [12]. Recent research has shown that this problem can be solved by using a few wireless nodes which are scattered across the chip as shown in Figure 1-4 [15]. The latency of the data packet reduces significantly which improves the parallel processing. Moreover, these wireless nodes can also be used to communicate with other chips on the board. Here, the communication between wireless nodes located in a chip is labeled as intra-chip communication and when the communication is occurring between the nodes located in different chips, it is labeled as inter-chip communication.

In this chapter, a study has been performed to establish transmission between wireless nodes located at each quadrant of a chip, moreover, a four chip system is used to analyze a multicore multichip system. Easy to design zigzag antennas, which have a small footprint and omnidirectional pattern, are used for simulation purposes. All simulations are performed in ANSYS HFSS. Furthermore, transmission analysis is performed to understand the behavior of on-chip antennas in a complex, modern flip-chip package.

2.1.1 Related work on transmission analysis and channel modeling

The research to analyze the transmission between on-chip antennas is on-going since the last decade. Work is performed by Dr. Zhang and his students to analyze the performance of inter-

chip transmission for 23GHz to 25GHz [35]. Later they have also performed work for intra-chip transmission channels [36][37]. They have shown that the dominant component for intra-chip transmission is surface waves. Another work, performed by Redfield, et al. [38], has modeled the channel inside a computer chassis as shown in Figure 2-1. They have taken measurements with the standard components inside a computer chassis.

Furthermore, Kikkawa [39] has provided the simulated and measured transmissions for on-chip dipole antennas designed to work at 3.5GHz. A picture of the Kikkawa's model along with the result is shown in Figure 2-2. In [40], A channel model at mmWave frequency band 57-64GHz has been generated using measurements between antennas inside a metal box. A work on channel model has also been performed inside a server chassis at the unlicensed mmWave band 57-64GHz [41]. In [42], Matolak et al. have theoretically discussed the challenges involved in channel

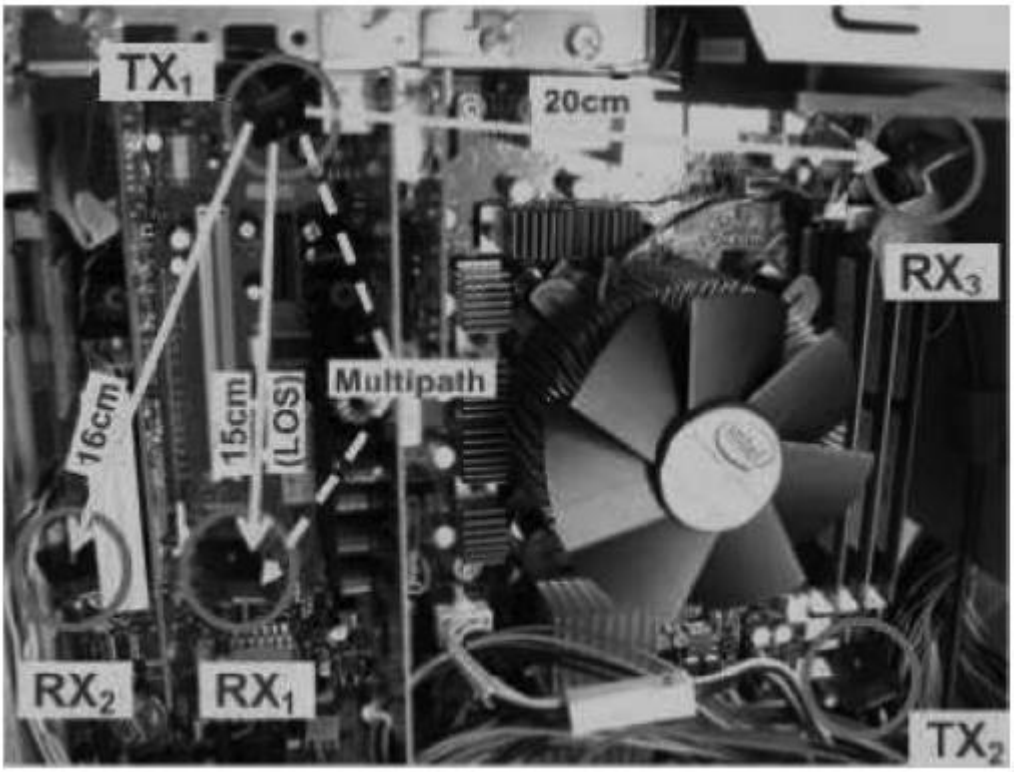


Figure 2-1. The communication scenario analyzed by Redfield, et al. [38].

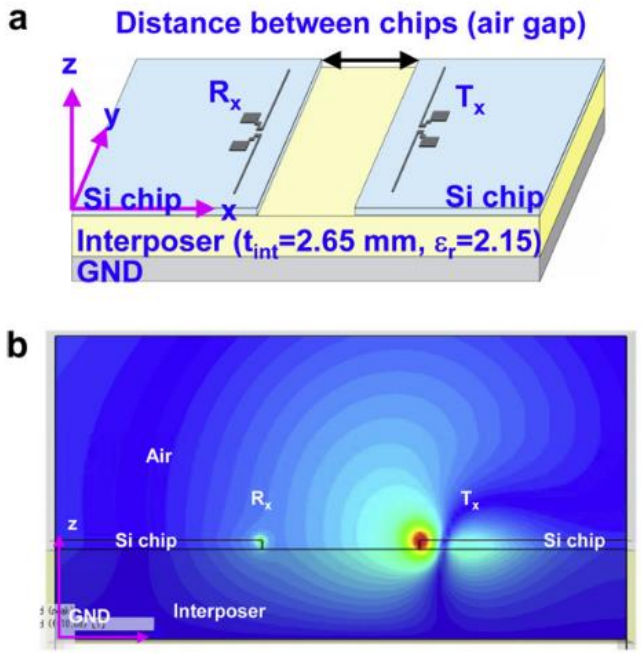
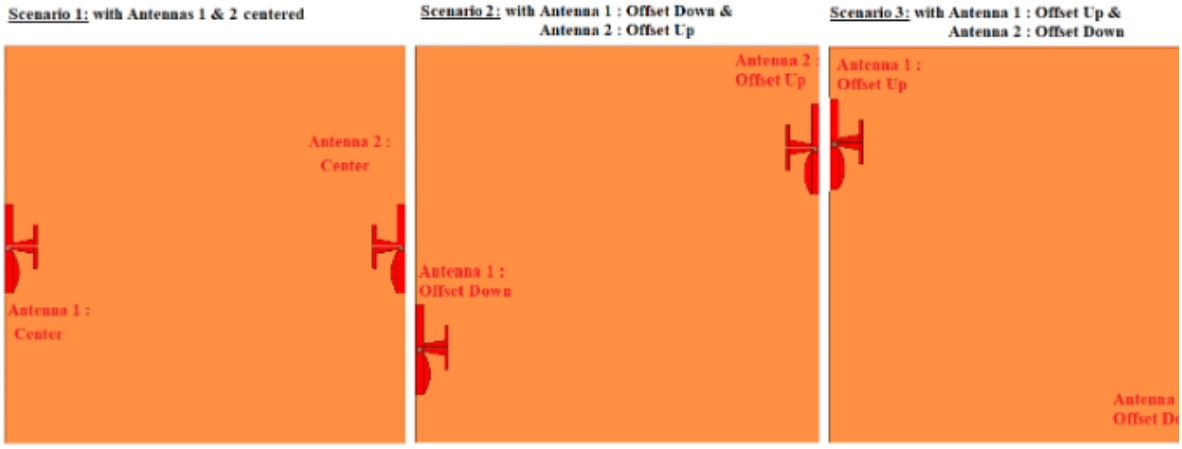


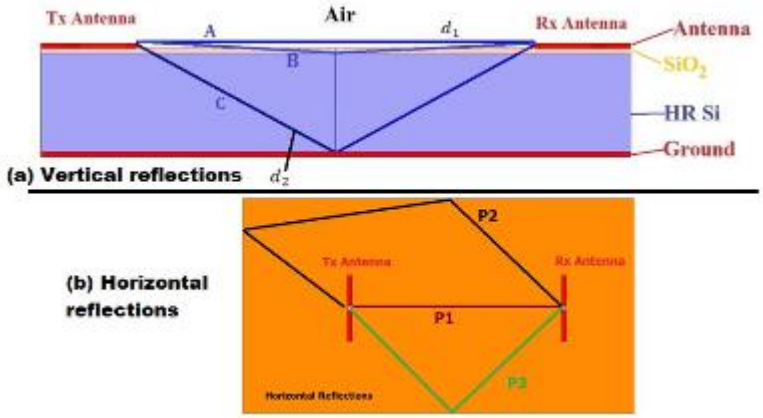
Figure 2-2. Inter-chip transmission analysis between AoCs fabricated on silicon which is placed on an interposer materials [39].

modeling for wireless network-on-chip which involves intra-chip communication. Moreover, they have further worked to design an antenna just above the passivation layer [43]. This is extra overhead, however, it may help to improve the transmission.

Recently, work is performed by Gade, Ram, and Deb [44] on channel modeling using folded dipole antenna and log-periodic antenna, but this work is based on simulations which are performed in CST Microwave studio. Another recently published work has focused on WiNoC and intra-chip transmission [45]. This work is conducted with measurements at Ka-band (26-40GHz) and V-band (40-75GHz) with different scenarios and placement of antennas as shown in Figure 2-3, however, the work is performed on high-resistive silicon. Though it involves the ground plane at the bottom, this work does not take into account the PCB board and, the metal wires which can also affect the propagation between the wireless interconnects.



(a)



(b)

Figure 2-3: (a) Scenarios and antennas considered by Masri, et al. [45]. (b) Reflections of the EM wave from different obstacles and ground plane.

2.1.2 Design of antenna configurations for multi-chip systems

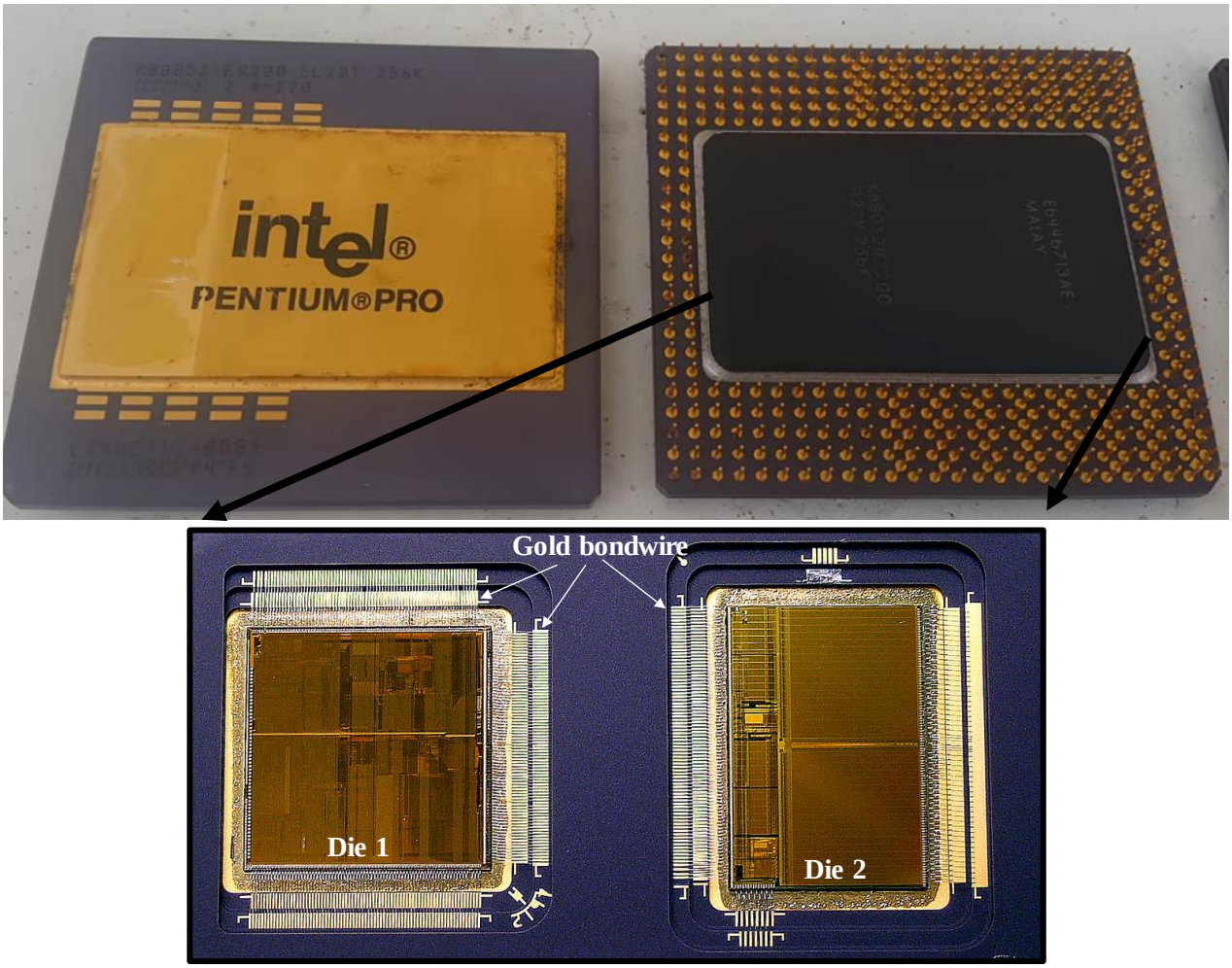
The on-chip antenna has to provide the best power gain for the smallest area overhead. Several on-chip antenna designs in the mmWave bands such as, linear dipoles, patch antennas and log-periodic antennas have been investigated. Our choice of the zigzag antenna for this paper, is based on its small footprint and its omnidirectional pattern [46], which allows for easy placement and ability to communicate with other chips at various orientations. Moreover, a sufficiently omnidirectional antenna can also enable broadcast among the wireless nodes in the platform, which is greatly beneficial for handling broadcast or multicast messages to maintain memory or cache coherency protocols and status updates [47]. For this reason, we do not adopt beam-forming

antenna arrays, which are the common focus for mmWave systems in other application areas such as 5G communications [48]. In addition, such mmWave antennas, which are fabricated using top layer metals of CMOS processes, are suitable for near-term solutions to the wired interconnect problem compared to other alternatives like Graphene or Carbon Nanotube (CNT) based antennas, although they might operate at higher frequencies [49]. Due to these reasons, we have, here, designed mmWave zigzag on-chip antennas and their co-planar waveguide feed structure to resonate in the mmWave frequencies such as 30GHz and 60GHz. Next, we discuss the objective of our work.

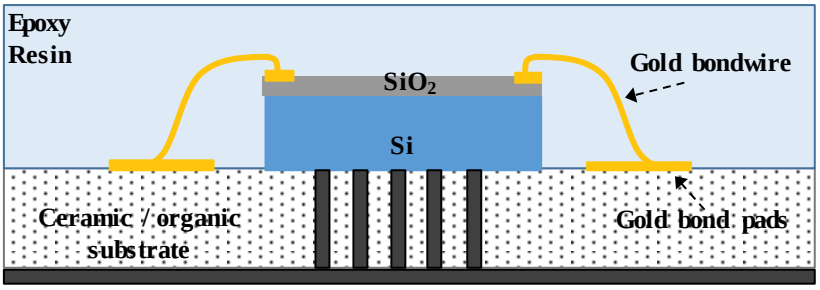
2.1.3 Objective of chapter

The objective of this chapter is to study the transmission coefficients between on-chip antennas in a chip package. There are two types of chip packages which are considered in this chapter: first, a wire-bonded package, generally found in older processors, and secondly a flip-chip package that is used in modern processors. It was used in Intel Pentium Pro 140 and others. As an example, a top view of the Intel Pentium Pro processor is shown in Figure 2-4. This package is not only an example of a wire-bonded package but also an early form of a multichip module (MCM). Moreover, a generic side view of a wire-bonded package is shown in Figure 2-4 (b). Later on this chapter, this environment is used for simulation of wireless interconnects because of its simplicity.

Further in the chapter flip-chip package is also used for simulations. However, the flip-chip package is more complicated in design and simulations due to the use of C4 solder balls (or microbumps). Due to the limitations of readily-available equipment, first, the simulation and measurement are performed in a wire-bonded package with zigzag antennas around 30GHz. Using



(a)



(b)

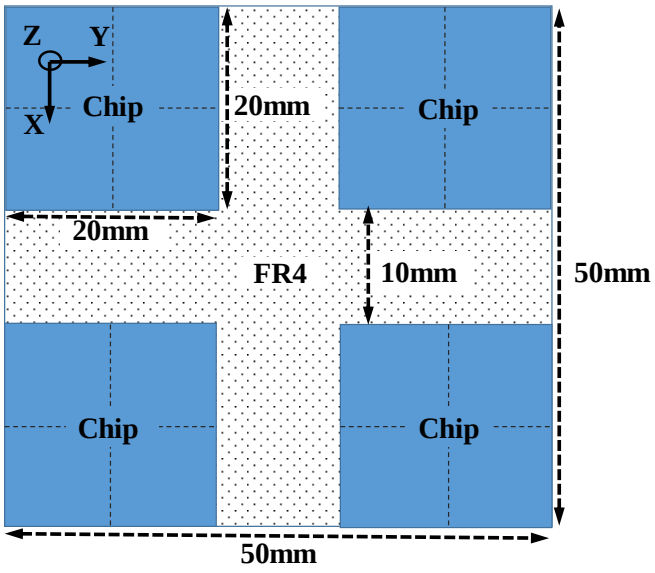
Figure 2-4: Wire-bonded processor package: (a) Intel Pentium Pro chip package (front and back) along with inset view showing thin gold wire bonding [51][52], (b) generic view of cross-section of the chip[50] (Figure not to scale).

the measurement data, a channel model is created for use in the future. Further, simulation of antenna and analysis of transmission is performed in the wire-bonded package along with the metal wires in BEOL layers. The metal wires are explained in more detail later. In the next section, simulations of wireless interconnects as zigzag antennas are performed in a simple wire-bonded package.

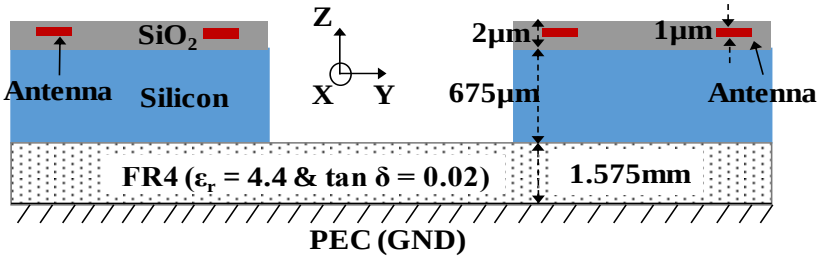
2.2 Simulation of on-chip zigzag antenna in multi-chip systems at 30GHz

In this section, the design and simulation of on-chip antennas in the multi-chip system are discussed. The on-chip antennas are designed and optimized in ANSYS High Frequency Structure Simulator (HFSS). The simulation of silicon chips with on-chip antennas operating at 30 GHz is performed in a multi-chip system environment. The simulation setup consists of four silicon chips with typical dimensions of 20mm x 20mm placed on top of an organic substrate (FR4 - ε_r = 4.4, tan(δ) = 0.02) of thickness 1.575mm. Each chip is equally divided into four quadrants as seen in the layout shown in Figure 2-5 (a). A cross-sectional view is also shown in Figure 2-5 (b).

The chips are made of silicon (ε_r = 11.7 & ρ = 55Ω-cm) with thickness 675µm. A 2µm thick silicon-dioxide SiO_2 (ε_r = 3.4) layer is considered above the silicon. A Perfect Electric Conductor (PEC) boundary at the bottom of the organic substrate is considered for simulation purpose to emulate the effect of ground plane. Furthermore, the design of the on-chip antenna should be small compact and low-profile for implementing on or inside the silicon-dioxide layer. The design of on-chip antenna is shown in Figure 2-6(a). It is a single metal (aluminum) layer zig-zag antenna so it can be fabricated on a silicon chip using conventional CMOS-based fabrication process. Also, it should be noted that the epoxy resin is not used here as seen in the cross-section view, because the dielectric constant is low, and it will be easier to measure these antennas when fabricated.

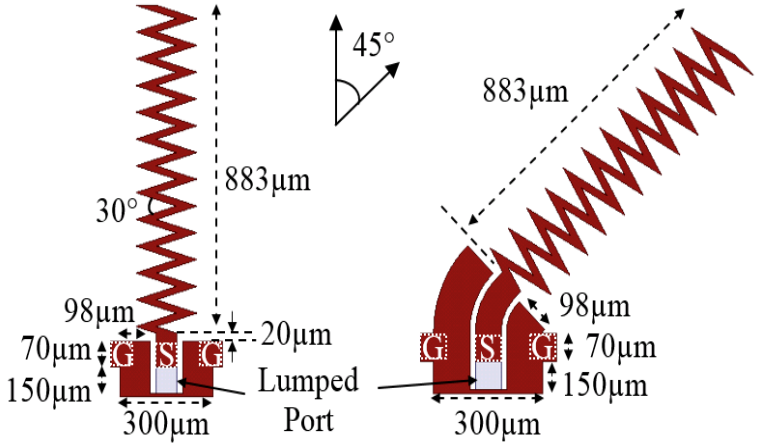


(a)



(b)

Figure 2-5. (a) Top view of the multi-chip system. (b) Cross section of multi-chip system setup. Note: Figures are not to scale.



(a) (b)

Figure 2-6. On-chip antennas operating at 30 GHz. (a) Orientation 1 (O1), (b) Orientation 2 (O2). The width of the signal trace is 70µm.

The on-chip antenna is 883µm long for operations at 30GHz. The thickness of the aluminum layer is 1µm. The antennas are modified to include probe pads to use Ground-Signal-Ground (GSG) probes for measurement. Cascade ACP40-A is used in the next subsection as the GSG probe. They have a pitch of 150µm and a minimum pad size requirement of 50µm. So, a probe pad of size 70µm x 70µm with a pitch of 150µm are designed and shown in Figure 2-6. The width of the signal trace is 70µm. For simulation purpose, HFSS lumped port is used for exciting the CPW feed of the on-chip antennas

Moreover, another on-chip antenna configuration is designed which is rotated 45° as compared to the previous antenna and is shown in Figure 2-6 (b). The first one is orientation 1 (O1) and the latter is orientation 2 (O2). The reason of the two different orientations is to study the effect of orientation on the transmission between on-chip antennas. For O2, the bend in the feed line shown in Figure 2-6 (b) is to accommodate the movement of GSG probes in the measurement system which is constrained to only linear three-dimensional motion. Next, the on-chip antennas are placed at the center of each quadrant in the silicon chips. Three configurations (Conf) of the silicon chips are designed using the two different orientations of on-chip antennas. The arrangements of on-chip antennas on a chip are shown in Figure 2-7, and labeled as Conf 1, Conf 2, and Conf 3. Conf 1, which is shown in Figure 2-7 (a), has antennas parallel to each other. Conf 2 and Conf 3 are shown in Figure 2-7 (b) and Figure 2-7 (c), respectively. Conf 2 and Conf 3 have antennas positioned similar to Conf 1 but are rotated 45° away from and towards the center of the chip, respectively. We use these three configurations to study the impact of antenna orientations, the ground plane, and FR4 substrate on transmission characteristics between the on-chip antennas.

It should be noted that all the on-chip antennas are located in the far-field region of each other. The far-field boundary is considered to be at a distance of $\lambda/2\pi$ from antenna [53], which, at

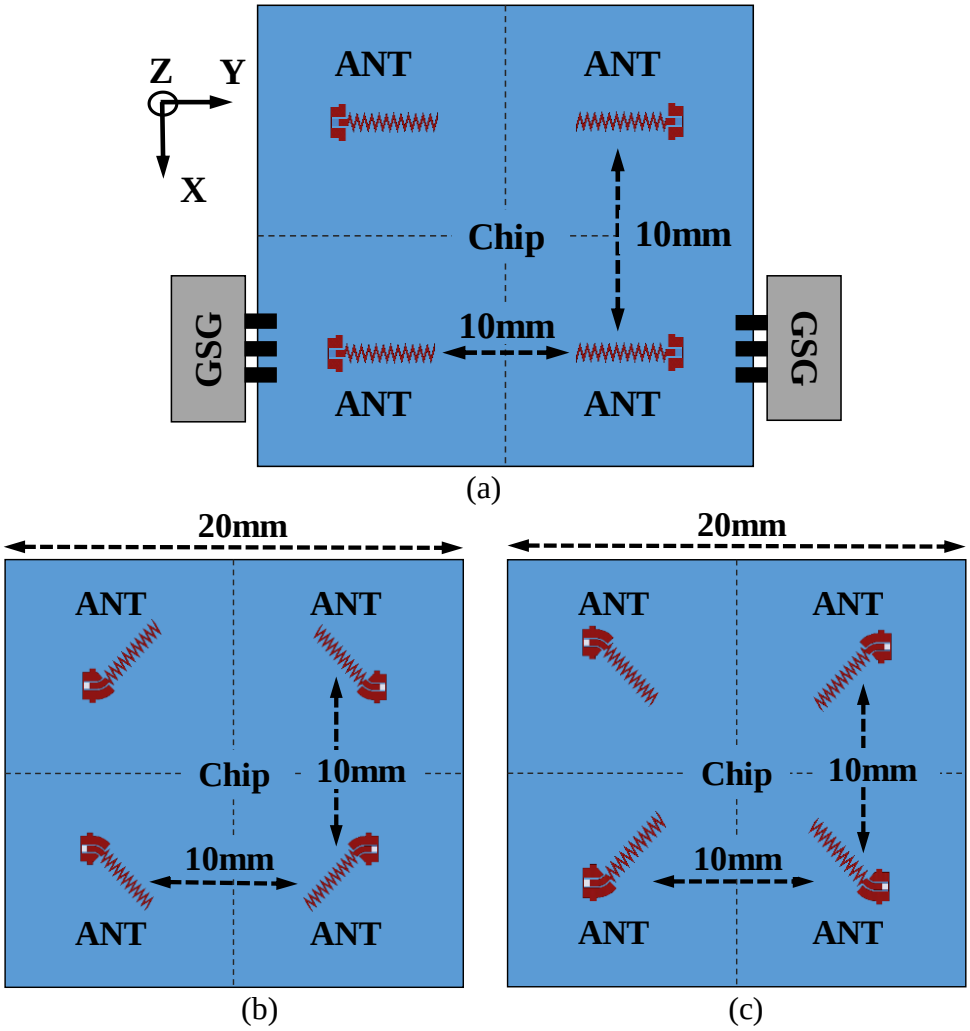


Figure 2-7. Silicon chips with antennas (ANT) in MCMC system. (a) Configuration (Conf) 1, (b) Configuration 2, and (c) Configuration 3. Note: (i) Figures are not to scale. Antennas are enlarged to show the orientations. (ii) The antennas are placed at the center of the quadrant.

30GHz corresponds to 1.6mm in free space. In our layout, the minimum distance between antennas in the chip is 10 mm as shown in Figure 2-8, therefore, all on-chip antennas are placed in the far-field region. For the simulation model, four chips of the same configuration are placed in a multi-chip system on top of the FR4 board as shown in Figure 2-5 (a). For each such arrangement corresponding to the three configurations, simulation is performed using ANSYS HFSS.

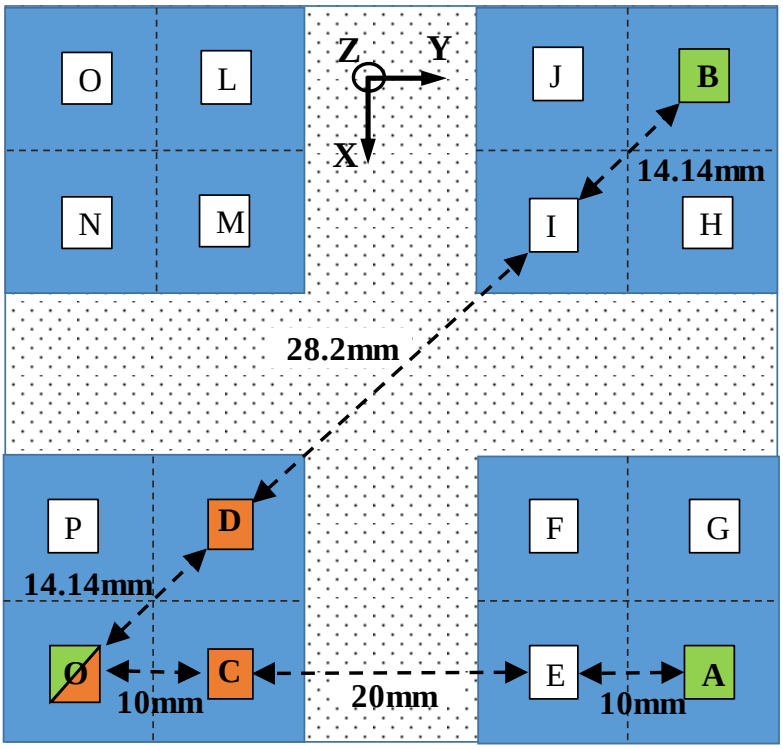


Figure 2-8. Top view of multi-chip system showing the placement of antennas under investigation. Note: (i) Figures are not to scale. Antennas are enlarged to show the orientations. (ii) The antennas are placed at the center of the quadrant, (iii) Antenna O is considered as reference for the analysis of transmission coefficients. All distances are from center-to-center of the antennas.

The on-chip antennas are optimized to have a reflection coefficient (S_{11}) of below -15dB at 30GHz shown in Figure 2-9. For each configuration, the reflection coefficient (S_{11}) is shown for only one antenna since all four are identical. The simulated radiation efficiency of zig-zag antenna is 15% for all configurations. For transmission coefficients, there are numerous combinations of antenna pairs. So, to make the discussion tractable, only five antennas are considered as shown in Figure 2-8. These antennas are selected because they include the expected worst cases that is, farthest antenna pairs for intra- and inter-chip pairs (A, B, C and D from O). All transmissions for 30GHz frequency in this paper are measured relative to common ANT O. The simulated transmission coefficients for inter-chip communication are shown in Figure 2-10 (a), and intra-chip communication are shown in Figure 2-10 (b).

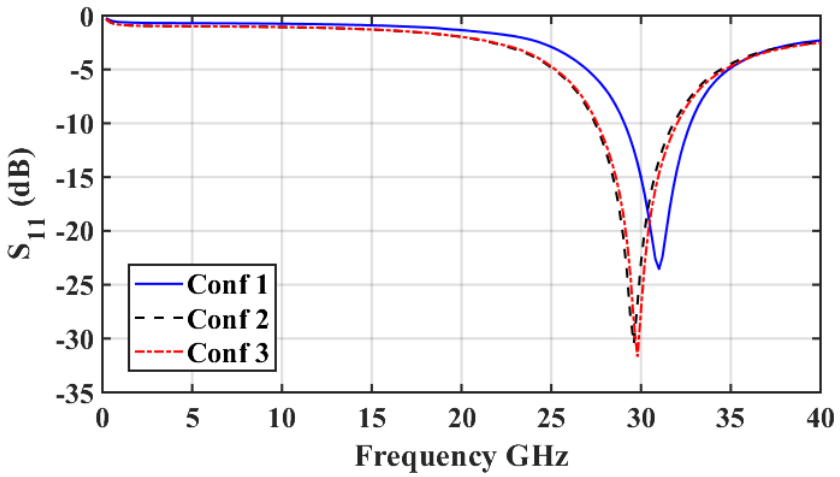
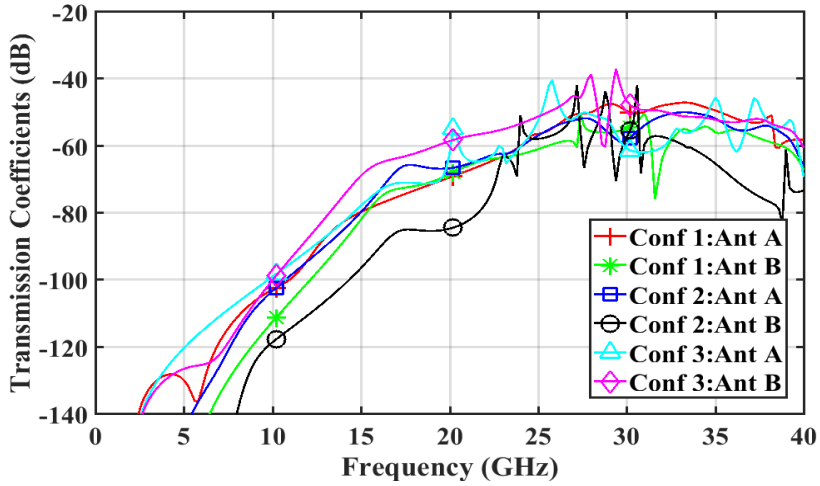
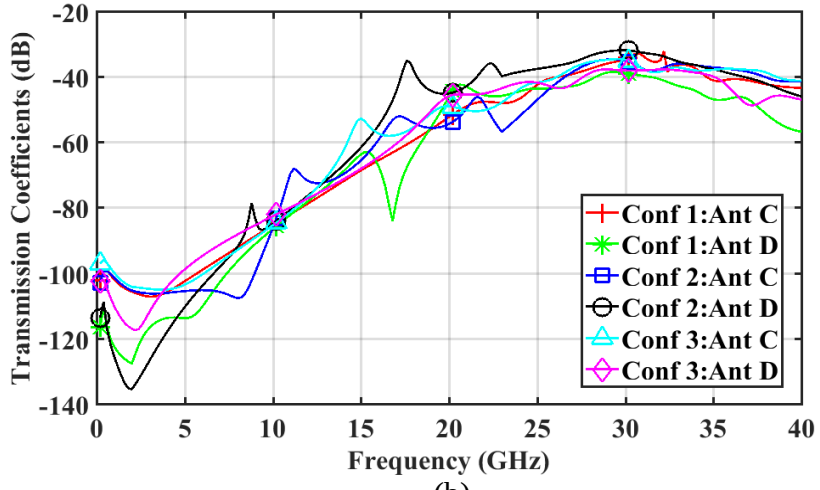


Figure 2-9. S_{11} of the antennas in all configurations.



(a)



(b)

Figure 2-10. Transmission coefficients. (a) Inter-chip scenario, (b) Intra-chip scenario.

It is seen that the intra-chip transmission at 30GHz, varies from -31dB to -38dB, and inter-chip transmission varies from -46 to -60dB, which is expected since the distance between the antennas has increased in the latter case. Moreover, in Figure 2-10 (a) at 30GHz, the transmission between antennas A & O and antennas B & O in Conf 3 is -60.68dB and -46.5dB, even though the distance between antennas A & O is smaller than that between antennas B & O. This is due to the structure of the multi-chip system and the interference caused by the reflected multi-path propagations from the ground [54]. Also, Figure 2-11 shows the simulated magnitude of the electric field along the line connecting ANT O & ANT A and ANT O & ANT B. Since, the path between these antenna pairs passes through the metal trace of other antennas such as ANT C (at 9mm on blue trace), ANT E (at 29mm on blue trace) and ANT A (at 38mm on blue trace), the discontinuities in the electric field are seen in the plot.

We can further observe that the field distribution varies across the structure. To investigate this further, we study the magnitude of the electric field distribution, shown in Figure 2-12(a) to Figure 2-12(c) for all three configurations in the plane of antenna (surface of silicon-dioxide) and cross-section plane containing antennas O and A at 30GHz. The field distribution depends on -

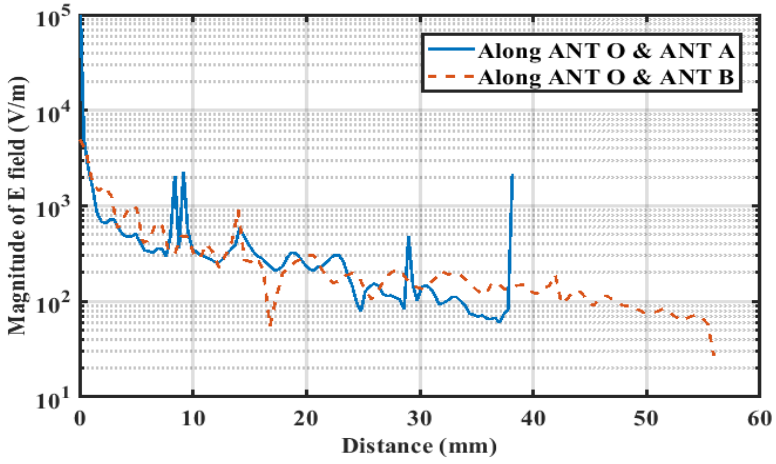


Figure 2-11. Magnitude of electric field (V/m) along the line connecting ANT O and ANT A & ANT O and ANT B (only ANT O is excited) in Conf 1. Antenna Arrangement is shown in Figure 2-8.

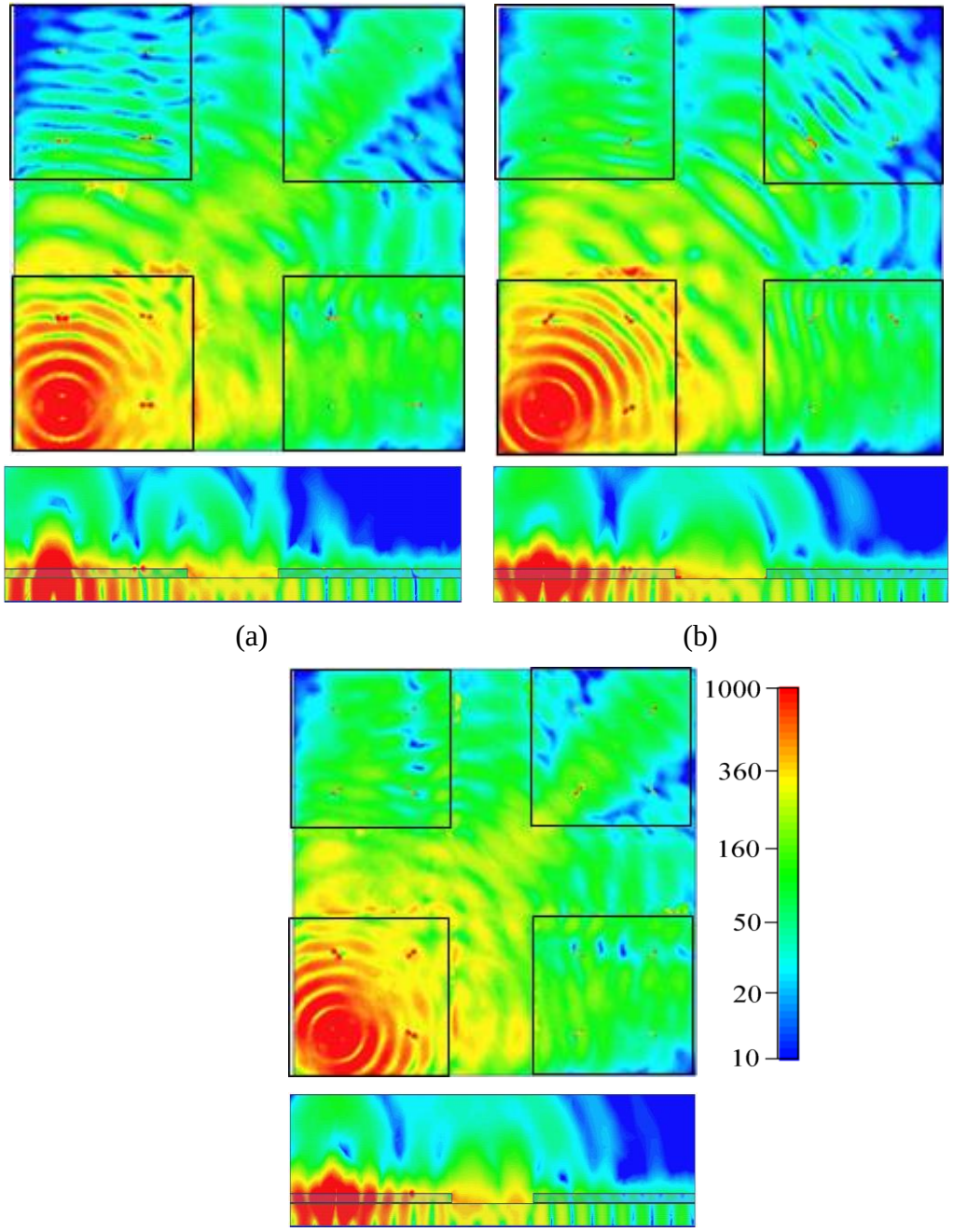


Figure 2-12. Magnitude of electric field (V/m) distribution on the surface of silicon and cross-section view across ANT O and ANT A when ANT O is excited at 30GHz. (a) Configuration 1, (b) Configuration 2 and (c) Configuration 3 as shown in Figure 2-7.

structure, geometry, the material used, and the operating frequency. In Figure 2-12 (c), the low intensity of field distribution can be noticed at the position of antenna A. This is the reason for the fluctuations in the transmissions between antennas. The distribution of field in Conf 2 and Conf 3 is different for ANT B, therefore the transmission between ANT B & O is better for Conf 3.

Furthermore, as confirmed by [36], the dominant way of propagation in intra-chip propagation is surface waves. This can be seen in the cross-sectional view of the structure in Figure 2-12 where high magnitudes of field distribution are on the surface of the chip where the on-chip antenna is excited. Another observation from the electric field plots in Figure 2-12 is the diffractions of waves at the edges, which can significantly increase the multi-path effect. If directional on-chip antennas or on-chip phased array for inter-chip communication are used, then these edge diffractions might cause the beam to distort which may reduce the gain. Moreover, as the field propagates to other chips, the low-intensity regions become significant, which can be observed in Figure 2-12. This shows that the expected omnidirectional radiation of the zigzag antenna is distorted due to structures, geometry, and materials of the setup. Therefore, the analysis of field distribution needs to be considered while placing on-chip antennas for data communication between chips in the multi-chip systems.

Furthermore, a study is performed with changing the resistivity of silicon to analyze the change in S_{11} of the antennas in Conf 1. The previous simulations are performed for various resistivities of silicon 10Ω-cm, 20Ω-cm, and 1000Ω-cm. The S_{11} for one antenna for different resistivities is compared with the S_{11} of the antenna with 55 Ω-cm in Figure 2-13. It can be seen from the plot that the antenna is resonating at about the same frequency, however, the magnitude of S_{11} is increasing as the resistivity is decreasing. Further, analysis is performed in terms of the radiation efficiency of the antennas. Table 1 is shown where it can be noticed that the radiation

efficiency of the antenna significantly depends on the silicon resistivity. As the resistivity of silicon decreased the radiation efficiency reduced. At 10Ω-cm, the standard resistivity of silicon used in processor chip, the radiation efficiency dropped to about 0.2% despite S_{11} of about -10dB at 30GHz.

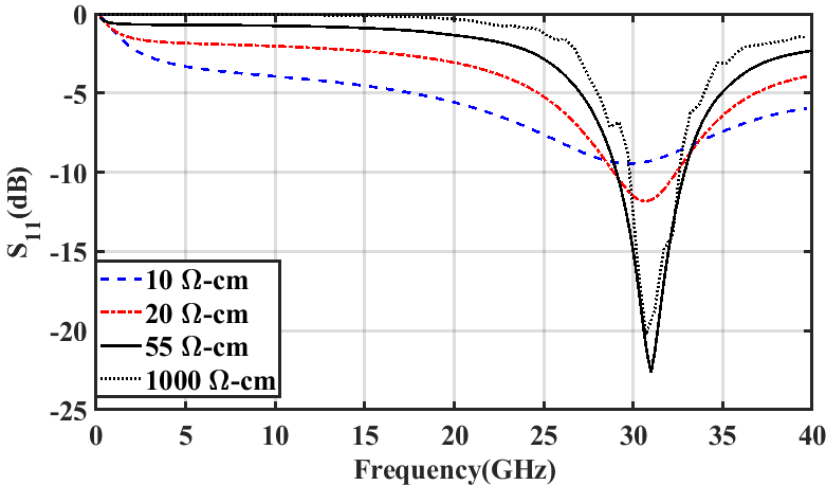


Figure 2-13. Magnitude of S_{11} of on-chip antenna for Conf 1 for different resistivity of silicon.

Table 1: Radiation Efficiency of on-chip antenna for Conf 1 for different resistivity of silicon.

Silicon Bulk Resistivity (Ω-cm)	10	20	55	1000
Simulated Radiation Efficiency at 30GHz (in %)	0.2	1	15	30

In the next section, the simulated antennas are fabricated on a 55Ω-cm silicon wafer. The fabrication process along with measurement procedure is discussed.

2.3 Fabrication & measurements of on-chip antennas

The discussion in this section is divided in two different subsections: (a) fabrication of antennas, and (b) measurement of antennas.

2.3.1 Fabrication of on-chip antennas

The fabrication of antennas is performed at Semiconductor and Microelectronics Fabrication Laboratory (SMFL), RIT. A 6-inch p-type (100) silicon wafer of thickness 675µm and resistivity of 55 Ω-cm was used. The resistivity of silicon is verified by a 4-point probe method. The steps of fabrication of the on-chip antenna are shown in a flowchart in Figure 2-14. The first step in the fabrication process involves wafer cleaning using the RCA cleaning method. Next, a 2µm layer of oxide is grown using a wet oxidation method in a Bruce Thermal Furnace. After growing the

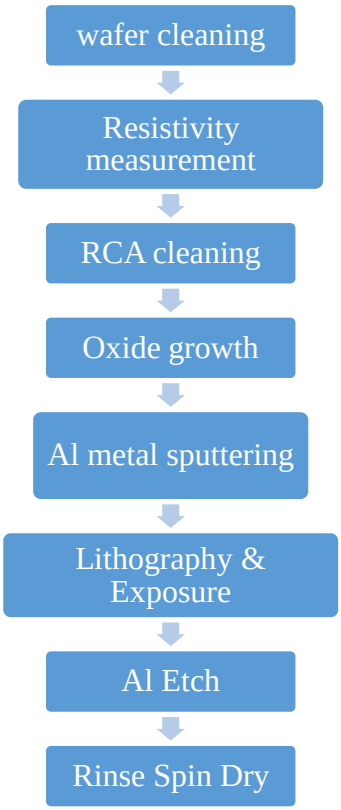


Figure 2-14. CMOS fabrication steps [55].

silicon-dioxide, the thickness of the oxide layer is confirmed using a Prometrix SM200 SpectraMap reflectometer. The aluminum is then deposited via a sputter deposition process in a CVC 601 Sputter. After aluminum deposition, a layer of photoresist is applied on the wafer using an automated SSI Track, and the shape of the antenna is defined through a 1x contact-lithography

process with a Karl-Suss MA150 Aligner. After the photoresist development process, aluminum is etched using a chlorine-based dry etch process, in a Lam 490 Plasma Etch, to ensure the needed resolution and sharpness of the antenna features. A picture of wafer with aluminum antennas is shown in Figure 2-15.

Lastly, the wafer is cut into 20mm x 20mm dies using a KS780 Dicing Saw. These silicon dies are used to make a multi-chip arrangement. Microscopic pictures of antennas are shown in Figure 2-16. In the next section, procedures of measurement & characterization of these antennas are discussed along with the measured results.

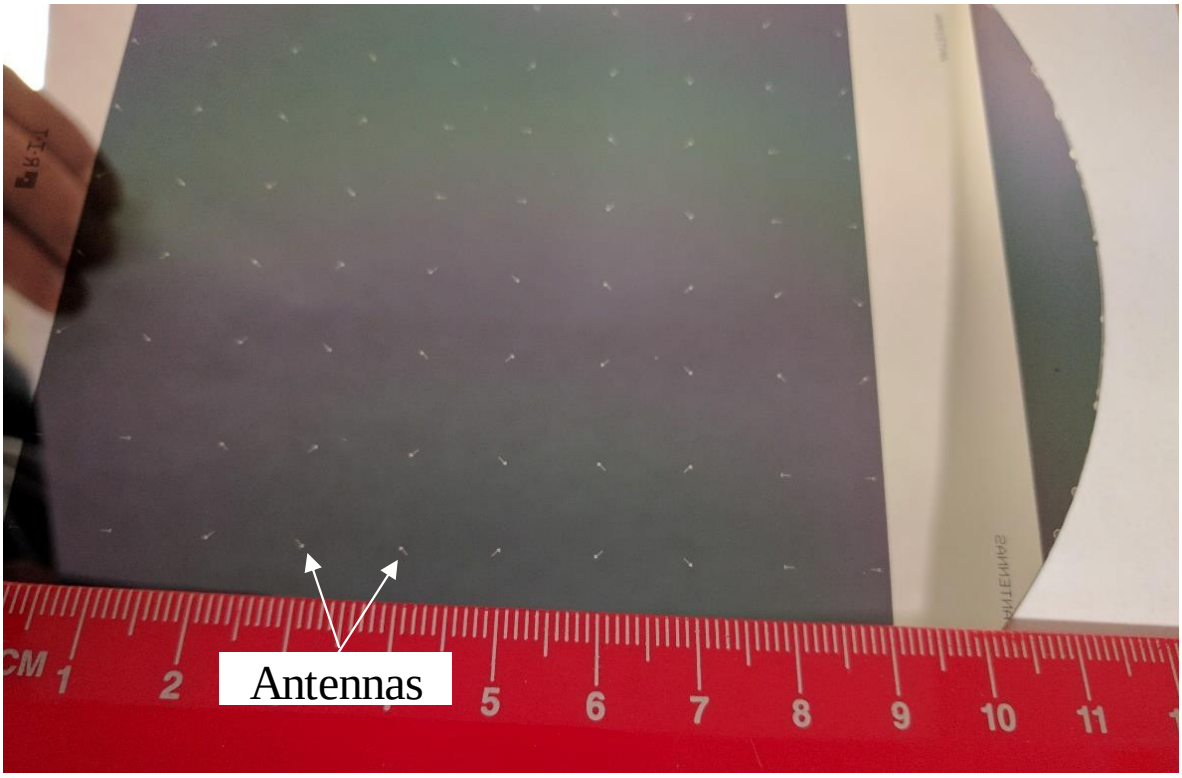
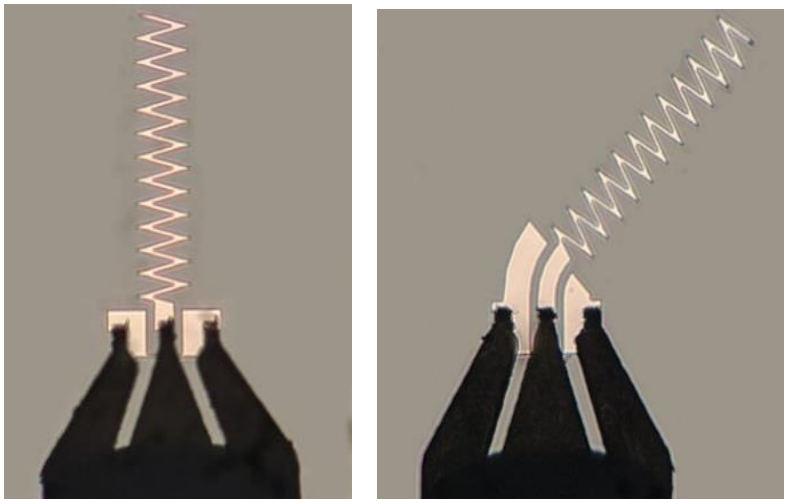


Figure 2-15. Picture of silicon wafer with fabricated antennas.



(a) (b)

Figure 2-16. Micrograph of fabricated antennas on silicon, (a) an antenna from a Conf 1 die, (b) an antenna from a Conf 2 die.

2.3.2 Measurement & characterization of on-chip mmWave antennas

In this section, the measurement procedure and challenges in measurements are discussed. Cascade Summit 9000 probe station along with Agilent 8363B vector network analyzer (VNA) is used for testing of the fabricated antennas. The measurement setup is shown in Figure 2-17. The VNA is calibrated from 1GHz to 40GHz using Short-Open-Load-Thru (SOLT) method with Cascade impedance standard substrate (P/N: 106-682). The IF bandwidth is set to 5kHz to increase the dynamic range of VNA, and reduce the noise in measurements. Also, each measurement is further repeated 10 times to average out the noise. As mentioned in section IV, a Cascade ACP40-A are used as GSG contact probes. They have a pitch of 150µm and minimum pad size requirement of 50µm. Also, the simulation design shown in Figure 2-5 has a ground plane. This ground plane is not fabricated on silicon wafer, rather the metal chuck of the probe station is emulating the effect of ground plane.

Using the measurement setup, first the reflection coefficient (S_{11}) of fabricated antennas in different configurations is measured. It should be noted that the reflection coefficient (S_{11}) of all

on-chip antennas in a configuration is same due to same design, therefore, only one trace of reflection coefficient (S_{11}) from each of the three configurations is shown in Figure 2-18. The reflection coefficient (S_{11}) shows that the fabricated antennas resonate at 25GHz with a S_{11} magnitude of -10dB to -12dB. However, the simulated reflection coefficient (S_{11}) of antennas in all configuration shows the resonant frequency to be around 30GHz as indicated in Figure 2-9. In order to investigate the reasons for this shift in resonant frequency between the simulated and fabricated antennas we modeled the probe structure to study its impact on the resonant frequency.

The 3-dimensional probe model, shown in Figure 2-19, has been created from US Patent no. 5506515 by Cascade [56] in conjunction with many dimensional measurements and microscopic pictures of the probe from various perspectives. The probe is excited by a HFSS lumped port at the k-connector. The S_{11} of the antenna, when simulated in the presence of the probe, is seen in Figure 2-20 to reduce by about 1.5GHz. The SOLT calibration that we adopted in our measurements, is also seen to introduce additional measurement discrepancies between the

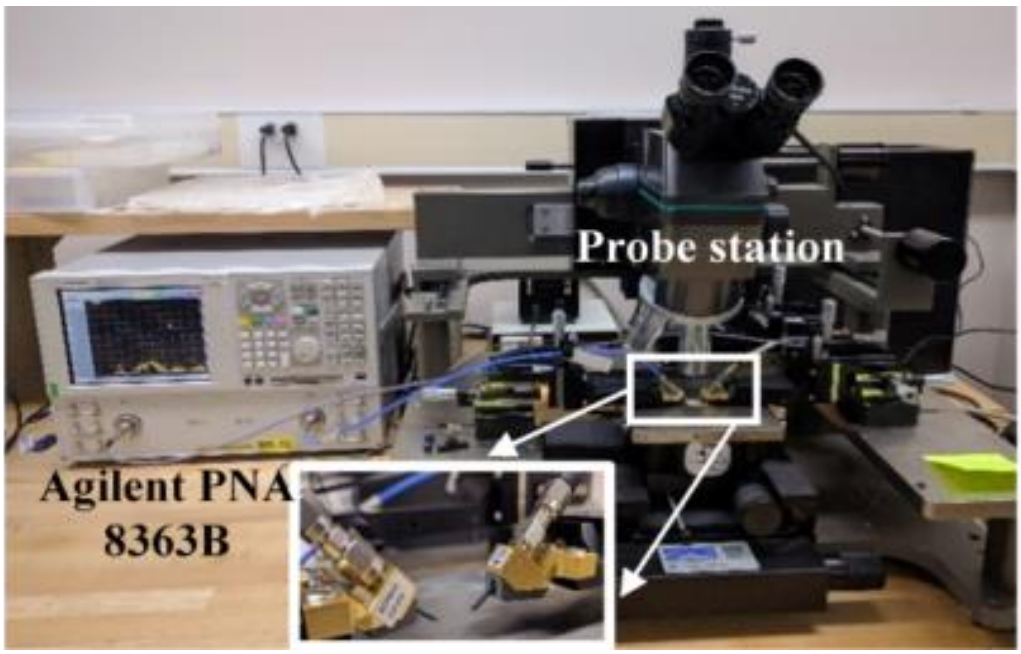


Figure 2-17. Measurement setup.

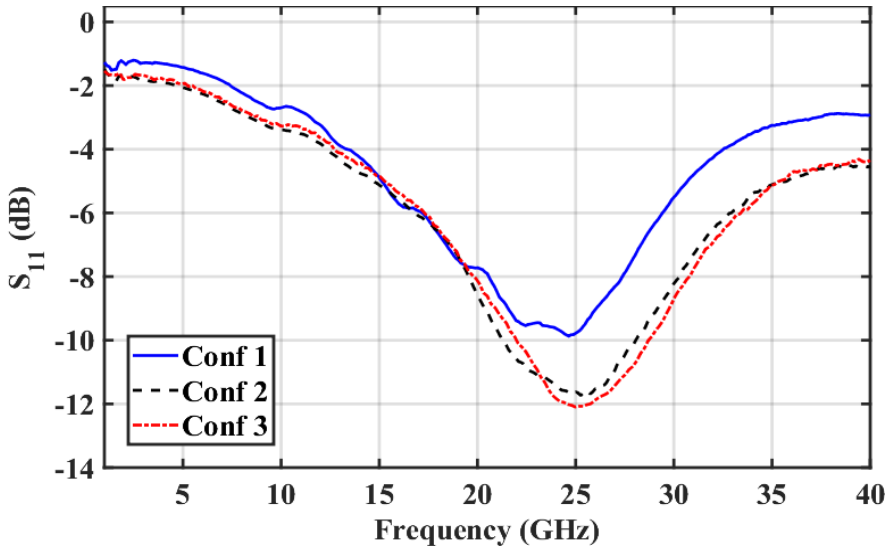


Figure 2-18. S_{11} of the antenna in all three configuration.

probe tip and the antenna feed structure [57]. These discrepancies vary between specific probes and Device-Under Test (DUT). Some other challenges related to the measurement of mm-wave antennas are reviewed in [58]. Therefore, typically at mm-wave frequencies, a few fabrication iterations are necessary to match simulation with measured results. Furthermore, it can be also noticed that the slightly longer feed in Conf 2 and Conf 3 provides a better match as can be inferred from the simulated reflection coefficient in Fig.4, where it is about 2dB lower than Conf 1.

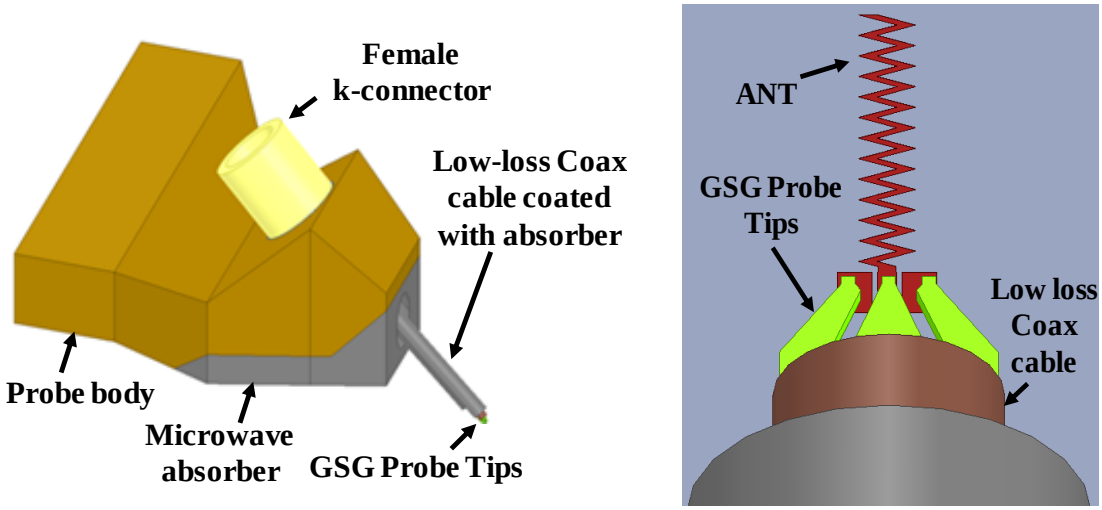


Figure 2-19. Cascade GSG probe modeled in HFSS and close-up top view of one of the zigzag antennas of Conf 1 with GSG probe on its contact pads simulated in HFSS.

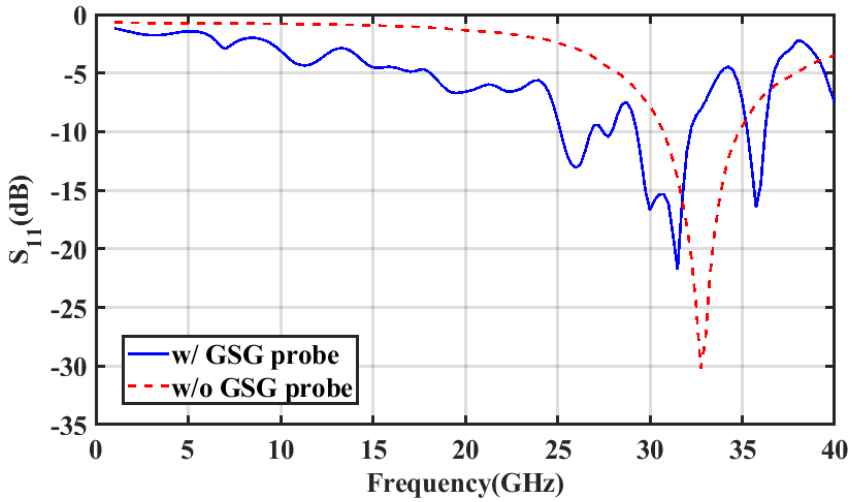
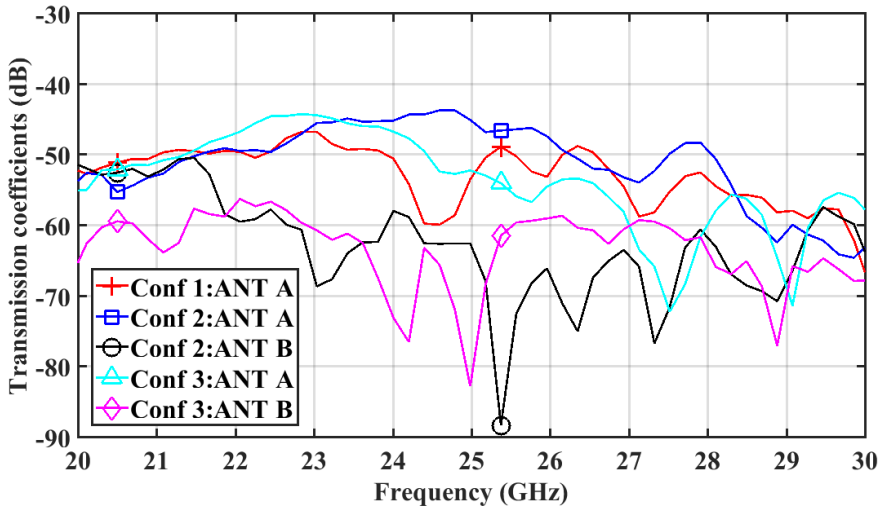


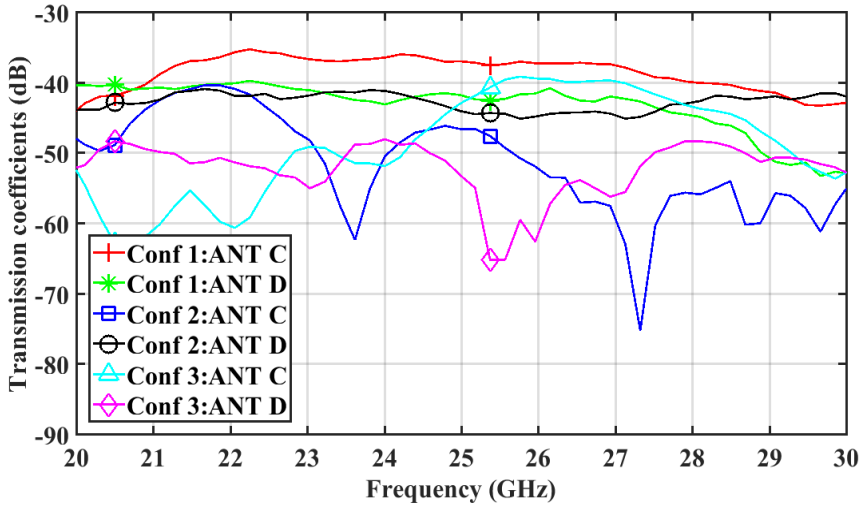
Figure 2-20. Simulated S11 of on-chip antenna with and without probe.

Also, the -10dB bandwidth of the fabricated antennas in Conf 2 and Conf 3 are about 6.5GHz. Here, fabricated antennas in Conf 1 have a reflection coefficient higher than -10dB, so in this case, 7dB bandwidth is considered which comes out to be about 10GHz. Furthermore, transmission coefficients (S_{21}) between ANT O and other antennas ANT A, B, C & D in all configurations in the multi-chip system are measured between 20GHz to 30GHz and plotted in Figure 2-21 when the chip boundaries are 10mm apart. Transmission between ANT B and ANT O in Conf 1 cannot be measured due to constraints in the movement of probe arms. All the measurements show that there is sufficient transmission between antenna pairs which varies from -35dB to -60dB at resonant frequency 25GHz. For intra-chip transmission, ANT C & ANT O in Conf 1 as shown in Figure 2-21 (b) has a maximum transmission. As expected, the intra-chip transmissions are more than the inter-chip transmission by about 10dB. Similar to the simulations, antenna B in Conf 2 and 3 shows dips in transmissions from 20 to 30GHz frequency intervals due to low field distribution.

The transmission measurements with respect to ANT O also show that some antennas like Conf 3:ANT D, Conf 2:ANT B, and Conf 3:ANT B have dips around the resonant frequency of 25GHz. These dips in transmissions are the result of multi-paths involved in propagation. This shows that the reflection from the ground plane and the structure of chip changes the transmission due to reflections.



(a)



(b)

Figure 2-21. Transmission coefficients (S_{21}) for ANT A & B (a), and ANT C & D (b) relative to ANT O in all configuration when the distance between chip is 10 mm. Note: ANT B in configuration 1 is not measured due to constraint in movement of probe arms.

2.3.3 Challenges in fabrication and measurement of antennas

The millimeter-wave antennas are challenging to fabricate and characterize accurately [58][59][60]. An illustration collecting the significance, challenges, and solution is shown in Figure 2-22. There are various parameters and materials involved in fabrication and measurements.

- To design a millimeter-wave antenna, good modeling of material or substrate is required. The material characterization at millimeter-wave frequency is not readily available. Most of the companies provide accurate characterization till 10GHz. There are few publications able in the literature which have characterized some of the material properties at millimeter-wave frequencies. One of that publication is [62], however, it is difficult to cross-verify these measurements.
- Simulation software also possesses another challenge when working with millimeter-wave frequencies. Knowledge of meshing is required to accurately simulate the small mmWave antenna on the thin multi-layer structure.

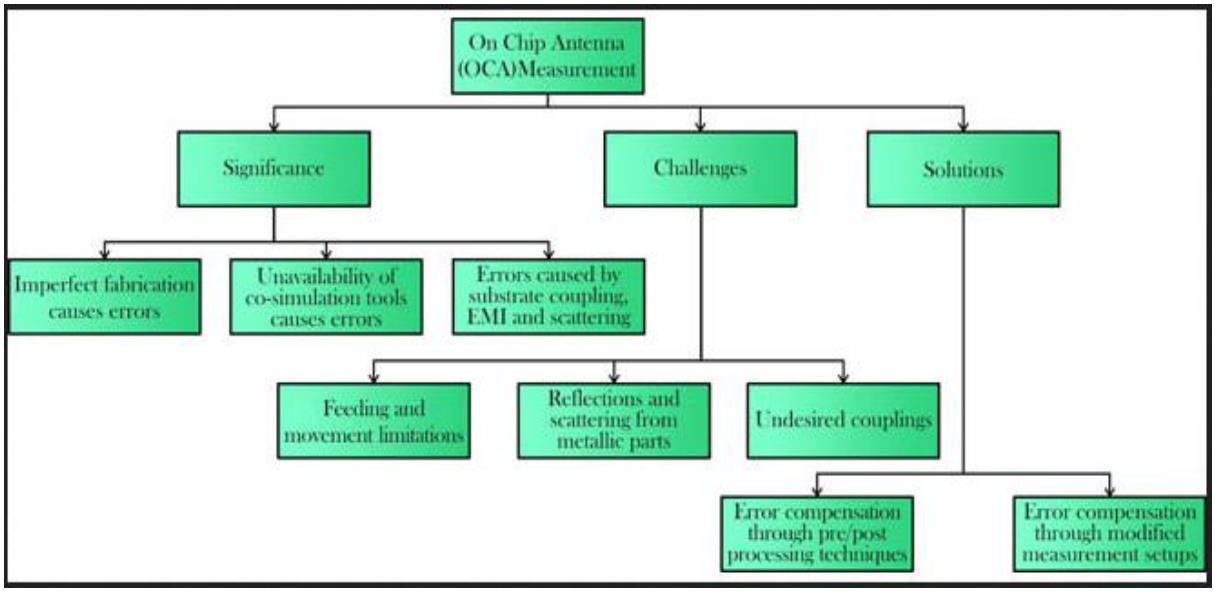


Figure 2-22. On-chip antenna measurement – significance, challenges and solutions. Graphical abstract of [59].

- Accuracy of measuring instruments when dealing with the on-chip antenna. It is important to increase the input power levels and the IF bandwidth for the measurement. This improves the received signal strength.
- Also, calibration methodologies cause errors [57]. Thru-Reflect-Line (TRL) is found to be better than the SOLT method.
- GSG probes may affect the measurement. The probe is quite near to the antenna-under-test this affects the radiation and scattering properties of the antenna [60][59].
- Above 100GHz, the probes themselves starts to radiate, therefore to match the simulations and measurement results, the simulations should include the measurement probes [61].
- Measurement in a flip-chip environment: In modern processors, the flip-chip environment is used as a package. Measuring on-chip antenna in such a complicated and small environment is difficult. Because the antennas need to be flipped on a substrate, this makes the placement of GSG probes complicated.
- Another issue may be the effect of high temperatures on the on-chip metal antennas. Processor chips generally heat up quickly due to the heat generated by the thin high resistive metal wires. These high temperatures may expand the metal antenna thereby slightly decreasing the resonance frequency. Antenna measurements should be taken with silicon chip placed on a hot plate probe station to better understand the effects.

2.4 Large-scale channel model for inter-chip communication in multi-chip systems

In this section, we derive parameters of large-scale channel modeling for inter-chip wireless communication links, which can be used to evaluate path losses for inter-chip communication systems. Large-scale channel model is required to predict the required transmit

power for specific SNR of the received signal in a communication system. This will enable the development of design rules for transceiver circuits and overall interconnection architecture regarding antenna placement and orientation. Generally, the large-scale channel according to the log-normal model [63] is given by:

$$PL(d)|_{dB} = PL(d_0)|_{dB} + n \times 10\log_{10}\left(\frac{d}{d_0}\right) + X_\sigma \quad (1)$$

where $PL(d)|_{dB}$ is the average path loss at a distance d relative to path loss $PL(d_0)|_{dB}$ at a close-in reference distance d_0, n represents the path-loss exponent, and X_σ is a zero-mean Gaussian random variable with standard deviation σ denoting the attenuation (in dB) caused by shadowing. For channel modeling, we have chosen a frequency range from 20GHz to 30GHz based on the operating range of the antennas. The VNA is calibrated in this frequency range. This range is ultra-wideband (UWB), so the channel characteristics are a function of frequency and distance between antennas. Therefore, the average transmission across the frequency range is used to find channel characteristics as a function of distance [64]. Furthermore, the reflection coefficients (S_{11} and S_{22}) of antennas is about -10dB. So, to remove the losses due to the reflection from the antenna, the measured transmission coefficients, S_{21}, are processed using the transmission coefficient, G_a:

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (2)$$

In our model, G_a is used as a path loss between the antennas. Moreover, the channel under investigation for the multi-chip system is considered as a time-invariant due to the absence of relative motion between the chips in a multi-chip system.

Generally, for indoor and outdoor environments large-scale channel models indicate the path loss in the channel only, so, it should not depend on the antenna or the transmitted power

level. Unlike in free space, where the simplicity of Friis' equation to evaluate a reference path loss can be used, inter-chip channel modeling depends on the on-chip antennas. The fabricated on-chip antennas are not in a free-space environment and the rigid structure of the fabricated on-chip antenna adds constraints to performing measurements. In this way, the channel model becomes dependent on antenna design and the structure of the chip. Therefore, for inter-chip channel modeling, we measure the transmission between antennas at a specific distance (or shortest distance possible) and use that as a reference in (1). In this paper, the reference distance (d_0) between fabricated antennas ANT A and ANT O is considered to be 40mm by placing the chips 10mm apart. For ANT B and ANT O, the reference distance is 42.42mm by placing chips adjacent to each other that is zero millimeter apart.

As discussed in the previous section, the multi-chip systems use a substrate which, in our case, is an organic substrate, namely FR4. The fabricated silicon chips are mounted on top of the FR4 substrate. Here, FR4 substrate has no ground plane of its own so the metal chuck of probe station would work as the ground plane. The arrangement of chips on FR4 along with probes is shown in Figure 2-23. A pair of antennas are identified on two different chips. Keeping the distance between the two antennas constant, the chip pair is moved to different locations on the FR4 board and corresponding inter-chip transmission measurements are made. A sequence of measurements are made for different distances between the chips and hence the antennas. After these measurements are post-processed with (2), the measured average path loss as a function of distance between the antennas is plotted and shown in Figure 2-24(a). Inter-chip transmission measurements are restricted to a distance of 75mm between the antennas due to the size of metal chuck of the probe station. Curve-fitting is performed on the measured average path loss to extract parameters required for modeling by (1). The derived model parameters are shown in Table 2. The

measured path loss model shows that the path loss exponent in case of inter-chip transmissions is close to 2, which is the path loss exponent for free space. This suggests that dominant propagation path is free space in inter-chip communication.

Moreover, the variation in path loss as the pair of chips are placed in different locations on the FR4 substrate is modeled by X_σ. The probability density function (PDF) for modeling X_σ based on experimental measurements is shown in Figure 2-24 (b). As can be seen, the path loss variation is restricted to -2dB to +2dB around the model estimate. However, the standard deviation is a maximum of 1.3dB while in most cases it is less than 1dB signifying low shadowing effects at the antenna locations. The case of maximum standard deviation is for ANT B and ANT O in Conf 2. With the parameters provided in Table 2, the path loss model from (1) can be used to measure the path loss at other distances between similar antennas in similar multi-chip systems. A similar methodology can be adopted for channel modeling at other mmWave frequencies such as 60GHz. This analysis will be useful in estimating path loss and establishing link budget for specific architectures depending on antenna orientations placement.

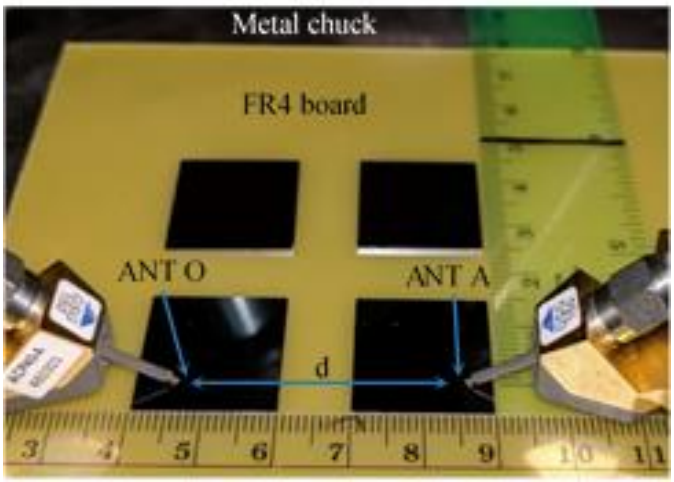


Figure 2-23. Measurement setup for path loss measurement. The silicon chips are placed on FR4 board at different distances. *d* is the distance between antennas.

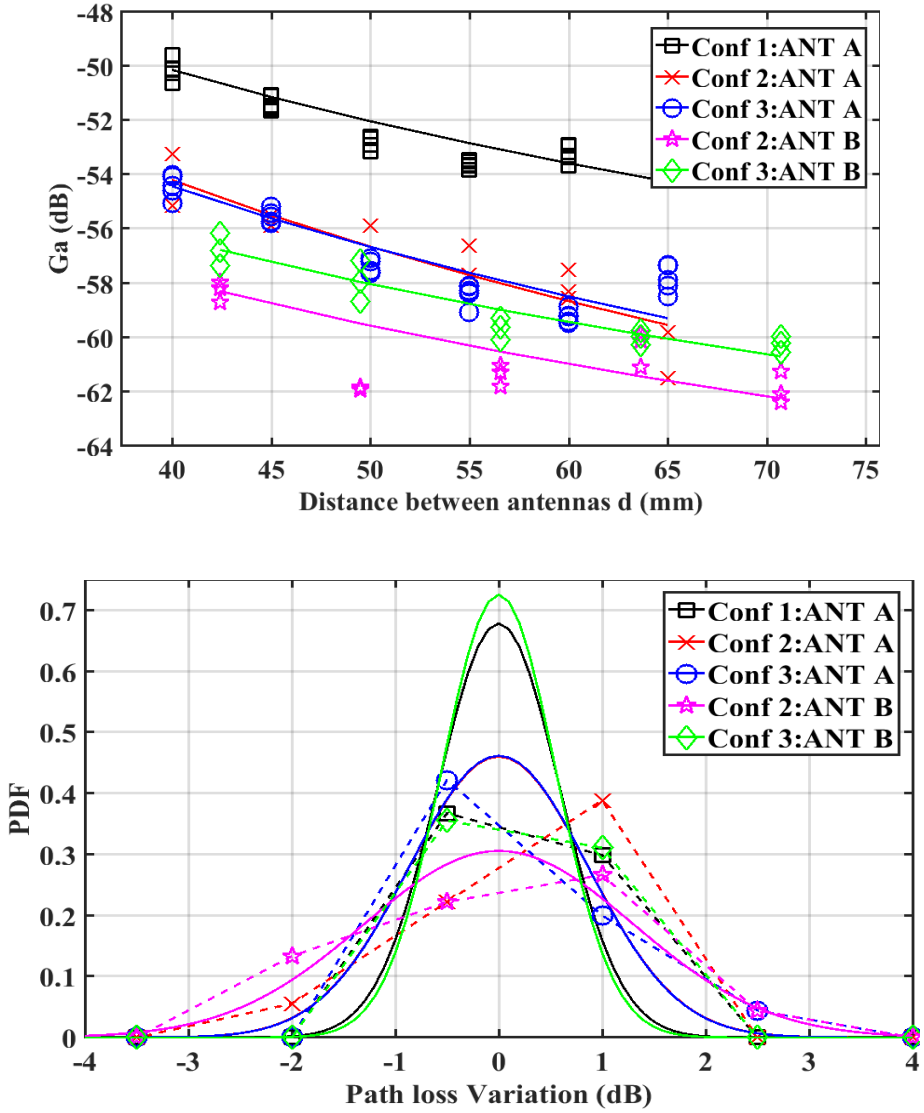


Figure 2-24. (a) Measured path-loss for fabricated dies with ANT O as reference fitted to a Log-Normal distribution. (b) Probability density function (PDF) of path loss variation.

Table 2: Modeled parameters for different configurations and orientations.

PL with respect to ANT O	d_0 (mm)	$PL(d_0)$ (dB)	n	σ (dB)
Conf 1: ANT A	40	-50.13	1.95	0.587
Conf 2: ANT A	40	-54.19	2.53	0.866
Conf 3: ANT A	40	-54.42	2.30	0.863
Conf 2: ANT B	42.42	-58.29	1.78	1.304
Conf 3: ANT B	42.42	-56.76	1.77	0.550

2.5 On-chip antennas in the 60GHz band with metallic wires

Following our studies with 30GHz antennas, we investigate 60GHz antennas as they will occupy smaller footprints in dense processor chips. However, in real chips, particularly in large multi-core processors, millions of copper interconnects are present in the silicon dioxide layers. We know that the metal objects influence the propagation of electromagnetic waves and if the metal objects are placed near the antenna, the objects influence the antenna's properties like resonant frequency, bandwidth and radiation pattern. In this section, we first model numerous metallic wires into structures that can be used for practical simulations and then evaluate and analyze 60GHz on-chip antennas in their presence.

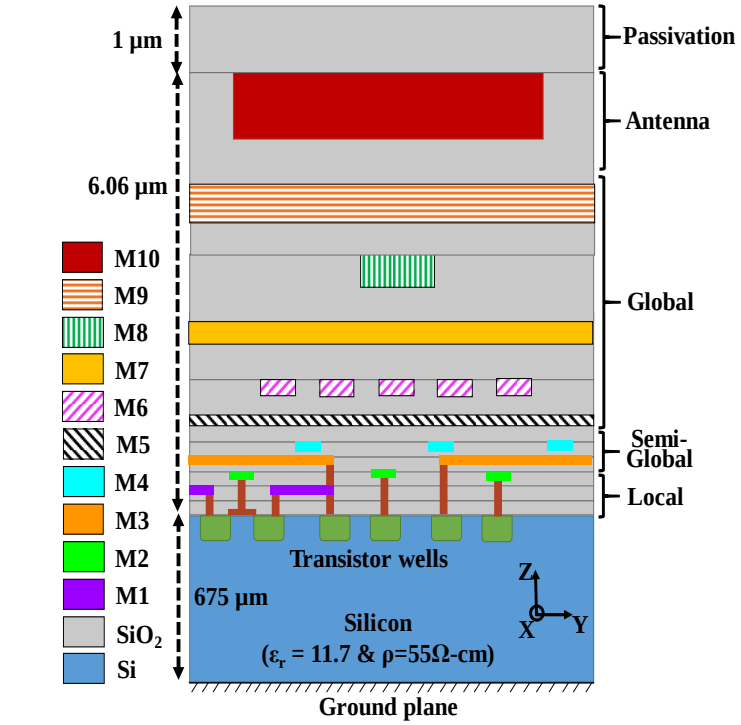
2.5.1 Modeling of on-chip metallic wires

General process of fabricating the transistors, resistances and other devices except metal interconnects on silicon is referred to as front end of line (FEOL). The other part of fabrication which is depositing metal interconnect with insulating layers and bonding contacts is referred to as back end of line (BEOL). As an example of metal interconnects fabricated using BEOL, the side-view of a die with ten layers of metal interconnects (M1-M10) including the top layer used for the antenna is shown in Figure 2-25 (a). The dimensions of interconnects of different layers along with its use are shown in Table 3. Each layer is separated by an interlevel dielectric (ILD) layers such as silicon dioxide (SiO_2) which acts as an insulating layer. Generally, the thickness of ILD of a layer is equal to its corresponding thickness of metal layer. Modern processes use copper as the choice

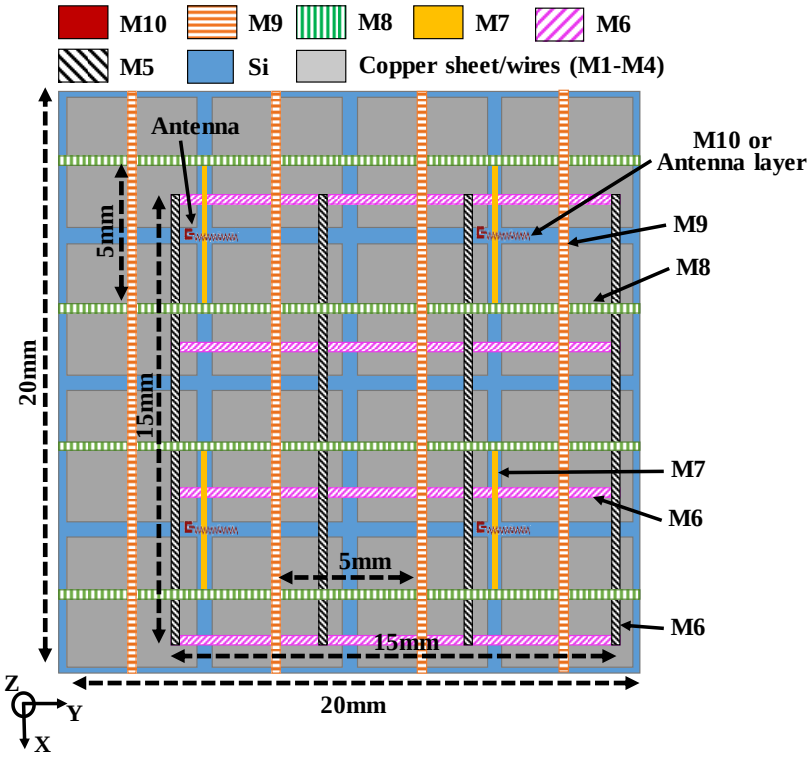
In modern processor chip, there could be 8-12 layers of metal. Each metal layer has its own functionality and therefore, the size. Moreover, the copper interconnects are laid down according to Manhattan architecture [65] that is, wires in each consecutive layer are laid in an orthogonal

manner with respect to each other. The reason is to minimize the cross-talk between adjacent layers. Figure 2-25(a) shows the side view of various layers involves in a generic modern processor. A top view of the chip is also shown in Figure 2-25 (a). It can be seen that the lower metal layers from metal 1 or simply M1 layer to M4 layer, the width of the wire is same. The wires in this layers are also known as local interconnects as they connects the transistors to nearby transistors or one device block to nearby device block. Above local interconnects, M5 and M6 layers are the NoC layers. In a mesh-based NoC topology, these layers consists of 32/64 wire bus which runs from core to core. M5 layer NoC bus runs top to bottom in the Figure 2-25 and M6 layer runs left to right, maintaining the consistency with the Manhattan architecture. Moreover, M7 layer may run the H-tree clock for a specific cores. Although there are different types of architectures of clock signal distribution, we are only considering the H-tree due to its efficiency and zero clock span. At the top layers that is M8 and M9 are the power grid and ground grid for the chip. In this section and later, copper wires/interconnects and metal wires/interconnects are used interchangeably.

In modern BEOL, the interconnects are divided into three tiers: local, semi-global and global as shown in Figure 2-25(a) depending on the length of interconnect and devices it connects. Global interconnects are used for power supply, clock signals or long-range communication. Due to their relatively long lengths, their cross section is wider than the other tiers to reduce resistance. In this work, we have considered metal layers (M5-M10) belonging to the global tier. The NoC metal interconnects which connect the processing cores in a multicore chip are designed using M5 and M6. In our work, we model the NoC architecture as a 2-D Mesh topology [66] as it is relatively easy to design, verify and fabricate due to its repetitive nature and is hence, chosen in hybrid wired and wireless NoC based systems [15]. Usually, NoC wires will be multi-bit (or wire) bus which



(a)



(b)

Figure 2-25. (a) Side view of the chip showing the copper interconnects in SiO2 layer, (b) Top view of the multi-core chip.

Table 3: Dimensions for wires in different metal layers. East, West, North and South are abbreviated as E, W, N, and S, respectively.

Layer	Width (µm)	Thickness (µm)	Layer Description
M10	-	1	ANT
M9	2	0.5	VCC/GND
M8	2	0.5	VCC/GND
M7	1	0.35	CLK
M6	0.1	0.3	NoC (E-W)
M5	0.1	0.3	NoC (N-S)
M4	0.05	0.02	E-W
M3	0.05	0.02	N-S
M2	0.05	0.02	E-W
M1	0.05	0.02	N-S

.are fabricated side by side, so to reduce the mesh size in HFSS the bus is considered as a single thick copper wire. We consider each multi-core chip to have 4 x 4 equal-sized cores (4.5mm x 4.5mm each) in a 20mm x 20mm die with the mesh links connecting each core to its cardinal neighbors. M7 is used for an H-Tree based clock network as it is known to reduce clock skew [67]. M8 and M9 are used for the power and ground supply straps [68]. Second, the semi-global tier is used for inter-block communications within a processing core spanning shorter distances compared to the global wires. M3 and M4 are considered to belong to the semi-global tier and are used to connect adjacent circuitry within a block or core. Lastly, local tier of interconnects which connect the transistors within a unit or cell. Local interconnects are very short and narrow. Usually M1 and M2 layers, which are in the local tier, are employed for connecting neighboring transistors. The various wired interconnects in the metal layers are shown in Figure 2-25(b). The M1-M4 layers are so dense that they are shown as a grey box in the figure. Further, we will show that the wires in the M3 and M4 layers which are of the form an unbounded grid like structure, can be replaced by a copper sheet at M4 layer for simulation purposes as we explain next.

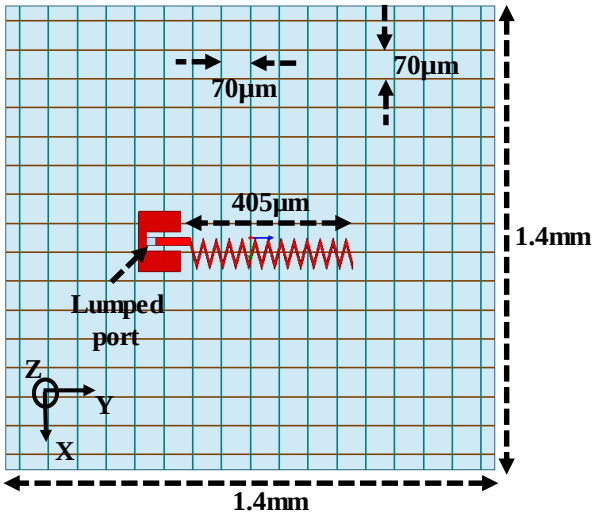
Typically, the wire interconnects in the M3 layer are orthogonal to the wires in M4 layer in order to reduce crosstalk among wires in adjacent layers by following what is known as

Manhattan architecture. In order to model these multiple layers of metallic interconnects, we can consider that they form a very large unbounded grid-like structure of the size of a processor core. This large grid-like structure is impossible to simulate in ANSYS HFSS due to colossal mesh size and computational cost especially, at carrier frequencies of 60GHz. Therefore, to simulate the effect of semi-global interconnects on the transmission between wireless interconnects in a multi-chip system, a simplified model is required which can emulate its effects. The aim of the following simulations is to show that the loading effects of a copper grid and of a copper sheet, on the antenna are equivalent. Using this equivalent model, for simulation, the effects of copper wires in a multichip multicore system can be analyzed. Before using the model, we prove that the effect of a copper grid of interconnects on the antenna is equivalent to that of a copper sheet through the following simulation.

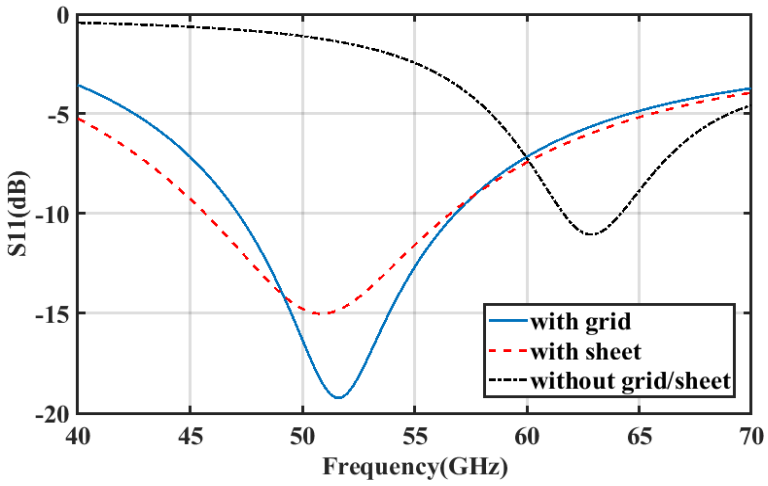
A small square area partially including the wire grid area inside each of the four cores around an antenna is simulated with a zigzag antenna. It is a small 1.4mm x 1.4mm area around one of the antennas shown in Figure 2-25(b) along with the small portions of surrounding copper sheet. The copper sheet represents the copper grid formed by M3 and M4 layers. Generally, the pitch of these wires vary from about 0.15μm in modern technology nodes (smaller than 65nm technology) to about 0.5μm or more in older technology nodes (larger than 65nm nodes). However, such dense and fine-grained structures are beyond the simulation capabilities of our tools. Hence, the minimum pitch of the grid considered here is 70μm.

In Figure 2-26 (a), a zigzag antenna with a length of 405μm is placed in antenna layer which is the M10 (layer as shown in Figure 2-25(a) and on top of a grid of interconnects with spacing of 70μm corresponding to the M3 and M4 layers of thickness 0.02μm. The wires in M4 layer are orthogonal to the wires in M3 layer. The thickness of silicon and silicon dioxide is 675μm

and 7µm, respectively. The size of the simulated area is 1.4mm x 1.4mm. Structures such as ground plane at the bottom of silicon and other interconnects are removed for this analysis to model the effect of the wires only. In another simulation, the grid of wires is replaced with a copper sheet at M4 layer with same thickness of 0.02µm (figure not shown). Also, a simulation is performed with just the antenna on silicon and without the grid or sheet. The results from the third simulation are used as reference to compare the previous two simulation (of grid and sheet). The simulated S_{11} of the three cases are shown in Figure 2-26(b). It can be seen that the shift in resonance of antenna



(a)



(b)

Figure 2-26. (a) Top view of copper grid (M3-M4) under an on-chip antenna, (b) plot of S_{11} with grid, with sheet, and without grid & sheet.

with grid and the sheet is the same, though there is a 3dB difference in magnitude of S_{11}. It can be concluded that the grid and sheet have the similar loading effect in terms of resonant frequency.

In Figure 2-27(a), the zigzag antenna is surrounded by four copper grids. Each of these grids is identical to the one in Figure 2-26(a) where it was placed directly below the antenna. This arrangement is representative of the structure described in Figure 2-25(b) with spacing between the cores, except the ground plane at the bottom of the chip. In Figure 2-27(b), the S_{11} is shown which indicates that there is very little to no effect on the resonant frequency of the antenna. The

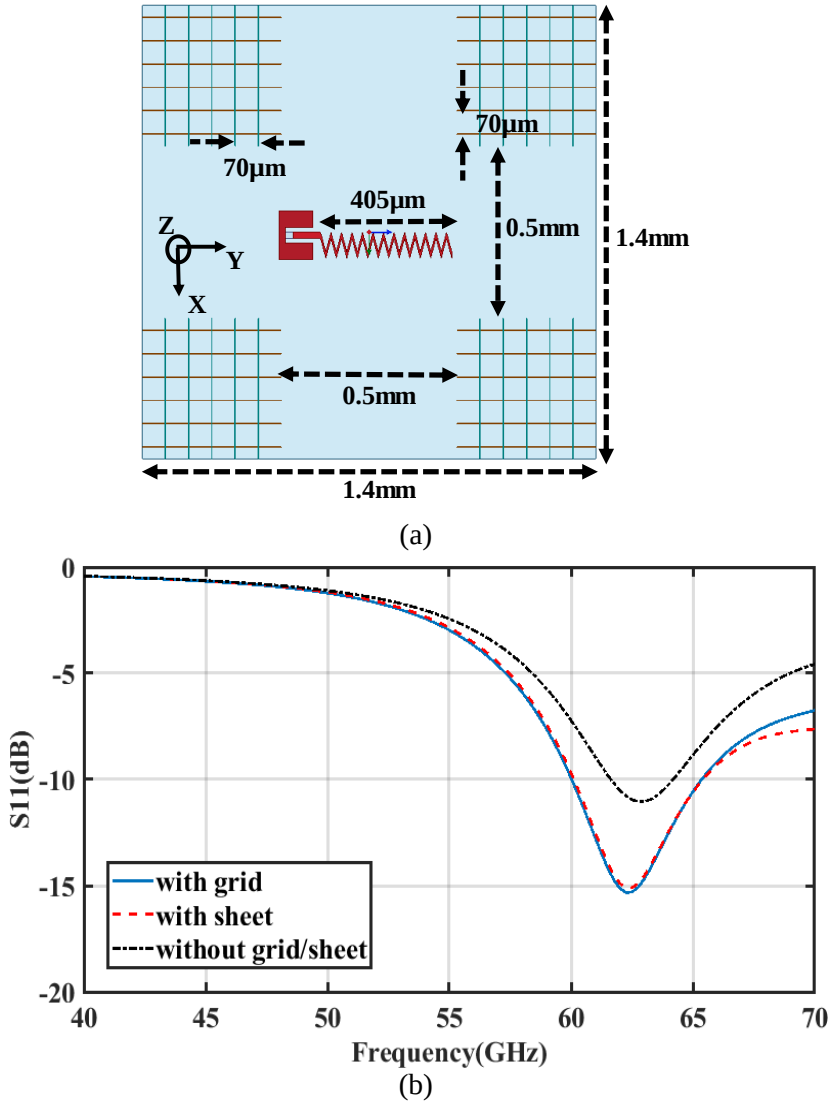


Figure 2-27. (a) Top view of copper grids (M3-M4) beside the on-chip antenna, (b) plot of S_{11} with grid, with sheet, and without grid & sheet.

difference of about 4dB in the magnitude of S_{11} can be noticed from Figure 2-27(b). Similarly another simulation is performed by replacing the grid structure with a sheet of copper, and the results are shown in Figure 2-27(b). The S_{11} plot with copper sheet overlaps with the S_{11} plot with copper grid. This shows that the effects of both the grid and sheet are equivalent for the case where antenna is surrounded by the grid with spacing between the individual sheets. As the pitch of the wires here are considered to be 70µm in this model, it can be concluded that a finer pitch resembling those in modern fabrication technologies will also behave similarly and can be modeled as a copper sheet.

Having established the equivalence of copper grid with a copper sheet in terms of S_{11}, the effect of the sheet in the M4 layer on the transmission characteristics in terms of S_{21} is analyzed. In Figure 2-28(a), a small chip with 2x4 cores is shown where the copper grids are replaced by copper sheets, and the ground plane at the bottom and other interconnects are removed. The antenna is the same as used in above cases. The magnitude of S11 and S22 are shown in Figure 2-28(b). The S11 for all cases is below -20dB with the antenna resonating at 64GHz. In Figure 2-28(c), the S21 plot is shown in a system with and without the interconnect model (as copper sheet).

Unlike in the system without interconnect models, the transmission between the antennas with interconnect models have dips even as the antenna is resonating at 64GHz. This shows that the transmission between antennas is dependent on the existence of the metallic interconnect model. In Figure 2-29 (a) and (b), magnitude of electric field is plotted at 65GHz in HFSS. As shown in Figure 2-28 (b) the S11 and S22 at 64GHz have worsened by 3.5dB and 6.5dB in the presence of the metallic plane. In addition, as can be seen in Figure 2-28 (c), S21 reduces by about 15dB at 64GHz. Further, radiation efficiency of the antenna with grid and without grid (Figure

2-29 (a) and (b)) is 8% and 19% respectively due to destructive interference with the antenna radiation.

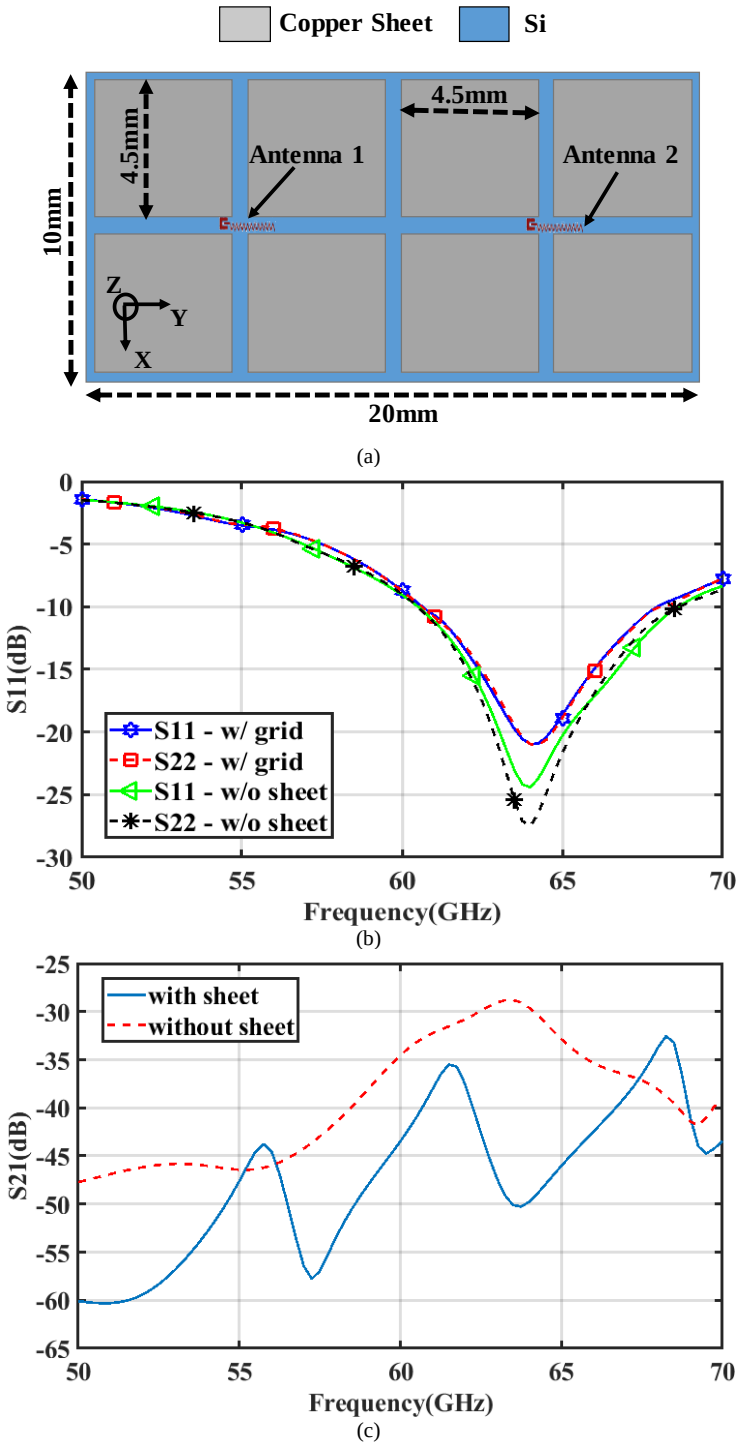


Figure 2-28. (a) Top view of the2x4 multicore chip with 8 copper sheets and two antennas, (b) plot of S_{11} and S_{22} of antennas, (c) plot of S_{21} between antennas.

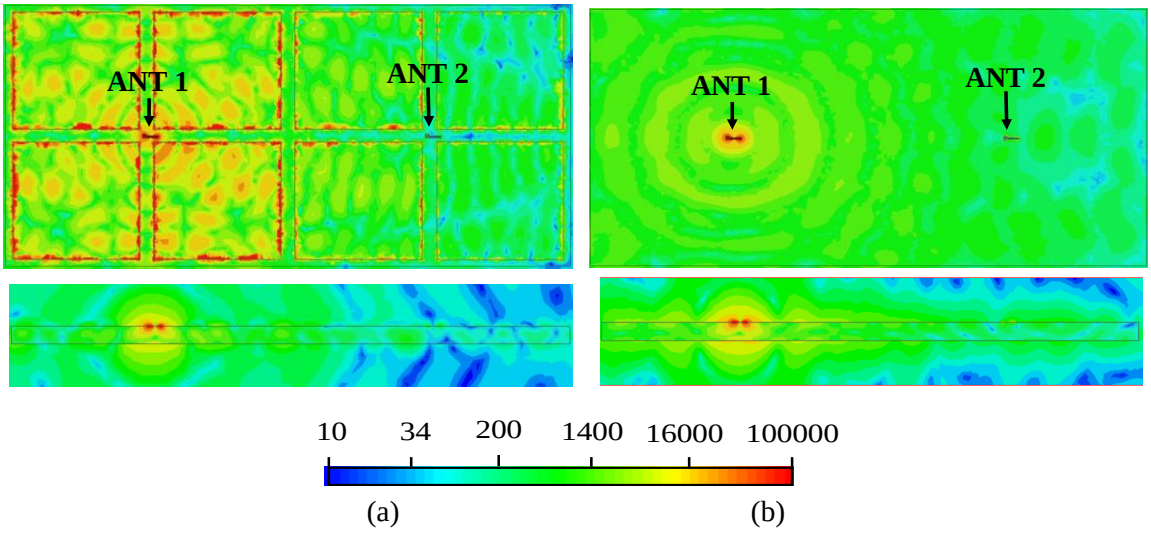


Figure 2-29. Magnitude of electric field (V/m) at the plane of antennas in two scenarios that is (a) with copper sheets and (b) without copper sheets.

The electric field plots show significant effects of the copper sheet on electric field propagation supporting our inference above. Based on the results in Figure 2-28 and Figure 2-29, we can infer that the S21 differs significantly in presence of metallic interconnect model compared to a scenario where they are not present. Moreover, orthogonal wires in adjacent metal layers on a chip, which require advanced and expensive fabrication processes, can be modeled as a continuous sheet due to similar impact on antenna characteristics. Therefore, in the next section, similar strategy is implemented for simulating an MCMC system.

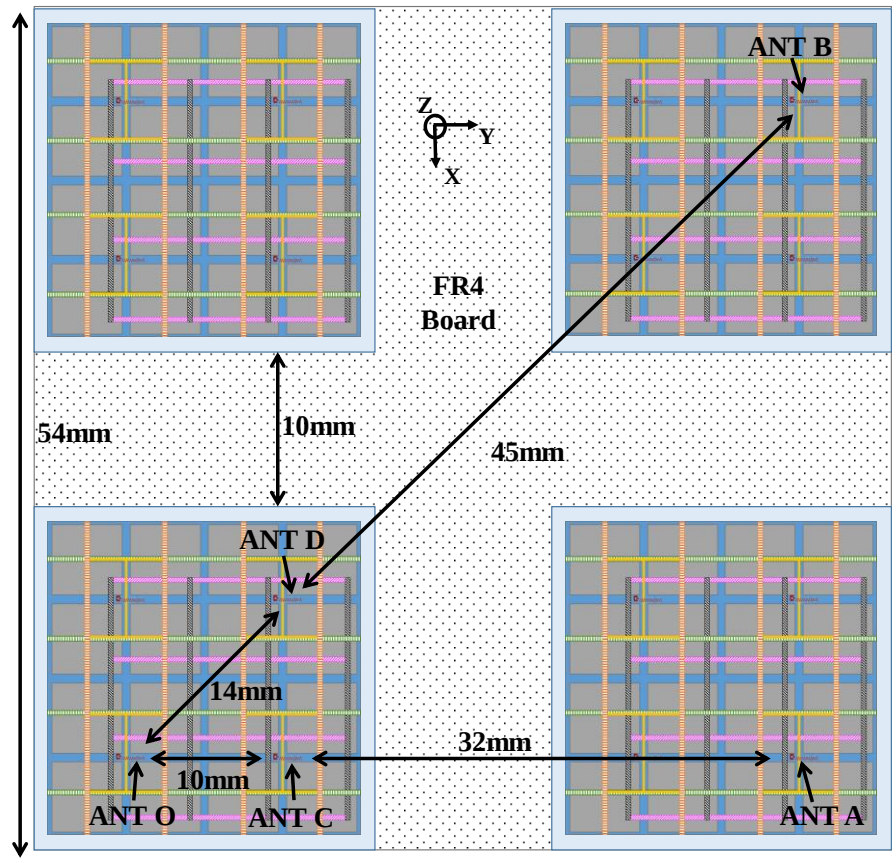
2.5.2 60GHz transmission analysis in presence of metal interconnects

The interconnect model (as copper sheet) described above is used in the simulation performed here. In addition to the copper sheet modeling M1-M4 layers, other metal layers (M5-M10) are also considered here. The dimensions of the length, width and thickness of copper wires is shown in Figure 2-25 and Table 3. As discussed earlier that NoC bus is usually multi-wire bus, but for simulation purposes to reduce the computational demand, the NoC bus is considered as a single thick wire. The chip along with copper interconnects is replicated into four chips and placed

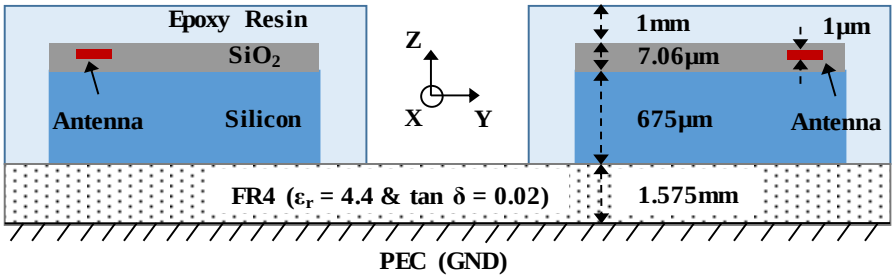
on FR4 board ($\varepsilon r = 4.4$ and $\tan(\delta) = 0.02$) of thickness 1.575mm. Figure 2-30(a) shows the arrangement of the multichip system. The spacing between the chips is 10mm. Moreover, the chips are coated with an epoxy resin layer of 1mm. Epoxy resin ($\varepsilon r = 2.9$) is commonly used to cover the silicon chip for protection and robustness. The side view of the chip is shown in Figure 2-30(b). The antenna used for transmission analysis is shown in Figure 2-30(c) which is a zigzag antenna modeled at the M10 layer shown in Figure 2-25. Now, there are four antennas on each chip that is a total of 16 antennas in a four-chip system.

To analyze the transmission between these many antennas will be complicated. Therefore, only five representative antennas are selected for analysis. The antennas under analysis are shown in Figure 2-30(a). These antennas are selected because they include the expected worst cases that is farthest antenna pairs for intra- and inter-chip pairs. A common antenna ANT O is chosen as a reference. Two antennas ANT A and ANT B are selected to form inter-chip pairs with ANT O. Here, ANT B and ANT O are the farthest apart. The Two other antennas ANT C and ANT D are selected to form intra-chip pairs with ANT O as they are on same chip. The distance between antennas are shown in the Figure 2-30(a).

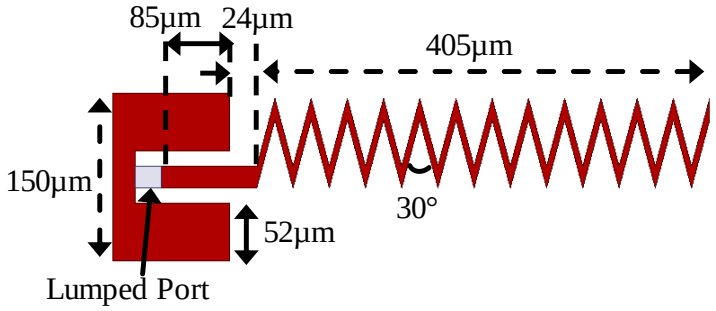
Simulations of the multichip system with interconnects (WI) and without interconnects (WOI) are performed in ANSYS HFSS. It should be noted that the WOI case still has FR4 board, bottom ground plane and epoxy resin. The reflection coefficient and transmission coefficients are plotted from frequency 50GHz to 70GHz. Figure 2-31(a) shows reflection coefficient (S11) in both cases. It should be noted that though the same antenna is used in previous analysis while showing equivalence between grid and sheet, the antenna in Figure 2-26 and Figure 2-27 has different S11



(a)



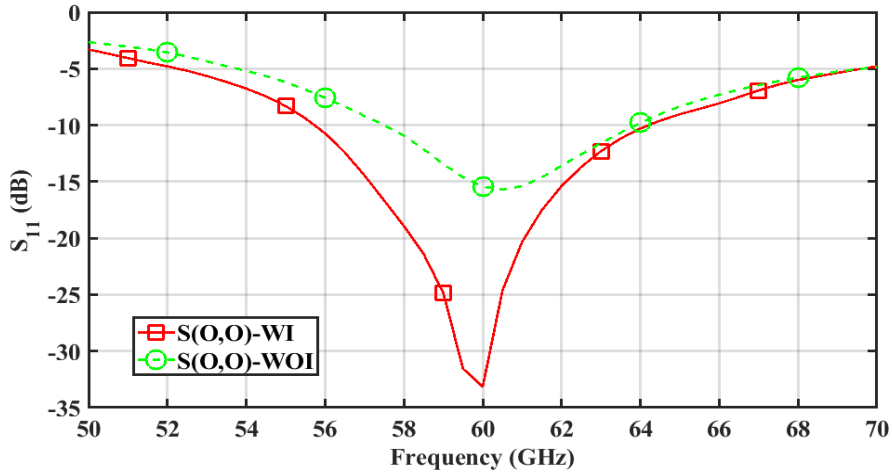
(b)



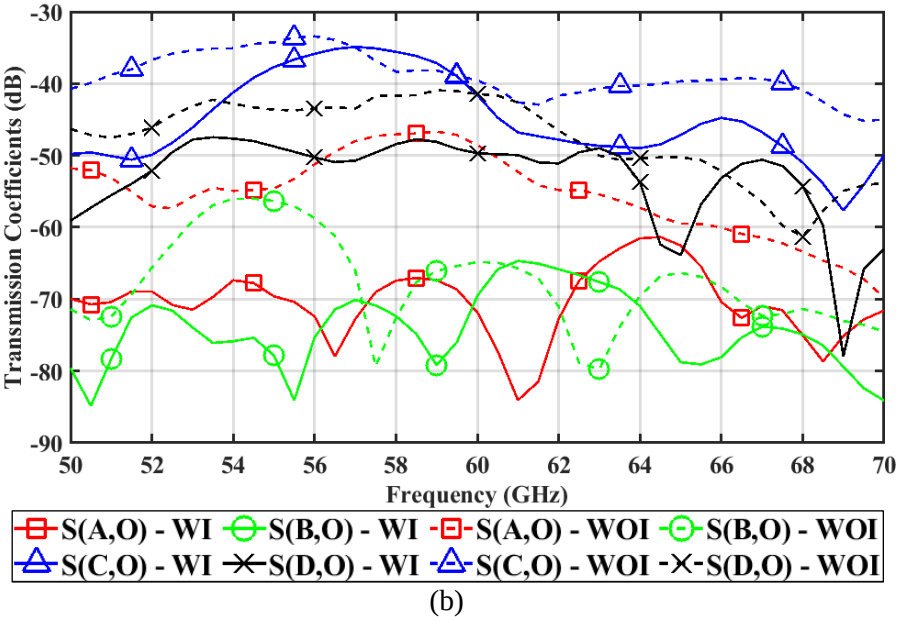
(c)

Figure 2-30. (a) Top view of the multichip system (Note: Distances are measured from the center of the antenna), (b) Cross-sectional view of the multichip system, (c) Zigzag antenna used at 60GHz.

characteristic with no grid or sheet from the S11 - WOI case in Figure 2-31(a) due to the absence of FR4 board, bottom ground plane and epoxy resin. In presence of copper interconnects the antennas resonate at 60GHz as shown in Figure 2-31(a). However, when all copper interconnects and copper sheets are removed, the resonant frequency of antennas shifts to about 61GHz. Moreover, the magnitude of reflection coefficient drops showing an impedance mismatch. This shows that the design of mmWave on-chip antennas requires the knowledge of the layout of the copper interconnects.



(a)



(b)

Figure 2-31. (a) Reflection coefficient (S_{11}): WI=with interconnects, WOI=without interconnects, (b) Transmission coefficients.

Transmission between antennas are analyzed for inter-chip and intra-chip pairs and shown in Figure 2-31 (b). For the inter-chip antenna pairs the transmission coefficient can be seen to vary between -60 to -85dB with copper wires. This is lower than the transmission coefficient without copper wires by 20dB for antenna pair ANT A & O. Moreover, for intra-chip pairs, the transmission coefficients with copper wires varies from -40dB to -50dB. Significant difference can be seen for antenna pair ANT D & O in presence and absence of metal interconnects. The transmission between ANT D & O is about -50dB with copper wires and about -40dB without copper wires. This shows that the copper wires can significantly change the transmission between on-chip antennas.

Furthermore, the radiation pattern of the antenna is shown in Figure 2-32 (a). The electric field distribution is also provided with and without the presence of copper wires in Figure 2-32 (b) and Figure 2-32 (c), respectively. It shows that the distribution is affected by the M3 and M4 layers, which are modelled as copper sheets, when compared with the field distribution without the copper wires. Overall, generally neglected copper interconnects are seen to affect the resonant frequency and transmission coefficients between on-chip antennas. Therefore, appropriate consideration must be given to the metal interconnects when designing on-chip antennas.

2.6 Simulation of on-chip zigzag antennas in a flip-chip multi-chip packaging

Modern processors use Flip-chip Ball Grid Array (FCBGA) and Flip-chip Land Grid Array (FCLGA) [3]. In Flip-chip technology, the chip is flipped on top of a substrate which can be an organic, ceramic and Polytetrafluoroethylene (PTFE). In such processors the heat sink is separated from the chip by a heat spreader which provides a larger surface area for heat extraction [3]. In this section, we present the transmission characteristics of the antennas discussed in this paper in processor environments with flip-chip packaging and heat spreader. The four antennas are placed

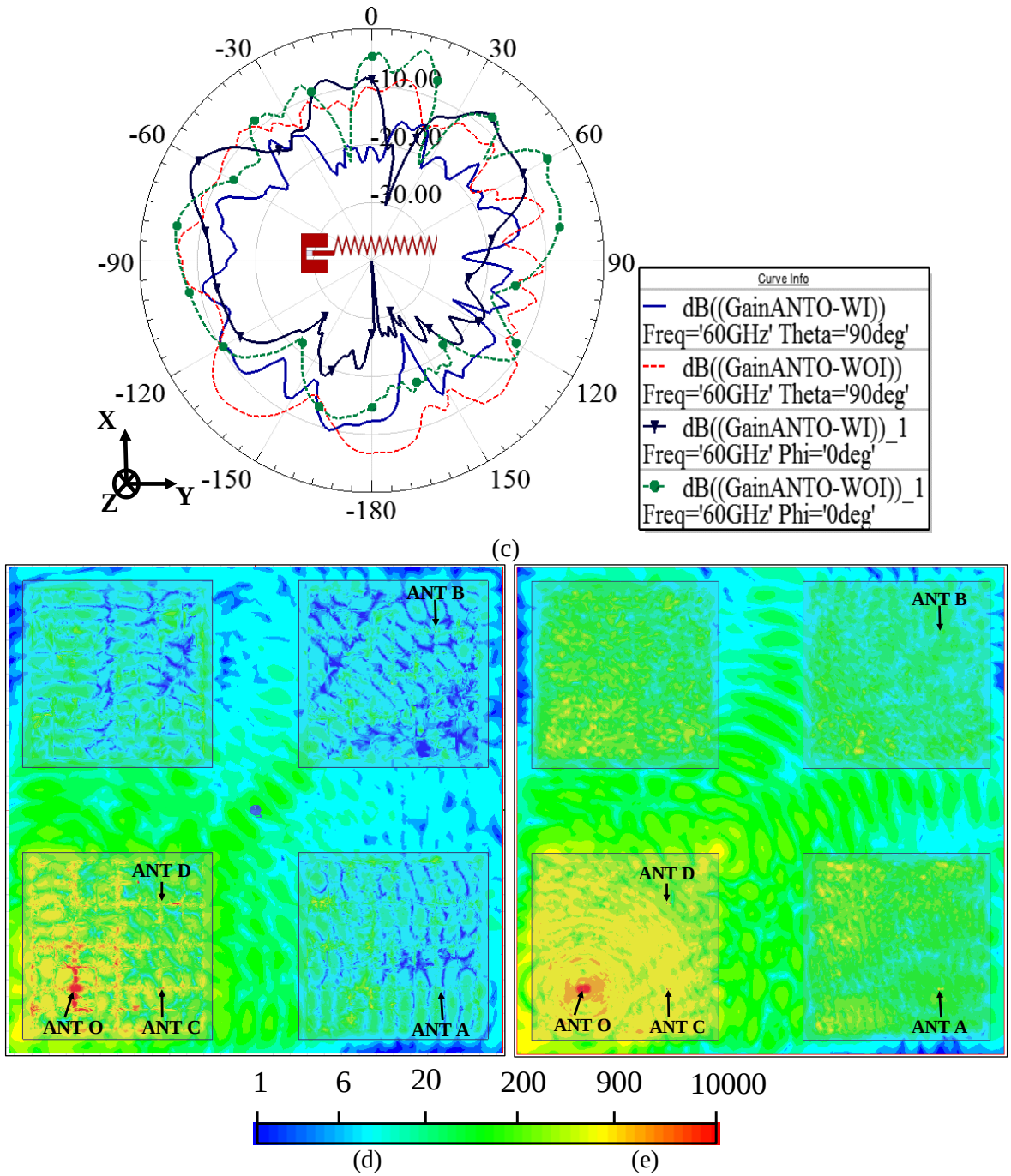


Figure 2-32. (a) Radiation pattern of ANT O in XY plane. Magnitude of E-field (V/m) at M10 layer height when ANT O is excited at 60GHz (b) with and (c) without interconnects.

in the center of four equally divided quadrants on a 20mm x 20mm silicon chip [69]. The cross section of package adopted from Intel Xeon [3] is shown in Figure 2-33 (a). The top-view is presented in Figure 2-33 (b). The optimized antenna is shown in Figure 2-33 (c). Two PEC

boundaries are considered here – one for heat spreader cover and another is for lands/solder balls/metallic processor loading mechanism as shown in [3]. Dielectric constant and loss tangent for the structure has been acquired from [62]. The diameter and pitch of solder balls is 0.6mm and 1mm, respectively. The number of solder balls in grid array is 364.

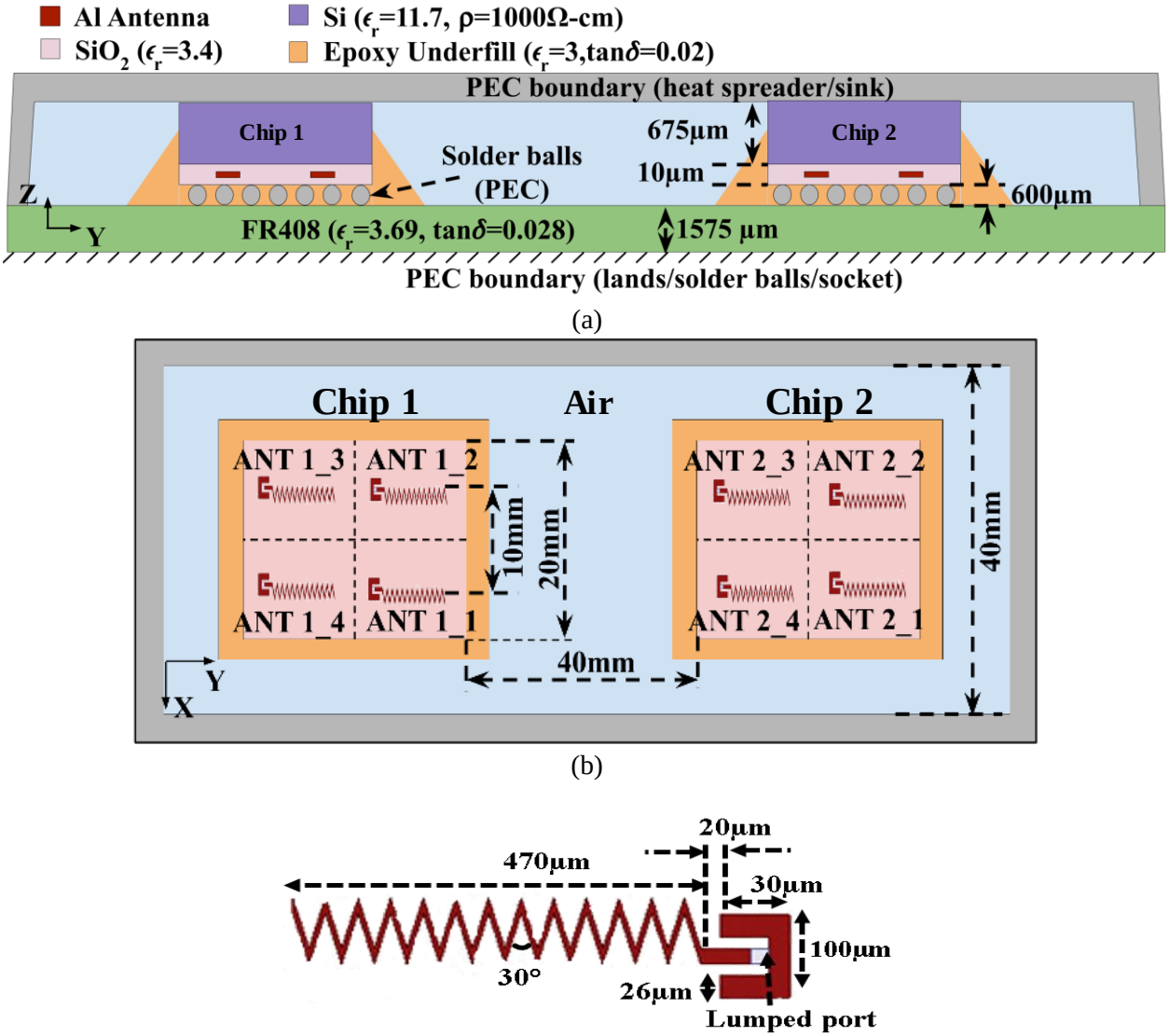
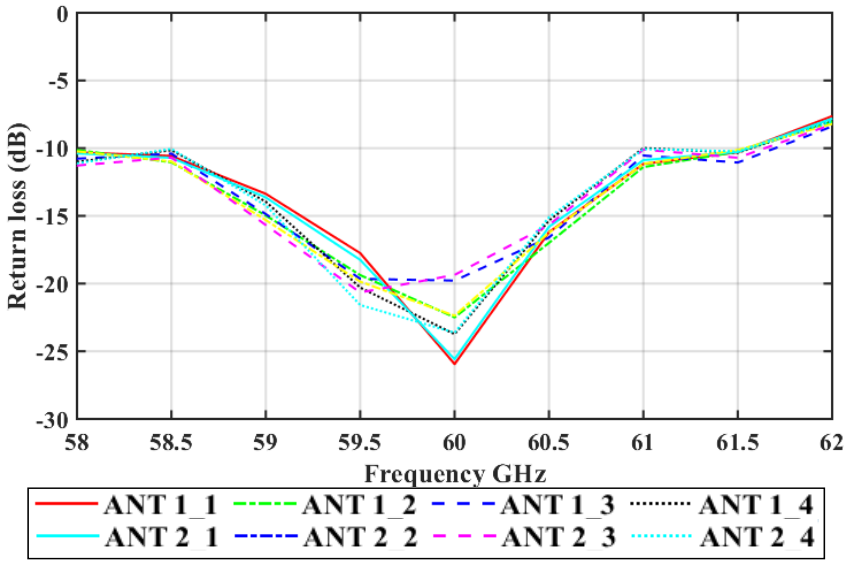
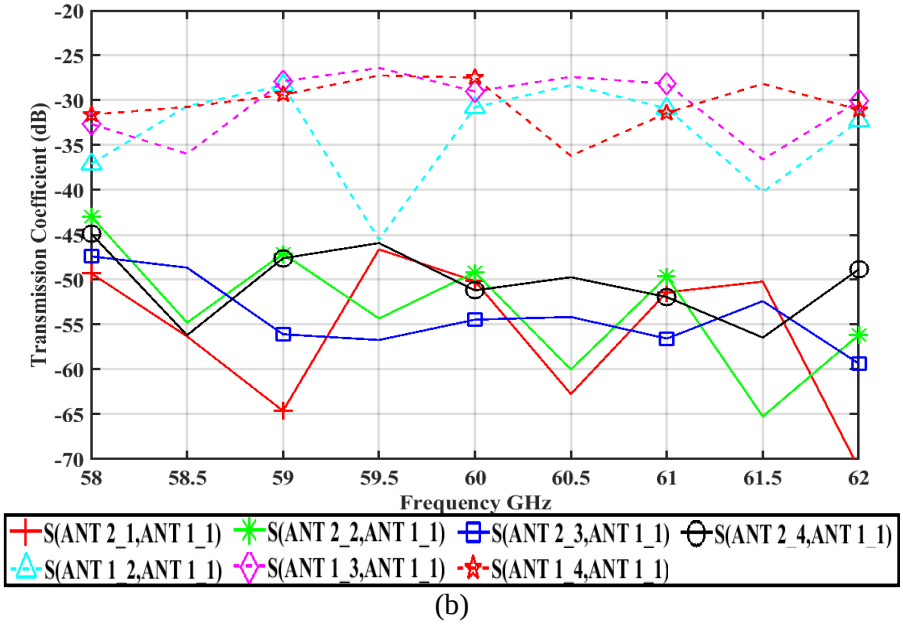


Figure 2-33. (a) Cross-sectional view of the multichip system [69], (b) Top view of the multichip system (not to scale), and (c) Zigzag antenna.

Due to the complexity of the system discrete frequency sweep at intervals of 0.5GHz is simulated. The S11 for all eight antennas in the system are shown in Figure 2-34 (a). The transmissions between ANT1_1 in chip 1 and all other antennas covering intra-chip and inter-chip pairs are shown in Figure 2-34 (b). It can be observed from Figure 2-34 (b) that at 60GHz the intra-chip transmission coefficients between the antenna pairs are around -30dB. On the other hand, the



(a)



(b)

Figure 2-34. (a) S_{11} responses for all antennas, (b) Intra- and inter-chip transmission coefficients between antenna pairs in the system.

inter-chip transmission at 60GHz between the different pairs of antennas ranges from -50dB to -55dB. This trend is similar to the packaging configuration studied in the previous subsection where the transmission (between ANT A and ANT O) without considering the wires (WOI case in previous subsection) in Figure 2-31(b) is also around -50dB at the resonant frequency.

2.7 Conclusion

This chapter has presented transmission characteristics of on-chip antennas for intra-chip and inter-chip communication in multi-chip systems. Through simulation at 30GHz, we have characterized the inter-chip transmission, and studied the electric field distribution to explain the transmission characteristics. The simulation results have been validated with fabricated antennas in different orientations on silicon dies, that can communicate with inter-chip transmission coefficients ranging from -45dB to -60dB while sustaining bandwidths up to 7GHz. Our fabricated antennas show a shift in resonance to 25GHz. In order to investigate the reasons for this shift we modeled the probe structure to study its impact. On including the probe in our simulation model the resonant frequency was found to shift by 1.5GHz.

The SOLT calibration that we adopted in our measurements, is also seen to introduce additional measurement discrepancies between the probe tip and the antenna feed structure. It is shown that the antenna radiation efficiency reduces with decrease in the resistivity of silicon that results in increased losses. Using the experimental measurements, a large-scale, log-normal channel model is derived, which can be used for system level architecture design. In most cases, the shadowing effect remains below 1dB. We have designed on-chip antennas and studied them at 60GHz in the presence of densely packed multilayer copper wires typical of NoC based multicore processors. Dense wires have been shown to be equivalent to copper sheets and modeled as such, to reduce the complexity of simulations. Using this interconnect model, reduction in inter-chip

transmission is obtained as much as 20dB. In presence of densely packed metallic wires in close proximity to the antenna is shown to reduce its radiation efficiency by about 11%. Furthermore, we found the intra- and inter-chip transmission characteristics of these antennas to be similar in a flip-chip packaging environment, indicating their suitability for such a technology as well.

3 Beamforming with mmWave interconnects in multi-chip systems: Present and Future Work

3.1 Introduction

Beamforming has always been an attractive topic for researchers working at mmWave frequencies. Since the propagation loss or path loss is higher for mmWave frequencies as the distance between transmitter and receiver increases, so beamforming can be useful to counter the effects of path loss. The array can increase the gain of the antenna system towards a particular adjustable direction. Moreover, at mmWave frequencies, the dimensions of antenna and array are small enough to fabricate them on a silicon chip.

In this chapter, beamforming with mmWave antenna is discussed. The objective here is to design and develop linear antenna array which can be used for beamforming for intra-chip and inter-chip communications in modern processors under the constraint of size, fabrication restrictions, and performance of the whole antenna system. A conceptual scheme of beamforming between wireless interconnect is shown in Figure 3-1. It is a four-chip MCMC system. For example, three wireless interconnects (WIs) are shown: two WIs on one chip and one WI on other chip. The idea is to use one antenna array system to communicate intra-chip using beam 2, if there is a need to communicate inter-chip then the beam of the array should change to beam pattern 1, just by changing the phase between the feed of the network.

In this scenario, a four-chip MCMC system with three WIs is shown, but depending on the network architecture like small-world [69] used by the system the positions of the WIs may change so beam-steering using phased arrays will be helpful to direct the radiation towards desired WI. It

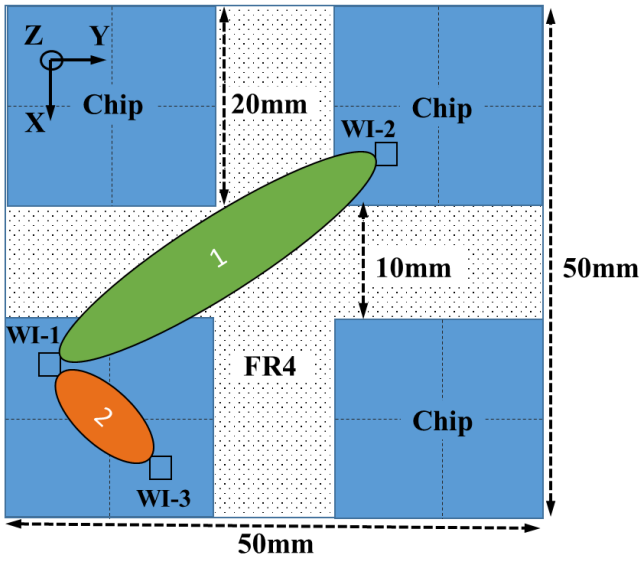


Figure 3-1. Conceptual plan of beam pattern between three wireless interconnects. WI = wireless interconnect.

can also be helpful to determine the direction of maximum signal strength, in other words, auto-calibration of the beam towards other WIs if the locations of them are not known or defined. Here, in the current scenario, since the required beam directions are fixed, multiple directional antennas can be used, but it may increase the area overhead on the chip. However, a phased array uses the same antenna elements to steer the beam in different directions, but a compact feed system is required. To demonstrate the concept, a simple linear array is implemented.

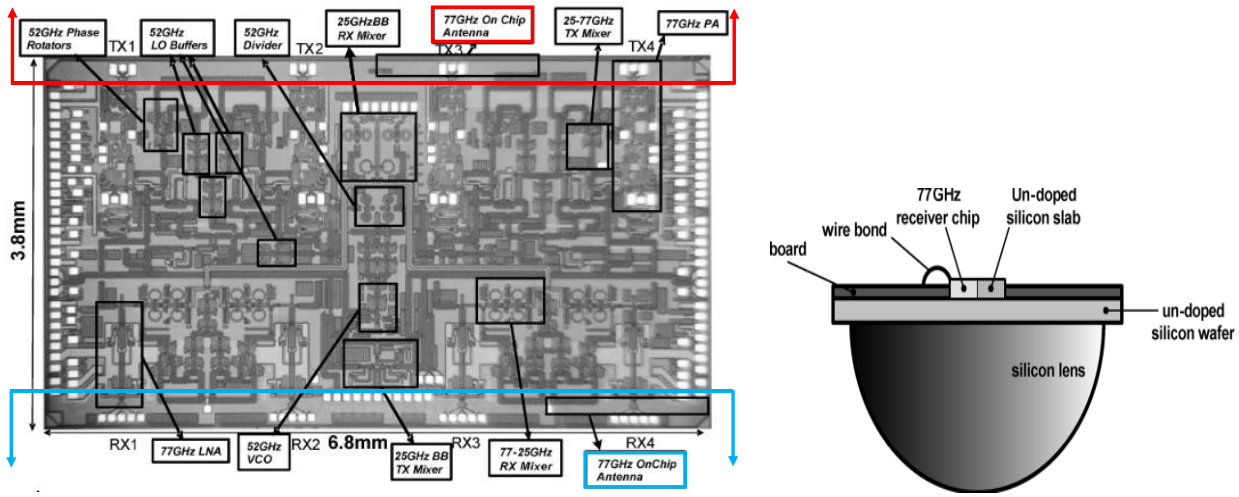
In the next section, a literature survey about the beamforming is presented focused on the on-chip antenna array. However, due to the recent advancement in 5G technology [71], there have been relatively more work in an antenna array in a package than antenna array on the chip, so few works on beamforming in 5G technologies are also included because the design concepts are similar.

3.2 Related work on antenna array on a chip

Although there have been many works on antenna-on-chip (AoC), there is relatively fewer work on antenna array on a chip. Most of the work on antenna array and beamforming system is focused on 5G and WiGig systems. These work have antennas in package (AiP) or antenna on display (AoD) [72]. Those works are discussed in this section.

One of the early 77GHz mmWave phased array was made by Babakhani, et al. at Caltech [73]. This phased array was made on a CMOS chip with different components of communications systems like modulators, oscillators, amplifiers, et al as seen in Figure 3-2. Moreover, this array system utilizes a silicon lens to improve the gain of the system as the system is designed to communicate with an external off-chip system.

Sengupta and Hajimiri have designed a two-dimensional 4x4 radiating array implemented in 45nm SOI CMOS at 280GHz [74]. The chip is 2.7mm x 2.7mm. The phased antenna array is



(a) (b)

Figure 3-2. (a) 77GHz phased array chip [73] showing both TX array (top side) and RX array (bottom side), (b) Silicon lens used to improve the gain.

shown in Figure 3-3. It consists of loop antennas. It consists of a distributed source which generates THz signal using DC power. Moreover, this antenna array is further used in THz imaging [75].

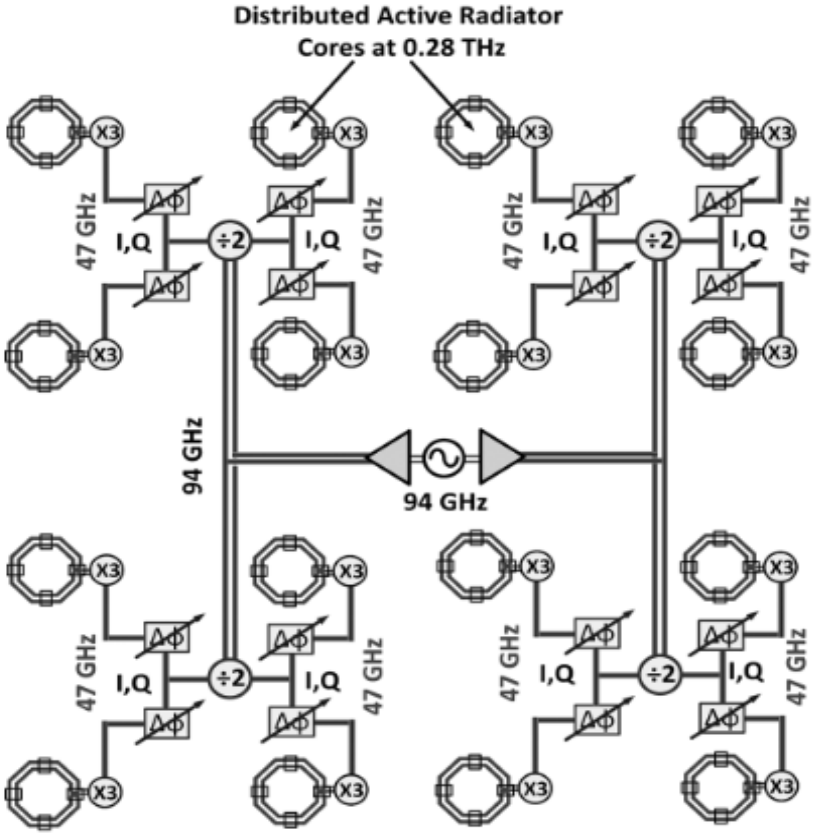


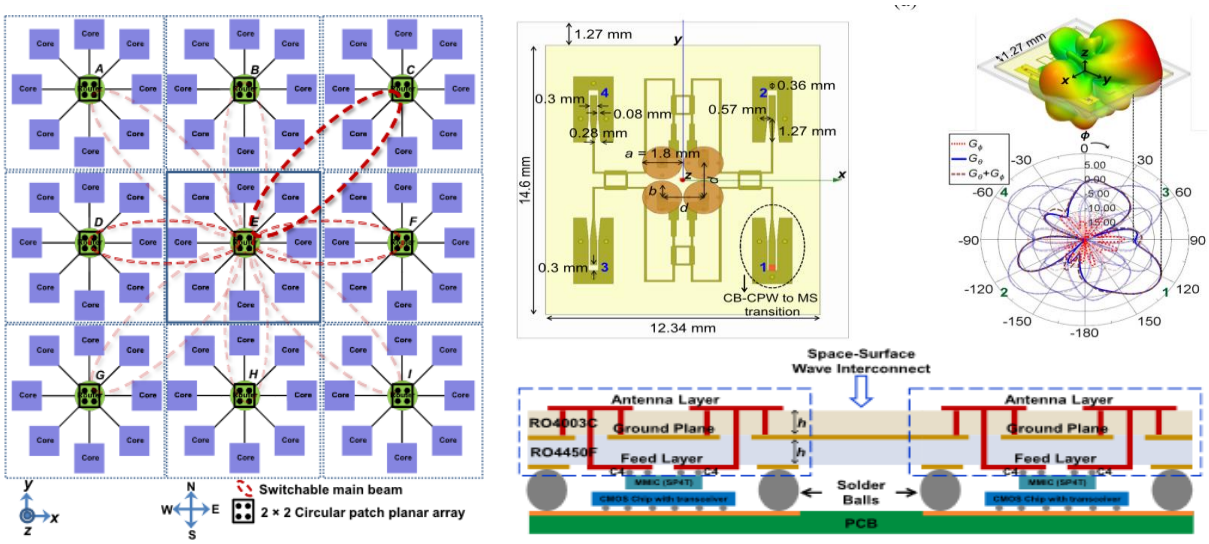
Figure 3-3. Array of Loop antennas operating at 280GHz by Sengupta, et al. [74].

Baniya, et al. have shown a chip to chip switched beam at 60GHz using circular patch antennas which are placed in the package and not a chip [76]. As shown in Figure 3-4 (a), a chip will have multiple cores and one antenna array system, which the chip will use to connect with other chips on a PCB board. Furthermore, this array can be used with a butler matrix system [77] for beamforming feed as shown in Figure 3-4 (b).

Another work has been performed for BGA flip-chip packages by Rashidian, et al [78], not on a silicon chip, but on low-temperature co-fired ceramic (LTCC) substrate. This work

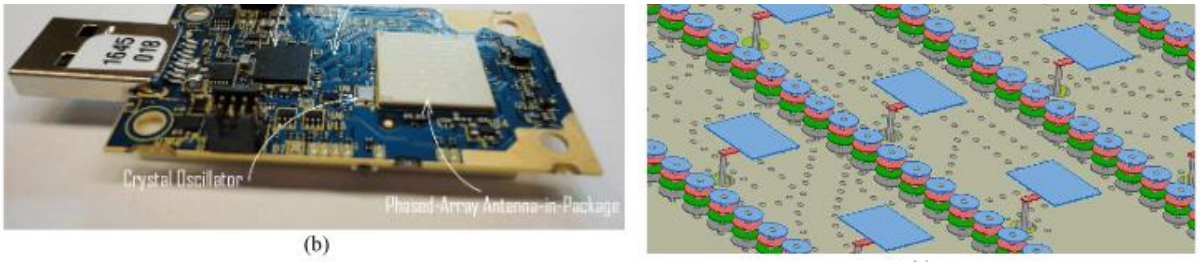
incorporates 60GHz phased array antennas in LTCC which is placed on top of a flip-chip BGA as shown in Figure 3-5. There is some more work at 60GHz phased array antennas which are referred here [79][80].

A collection of work performed on phased antenna arrays for 5G is published by Hong [72]. Nearly all of the work performed for 5G-related applications are done in LTCC or thin substrates like RO3003/5880, or other lossless substrates. Therefore, those works are not discussed in many details, however, this work shares the mmWave frequencies design consideration as the



(a) (b)

Figure 3-4. (a) 3×3 MCMC architecture with HyNoC interconnection using pattern switchable mmWave antenna arrays [76]. (b) Side, Top view and radiation pattern of circular patch antenna array [77] with phase Port 1 (φ0=+135◦), Port 2 (φ0=−135◦), Port 3 (φ0=+45◦), and Port 4 (φ0=−45◦).



(b) (c)

Figure 3-5. An example of antenna array in package by Rashidian, et al. [78]: (a) side view of proposed system, (b) perpective view of implemented system where phased array is placed on the white substrate. on chip, (c) a view of electromagnetically-coupled patch antennas used for phased array.

5G beamforming work also requires careful consideration of metal casing like a mobile handset. Therefore, some recent and important work is referred to here and discussed. Another review article published by Cao, et al. on 5G beamforming is [81].

Some work has been done by Xu, et al. demonstrating a 28GHz antenna array integrated with a mobile set housing which is covered with metal [82]. They perform radiation performance testing along with simulations to find the surface current on the metal housing the mobile set. Another paper has shown work on a hybrid antenna design with an antenna in package and an antenna on display for a 5G mobile handsets [83]. Furthermore, the antenna elements placed in the array couples power into each other, phenomenon also known as mutual coupling. Few ingenious ideas to reduce mutual coupling are mentioned in [84] and [85].

3.3 Theoretical design – antenna array

In this section, the theory about the beamforming using antenna array is discussed. The theoretical formulas are taken from [86]. Considering *N* element linear array arranged on X-axis having a progressive phase difference of β as shown in Figure 3-6, the array factor (*AF*) is:

$$AF = \left| \frac{sin\left(\frac{N\psi}{2}\right)}{\sin\left(\frac{\psi}{2}\right)} \right| \tag{3}$$

where *N* is the number of antenna elements in the array

$$\psi = k \times d \times \sin(\theta) \times \cos(\phi) + \beta \tag{4}$$

$$k = \frac{2\pi}{\lambda}; d\ is\ the\ distance\ between\ elements, \beta = phase\ difference \tag{5}$$

For a maximum beam towards a direction with $\phi = \phi_m$ and $\theta = \theta_m$, *AF=1*. Therefore from the above equations, we get:

$$AF = 1 = \left| \frac{sin\left(\frac{N\psi}{2}\right)}{\sin\left(\frac{\psi}{2}\right)} \right| \tag{6}$$

$$\therefore \frac{\psi}{2} = 0$$

$$\psi = 0 = kd \times \sin(\theta_m) \times \cos(\phi_m) + \beta \tag{7}$$

$$\beta = -kd \times \sin(\theta_m) \times \cos(\phi_m) \tag{8}$$

For the MCMC system, the wireless interconnects are all supposed to be in the same plane parallel to the XY plane spread across the PCB as shown in Figure 3-1, therefore the θ_m should be 90°. On the other hand, the φ_m is going to change depending on the antenna array locations. Calculated values for phase (β) for different *d* is shown in Table 4.

In this work for d=3λ/8, the progressive phase difference (β) is considered, first, as zero for broadside beam, then $\beta = \pm 135°$ for endfire beam in $\varphi = \pm 180°$ and lastly, an arbitrary phased beam angle of 135° is selected. The arbitrary beam angle is achieved of $\varphi = 135°$ from X-axis in XY plane using $\beta = 96°$.

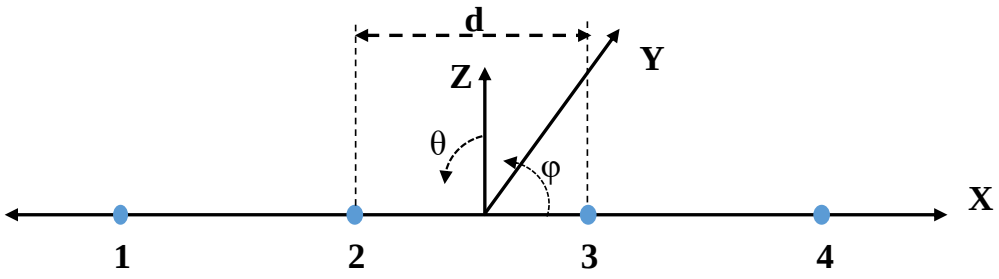


Figure 3-6. An antenna array showing arrangement of antenna (blue dots) in X axis.

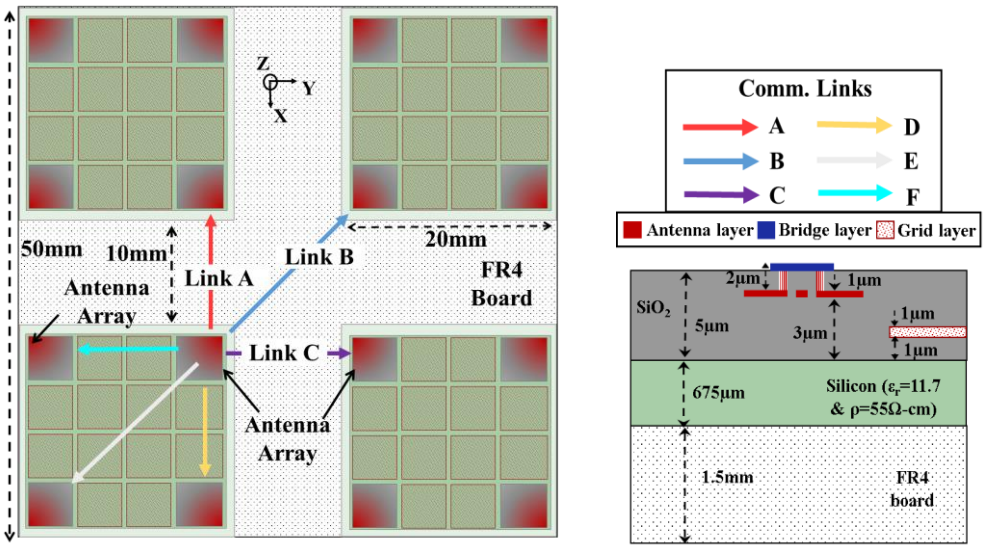
Table 4: Calculated phase (β) for a max beam angle and elemental spacing (d). $\theta_m = 90°$. From Eq. 8.

Elemental Spacing *d*	**Broadside** ($\phi_m = 90°$)	**Endfire** ($\phi_m = 180°$)	**Phased** ($\phi_m = 135°$)
3λ/8	0°	135°	96°

3.4 Simulation results of arrays – Broadside, Phased and Endfire

Before starting with the design of the arrays, first, the setup of MCMC system is discussed. In Figure 3-7, a simplified arrangement of a four-chip MCMC system is shown with its side view, which is influenced by the arrangement shown in section 2.6. Each corner of the chip has a wireless interconnect (WI), which is shown in red color in figure. This WI requires wireless links in fixed directions. Link A, B and C connect wireless interconnects between different chips – inter-chip links, and link D, E and F connect wireless interconnects within the same chip – intra-chip links. So, the radiation from the antenna can be directed towards the desired direction, this might help to improve the transmission coefficients. Further, it will provide flexibility in designing the link budget for the transceiver system.

Since the required beam directions are fixed, multiple directional antennas may be used, but it may increase the area overhead on the chip. However, a phased array uses the same antenna elements to steer the beam in different directions, but a compact feed system is required.



(a) (b)

Figure 3-7. (a) Top view of a multichip multicore system showing various communication links between wireless nodes influenced from previous section 2.6. (b) Side view of the multichip-multicore system. (Not-to-scale)

The angle between link A, B and C is 45°, and same between links D, E and F. So, link B and E can be designed as broadside array, and others can be designed as a phased array with beam max in direction of 45° from the direction of link B and E. As the antenna element in consideration is a zigzag antenna, which is a compressed monopole antenna, shown in Figure 3-8(a). The radiation pattern is expected to be a donut-shaped pattern which has nulls in its axial directions. Therefore, to cover all the link directions, the elements are arranged 45° to the sides of the chip. Moreover, when the elements are arranged and oriented towards the axis of the array as shown in Figure 3-8(b), the total radiation of array in its axial direction is expected to have a null. Therefore, an additional orientation of the antenna is selected where the elements are placed orthogonal to the array axis as shown in Figure 3-8(c). This will help to analyze the endfire array type which has the beam max directed towards the axis of the array. Hence, two different antenna orientation is considered – Axial (A) and Orthogonal (O).

Various techniques to implement phase shift for beamforming are noted in the survey [87] like analog local oscillator (LO) active phase shifter. Even switched delay-line technique which is based on digital phase-shifting using switches either RF MEMS [88] or active CMOS switches [89] may be used. Since, these technologies require the latest CMOS technology nodes, which were not available so passive feed systems are used for demonstration purposes.

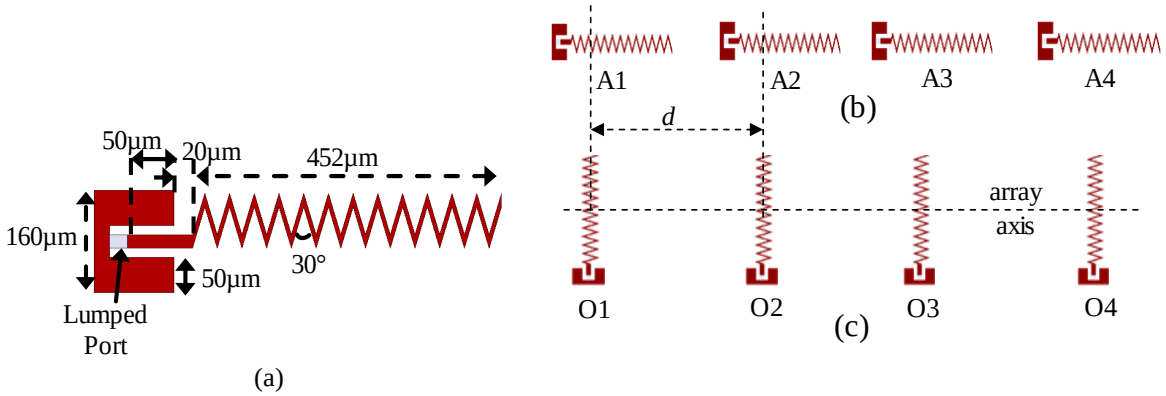


Figure 3-8. (a) Zigzag antenna element, (b) Axial array (A1-A4 are antenna elements), (c) Orthogonal array (O1-O4 are antenna elements).

3.4.1 Design constraints

It is important that before designing arrays, some design constraints should be discussed. The constraints are divided into two parts: fabrication and measurement. Since the process for fabrication of designed arrays is going to be standard CMOS process which is based on lithography. Another constraint for the on-chip arrays is the measurement constraints which is related to the restricted movement of probes.

3.4.1.1 Fabrication constraints

Since the feed system for on-chip arrays to be designed is co-planar waveguide (CPW), it should be noted that it requires a proper connection between the two ground planes. This connection is provided using a bridge that ensures the propagation of CPW mode, without it the transmission between the output ports and input ports of the feed can be severely affected. Moreover, the feed is expected to have bends and curves so the bridge will be helpful. The bridge should be made in another metal layer above the array's metal layer. Figure 3-7 (b) shows the side view of the chip to be designed. Figure 3-9 shows the design of the bridge. Apart from the requirement of the bridge, the fabrication tolerance and multi-layer alignment techniques are important for lithography-based fabrication processes.

It can be seen from the side view picture that the bridge is placed 1 μm above the array layer. Then the connection to the bridge is made using Al metal vias. To allow the fabrication

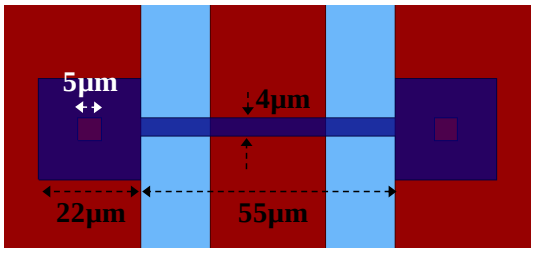


Figure 3-9. Top view of Bridge.

tolerances and multi-layer alignment on multi-layer structures, the bridge is designed with bigger metal contact to the contact cuts as shown in Figure 3-9. The contact cuts (via) are 5µm x 5µm with a height of 1µm. The bridge has large contacts 22µm x 22µm to avoid misalignment between different layers in the fabrication process. The actual bridge between two ground planes is 4µm wide and 55µm long. This bridge contact is used throughout this work. This bridge is not suspended in air but fabricated on the silicon dioxide layer as shown in Figure 3-7 (b).

3.4.1.2 Measurement constraints

The constraints on the design are not only because of the CPW feed and fabrication processes but also because of the measurement setup. A probe station along with a network analyzer is used as the measurement setup. The movement of the GSG probes, which would act as input to the antenna arrays on the chip, is linear motion in 3 dimensions (X, Y, and Z). So this constraint should be taken into account before designing the feed. A picture of the position of 3 probes on the probe station is shown in Figure 3-10.

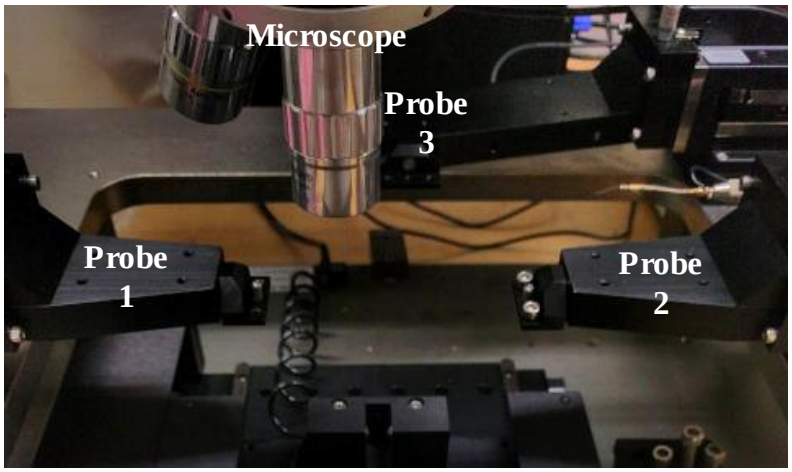
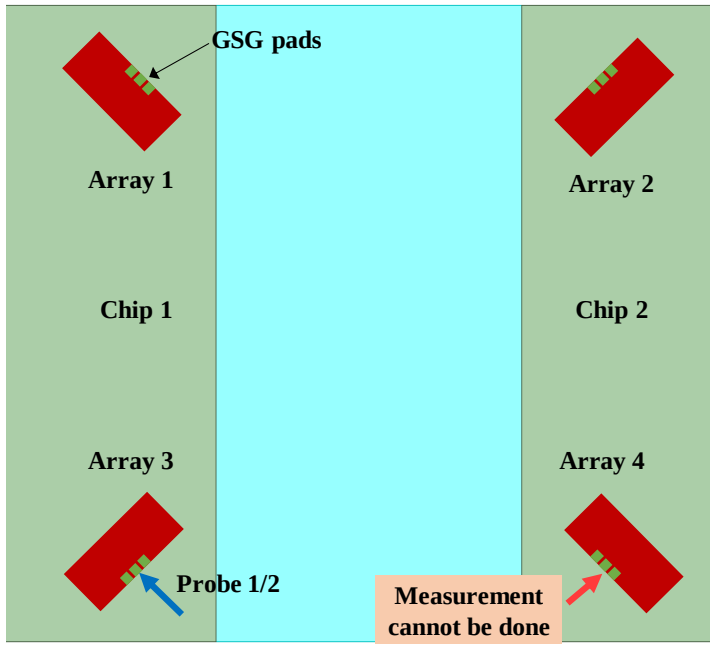
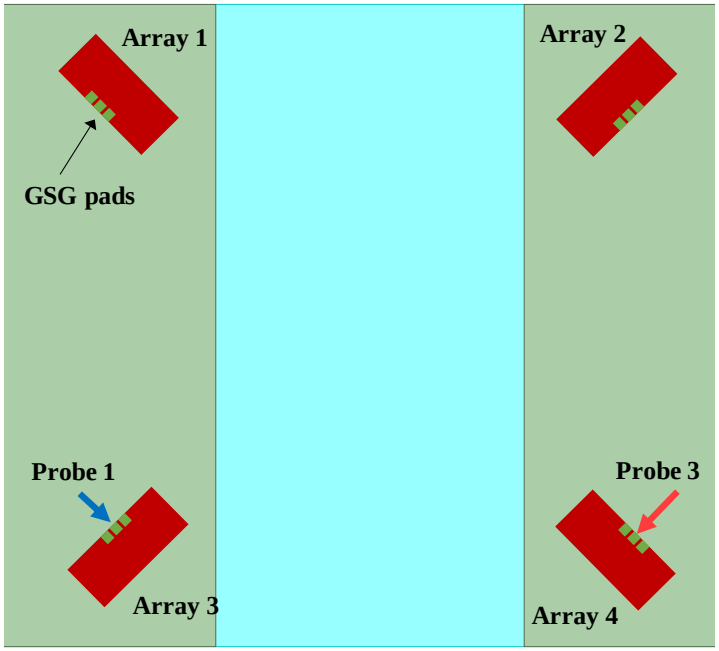


Figure 3-10. Probe position on the probe station.

In Figure 3-11, one of the scenarios is shown which can occur when measuring the transmission between two chips – inter-chip scenario. The GSG probe will land on the GSG pads of the array. However, the orientation of the GSG pads, shown in Figure 3-11 (a), restrict the two



(a)



(b)

Figure 3-11. Picture showing constraint in measurement for inter-chip scenario. (a) location of probe pads and approach of GSG probes not possible. (b) possible solution with flipped probe pads on array.

probes to land on the other GSG pads for measurement. This constraint can be avoided if the design of the array is flipped so that the GSG pads now located on the other side as shown in Figure 3-11 (b). This constraint will affect the inter-chip measurement, therefore, arrays are flipped for the inter-chip scenario. This resolves the measurement constraints.

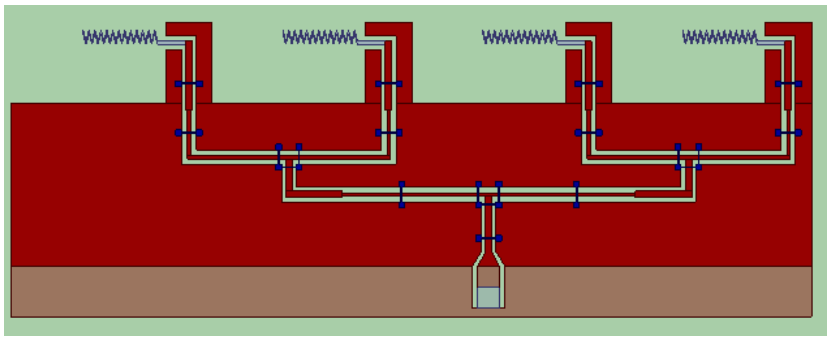
To avoid the restriction of the movement of probes, two different designs of each designed arrays are created for intra- and inter-chip scenario.

3.4.2 Axial Broadside Array

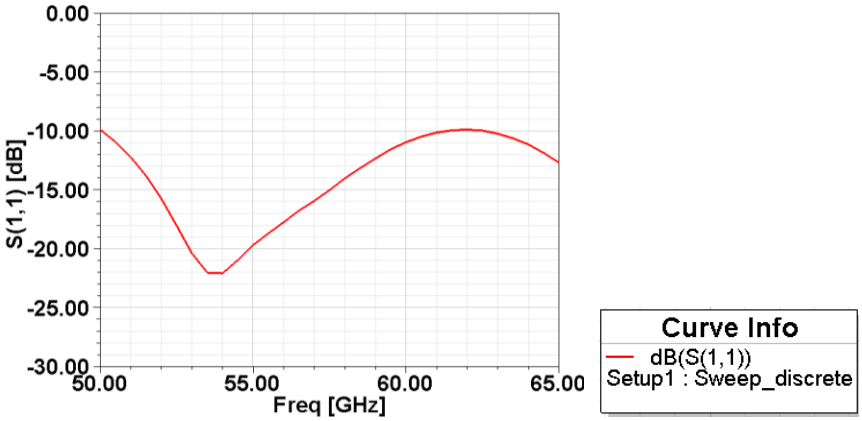
The Broadside array is formed using 4 zigzag antennas oriented along an array axis as shown in Figure 3-12 (a) and (c). This orientation of antennas will direct the radiation in the broadside direction when the phase difference to each element is zero. The antenna elements are kept 0.75mm (center to center) apart which is $3\lambda/8$ distance. A picture of the side view is shown in Figure 3-7.

The feed system is designed to provide a zero phase difference between ports connected to the antenna elements. The feed system consists of three equal power dividers and GSG pads as input. Moreover, the bridges (which are in dark blue in the figure) have met with the fabrication tolerances. These bridges help to maintain CPW mode throughout the feed path. Two different feed structures are created for analysis. One feed structure has an untrimmed ground plane and another has trimmed ground plane. This is to analyze the effect of the change in dimensions of the ground plane.

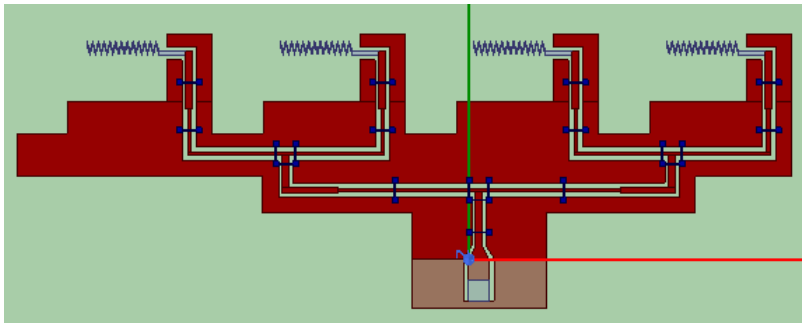
The arrays are optimized in HFSS. The S_{11} for the array at the edge of the silicon chip is shown in Figure 3-12 (b) and (d) for untrimmed-feed and trimmed-feed array, respectively. Although the S_{11} is below -10dB at 60GHz, the array seems to resonate at around 54GHz.



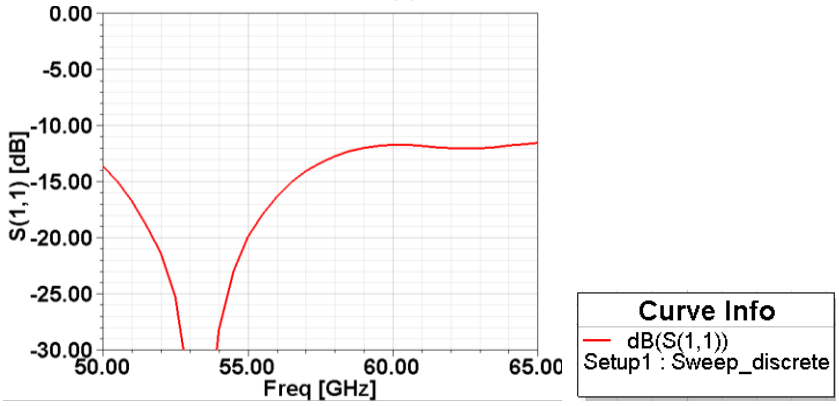
(a)



(b)



(c)



(d)

Figure 3-12. Axial Broadside array with untrimmed ground plane (a) top view, (b) S_{11} plot. Array with trimmed ground plane (c) top view, (d) S_{11} plot.

Now, the transmission coefficients between the arrays are discussed. The aforementioned arrays are arranged at each corner of the chip as shown in Figure 3-13 (a) and (c) for untrimmed-feed and trimmed-feed. Due to the phase variation in the feed structure, arrays 1 & 3 are expected to have a high magnitude of transmission coefficient. The structures are simulated in ANSYS HFSS to find the S-parameters. The intra-chip transmission coefficients between the arrays are shown in Figure 3-13 (b) and (d). The transmission comes out to be as expected with simulated S (3,1) as -35dB at 60GHz for the untrimmed-feed case and -43dB for the trimmed-feed case. It seems like trimming the ground plane is affecting the transmission results. It might be possible that more optimization is required in the trimmed-feed case, but the dimensions are kept constant to compare it with the untrimmed-feed case.

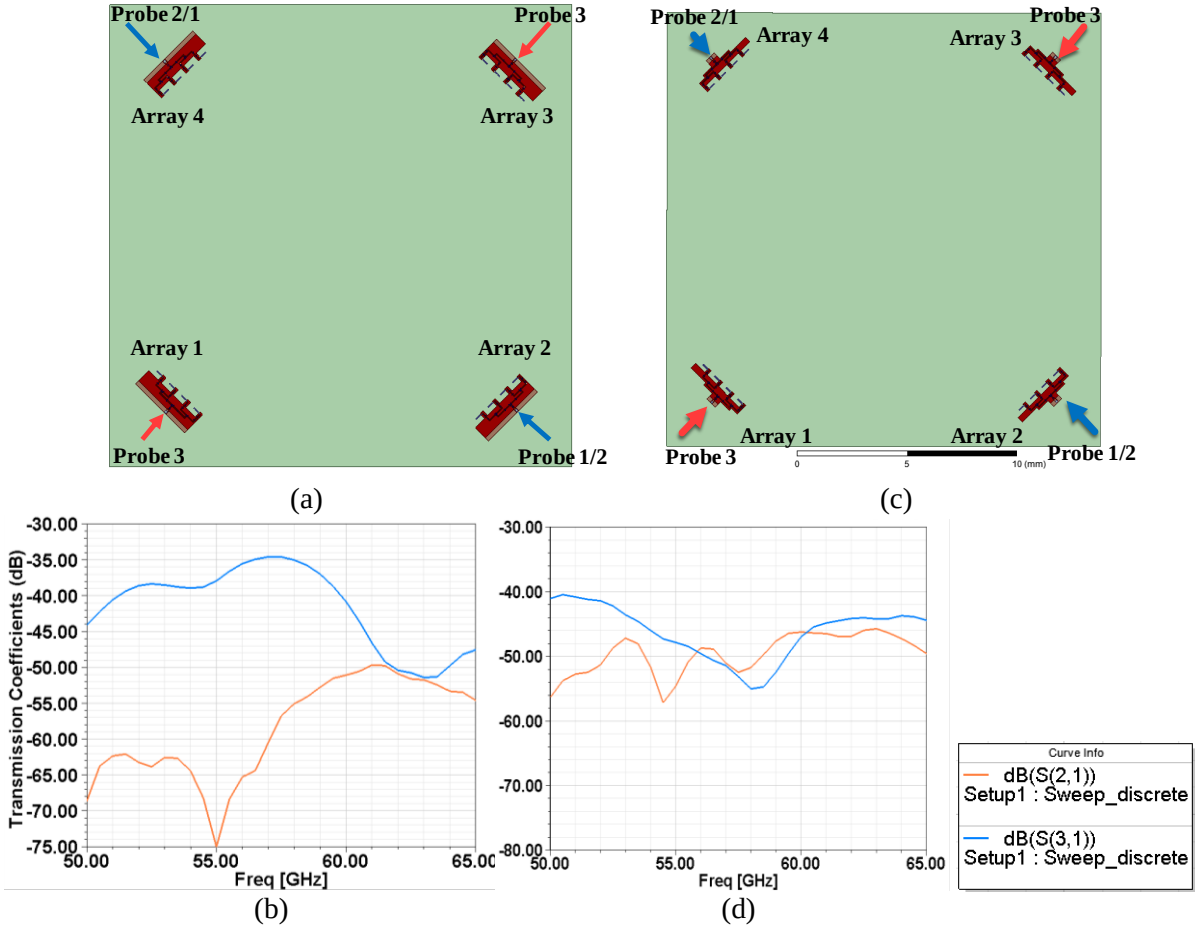


Figure 3-13. Intra-chip scenario: For untrimmed-feed array (a) Top view of the array arrangement, (b) simulated transmission plot. For trimmed-feed array (c) Top view, (d) simulated transmission.

Furthermore, the transmission analysis for the inter-chip case is also shown in Figure 3-14. The simulation scenario has chips placed 10mm apart. There are arrays placed at the edge of the

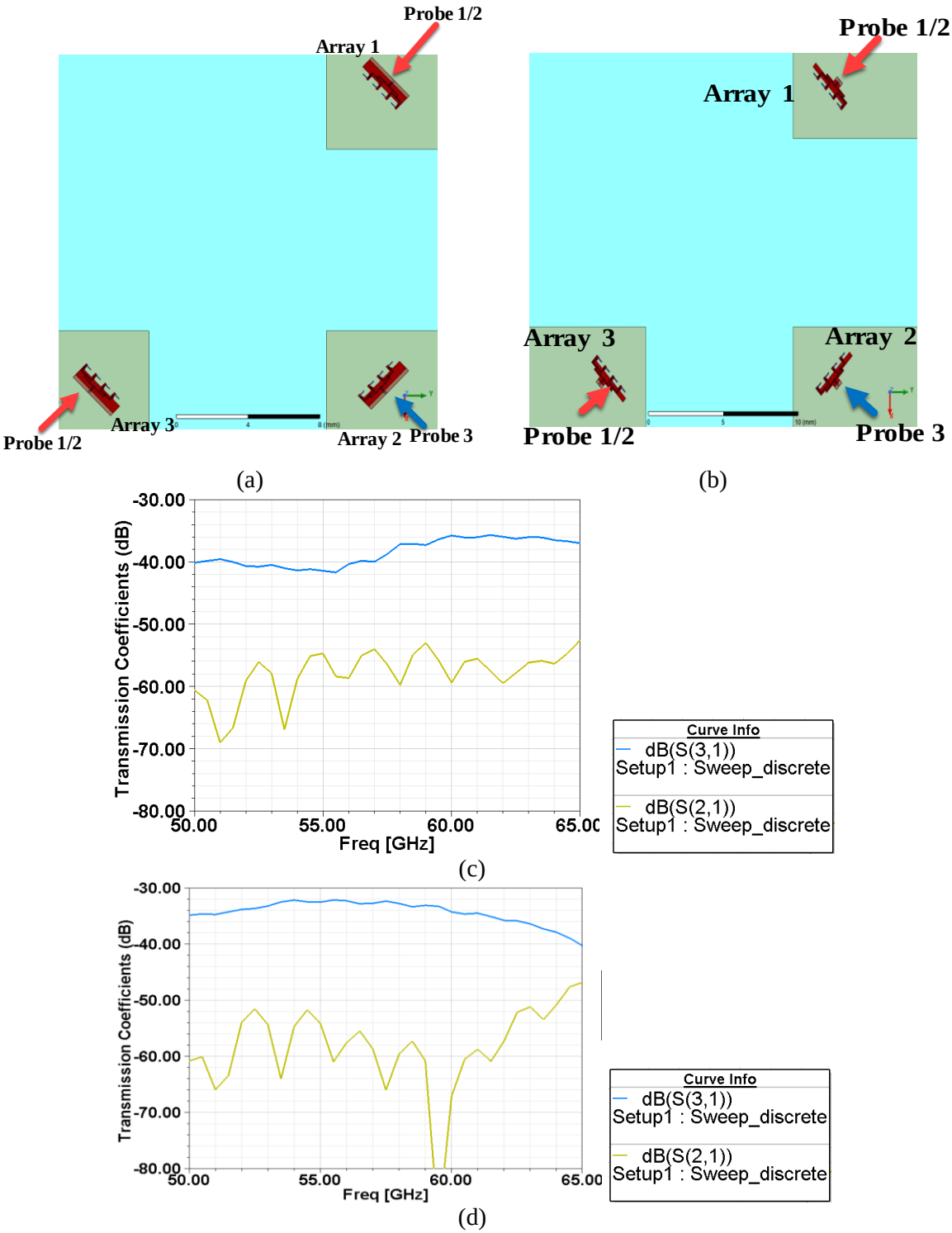
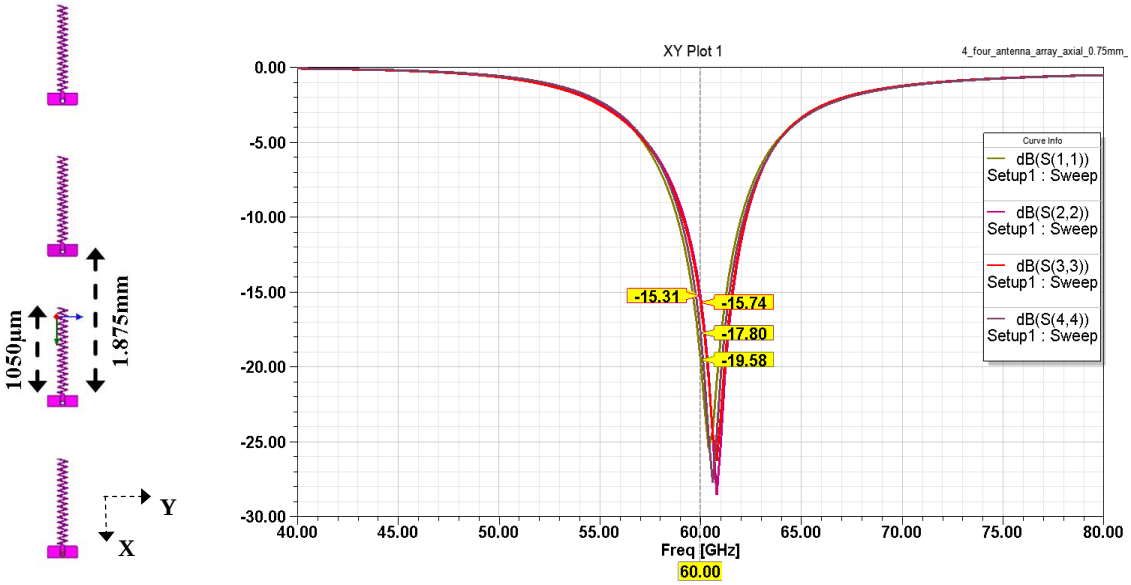


Figure 3-14. Inter-chip scenario: Top view of arrangement for arrays w/ (a) untrimmed-feed, (b) trimmed-feed. Transmission coefficients between arrays w/ (c) untrimmed-feed, (d) trimmed-feed.

chip. These arrangements are simulated in the ANSYS HFSS. The results show that the best transmission occurs as expected between arrays 1 and 3 in both the cases of the untrimmed and trimmed ground plane. The magnitude of simulated transmission coefficient S_{31} is around -35dB.

To study the beamforming in detail, the arrays are simulated without the feed system, where power is provided to the elements through individual HFSS lumped ports. These arrays of antennas are placed in three different environments which are free space, the center of the chip, and the edge of the chip for studying the axial broadside array on the chip. Although the antennas are re-optimized for the free space environment to resonant at the desired frequency, the purpose of this study is to analyze the change in radiation pattern depending on the location of the array on the chip.

First, the antenna array is analyzed in free space. The length of each antenna is optimized to 1050µm for resonance at 60GHz as shown in Figure 3-15 (a). The array is fed using 4 separate



(a) (b)

Figure 3-15. (a) Zigzag antenna axial arrangement in free space, (b) Reflection coefficients.

HFSS lumped ports with in-phase signals. The simulated reflection coefficients of the antenna array are shown in Figure 3-15 (b). It can be seen from the radiation pattern in the plane of the array that is XY plane that the beam is towards the Y-axis, which is the broadside direction.

Now, the antenna array is placed on the chip at different locations and orientations – at the center of the chip and the edge of the chip. Figure 3-16 shows various locations of the array that are (a) is the axial antenna array at the center without feed, (b) is the axial antenna array at the edge without feed, (c) axial array at the center with untrimmed feed system, (d) array at the center

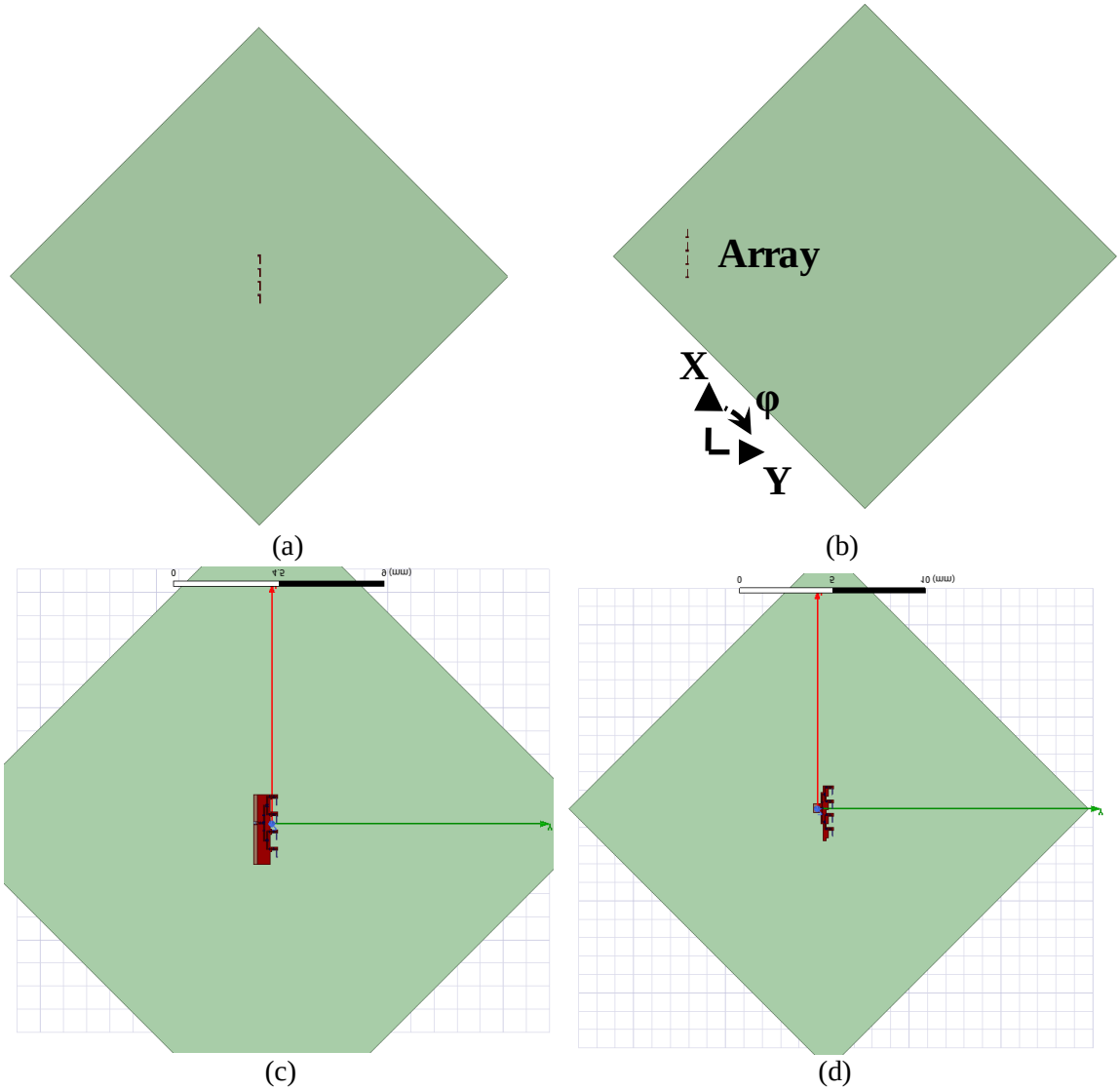


Figure 3-16. (a) Axial zigzag array on the chip in the center, (b) antenna array on-chip at the edge, (c) at the center w/ untrimmed feed, (d) at the center w/ trimmed feed.

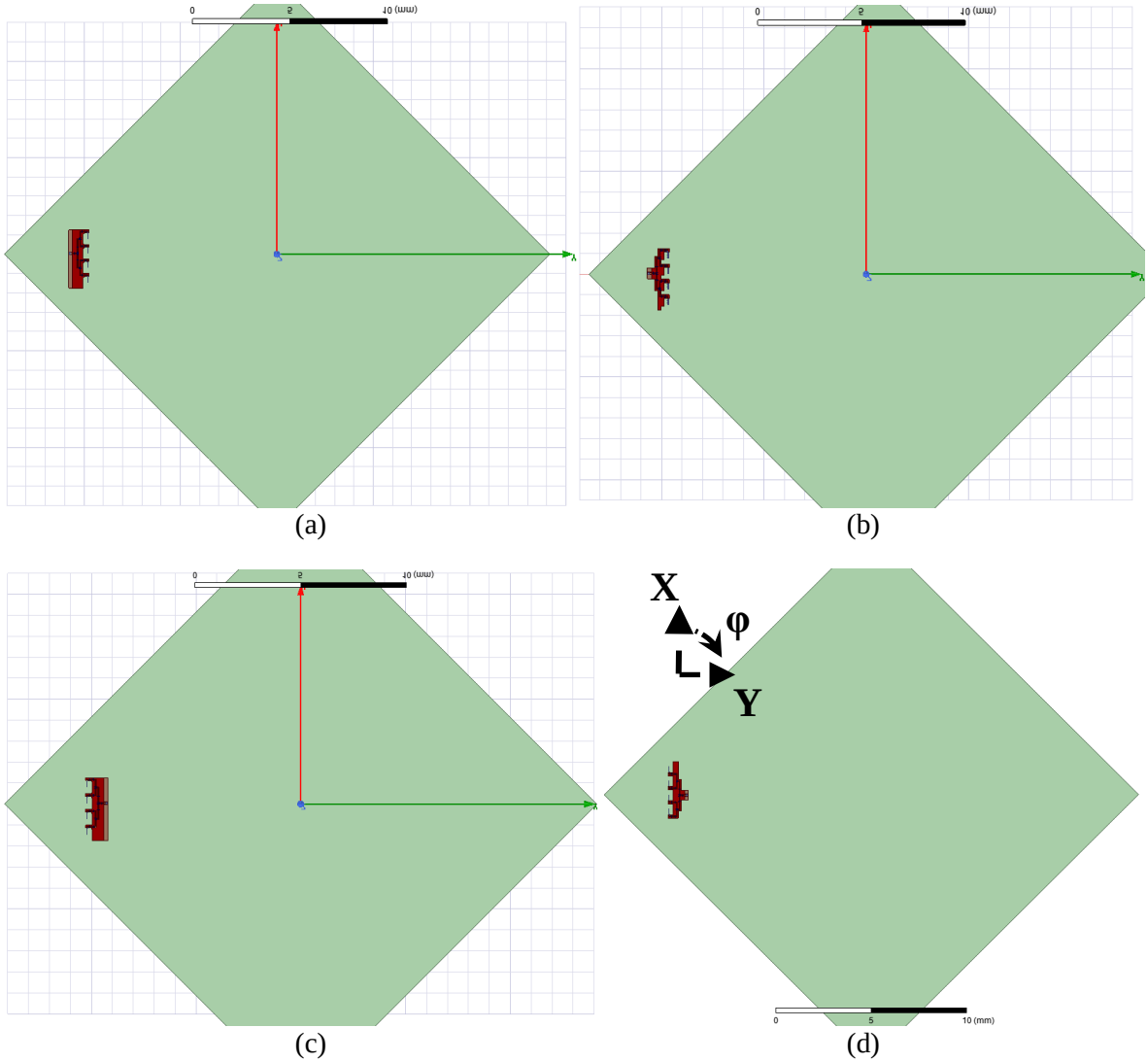


Figure 3-17. Broadside array on chip: (a) at the edge w/ untrimmed feed, (b) at the edge w/ trimmed feed, (c) at the edge flipped w/ feed, (d) at the edge flipped w/ trimmed feed.

with trimmed feed system, and in Figure 3-17 (a) axial array at the edge with untrimmed feed system, (b) array at the edge with trimmed feed system, (c) axial array at the edge (flipped orientation) with untrimmed feed system, (d) array at the edge (flipped orientation) with trimmed feed system. The radiation pattern and distribution of the electric field are discussed next.

The radiation patterns in the XY plane, corresponding to different environments and locations of the array discussed previously are shown in Figure 3-18. First, the radiation pattern of the array in free space is shown in Figure 3-18 (a) for comparison purposes. Figure 3-18 (b) shows

the radiation pattern of the array on the chip without a feed at the center. The array without a feed at the center of the chip, shown in Figure 3-16 (a), has a symmetrical environment that is the dimension of the chip around it, therefore the radiation pattern is symmetrical in shape with the radiation pattern in free space, but the gain is lower due to the losses in the silicon substrate. When

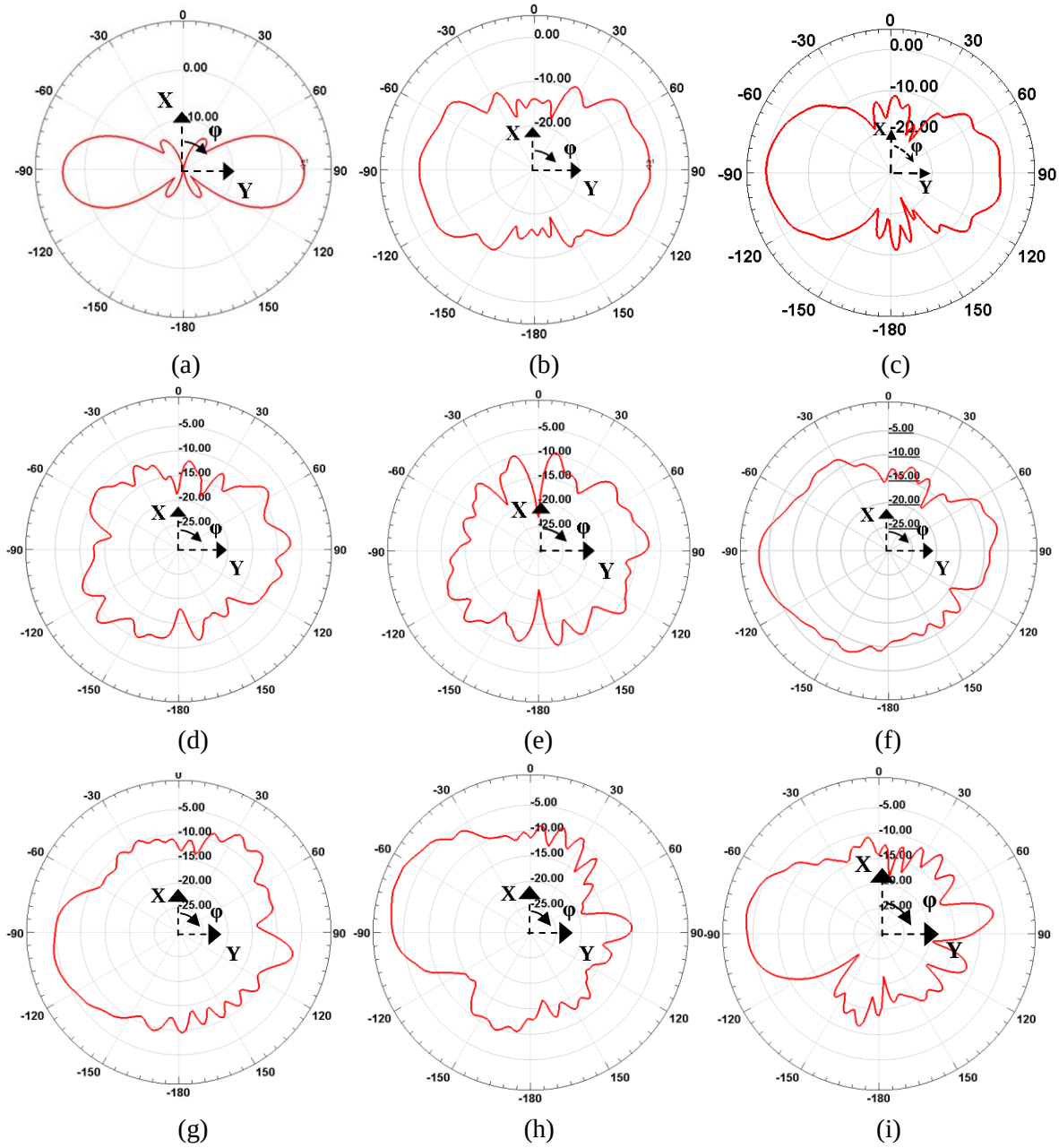


Figure 3-18. Radiation pattern of zigzag antenna broadside array in relevant XY plane (a) in free space, (b) on chip at the center, (c) on chip at the edge, (d) on chip at the center w/ feed, (e) on chip at the center w/ trimmed feed, (f) on chip at the edge w/ feed, (g) on chip at the edge w/ trimmed feed, (h) on chip at the edge flipped w/ feed, (i) on chip at the edge flipped w/ trimmed feed.

the array is moved to the edge of the chip as shown in Figure 3-16 (b), the radiation pattern has lost its symmetry shown in Figure 3-18 (c). Higher gain can be observed towards the side closer to the air that is – Y-axis direction, and lower gain towards Y-axis direction. There is large lossy silicon towards +Y-axis which is reducing the gain.

Figure 3-16 (c) shows an array with an untrimmed-feed located at the center of the chip. The radiation pattern that is shown in Figure 3-18 (d) is little distorted compared to the radiation pattern of the array w/o feed as plotted in Figure 3-18 (b). When the array w/ untrimmed feed is moved to the edge shown in Figure 3-17 (a), a better beam can be observed in the corresponding radiation pattern shown in Figure 3-18 (f). This is due to the air environment which is on the –Y-axis of the array. Moreover, the loss in the silicon substrate reduces the beam in the Y-axis direction, so the gain in that direction is reduced compared to the –Y-axis direction. Similarly, other radiation patterns for other locations of the array is shown in Figure 3-18. There is little variation of the gain with a similar shape of radiation pattern when arrays with untrimmed and trimmed feed are compared.

In Figure 3-19, the distribution of the electric field is shown corresponding to various locations of the array on the chip with both types of feed structures. Higher distribution of electric field shows that the radiation towards the beam max.

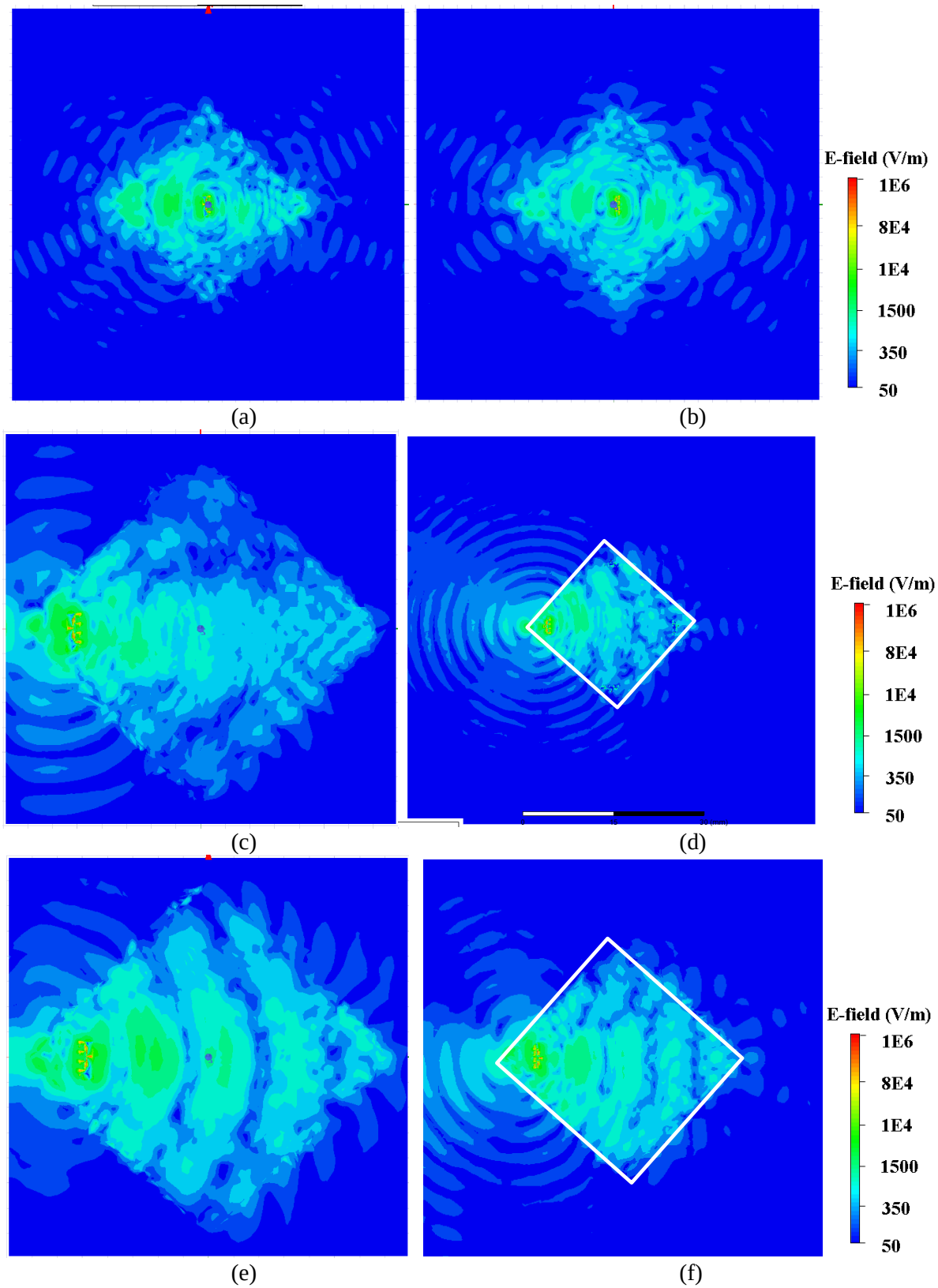


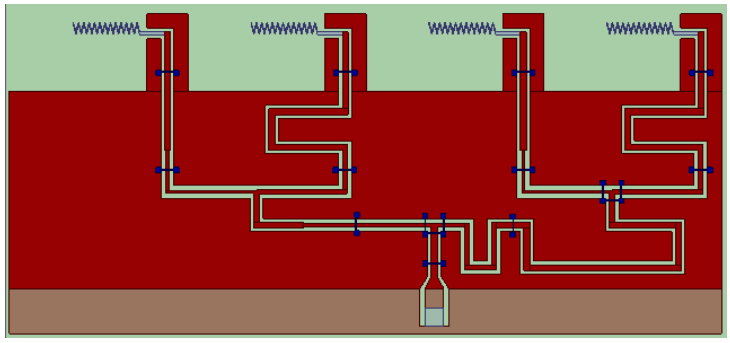
Figure 3-19. Electrical Field distributions (a) at the center w/ feed, (b) at the center w/ trimmed feed, (c) at the edge w/ feed, (d) at the edge w/ trimmed feed, (e) at the edge flipped w/ feed, (f) at the edge flipped w/ trimmed feed.

3.4.3 Axial Phased array

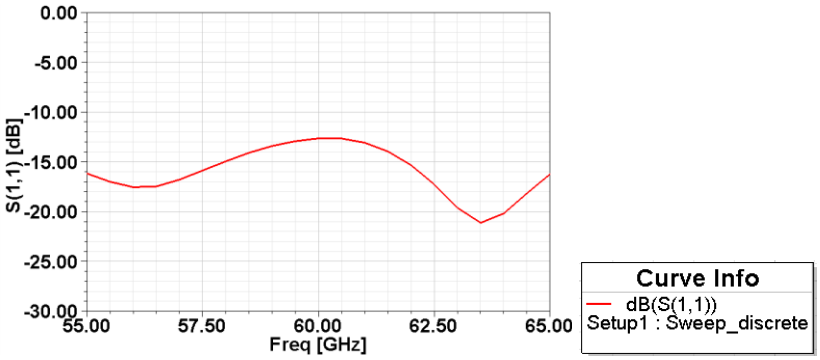
For phased array, the beam direction is required to be 45° from the broadside beam. This is achieved by using a phase difference of approximately 96° according to the theoretical formula in Eq. (8).

The antennas implemented here is the same as the broadside case, however, the feed system has changed because of the phase progression of 96°. The length of the CPW line is changed to different lengths as shown in Figure 3-20. The longer CPW lines are meandered to compress its length. Similar to the broadside feed system, the two ground of the CPW line is shorted at regular intervals, mostly after bends, to have the feed lines propagate the CPW mode. The connection is made using a bridge as per the discussion in the previous section. Moreover, the extra ground plane is trimmed off to analyze two different cases of – trimmed and untrimmed feed structures. The arrays are simulated in HFSS. The plots of the reflection coefficient are shown in Figure 3-20. The reflection coefficients of the array are around -15dB at 60GHz, which is satisfactory for demonstrating the operation of arrays.

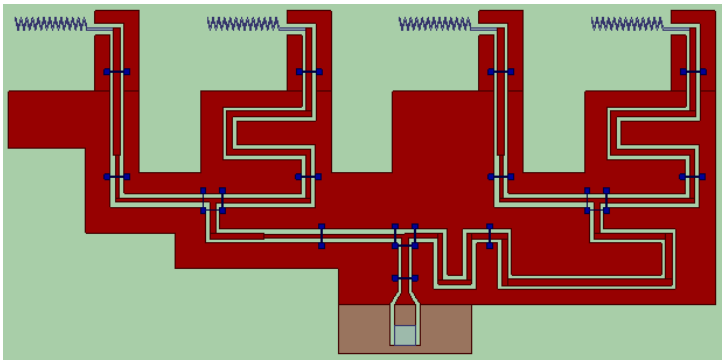
Similar to the previous case, the transmission analysis for an intra-chip case is performed by arranging four antenna arrays at all corner locations of a chip. The simulated transmission coefficients for intra-chip scenario are plotted in Figure 3-21. Due to the phase variation in the feed, the beam max of arrays 2 and 3 are directed towards each other, so the highest transmission coefficients are expected between them. The highest simulated transmission is -40dB at 60GHz for untrimmed-feed case. Other transmission for untrimmed-feed case is below -50dB at 60GHz. For trimmed-feed case, the transmission between array 2 and 3, S_{32}, is reduced to -45dB. It might be the trimmed ground is affecting the transmission.



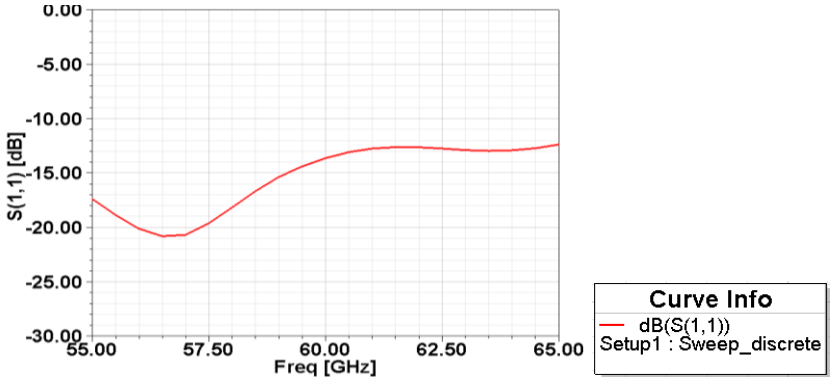
(a)



(b)



(c)



(d)

Figure 3-20. (a) Axial phased array with untrimmed feed, (b) magnitude of S_{11}, (c) axial phased array with trimmed feed, (d) magnitude of S_{11}.

Also, the transmission is analyzed for inter-chip scenario. The pictures of scenarios and plots of transmission coefficients are shown in Figure 3-22. The phase variation in the feed is provided so that the highest transmission is between arrays 1 and 2. The transmission in the case of inter-chip between untrimmed-feed array 1 and 2, S_{21}, which is -40dB at 60GHz. This is higher

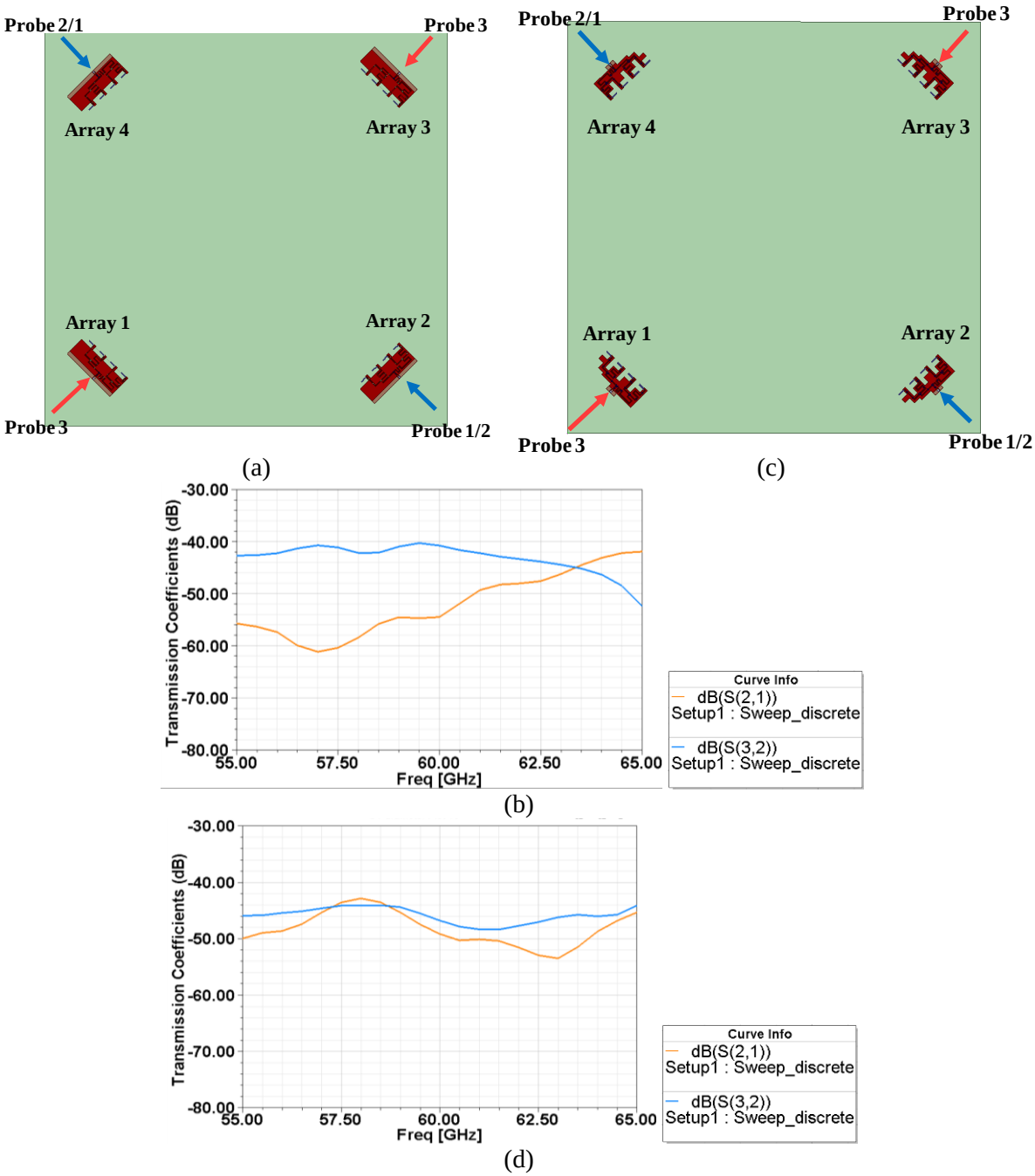


Figure 3-21. Intra-chip scenario: For untrimmed-feed array (a) Top view of the array arrangement, (b) simulated transmission plot. For trimmed-feed array (c) Top view, (d) simulated transmission.

than the other transmissions shown in the transmission plot Figure 3-22 (c). For trimmed-feed case, the highest transmission coefficient, S_{21}, is -37dB shown in Figure 3-22 (d). It can be observed from the plot that transmission coefficients between other pairs like S_{43} are lower by 10dB or more. This shows that the arrays are working as expected.

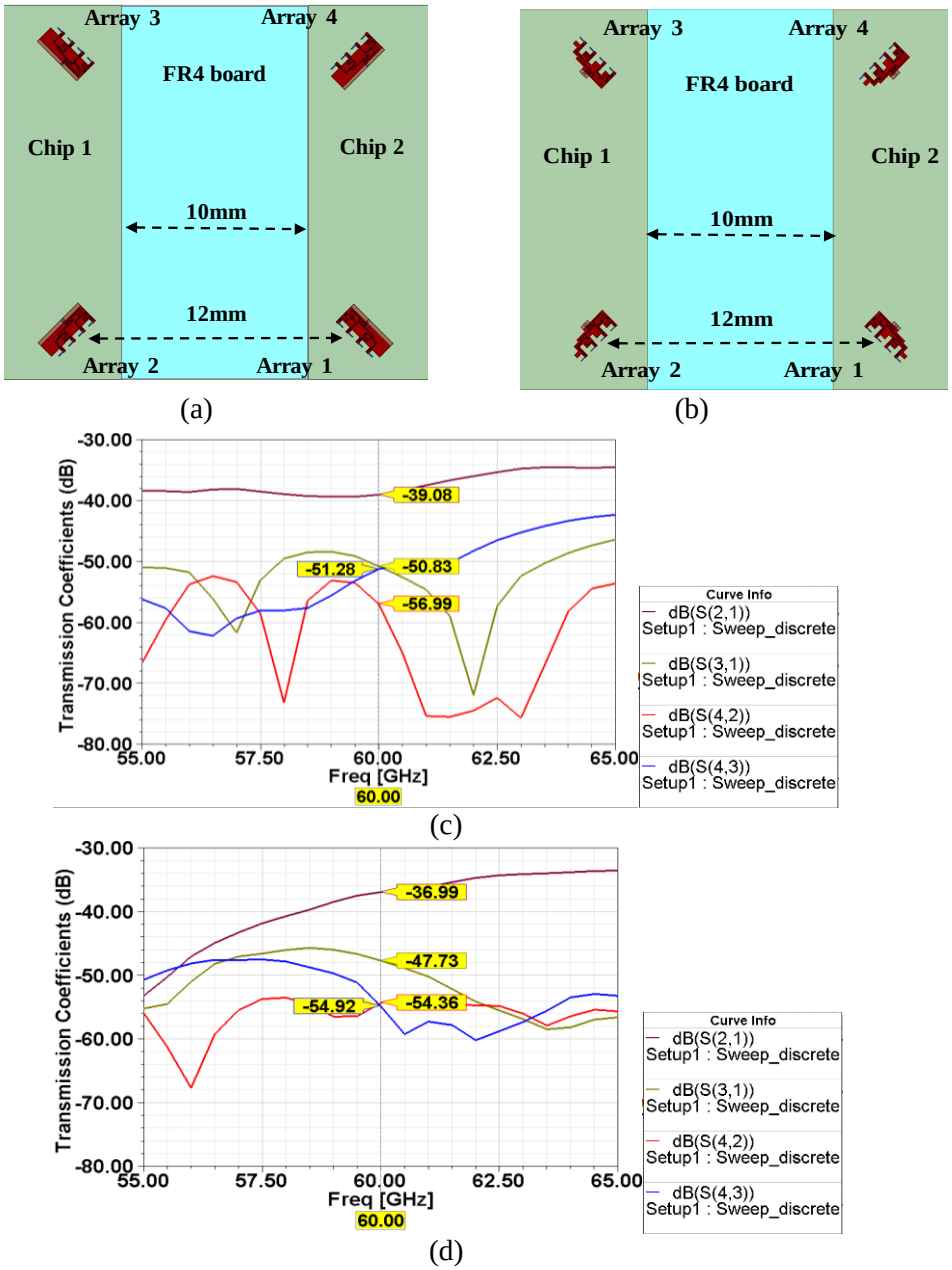


Figure 3-22. Inter-chip scenario: Top view of arrangement for arrays w/ (a) untrimmed-feed, (b) trimmed-feed. Transmission coefficients between arrays w/ (c) untrimmed-feed, (d) trimmed-feed.

To study the beamforming in a phased array, the radiation pattern and electric field are plotted for arrays at different locations, similar to broadside array case. The locations of the array on the chip are shown in Figure 3-23 and Figure 3-24. The radiation patterns of the array corresponding to the locations are shown in Figure 3-25. For the free-space radiation pattern, the array shown in Figure 3-15 for the broadside array is used. The phases at individual lumped ports are changed progressively to 96°. The radiation pattern is shown in Figure 3-25 (a), a beam is towards 45° from the X-axis can be observed. The other beam at -45° can also be seen and is unavoidable due to the nature of the linear array.

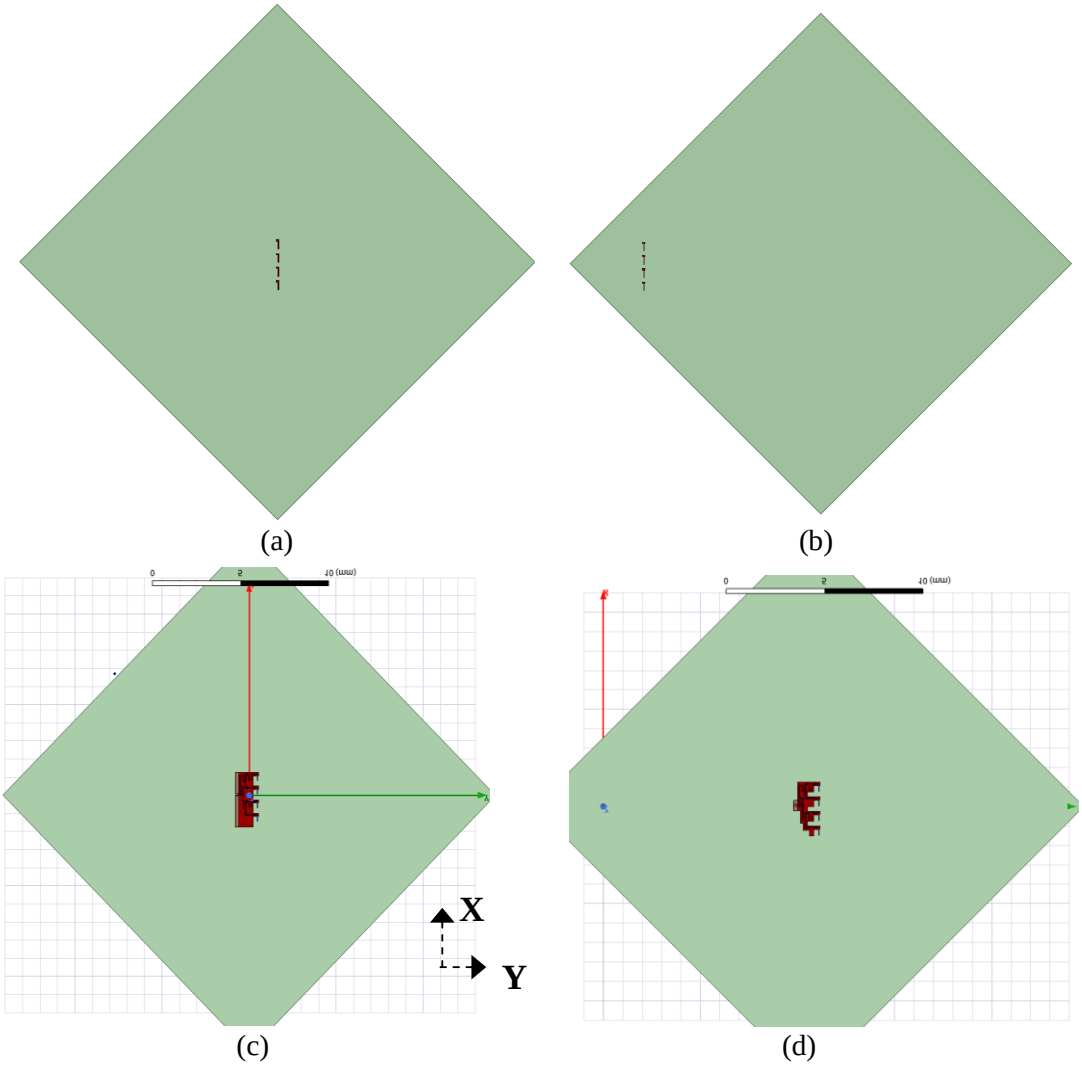


Figure 3-23. Antenna array on chip: (a) at the center w/o feed, (b) at the edge w/o feed, (c) at the center w/ feed, (d) at the center w/ trimmed feed.

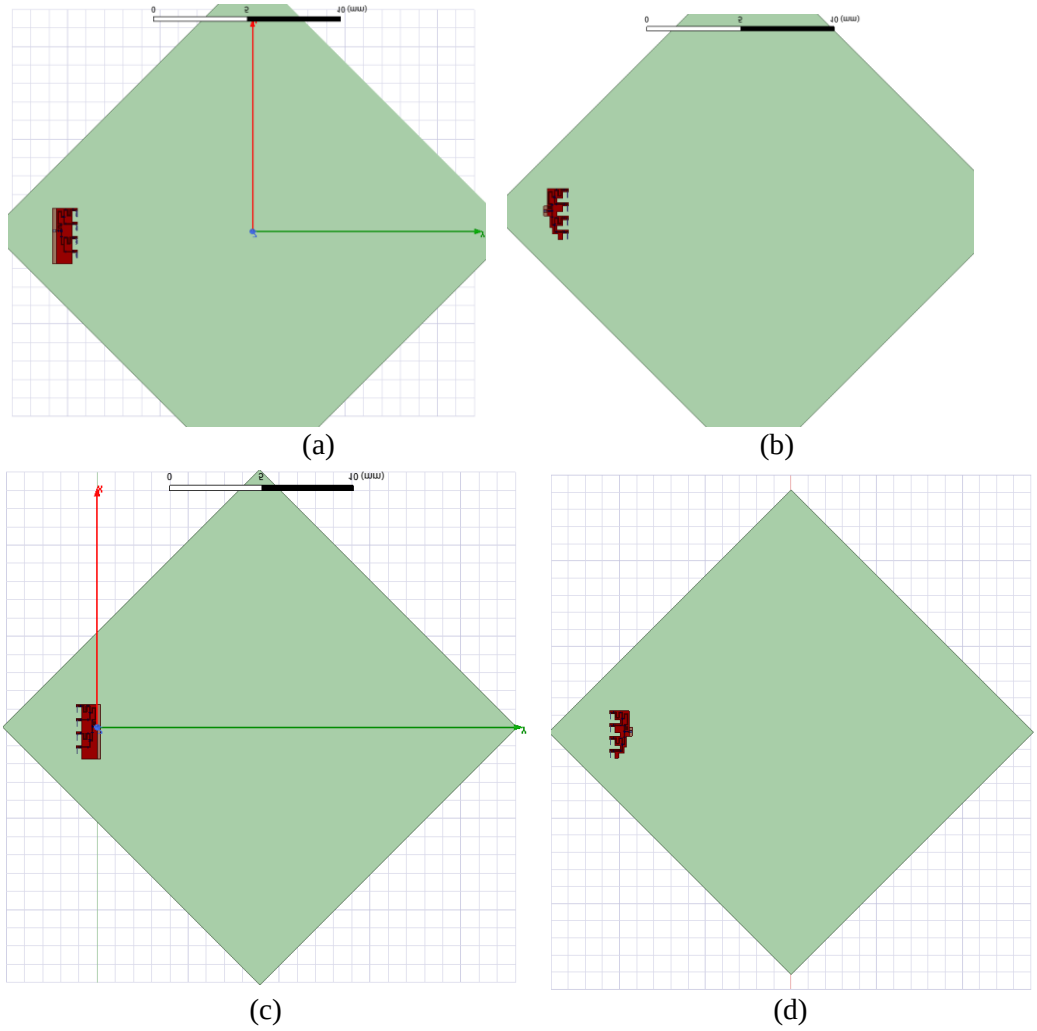


Figure 3-24. Antenna array on chip: (a) at the edge w/ feed, (b) at the edge w/ trimmed feed, (c) at the edge flipped w/ feed, (d) at the edge flipped w/ trimmed feed.

When the array with the individual lumped port is kept on the silicon chip at the center as shown in Figure 3-23 (a), then the radiation pattern has drastically changed as shown in Figure 3-25 (b). However, when the array is moved to the edge like in Figure 3-23 (b), then a beam is seen towards -45° and another beam towards +45° seems distorted. This is happening because +45° direction has a significantly more lossy silicon substrate, which is reducing the gain of that beam. When the array with the feed is placed in the center of the chip in Figure 3-23 (c) and (d), which generates radiation pattern shown in Figure 3-25 (d) and (e), respectively, significant distortion to the beam can be observed. When the array with feed is placed at the edge of the chip

as shown in Figure 3-24, a bigger beam towards the air that is -45° direction from X-axis can be observed and a smaller beam towards -45° from X-axis can be seen in Figure 3-25. The reason is significant lossy silicon substrate on one side of the array. Furthermore, the electric field is also shown in Figure 3-26 which provides further details on the radiation.

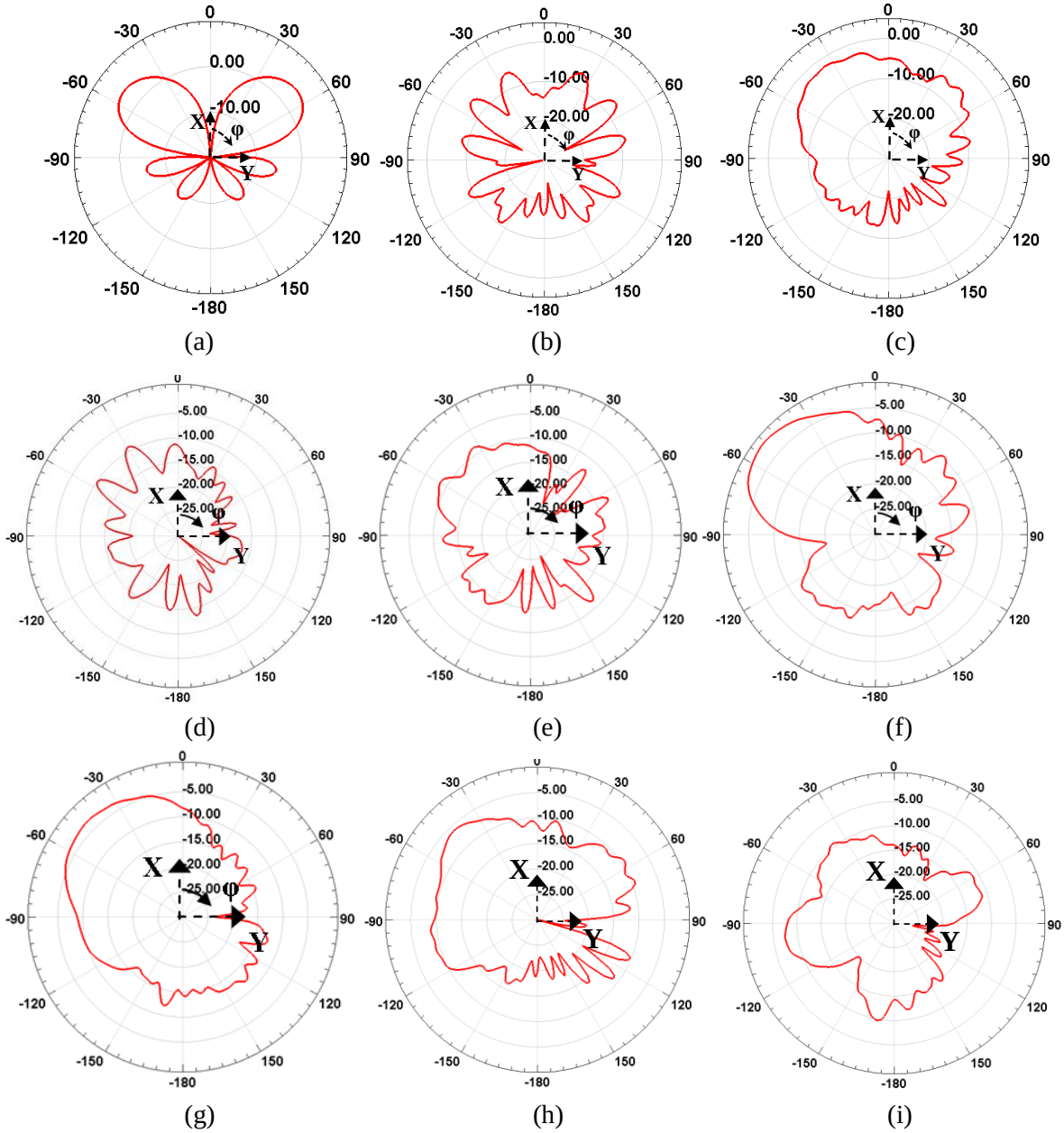


Figure 3-25. Radiation pattern of zigzag antenna broadside array in relevant XY plane (a) in free space, (b) on chip at the center, (c) on chip at the edge, (d) on chip at the center w/ untrimmed feed, (e) on chip at the center w/ trimmed feed, (f) on chip at the edge w/ feed, (g) on chip at the edge w/ trimmed feed, (h) on chip at the edge flipped w/ feed, (i) on chip at the edge flipped w/ trimmed feed.

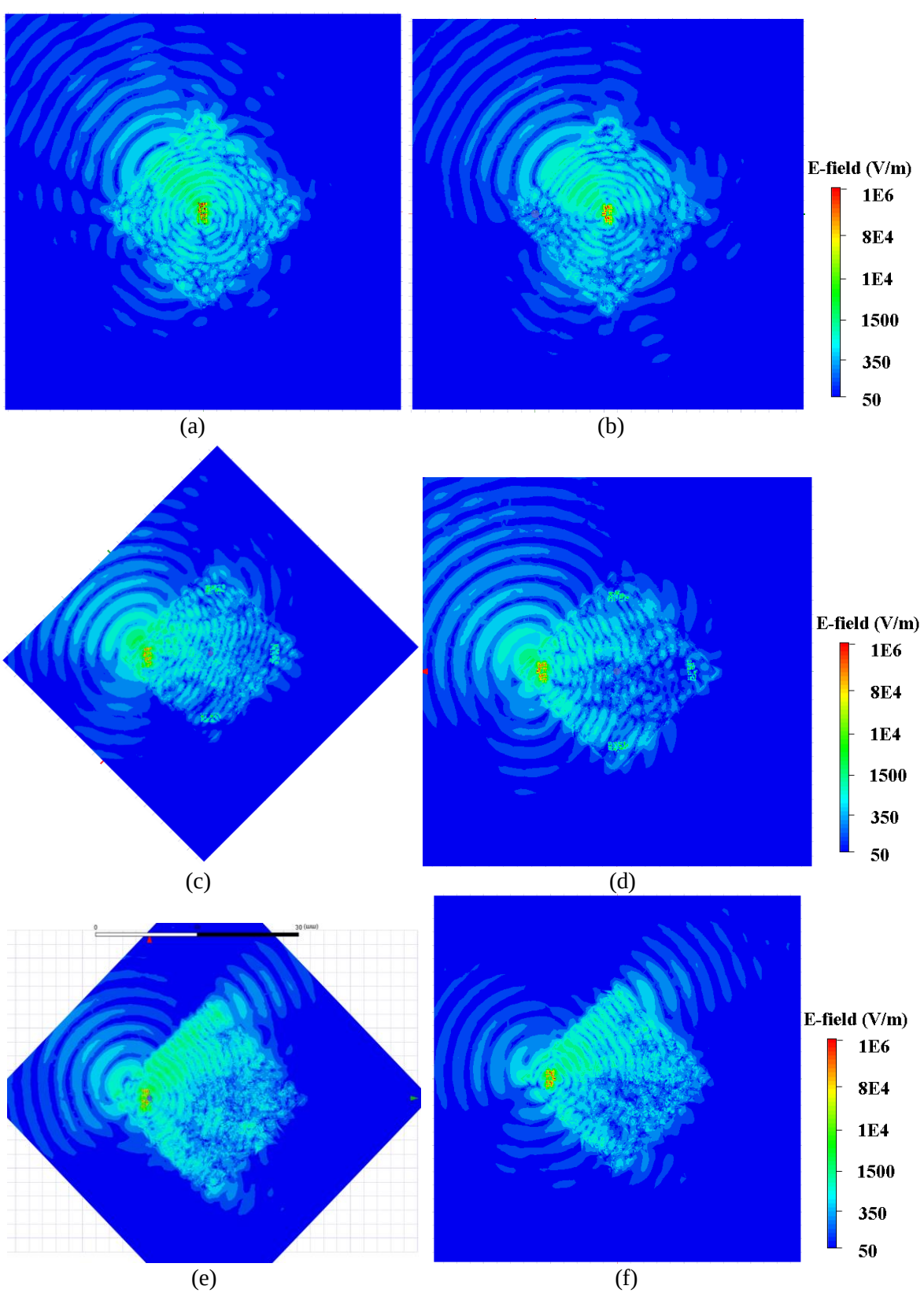


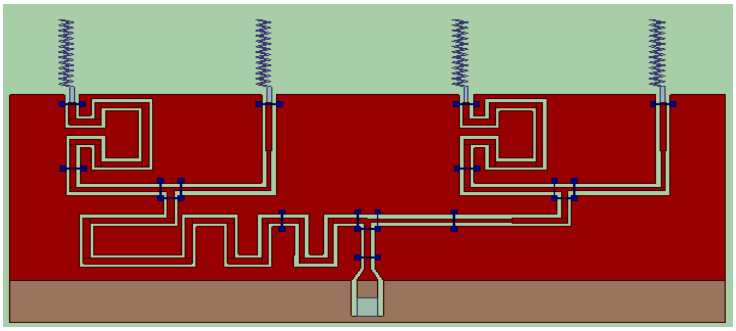
Figure 3-26. Simulated electrical field distributions (a) at the center w/ feed, (b) at the center w/ trimmed feed, (c) at the edge w/ feed, (d) at the edge w/ trimmed feed, (e) at the edge flipped w/ feed, (f) at the edge flipped w/ trimmed feed.

3.4.4 Orthogonal Endfire

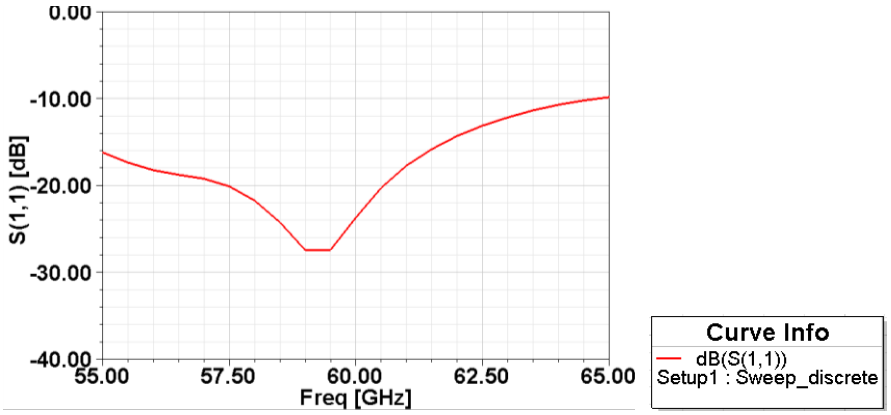
Lastly, the design of orthogonally-oriented endfire array is discussed. This design uses the zigzag antennas that are oriented towards the Y-axis, or the direction which is orthogonal to the axis of the array, so it is called “orthogonal endfire”. Using theoretical equations in section 3.3, the progression phase difference for an endfire beam is found to be 135°.

The feed system for the four-antenna array is designed in HFSS. The array with untrimmed-feed is shown in Figure 3-27 (a). Another design with excessive ground plane trimmed off is shown in Figure 3-27 (c). The simulated reflection coefficient for both the cases is shown in Figure 3-27 (b) and (d). The antenna arrays are optimized as much as possible. The S_{11} for the untrimmed-feed case is -20dB at 60GHz, and S_{11} for the trimmed-feed case is -25dB at 60GHz.

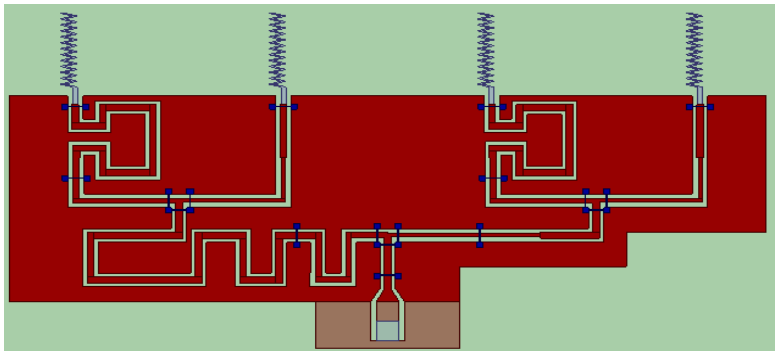
Now, the transmission analysis has been performed for endfire design. First, for the intra-chip scenario, the simulation is performed with four antenna arrays located at each corner on a single chip. The transmission results are shown in Figure 3-28. Due to the phase distribution of feed, the arrays 3 and 4 are expected to have the highest transmission, which is -37dB at 60GHz in case of untrimmed ground feed. For arrays with trimmed ground feed, the transmission S_{43} comes out to be -38dB at 60GHz. The transmission between other array pairs is less than -45dB at 60GHz. The difference between the highest transmission and second to the best is more than 6dB.



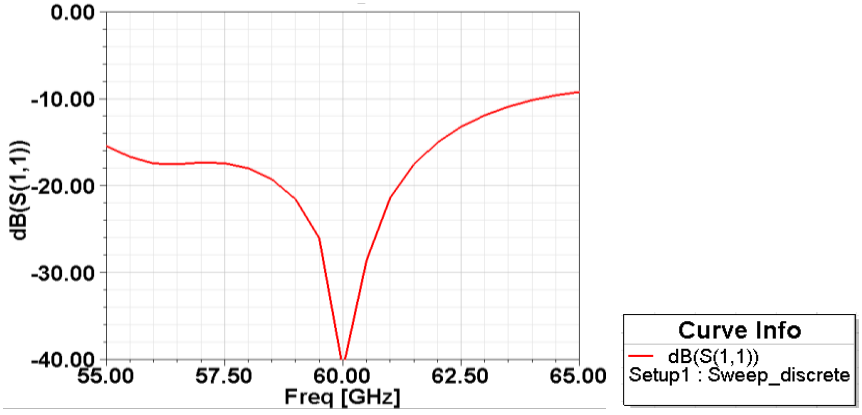
(a)



(b)



(c)



(d)

Figure 3-27. Orthogonal endfire array: (a) Top view with untrimmed feed, (b) S_{11}plot, (c) Top view of array with trimmed feed, (d) S_{11} plot for array with trimmed-feed.

Furthermore, the transmission analysis is performed for the inter-chip case. The simulation is performed to find the transmission coefficients between arrays of two different chip. The simulation scenarios along with the results are shown in Figure 3-29. Due to the phase variation of feed, array 1 and 2 is expected to have the highest transmission. From Figure 3-29 (c) and (d),

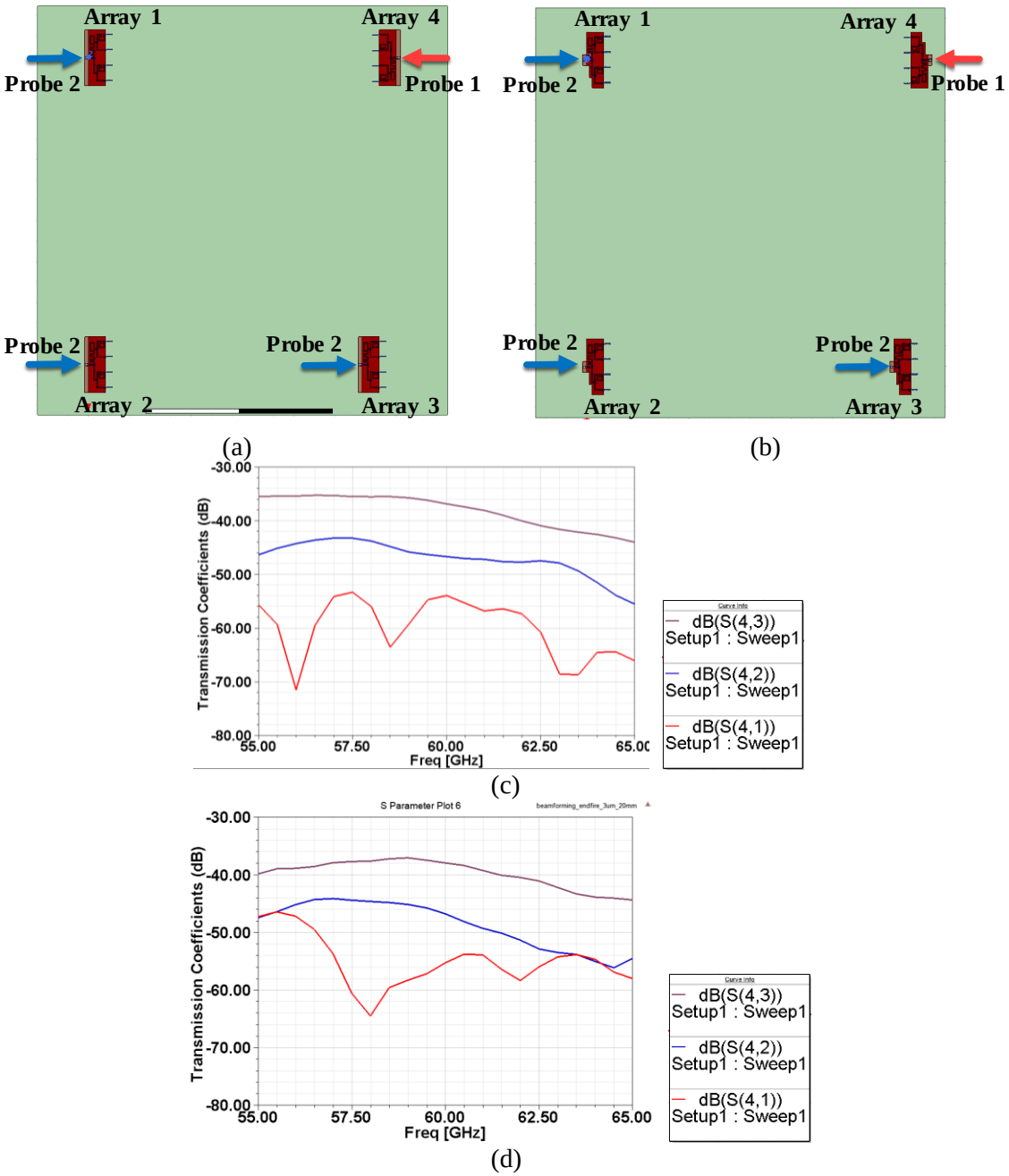


Figure 3-28. Intra-chip scenario: For untrimmed-feed array (a) Top view of the array arrangement, (b) simulated transmission plot. For trimmed-feed array (c) Top view, (d) simulated transmission.

it can be seen that the transmission between array 1 and 2 which is -34dB and -33dB at 60GHz for untrimmed and trimmed feed cases, respectively. Transmissions between other array combinations are 10dB below the highest transmission.

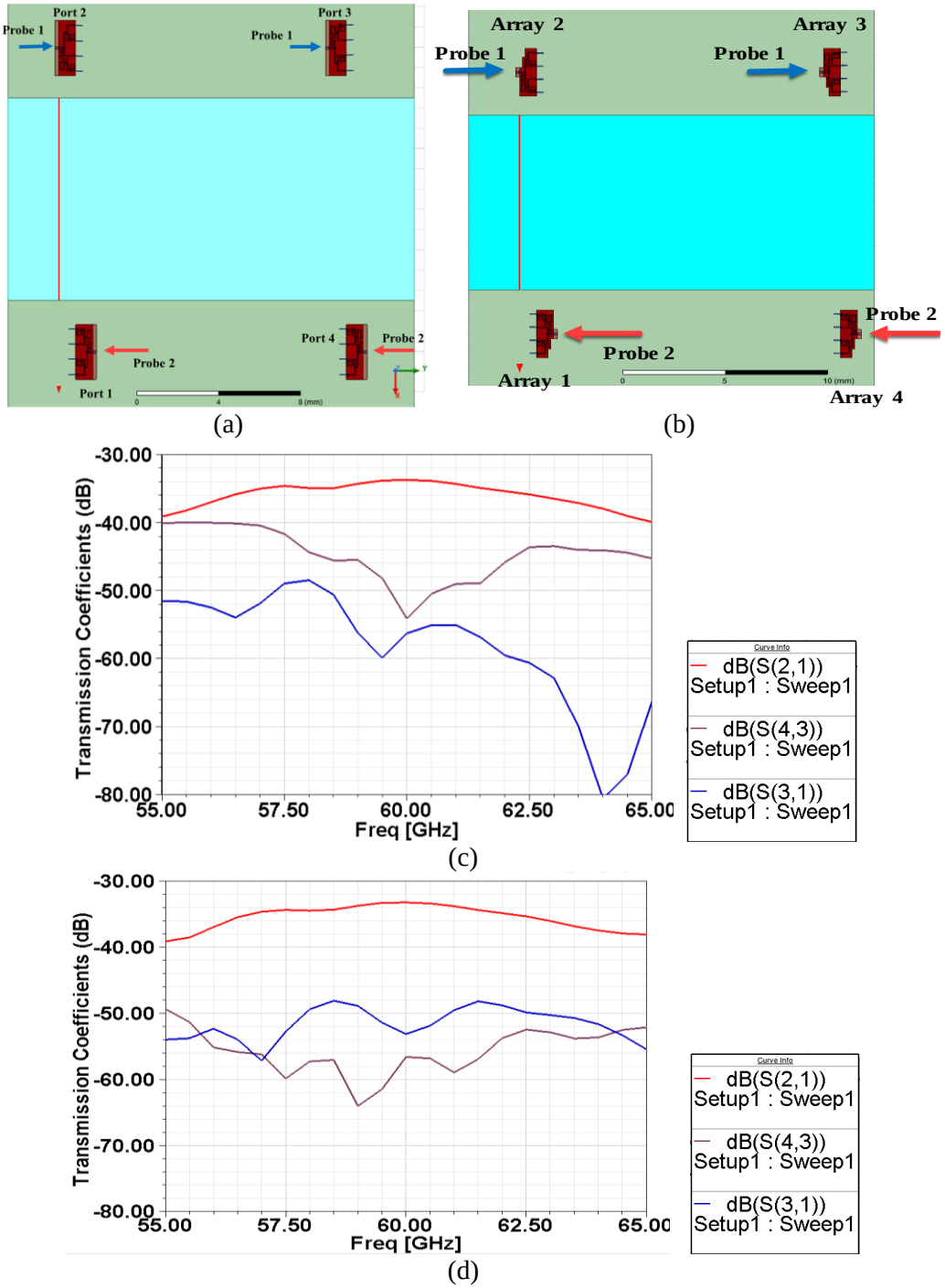
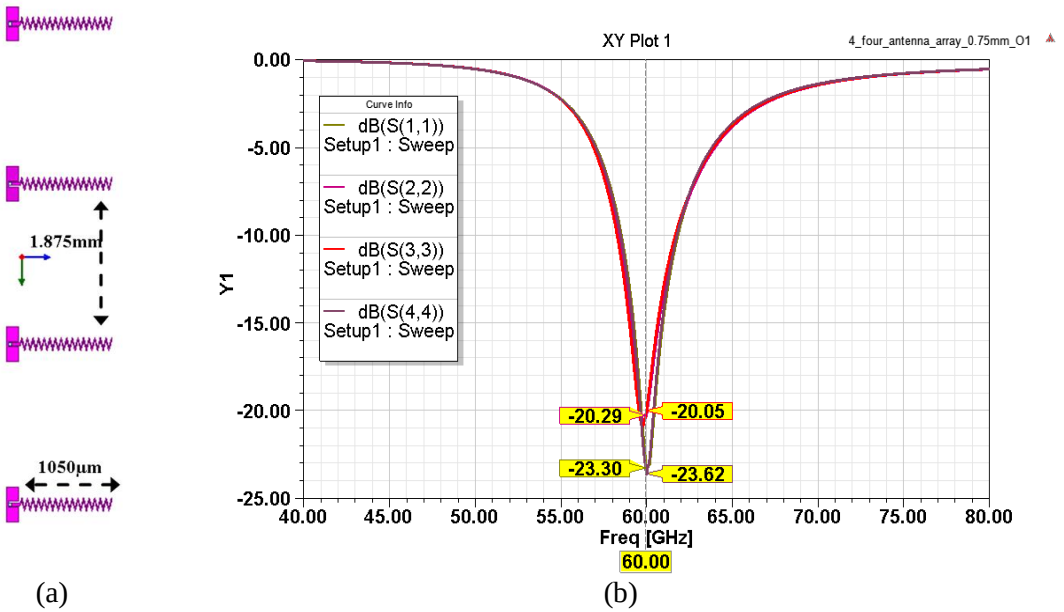


Figure 3-29. Inter-chip scenario: Top view of arrangement for arrays w/ (a) untrimmed-feed, (b) trimmed-feed. Transmission coefficients between arrays w/ (c) untrimmed-feed, (d) trimmed-feed.

Similar to the above cases, the radiation pattern and electric field in arrangement with the array in various locations are discussed. First, the antenna array is simulated in free space as shown in Figure 3-30 (a). The antennas are re-optimized for free space with a length of 1050μm and a spacing of 1.875mm. The reflection coefficients in Figure 3-30 (b) shows that the antennas are resonating at frequency 60GHz. It can be seen in Figure 3-33 (a) that the radiation pattern in the free space has a beam in the direction of the array axis that is towards –X-axis direction.

Next, the array without a feed system is placed on the center of the chip as shown in Figure 3-31 (a). In Figure 3-33 (b), the radiation pattern shows that there is a beam towards -X-axis. Similar to previous cases when the array is placed at the center of the chip, the radiation pattern gets distorted by the lossy chip and diffraction at the chip edges. Now, the array with feed system is placed at the center shown in Figure 3-31 (c) and (d), the radiation pattern is shown in Figure 3-33 (d) and (e), respectively. The pattern is distorted. Furthermore, the array with feed is moved to the edge of the chip as shown in Figure 3-32 (a) and (b), due to the phase variation the beam is



(a) (b)

Figure 3-30. (a) Orthogonal arrangement of antenna elements, (b) reflection coefficients of the antenna elements excited by individual lumped ports.

directed towards the –X-axis, which can be observed from the radiation pattern shown in Figure 3-33 (f) and (g). When this array is flipped at the edge of the chip as shown in Figure 3-32 (c) and (d), the endfire beam is also flipped, now directed towards +X axis. Because of the large lossy chip in the direction of the beam, the beam gets distorted. The distribution of the electric field is shown in Figure 3-34. The beamforming can be seen in the field plots as the areas of high electric field density.

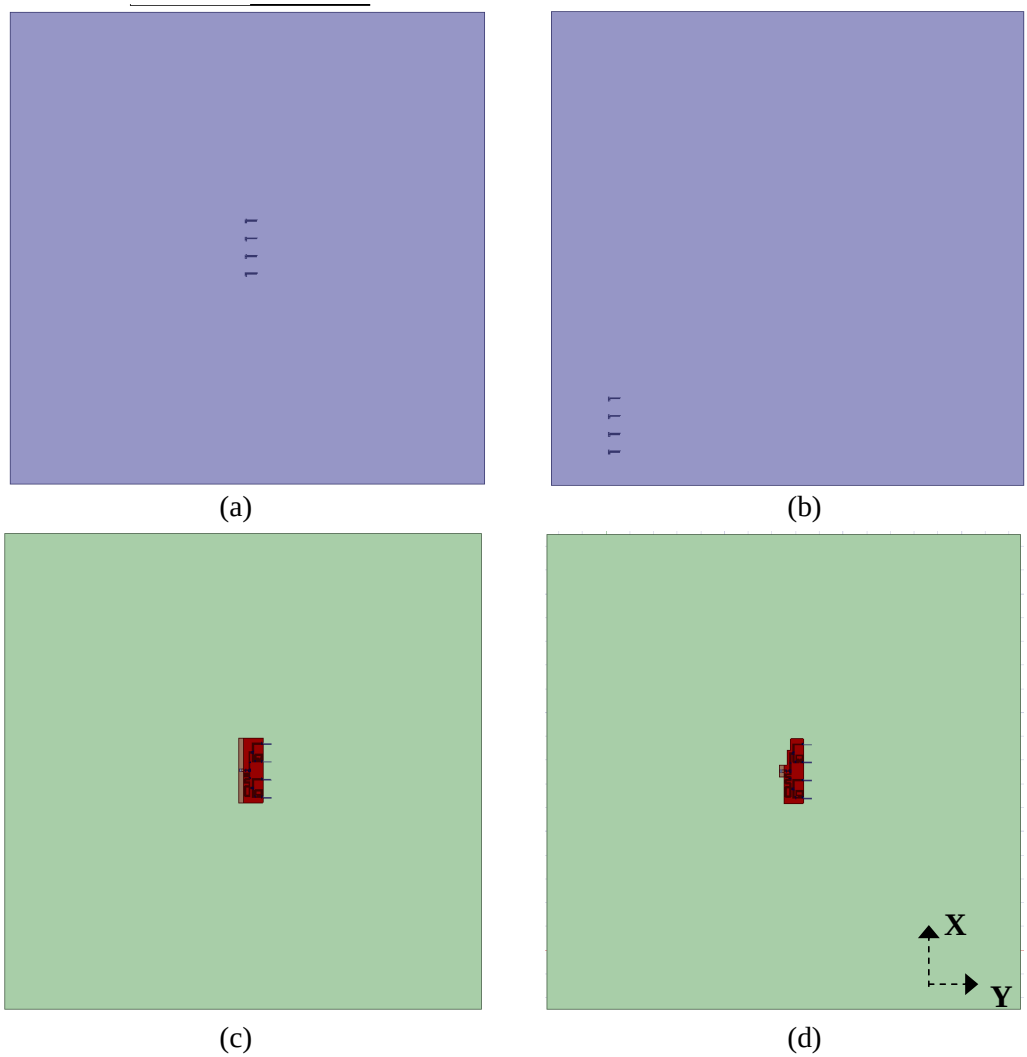


Figure 3-31. Antenna array on chip (a) at the center w/ feed, (b) at the center w/ trimmed feed, (c) at the edge w/ feed, (d) at the edge w/ trimmed feed, (e) at the edge flipped w/ feed, (f) at the edge flipped w/ trimmed feed.

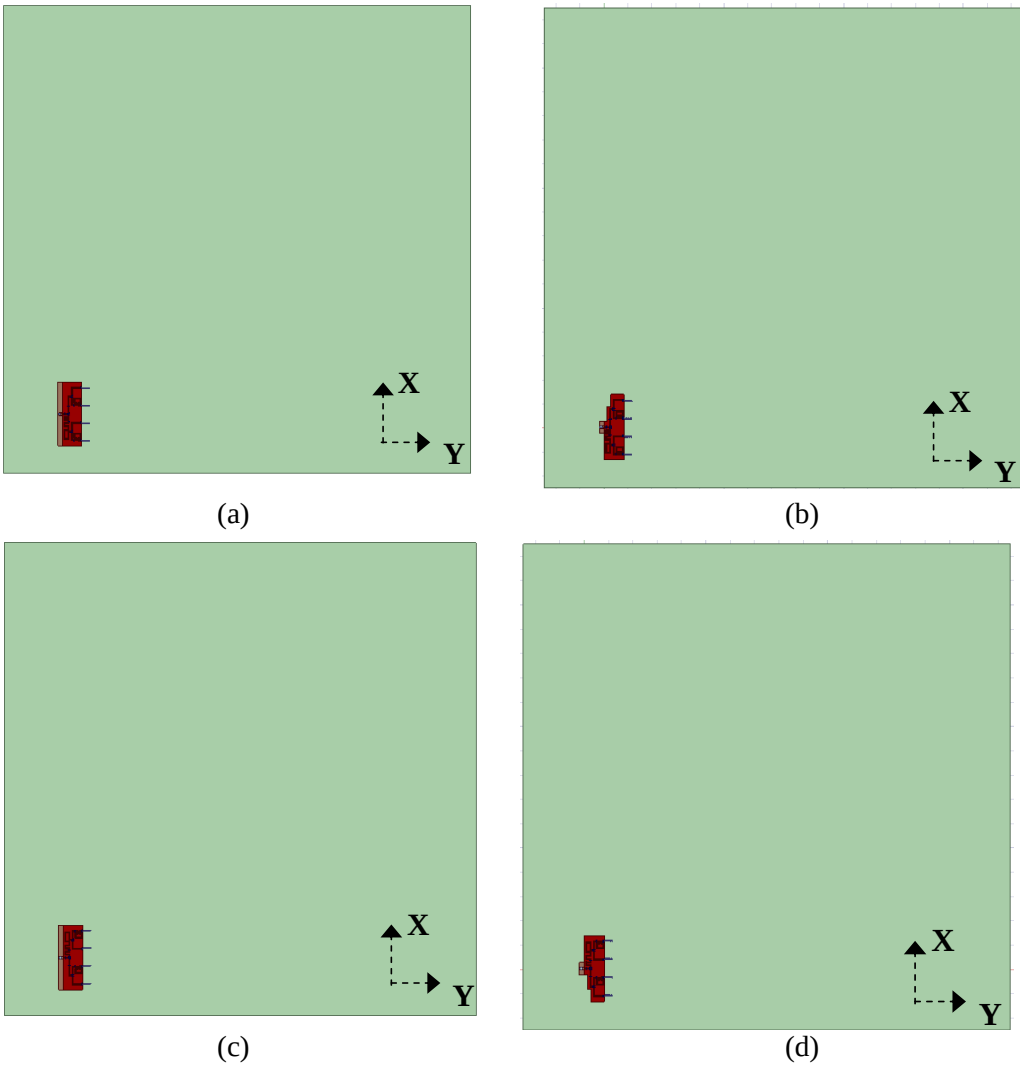


Figure 3-32. Antenna array on chip: (a) at the edge w/ feed, (b) at the edge w/ trimmed feed, (c) at the edge flipped w/ feed, (d) at the edge flipped w/ trimmed feed.

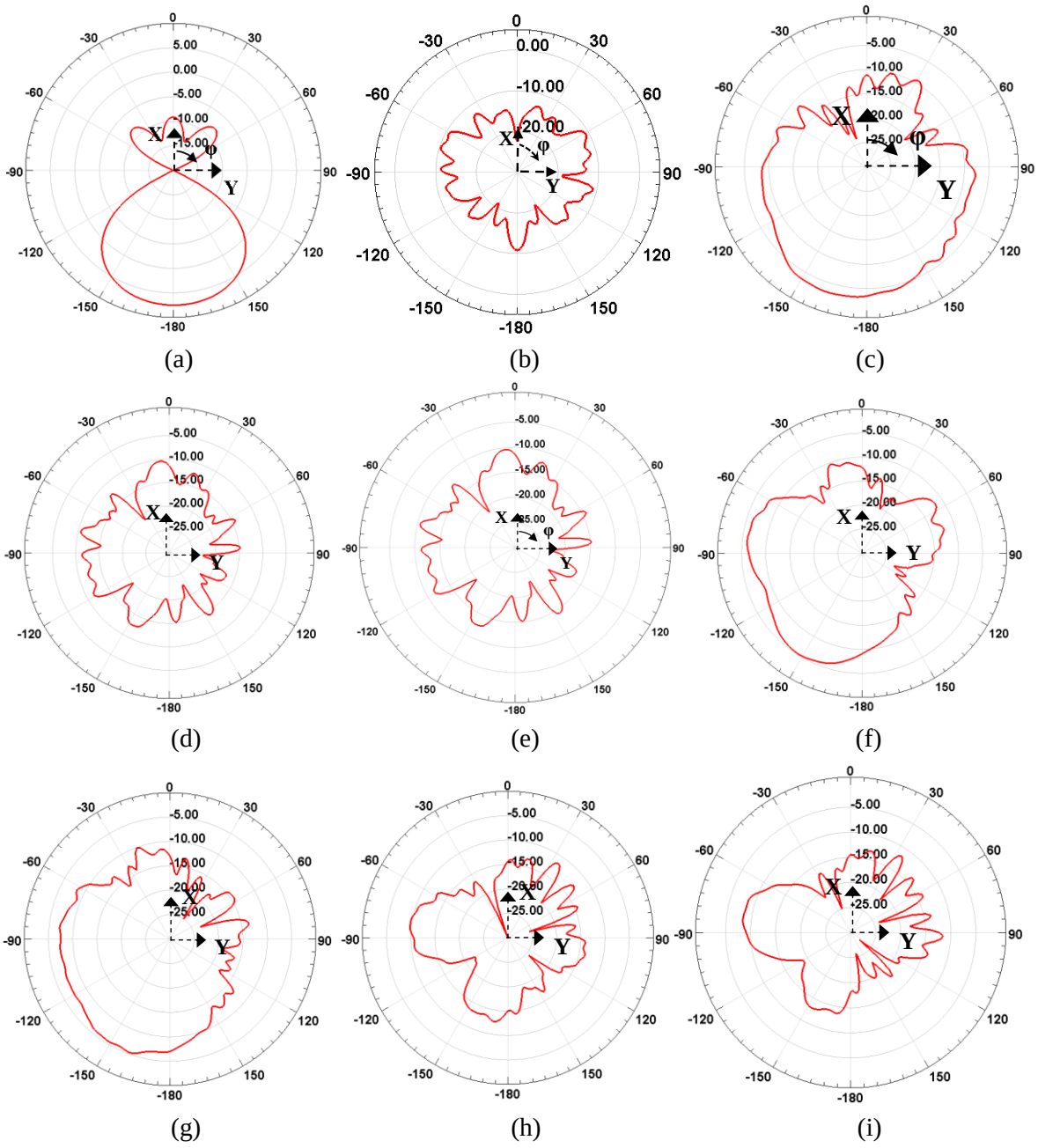
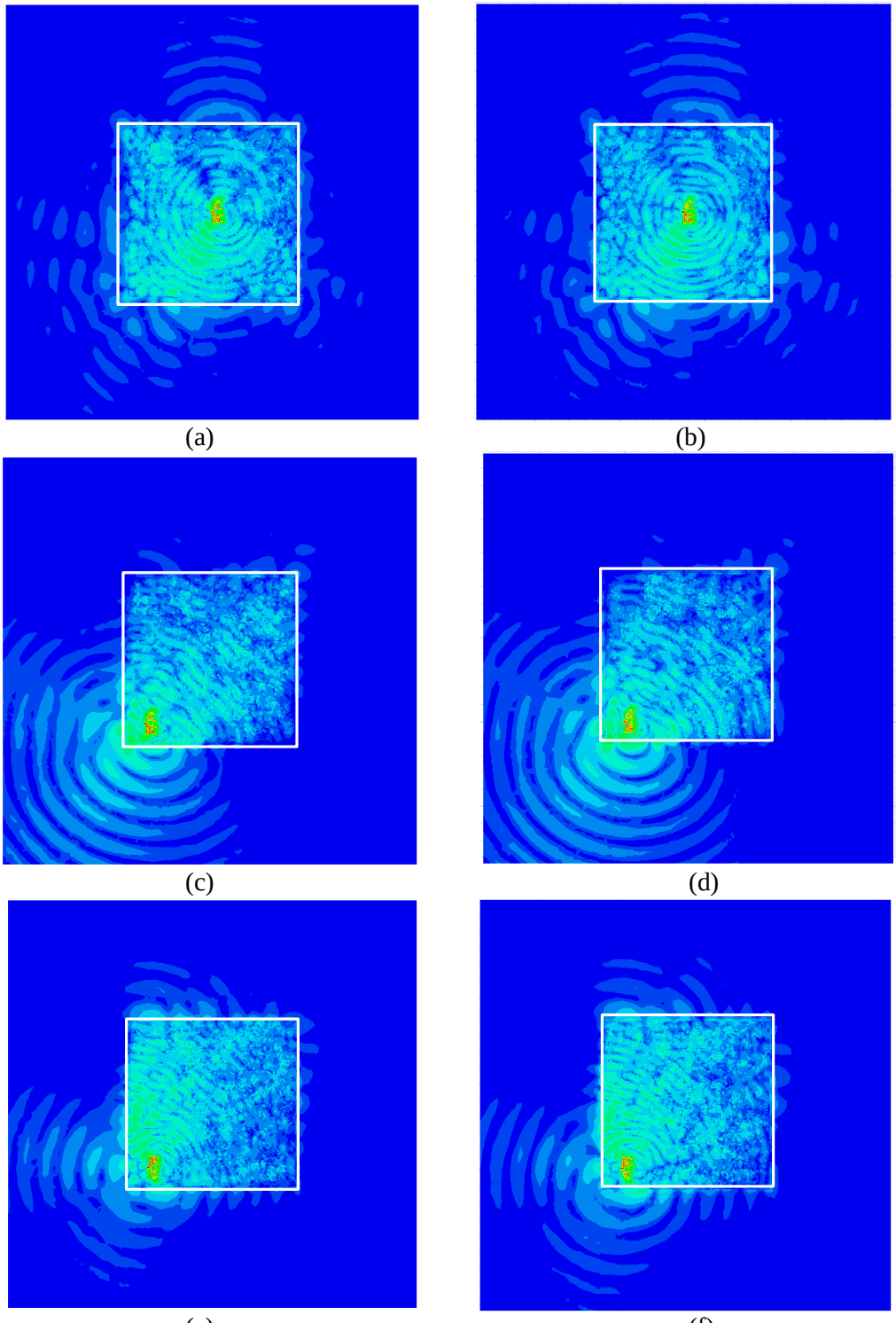


Figure 3-33. Radiation pattern of zigzag antenna broadside array in relevant XY plane (a) in free space, (b) on chip at the center, (c) on chip at the edge, (d) on chip at the center w/ feed, (e) on chip at the center w/ trimmed feed, (f) on chip at the edge w/ feed, (g) on chip at the edge w/ trimmed feed, (h) on chip at the edge flipped w/ feed, (i) on chip at the edge flipped w/ trimmed feed.



(a) (b) (c) (d) (e) (f)

Figure 3-34. Electrical Field distributions (a) at the center w/ feed, (b) at the center w/ trimmed feed, (c) at the edge w/ feed, (d) at the edge w/ trimmed feed, (e) at the edge flipped w/ feed, (f) at the edge flipped w/ trimmed feed.

3.5 Fabrication of chips

All the aforementioned designs are combined in one GDS file and sent for mask development. The picture of mask design is shown in Figure 3-35. Additionally, pictures showing various designs of the chip with untrimmed feed is shown in Figure 3-36. A zoomed-in picture of design with and without sheets is shown in Figure 3-37. There are 3 layers – 2 metal layers M1 and M2 and 1 contact cut (CC) (negative-mask) layer. Three silicon wafers are used for the fabrication. These wafers use the same mask which produces three sets of designs.

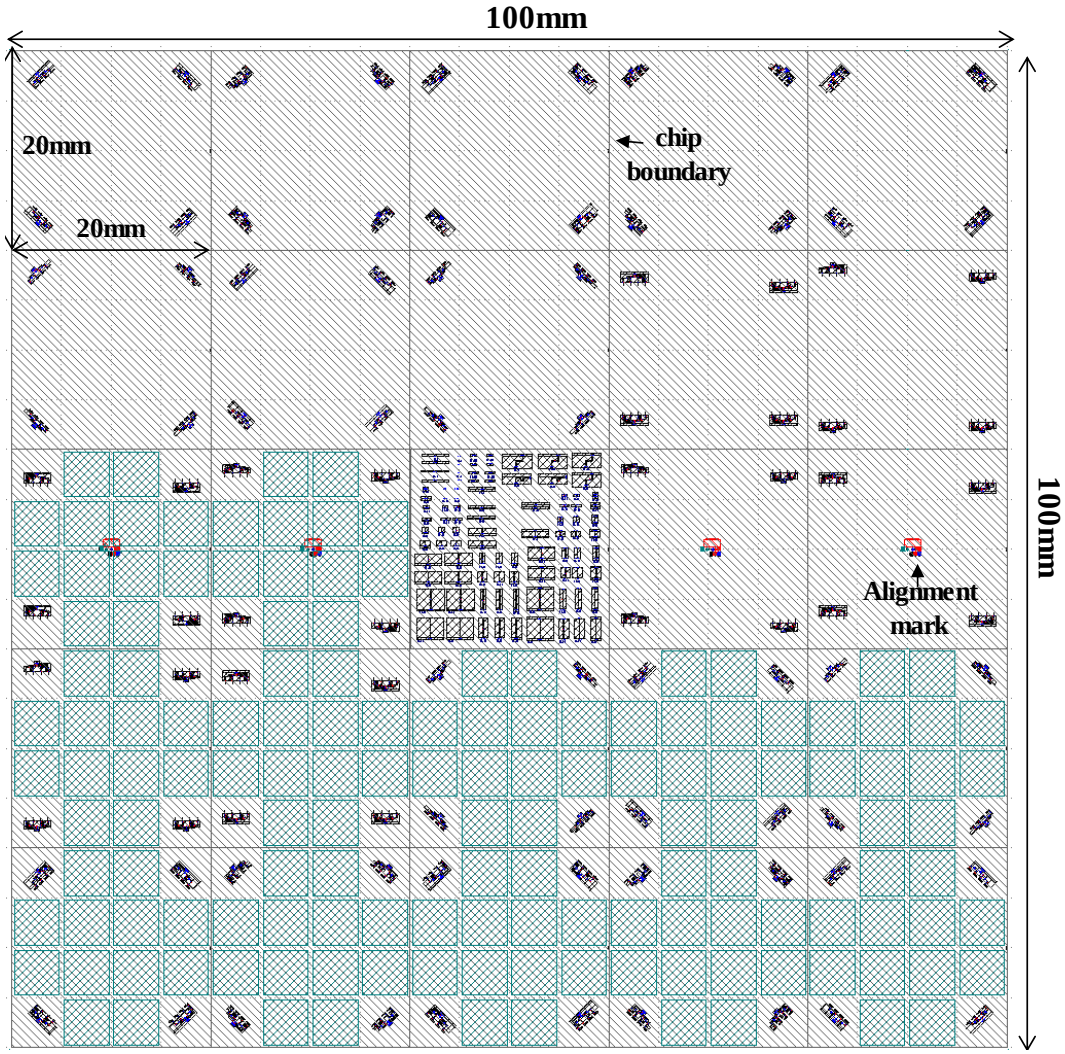


Figure 3-35. Picture of the wafer design for mask making.

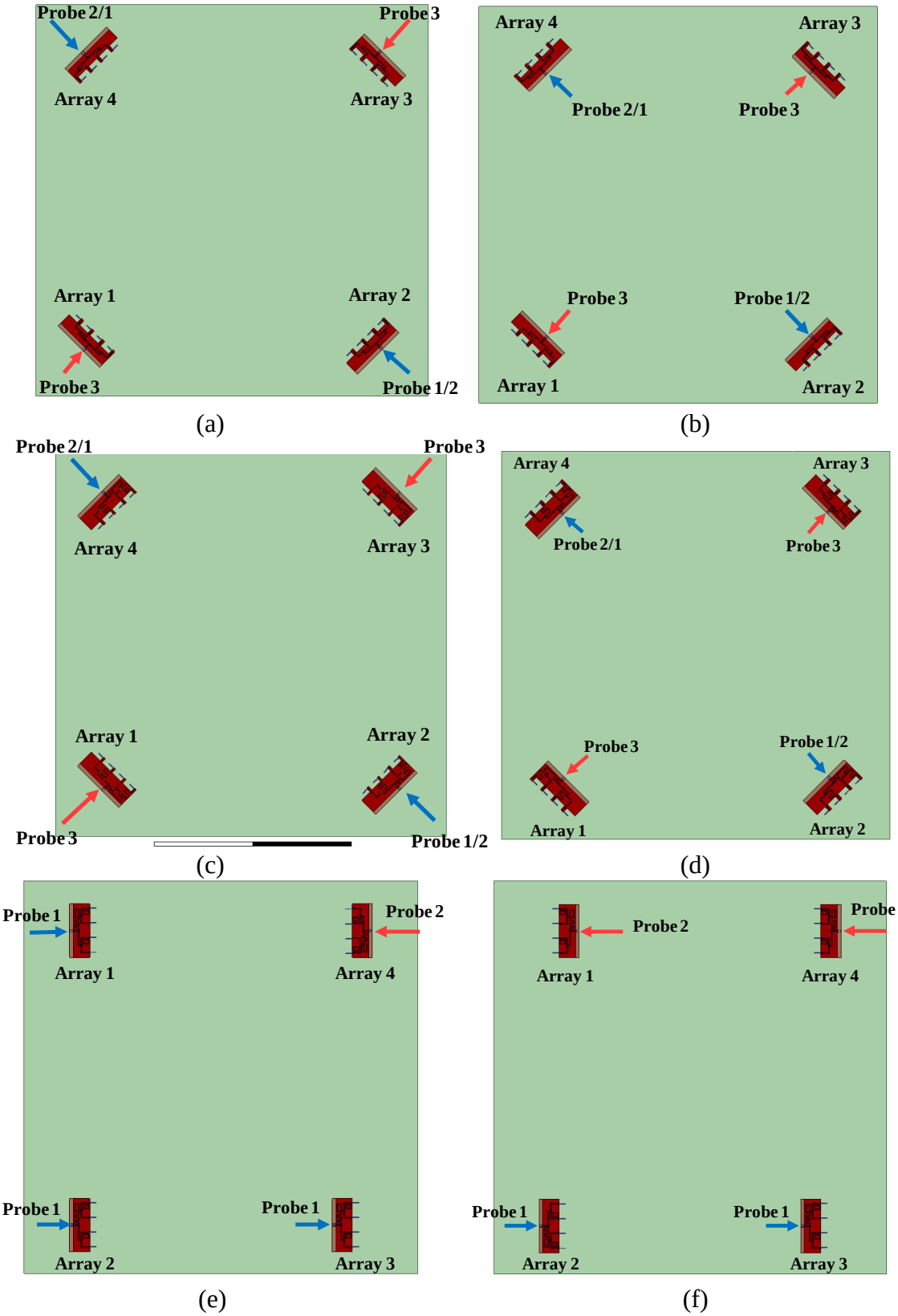


Figure 3-36. Final designs of the arrays with untrimmed feed on chip: (a),(c),(e) intra-chip; (b),(d),(f) inter-chip.

Moreover, as shown in the previous chapter that a core in a multi-core processor chip can be replaced with a metal square sheet at a lower level because of dense orthogonal wiring. Therefore, designs with square sheets representing different cores are also fabricated for a chip. These are later tested to find a reduction in transmission between antenna arrays.

Alignment marks are used to align multi-layer design. Alignment marks are shown in Figure 3-38. These marks are used to align the second metal layer and the contact cuts while performing lithography. The structure is fabricated in multiple layers as shown by the color code. Additional structures shown in Figure 3-39 are also fabricated on the chip.

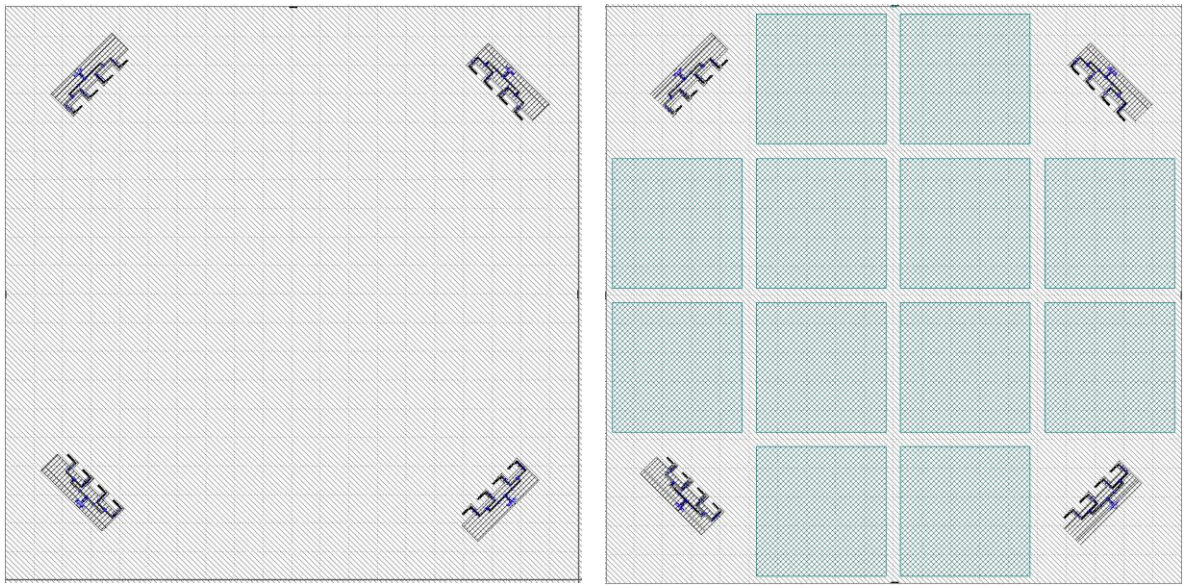


Figure 3-37. Comparison between the array designs without and with grids.

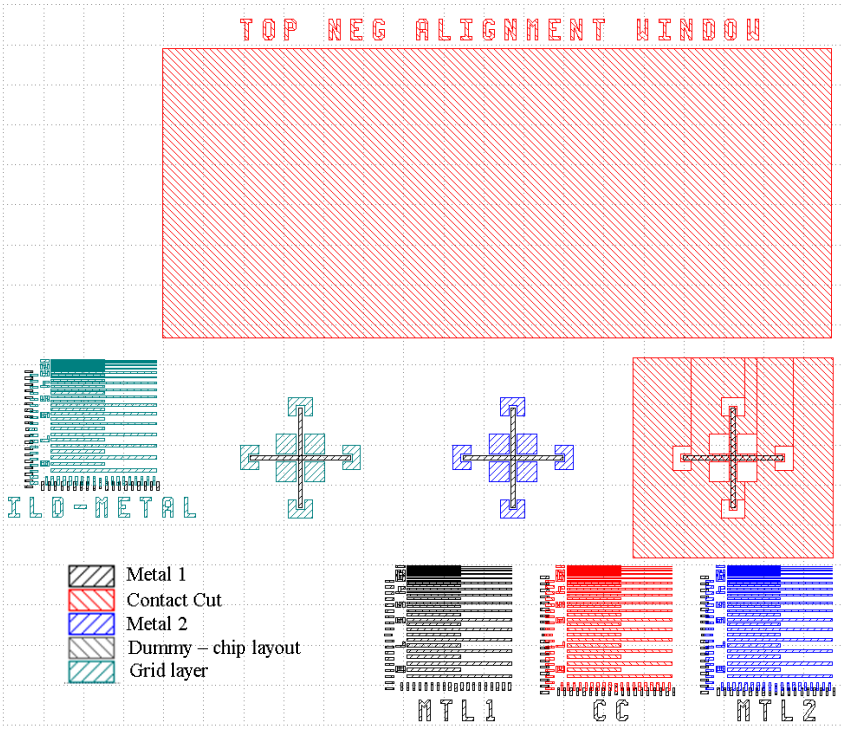


Figure 3-38. Alignment markers used to align multi-layer structures.

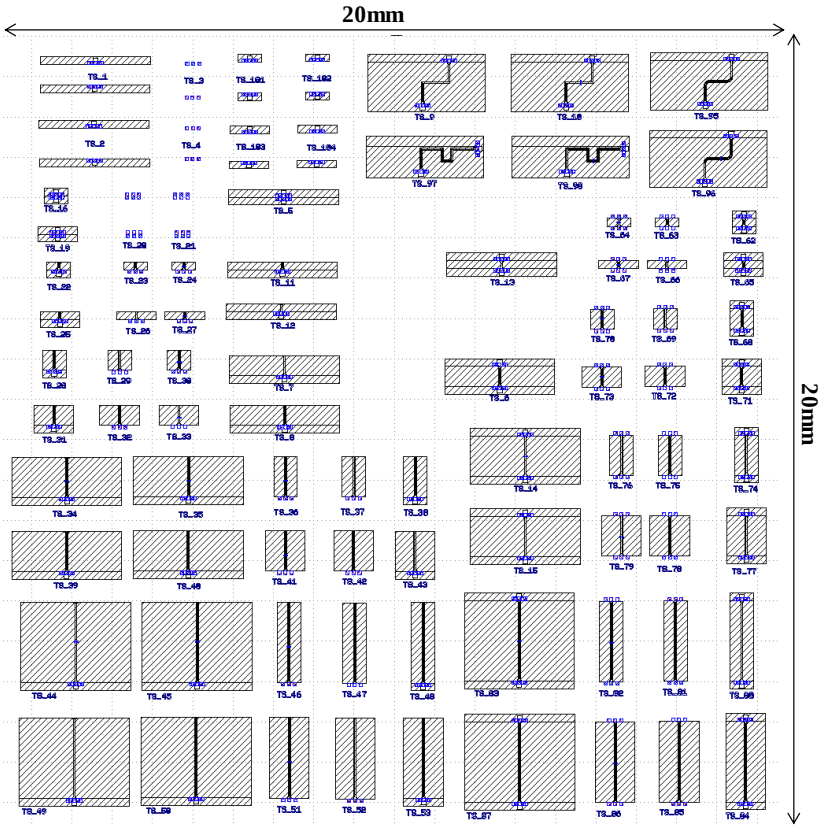


Figure 3-39. Additional transmission lines, reflect and shorts.

The fabrication of the chips is being performed at the RIT Cleanroom. The fabrication steps, as shown in Figure 3-40, involves various processes which are discussed as follows:

1) Resistivity measurement & RCA clean – First, the silicon wafers are measured for the resistivity using the instrument ResMap which uses four-point probes to measure the resistivity. Afterwards the wafers are cleaned using RCA clean method which involves use of hydrochloric acid, ammonium hydroxide and hydrofluoric acid. This process removes the organic and inorganic dust and particles on the surface of silicon wafer.
2) Oxide growth – Different methods are used to deposit silicon dioxide. One method is using a wet oxide growth method and another is CVD deposition (TEOS). The former uses Bruce furnace along with combination of several gases such as oxygen, Hydrogen Chloride (HCl), Chlorine, and water vapors to grow oxide at the surface of silicon. This process gets difficult as the number of layers increases. Therefore this wet oxide process is used only for the first 1µm layer of the oxide. Rest of the oxide layers are deposited using CVD (TEOS) deposition. Process of CVD deposition is quick once the machine is warmed up to required temperature.
3) Al deposition & lithography – It is performed using CVC 601 sputter to deposit Al metal layers. The deposited metal covers the whole silicon surface so it is required to pattern the desired structures using photoresist which is deposited over metal layer. The photoresist is exposed with i-line light using Suss MA150 Aligner. Mask have been generated for the process. Minimum feature constraint is 2µm. Also, the required exposure time is calculated, further optimized using experiments. After exposure, the photoresist is developed and the Al is ready to be etched.

4) Al Metal Etch and Photoresist strip: The metal is etched using wet chemical process. Using Fuji Al etch chemical mixture, the Al is etched off from undesired spaces. Later, the photoresist is stripped off from wafer using PRS-2000 solution.

Some of the steps are repeated again to deposit multiple Al and oxide layers. Microscopic pictures of the top view of arrays, pads and antenna and bridges are shown in Figure 3-41.

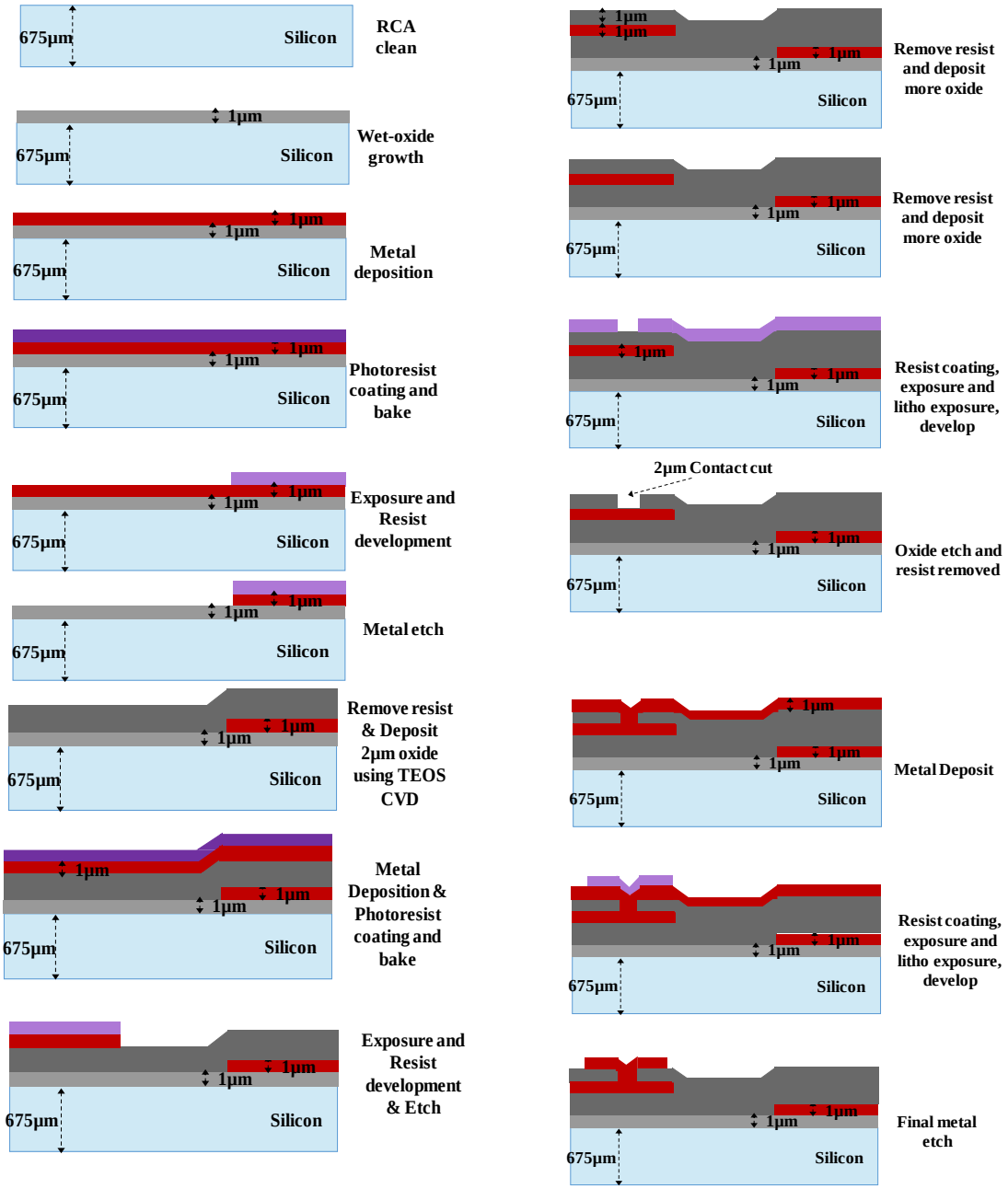
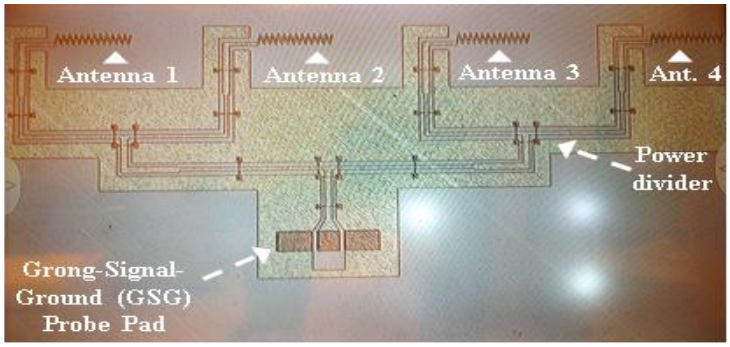
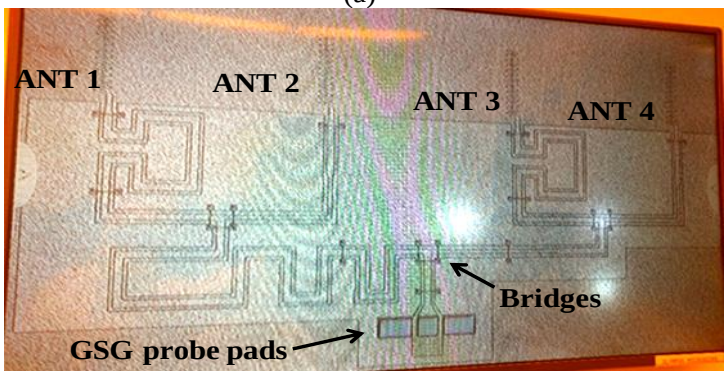


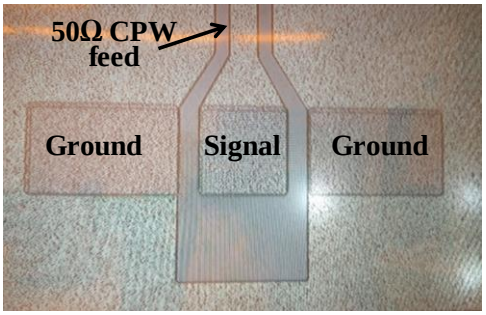
Figure 3-40. Steps involved in cleanroom fabrication process.



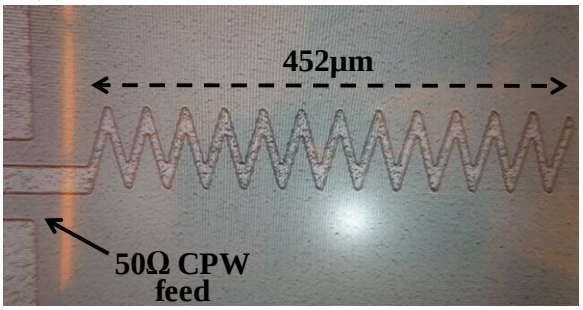
(a)



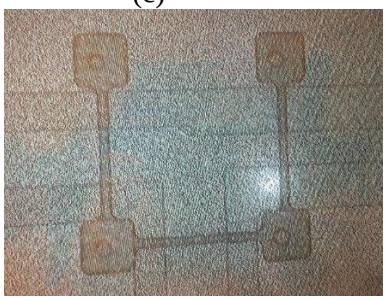
(b)



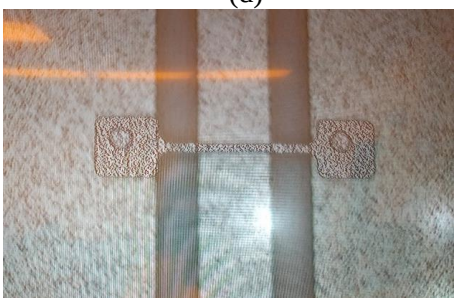
(c)



(d)



(e)



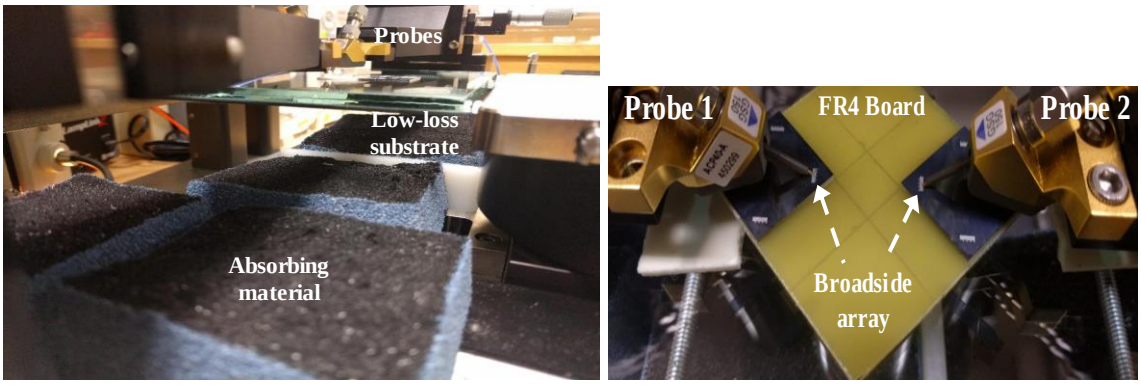
(f)

Figure 3-41. Pictures of the fabricated antennas array and individual elements: (a) axial broadside array design with trimmed ground plane, (b) orthogonal endfire array design with trimmed ground plane, (c) one of GSG pads, (d) antenna element, (e) & (f) bridge structures to connect grounds.

3.6 Measurement results

This section shows the results from the measurement of the various fabricated antenna arrays and compares them to the simulated results. To measure the s-parameters, the probe station requires certain modifications because it has metal chuck. It can affect the measurement of the array by creating an image current due to the current on the antenna. This would alter the parameters of the antenna and in turn measured results. The simulations does not have a ground plane. The modified probe station is shown in Figure 3-42. The metal chuck is moved out and a glass plate is inserted. Moreover, EM absorbing material is placed at the bottom of the low-loss substrate to absorb radiation which might, otherwise, be reflected by the metal of the probe station.

The measurement setup involves Cascade probe station along with Cascade GSG probes and Keysight N5247B PNA-X. The PNAX is calibrated using SOLT (short-open-load-thru) method with Cascade impedance standards substrate. This calibration process calibrate the system till the probe tips. As noted in the previous section that the antenna arrays have probe pads which feeds the antennas, these pads acts as parasitics. In order to remove its effect, the calibration reference plane is adjusted in post-processing steps.



(a) (b)

Figure 3-42. (a) Modification to the probe station, (b) picture of measurement of inter-chip transmission between broadside arrays.

3.6.1 Axial broadside array

The axial arrangement of antenna with broadside feed system is discussed first. The designed antenna array is shown in Figure 3-43. One is with untrimmed feed and another array has trimmed feed. Extra ground plane is trimmed off the untrimmed feed structure. Their corresponding S_{11} plot is also shown. From the S_{11} plots, it can be seen that the arrays have magnitude of S_{11} below 10dB at 60GHz frequency.

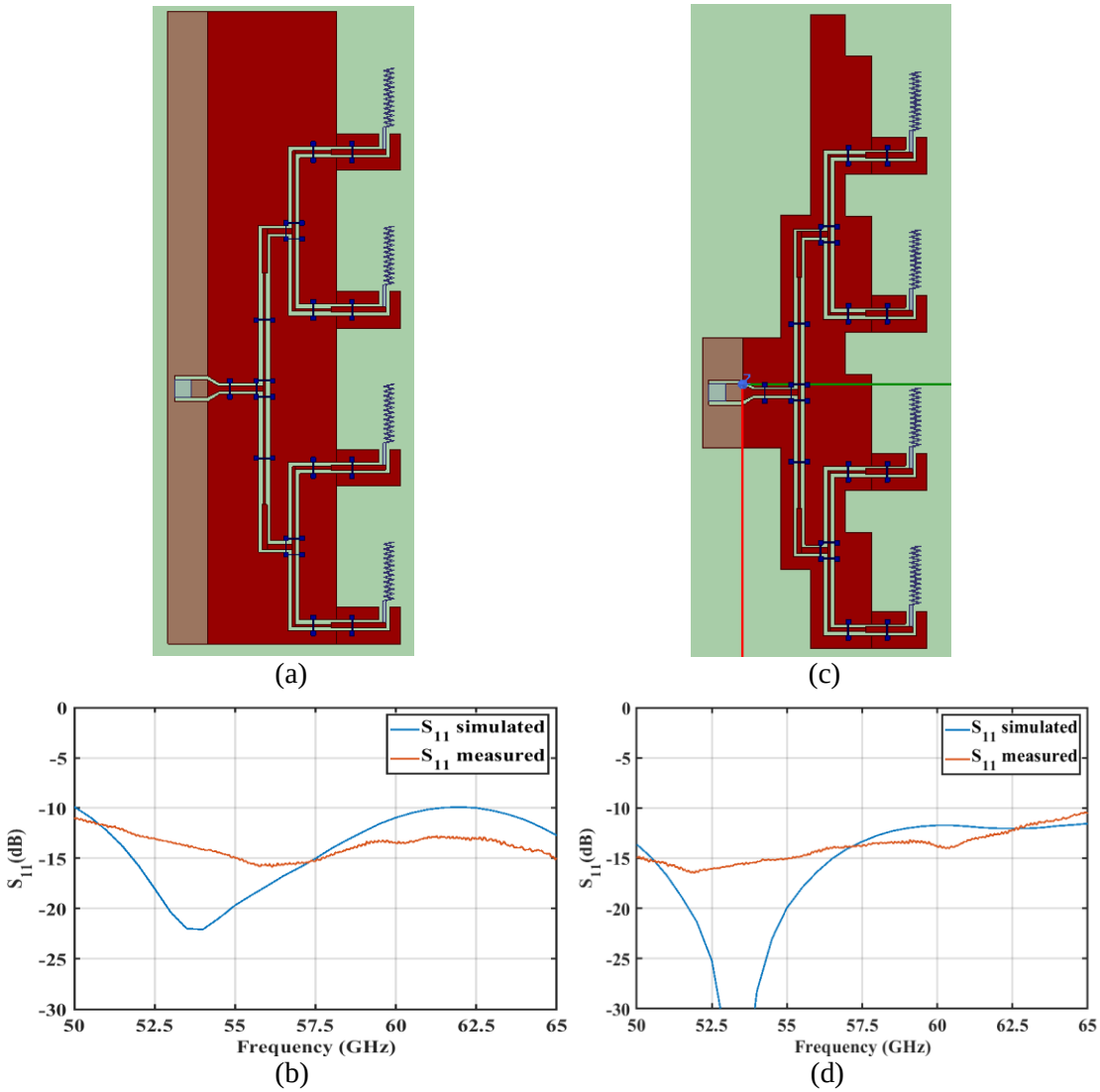


Figure 3-43. Axial Broadside array: (a) Array designed with untrimmed ground plane, and (b) its S_{11} plot, (c) Array designed with trimmed ground plane, and (d) its S_{11} plot.

Also, the transmission coefficients between arrays in case of intra-chip and inter-chip communication are measured and shown in Figure 3-44 and Figure 3-45. Although the measured

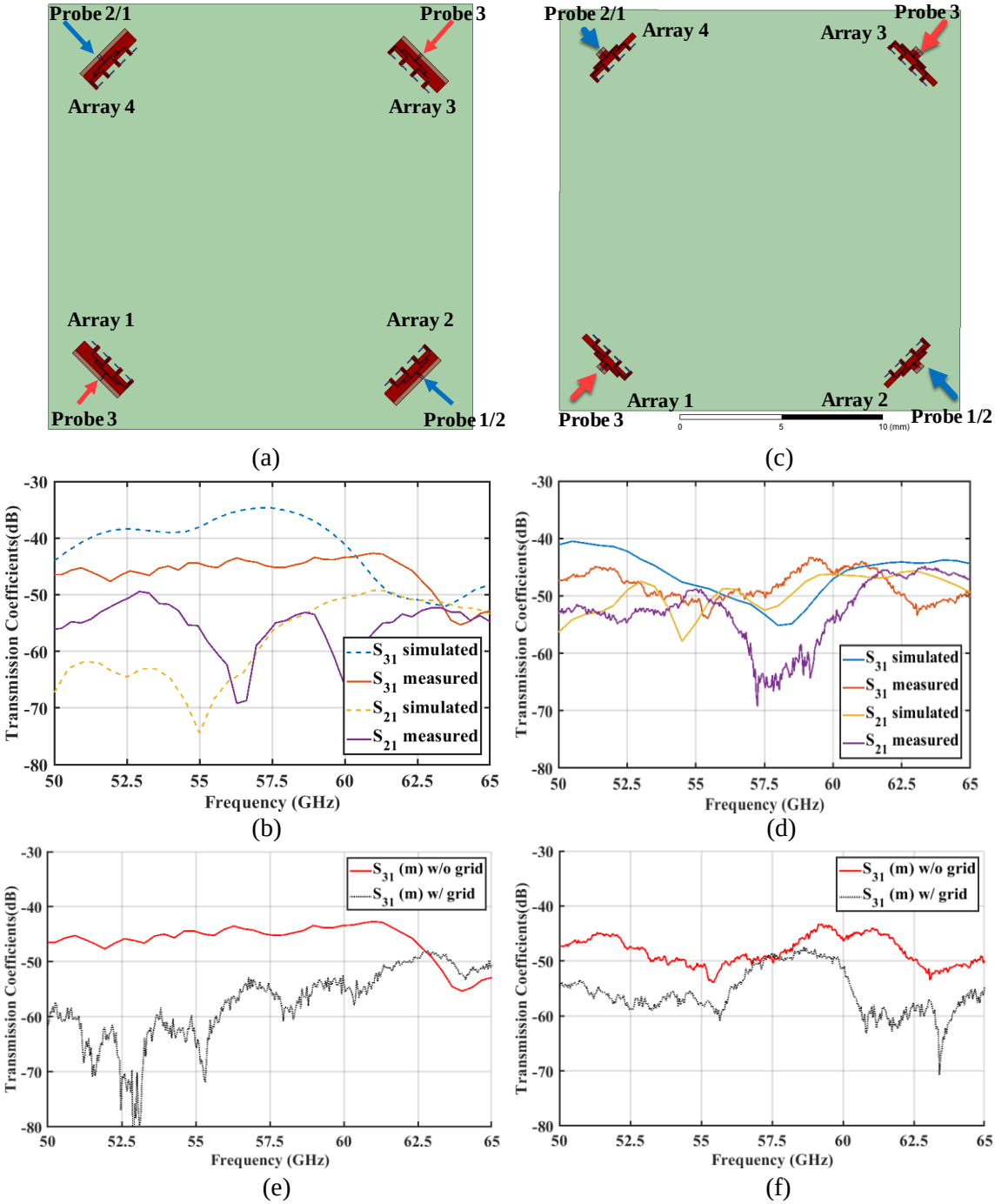


Figure 3-44. Intra-chip scenario for broadside arrays. For untrimmed-feed array arrangement, (a) Top view (close-up), (b) comparison between simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement (d) Top view (close up), (e) comparison between simulated and measured transmission coefficients. (f) measured transmission coefficients w/ and w/o metal sheets.

transmission shows more loss than the simulated transmission, the pattern of transmission over the desired frequency range is comparable. Higher loss in the transmission may be due to the difference in the parameters like material properties and dimensions. These parameters are not

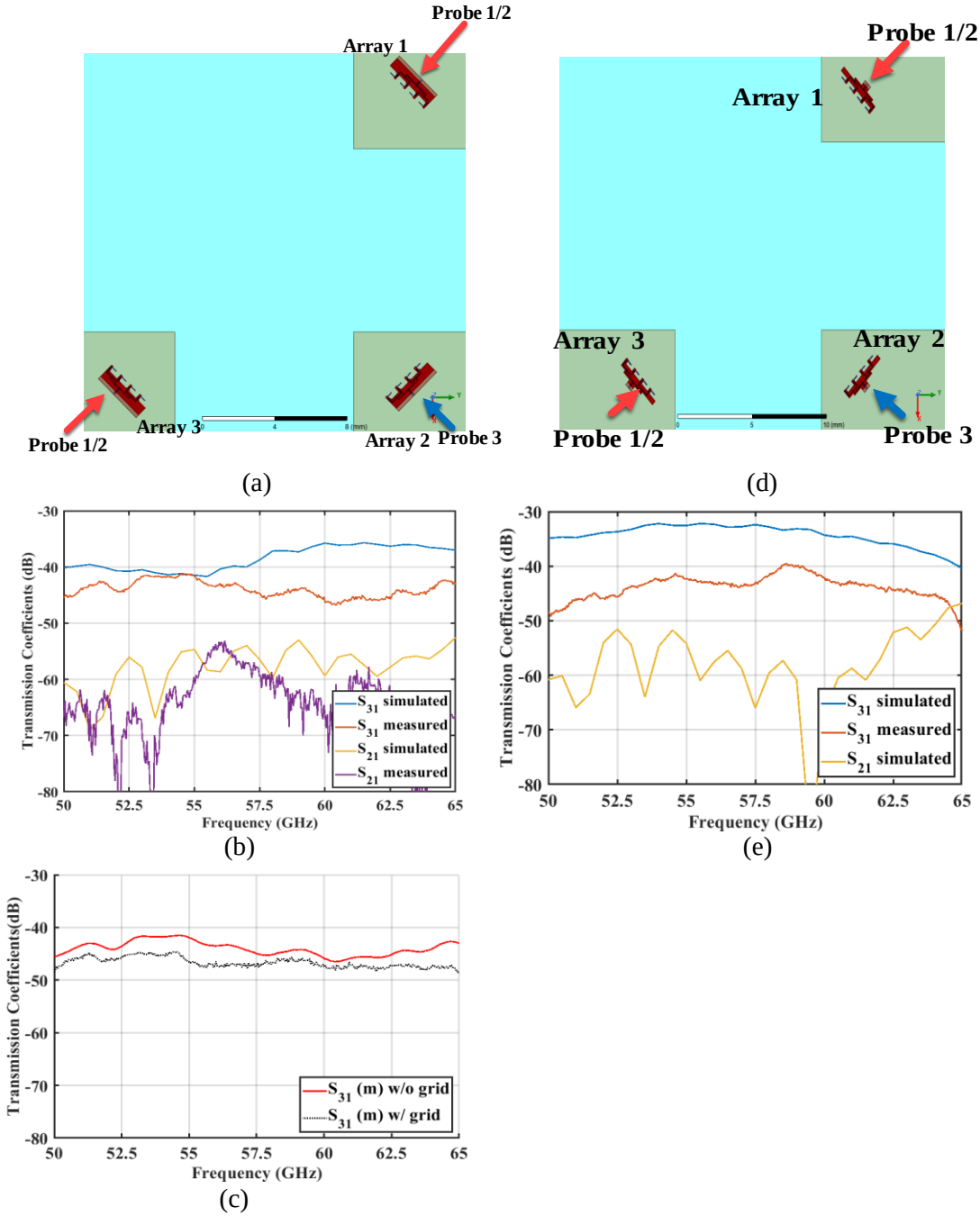


Figure 3-45. Inter-chip scenario for broadside arrays. For untrimmed-feed array arrangement, (a) Top view (close up), (b) comparison of simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement (d) Top view (close up), (e) comparison of simulated and measured transmission coefficients.

properly investigated in the literature for 60GHz bands, only few review articles are available in the literature [62]. The transmission values for intra-chip and inter-chip communication for various frequency is recorded and tabulated in Table 5. The simulated intra-chip transmission in the case of the untrimmed-feed array is -41dB at 60GHz, and the measured transmission for same case is -43dB. For trimmed-feed array, simulated and measured intra-chip transmission coefficient is -50dB and -65dB, respectively, at 60GHz. These values are quite lower than the untrimmed-feed case. It might be possible that the trimmed-feed arrays required more optimization, however, the dimensions of the structure kept constant for the comparison purposes. It can also been seen from the comparison of measured transmission coefficients w/ and w/o metal sheets that they are affecting the communication between the antenna arrays. At 60GHz, the reduction of transmission is up to 10 dB in the intra-chip scenario.

For inter-chip scenario, in the untrimmed-feed case the simulated transmission is -36dB and measured is -46dB at 60GHz. For trimmed-feed case, the simulated inter-chip transmission is -34dB, and measured inter-chip transmission is -42dB. Some of the measurements like the S_{21} for inter-chip w/o metal sheets, and S_{31} for inter-chip w/ metal sheet could not be performed due to the loss of the chips while fabrication. The comparison of S_{31} with and without the metal sheets shows that the inter-chip transmission for these untrimmed-feed arrays are not affected by metal sheets as intra-chip transmission. The plot in Figure 3-45(c) shows less than 3dB of reduction.

Table 5: Values of S_{31} transmission coefficients.

	Intra-chip		**Inter-chip**	
Transmission in dB	**Untrimmed**	**Trimmed**	**Untrimmed**	**Trimmed**
Simulated (at 60GHz)	-41	-50	-36	-34
Measured (at 60GHz)	-43	-65	-46	-42

3.6.2 Axial phased array

In this section, the axial array arrangement with phased feed system is measured and compared with simulations. The simulated radiation beam max is at 45° from the broadside direction due to phase variation in elements. The top view of the antenna array is shown in Figure 3-46 (a) with untrimmed feed and (c) with trimmed feed. The reflection coefficients of the antenna arrays are shown in Figure 3-46 (b) for untrimmed-feed and (d) for trimmed-feed at 60GHz is below -10dB. Transmission coefficients are also plotted for intra-chip and inter-chip cases in Figure 3-47 and Figure 3-48.

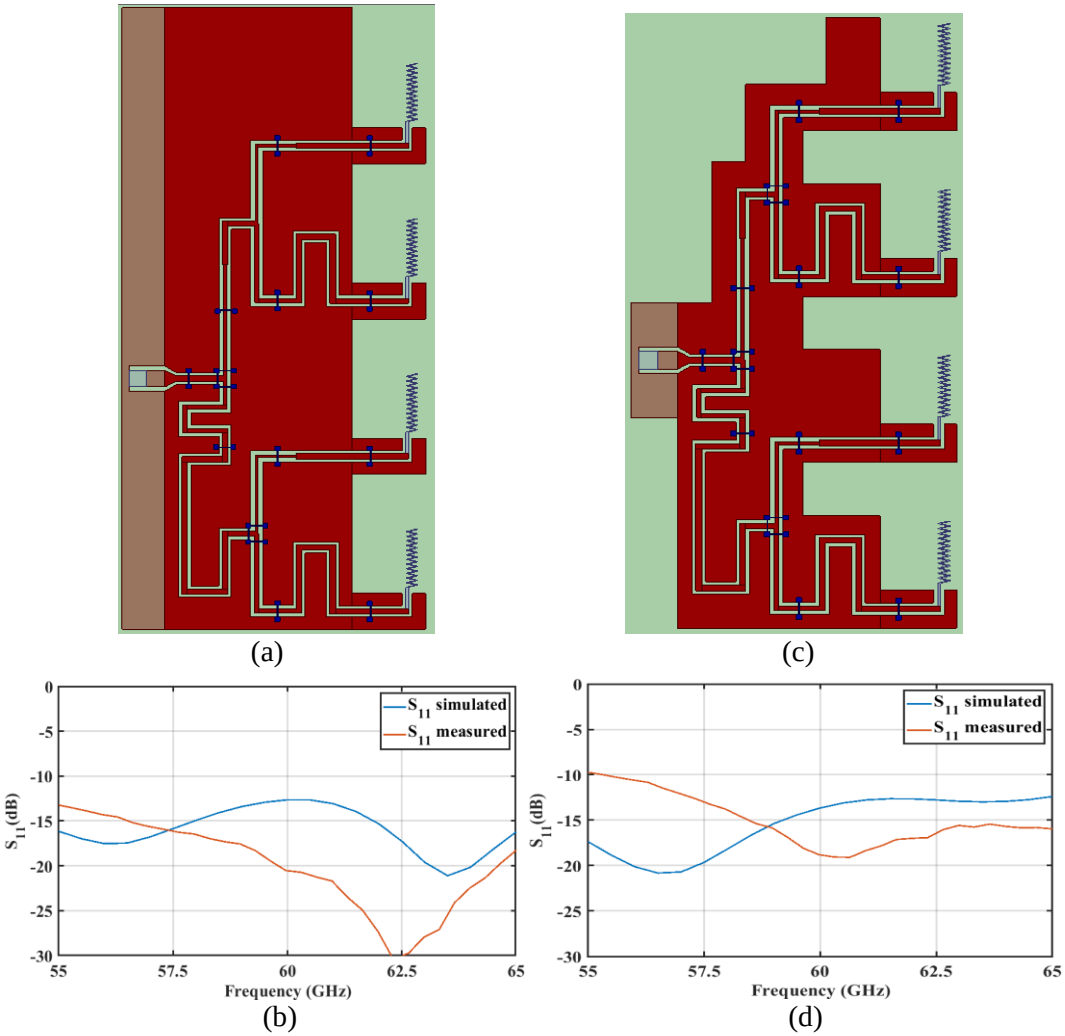


Figure 3-46. For untrimmed-feed array arrangement: (a) Top view of the array with untrimmed feed, (b) reflection coefficients – measured & simulated. For trimmed-feed arrangement: (c) Top view of the phased array with trimmed feed; (d) reflection coefficient – measured & simulated.

In case of intra-chip communication, the transmission coefficients are shown in Figure 3-47 (b) for untrimmed-feed array, and in Figure 3-47 (e) for trimmed-feed array. The simulated and measured transmission S_{32} for untrimmed-feed array is -37dB and -47dB at 60GHz,

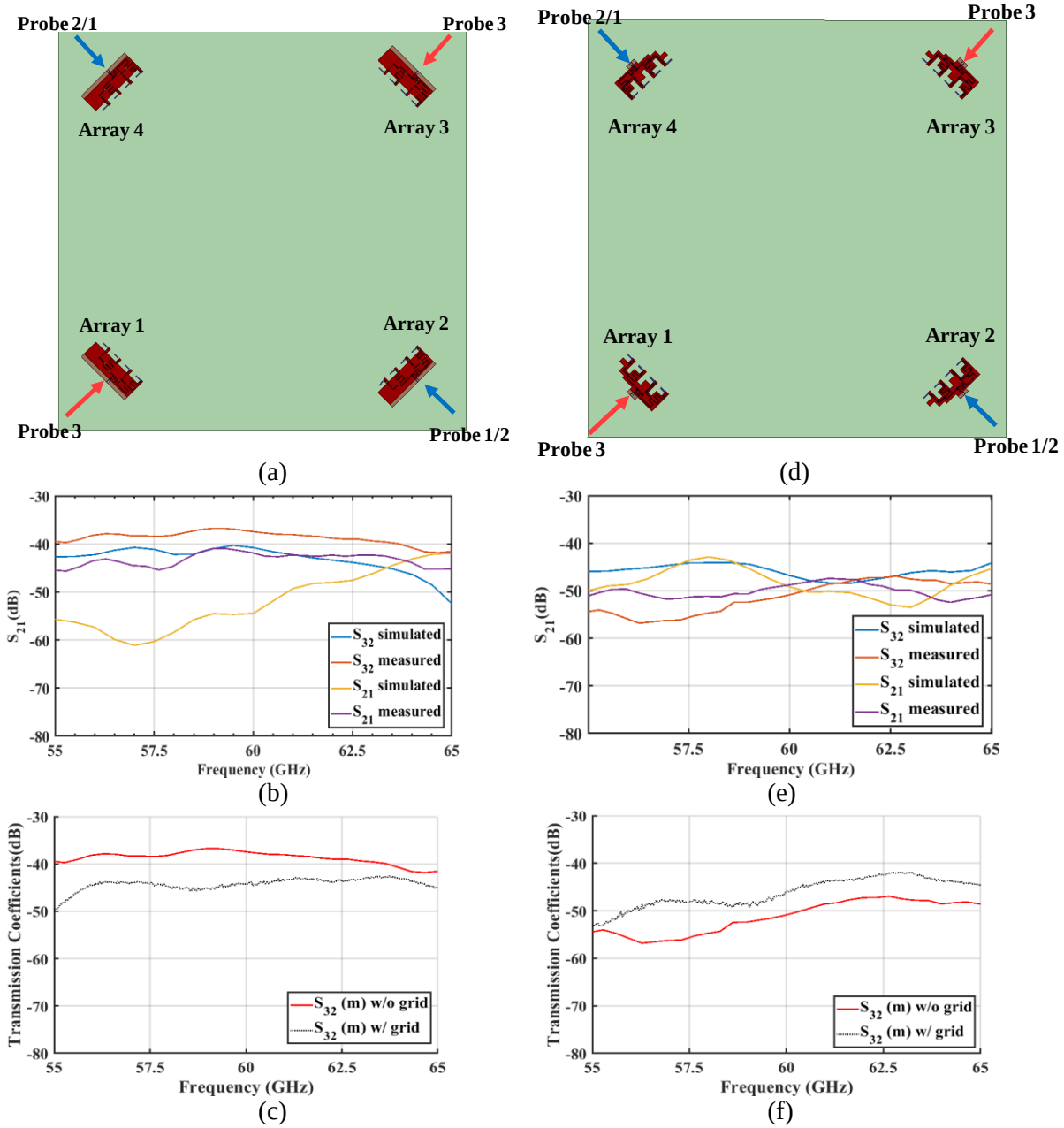


Figure 3-47. Intra-chip scenario for phased arrays. For untrimmed-feed array arrangement, (a) Top view (close-up), (b) comparison between simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement (d) Top view (close up), (e) comparison between simulated and measured transmission coefficients, (f) measured transmission coefficients w/ and w/o metal sheets.

respectively. It may be due to the loss in substrate and difference in parameters like material properties, etc. between simulation and measurement. The simulated and measured transmission S_{32} for trimmed-feed is -47dB and -51dB at 60GHz. Moreover, the effect of the metal sheets on transmission S_{32} for untrimmed-feed and trimmed-feed arrays are also plotted in Figure 3-47 (c)

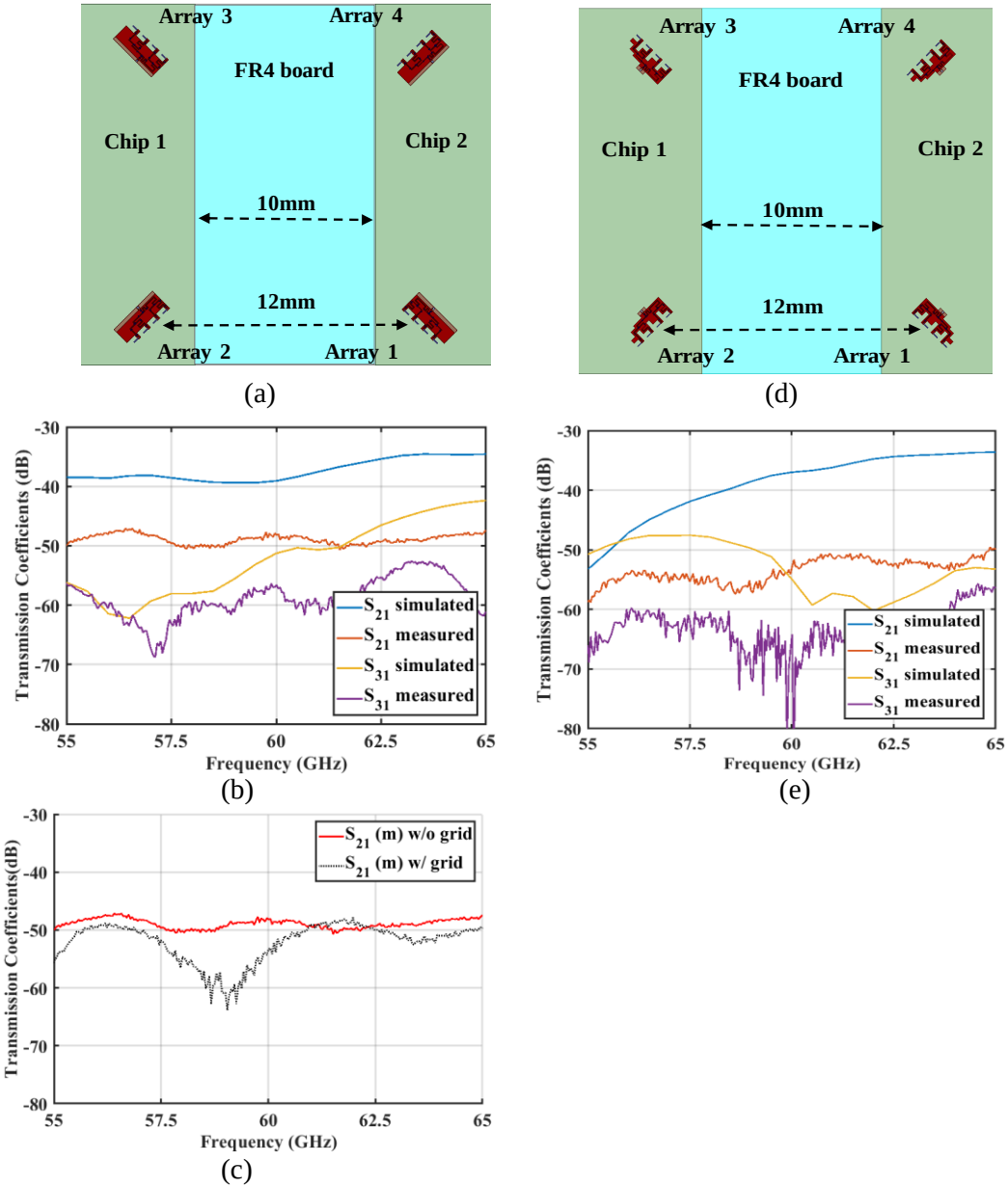


Figure 3-48. Inter-chip scenario for phased arrays. For untrimmed-feed array arrangement, (a) Top view (close up), (b) comparison between simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement (d) Top view (close up), (e) comparison between simulated and measured transmission coefficients.

and (d). The transmission S_{32} between array 3 and array 2 is reduced by about 5dB at 60GHz. Next, the inter-chip transmission is discussed and results are shown in Figure 3-48.

For inter-chip transmission the maximum transmission is expected between the array 1 and 2 since the beams of the arrays are directed towards each other due to the designed phase variation of the antenna elements. As seen from the plots in Figure 3-48 (b) and (e) that the simulated transmission S_{21} is indeed higher than other S_{31}. The simulated transmission coefficient S_{21} is -39dB and measured transmission coefficient is -48dB, which is higher than the S_{31} by more than 10dB. Although the measured transmission is lower than the simulation, the difference between measured S_{21} is quite higher than the measured S_{31}. Furthermore the measured S_{21} is little affected by the metal sheets as shown in Figure 3-48 (c).

Table 6: Measured transmission coefficients between phased arrays at 60GHz.

	Intra-chip (S_{32})		**Inter-chip (S_{21})**	
Transmission in dB	**Untrimmed**	**Trimmed**	**Untrimmed**	**Trimmed**
Simulated (at 60GHz)	-37	-47	-39	-37
Measured (at 60GHz)	-41	-51	-48	-53

3.6.3 Orthogonal endfire array

The orthogonal arrangement of the antenna elements with endfire feed system are measured. Due to the phase variation in the feed, the radiation beam is endfire – in the axis of the array. Figure 3-49 (a) shows the top view of the untrimmed-feed array. Simulated and measured reflection coefficients is shown in Figure 3-49 (b), the array is resonating at 60GHz with S_{11} below -20dB at 60GHz. Similarly, reflection coefficients for trimmed-feed array is shown in Figure 3-49(d).

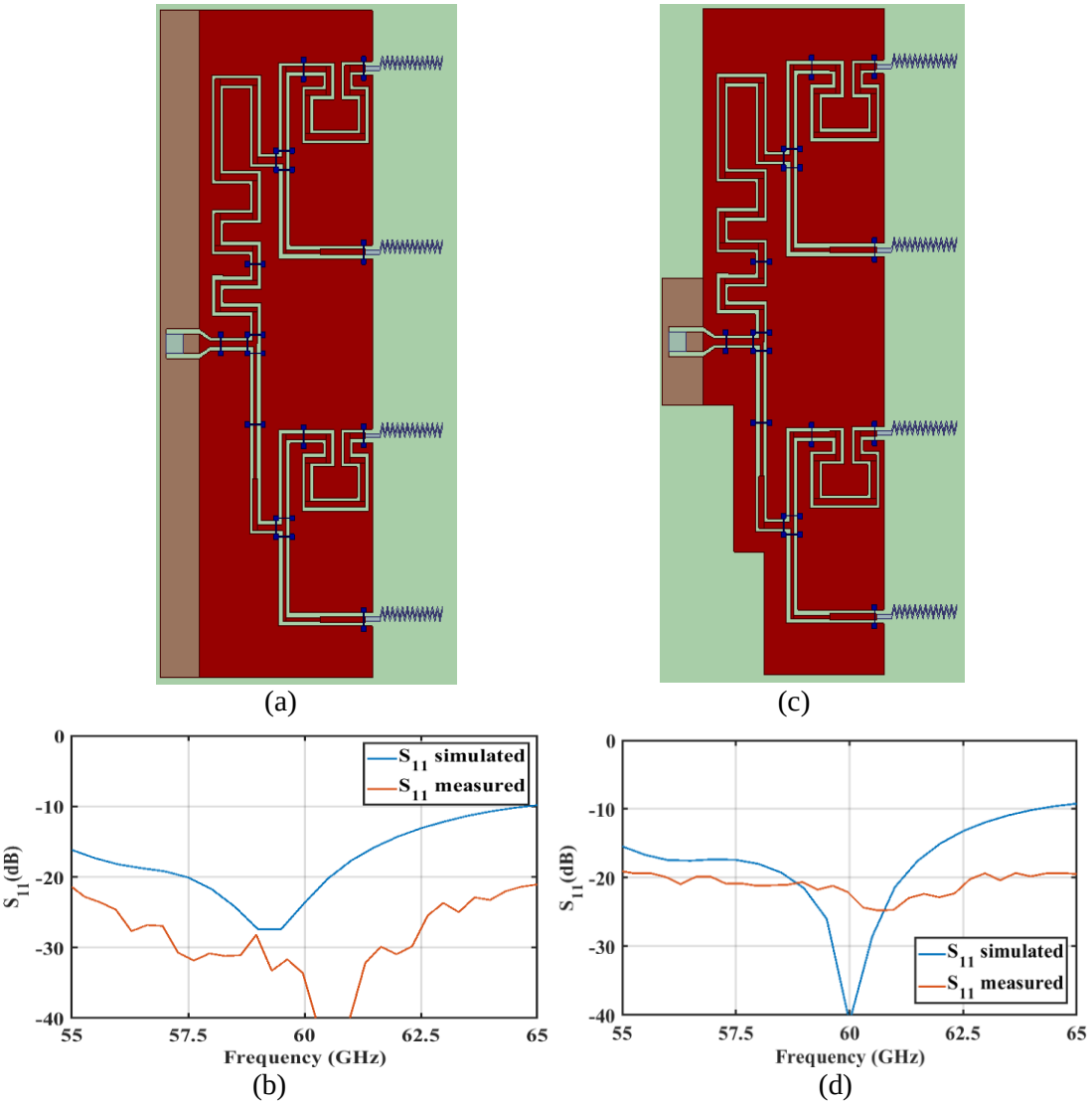


Figure 3-49. Untrimmed-feed array arrangement for orthogonal endfire: (a) Top view of the array, (b) reflection coefficients – measured & simulated. For trimmed-feed arrangement: (c) Top view of the phased array; (d) reflection coefficient – measured & simulated.

Similar to previous cases, the transmission coefficients are plotted in Figure 3-50 and Figure 3-51 for intra-chip and inter-chip cases. The transmission coefficients for intra-chip transmission is expected to be better for the array 4 and 3 due to the phase variation. As per the measured and simulated data, the transmission between 4 and 3 is better in case of untrimmed and

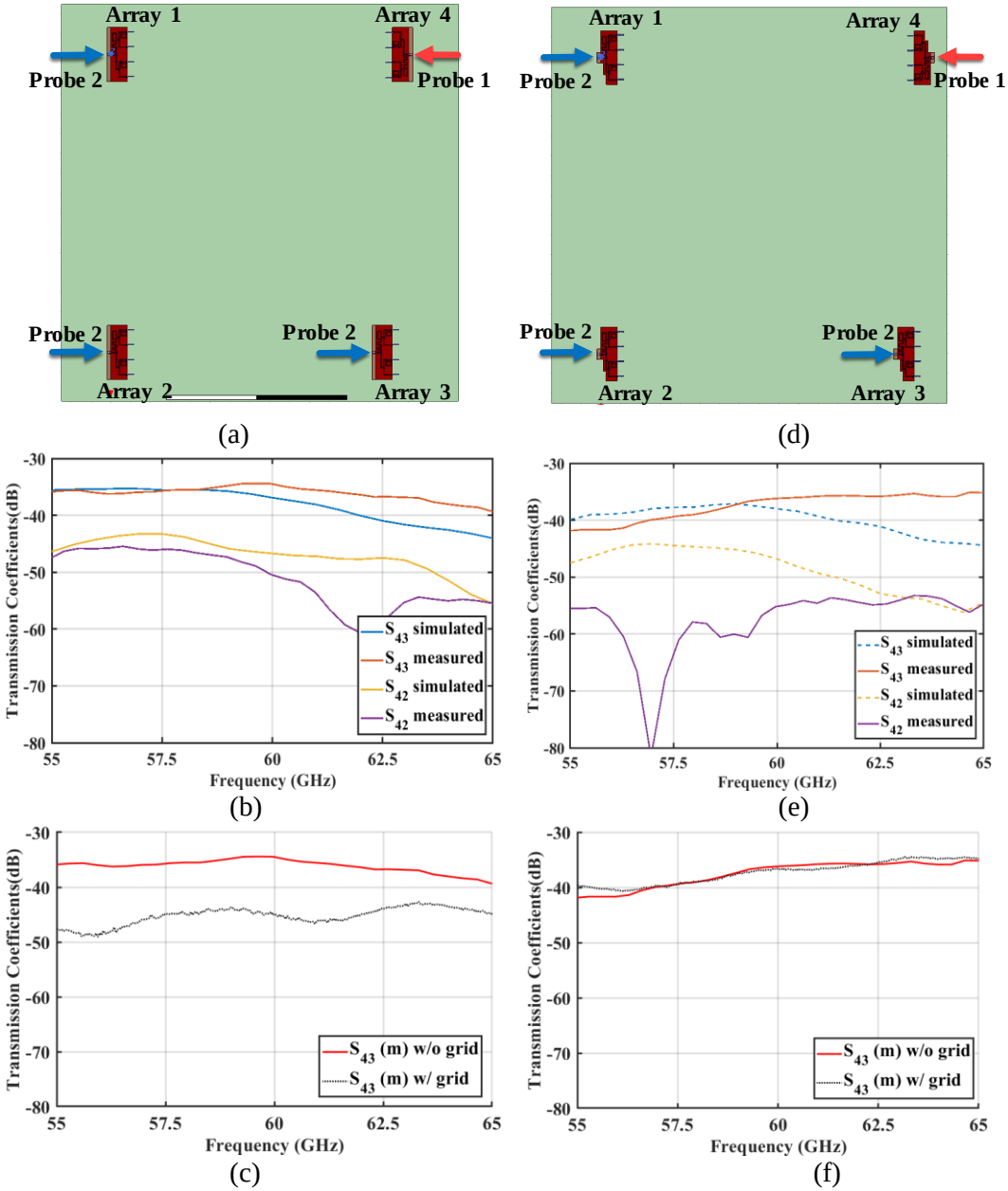


Figure 3-50. Intra-chip scenario for orthogonal endfire arrays. For untrimmed-feed array arrangement, (a) Top view (close up), (b) comparison between simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement (d) Top view (close up), (e) comparison between simulated and measured transmission coefficients, (f) measured transmission coefficients w/ and w/o metal sheets.

trimmed feed system. The simulated and measured S_{43} are -37dB and -35dB, respectively at 60GHz for untrimmed-feed array. On the other end, the simulated and measured S_{43} are -38dB and -36dB at 60GHz for trimmed-feed array. Simulation and measurement results show good match for intra-chip case. Next, the results from inter-chip measurements are shown in Figure 3-51.

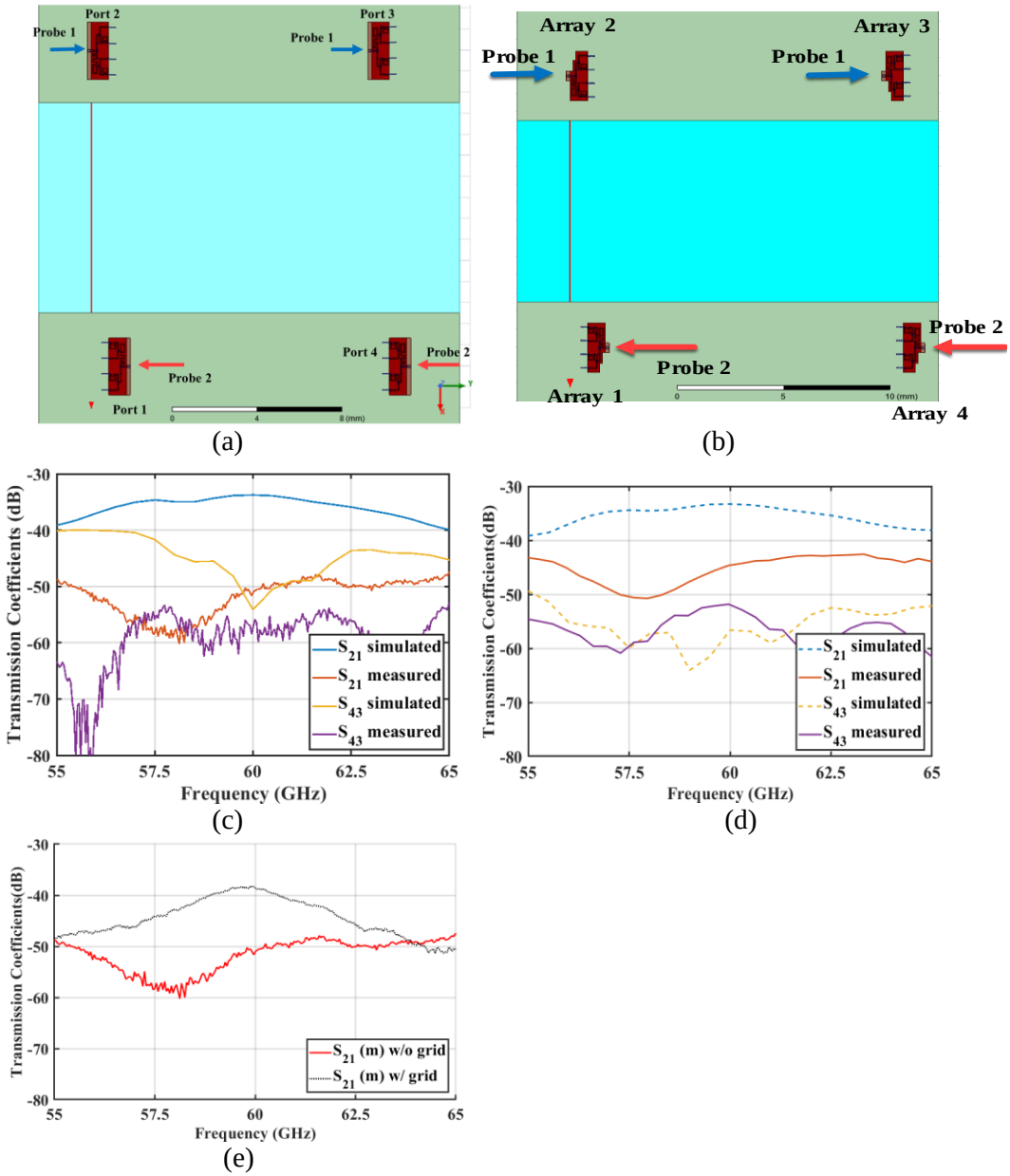


Figure 3-51. Inter-chip scenario for endfire arrays. For untrimmed-feed array arrangement, (a) Top view (close up), (b) comparison between simulated and measured transmission coefficients, (c) measured transmission coefficients w/ and w/o metal sheets. For trimmed-feed array arrangement: (d) Top view (close up), (e) comparison between simulated and measured transmission coefficients.

In inter-chip scenario, despite proper physical alignment of the chips, the results from simulation and measurement don't coincide as in the case of intra-chip transmission. This may be due to fabrication uncertainty, since there was only one pair of chip for these measurements (some of the chips from wafer 1 and 2 are lost while dicing process), so it is hard to verify. For untrimmed-feed array, the simulations show high transmission magnitude for S_{21} that is -34dB, while the results from measurement are more than 15dB lower that is -51dB. For trimmed-feed array, the simulated S_{21} is -33dB and measured S_{21} is -47dB at 60GHz.

In intra-chip scenario, the measured results S_{43} w/ and w/o metal sheets is shown in Figure 3-50 (c) & (f). The results for untrimmed-feed array shows difference of more than 10dB. On the other hand, for trimmed-feed array the difference is negligible. In inter-chip scenario shown in Figure 3-51, the results for trimmed-feed array is not available. For untrimmed-feed array, the results, in Figure 3-51 (e), shows that the measured S_{21} w/ sheets has increased significantly compared to the S_{21} w/o sheets. It might be possible that the arrays on chip with metal sheets are working properly, therefore we are seeing high transmission. Since, there are only one pair of chip for measuring S_{21} w/o metal sheet, so this cannot be verified now.

Table 7: Transmission coefficients between endfire arrays in case of inter-chip scenario.

	Intra-chip		**Inter-chip**	
Transmission in dB	**Untrimmed**	**Trimmed**	**Untrimmed**	**Trimmed**
Simulated (at 60GHz)	-37	-38	-34	-33
Measured (at 60GHz)	-35	-36	-51	-47

3.7 Conclusion

In this chapter, the design, simulation and measurement of on-chip phased arrays for multi-chip multi-core systems is performed. Three types of arrays are designed with different beam angles – broadside, phased, and endfire. Also, two different scenarios are considered, that are, intra-chip and inter-chip communications. For now, the antenna elements are fed with the delayed-line system to create the desired progressive phase for arrays. The antenna arrays are simulated in ANSYS HFSS. Furthermore, the steps involved in the fabrication of chips are discussed here.

For broadside array, the arrays are working at the 60GHz band. The beamforming at 60GHz is shown using a radiation pattern. The measured transmission when the beam max are directed in between the array pair for untrimmed-feed for intra-chip case vary from -43 to -55dB, and for the inter-chip case, it varies from -35dB to -40dB. For phased array, the beamforming at 60GHz is shown using simulated radiation pattern plots. For the intra-chip scenario, the measured transmission between the arrays with untrimmed-feed varies from -37dB to -42dB when the beam max are directed in between the array pair. Lastly, the endfire array for the intra-chip case shows a good consistency between the simulation and measured results. For inter-chip scenarios, despite best alignment between the arrays, the measured results are quite lower than the simulated results. This may be due to the fabrication variation.

The arrays are intended for beam steering in all directions with electronic phase shifters. Typically they would not have the feed systems of the type considered in the thesis. The feed system with path lengths delays was only for experimental validation of the concept of beam steering. Therefore, fixed angles were selected together with different antenna orientations. A variety of configurations have been illustrated that cover various scenarios as the beam is being steered electronically.

The measured and simulated results are satisfactory. Though there are more losses in measured transmission, overall the results show the feasibility of arrays on the silicon chip. The losses in measurements can happen due to the difference in various parameters in simulation like losses in the silicon substrate, variation in dimensions of the chip and arrays, variation in fabrication processes, etc.

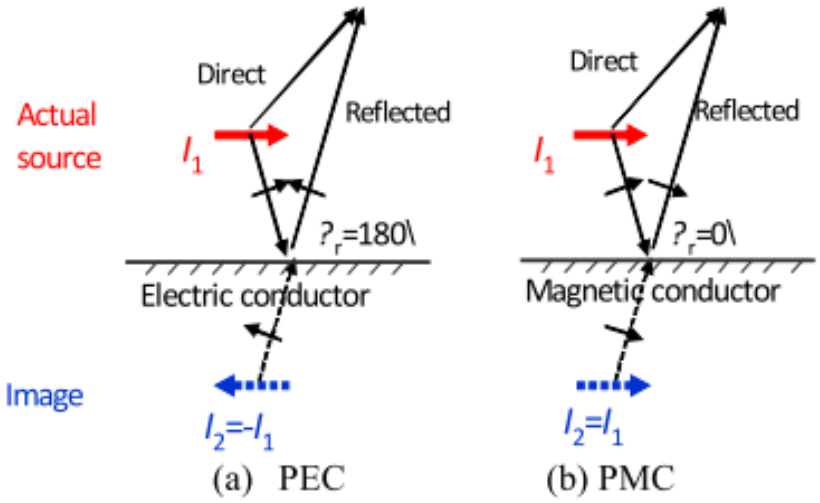
4 Techniques for enhancement of Intra- and Inter-chip transmission using AMC

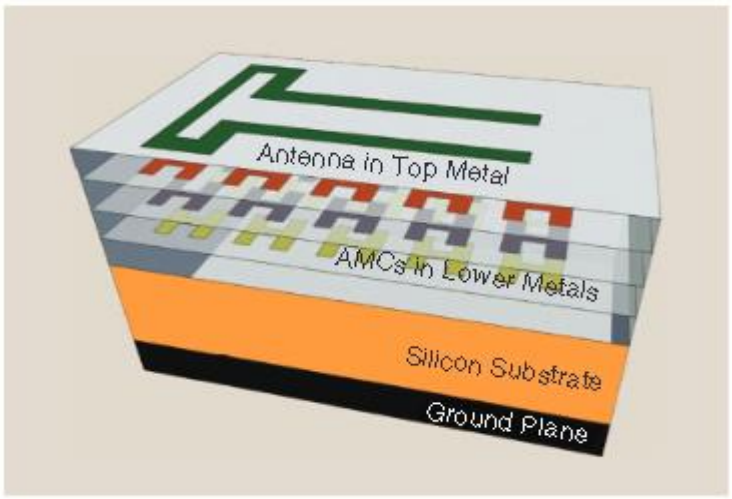
Artificial Magnetic Conductor (AMC) is a special arrangement of planar structures that can be used to manipulate the properties of electromagnetic waves like reflection, et al. AMC, when placed at a certain distance from the antenna, can help to increase the gain and therefore transmission between the antennas. Also, it can help reduce the mutual coupling between antenna elements in an array. AMC is also used in cases where the ground plane is very close to an antenna to improve its radiation efficiency.

A planar electric monopole or dipole in silicon dioxide has electrical current flowing on it which radiates the electromagnetic waves. When the ground plane or electrical conducting plane is close ($< \lambda/4$) to the antenna, the ground plane generates a reverse image current as shown in Figure 4-1 (a). The current on the antenna and its reverse current cancel out each other hence the overall radiation efficiency of the antenna is reduced. To improve the efficiency an AMC layer is placed under the antenna, this layer generates an image current in the same direction as the original current in the antenna shown in Figure 4-1 (b). As shown in Figure 4-1 (c), the AMC layers can be fabricated on lower metal layers using the CMOS process.

4.1 Work-related to the artificial magnetic conductor

Khan, et al. has developed a W-band double rhomboid bow tie-slot on-chip antenna with EBG at the bottom [94]. The overall size of the chip is 1mm x 1mm and operating frequency is from 75-100 dB with S_{11} of -6dB and below. The peak measured gain is -0.58dBi at 84GHz.





(c)

Figure 4-1. Image current formation due to (a) ground plane (PEC) and (b) AMC layer (PMC), (c) structure of AMC layer with antenna on top [95].

Other than AMC structures that require a large area to form a good performance structure, partially reflective surfaces are also used to enhance the radiation pattern of the on-chip antenna [96]. Bao, et al. have developed a novel AMC with a wideband loop antenna. The antenna has achieved gain enhancement at 60GHz band [97]. It is shown in Figure 4-2. In [98], Nafe, et al have proposed a new structure is proposed using a ground plane above the silicon and then AMC layer in between antenna and ground plane in silicon dioxide as shown in Figure 4-3. Also, it has been found that as the number of unit cells increases the gain of the antenna increases. They have used

square loop structures as an AMC unit cell. Moreover, another work has shown a wideband AMC and multi-band AMCs [99].

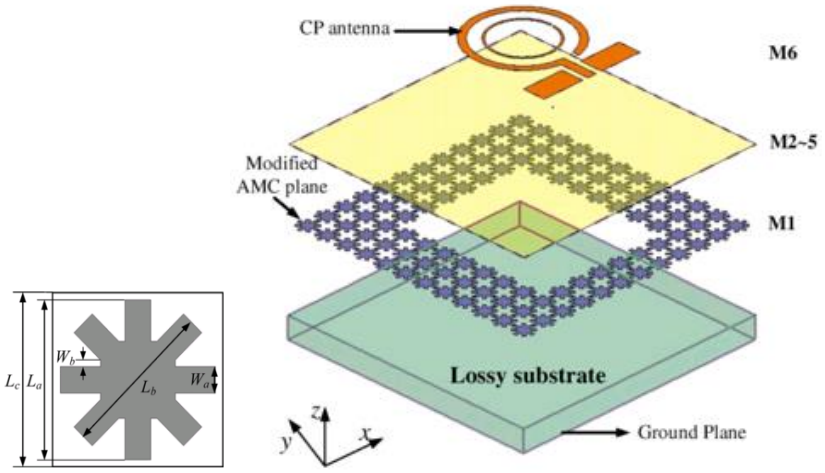


Figure 4-2.(a) Loop antenna with a modified AMC plane [97].

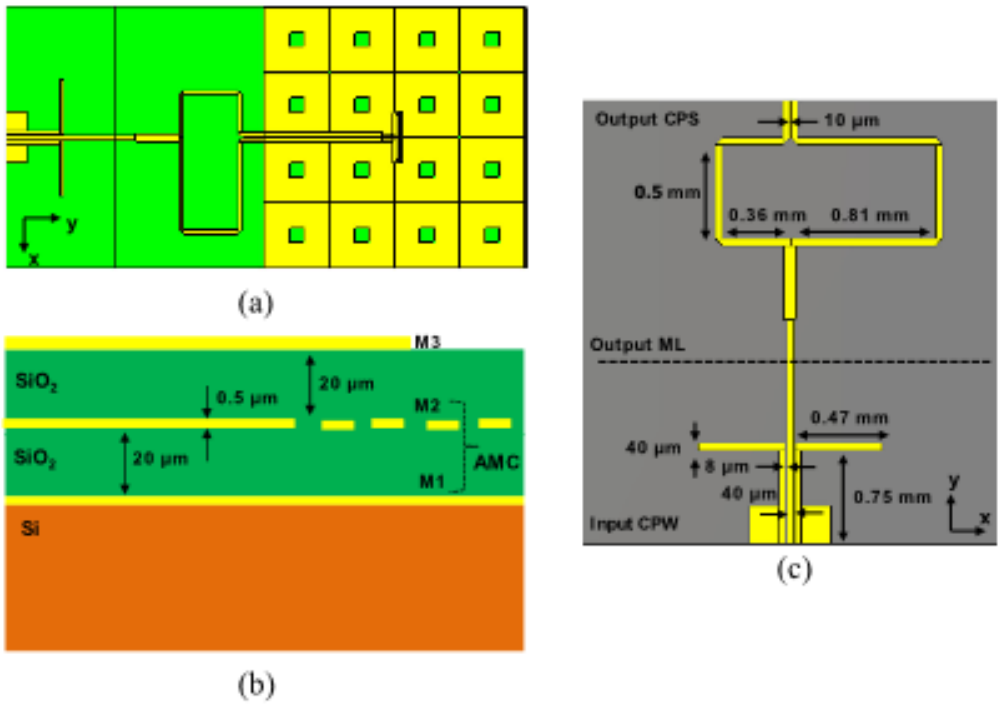


Figure 4-3. Antenna on an AMC layers [98].

4.2 Design of JC-AMC unit

In this preliminary work, a Jerusalem cross (JC) shape is used as an AMC. The cross-section of the setup of the chip is shown in Figure 4-5 (a). The AMC is designed keeping in mind the silicon with dielectric constant of 11.7 and resistivity of 55Ω-cm. Then the AMC is placed in the silicon dioxide layer 1µm above the silicon. The antenna is proposed to be designed at 8µm on the top of AMC layer. In Figure 4-5 (b), the shape of JC-AMC is shown along with its optimized dimensions. The shape of the AMC is optimized using the ANSYS HFSS. The setup of the model in HFSS is shown in Figure 4-5 (c) with Floquet port and master-slave boundaries. A plane wave

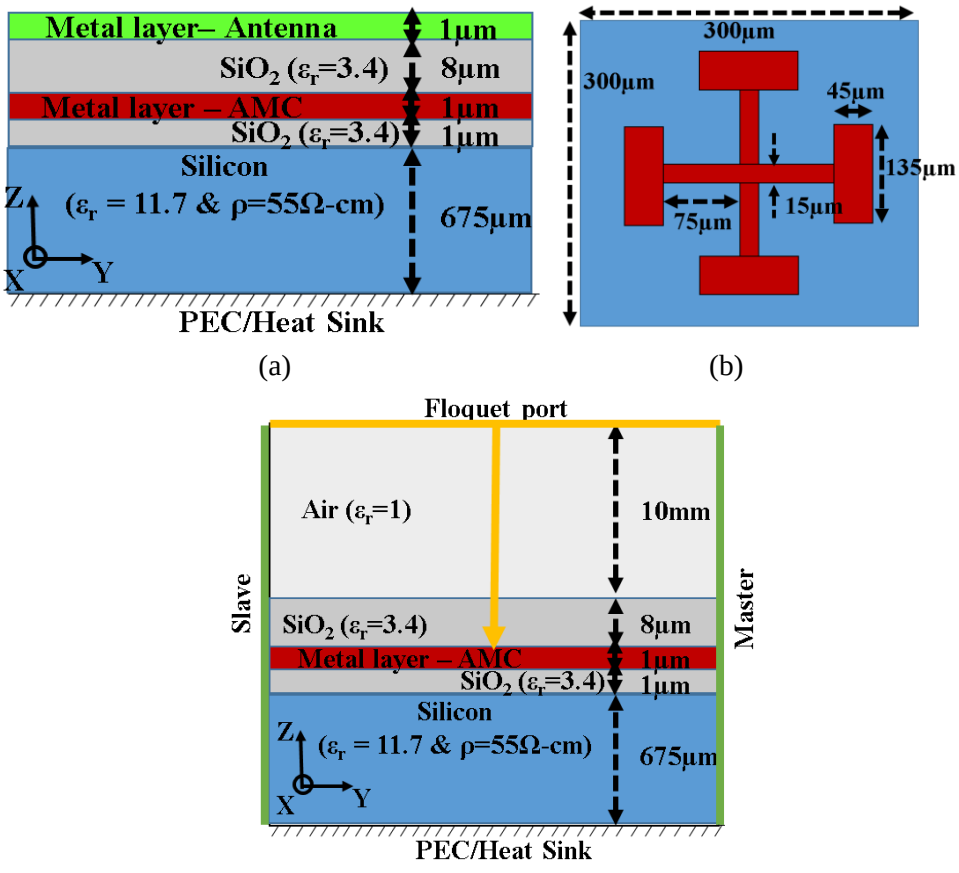


Figure 4-4 (a) Cross-section of the multicore chip, (b) Top view of JC-AMC, (c) Simulation setup for designing AMC unit cell.

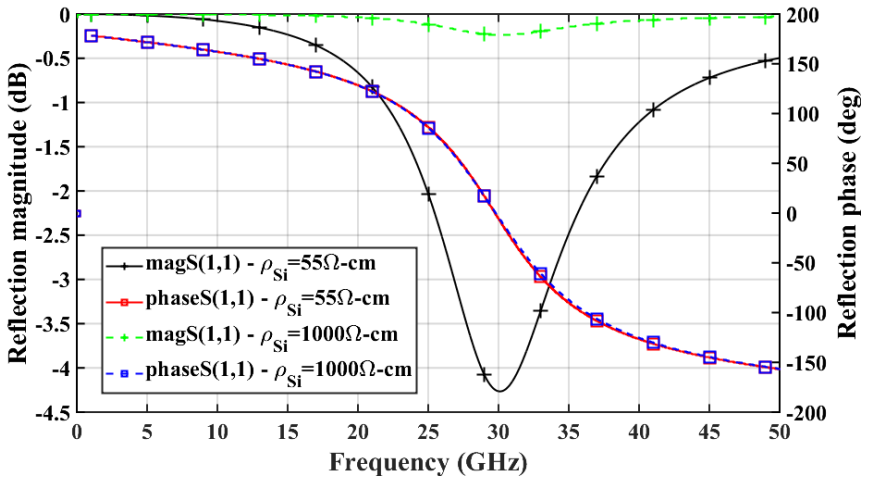
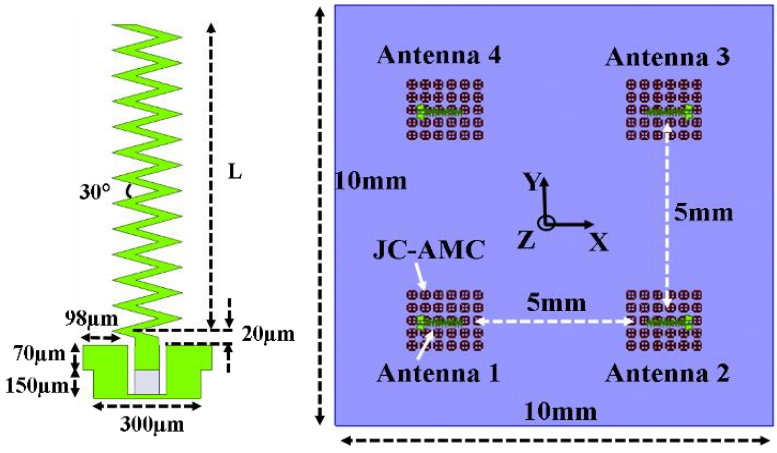


Figure 4-5 Reflection coefficients (magnitude in dB and phase in degrees) of JC-AMC.

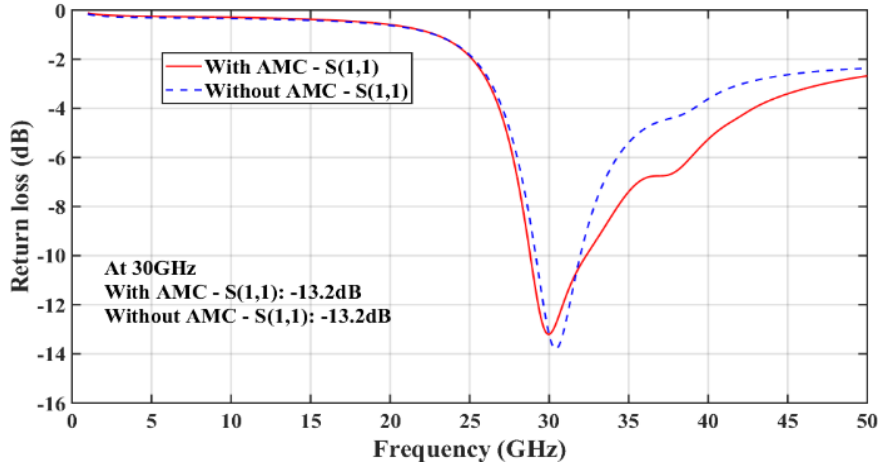
is directed towards the AMC from the Floquet port at the top of the setup. The power and phase of the reflected wave are simulated by the HFSS. The reflection coefficients at the Floquet port for different resistivities of silicon are shown in Figure 4-5. The results show that the AMC is reflecting power with a zero phase difference with respect to the incident wave.

4.3 Transmission enhancement

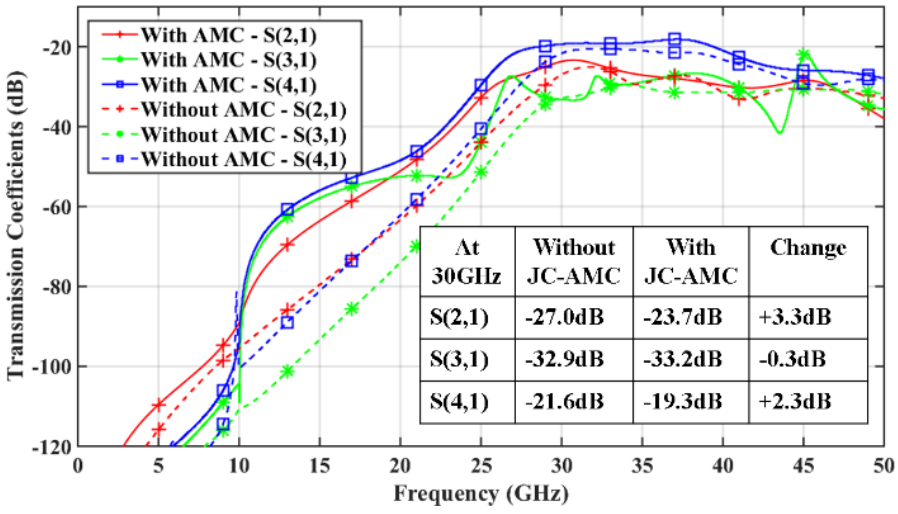
In this section, a multicore silicon chip of size 10mm x 10mm having a thickness of 675µm, and resistivity of 55Ω-cm is considered. This chip is equally divided into four quadrants each with potentially many cores. A zigzag monopole antenna, shown in Figure 4-6 (a), is used as wireless interconnect in each quadrant. The zigzag antenna is placed in the top metal layer. A 5x6 grid of above designed JC-AMC is put under the zigzag antennas in AMC layer shown in Figure 4-6 (b). The thickness of metal layers is 1µm. The length of the zigzag antenna (L) with and without JC-AMC is 860 µm and 930 µm, respectively. The antennas are re-optimized to resonance at 30GHz. The top view of the chip is shown in Figure 4-6 (b). The far-field boundary for the antenna is given by $\lambda/2\pi$ which is 1.6mm at 30GHz in free-space. The antennas are located at 5mm apart beyond their far-field boundaries.



(a) (b)



(c)



At 30GHz	Without JC-AMC	With JC-AMC	Change
S(2,1)	-27.0dB	-23.7dB	+3.3dB
S(3,1)	-32.9dB	-33.2dB	-0.3dB
S(4,1)	-21.6dB	-19.3dB	+2.3dB

(d)

Figure 4-6 (a) Zigzag antenna. (b) Top view of JC-AMC. (c) Reflection coefficient of antennas with and without AMCs. (d) Transmission coefficients between antennas w/ and w/o AMC.

After the simulation in ANSYS HFSS, the reflection coefficients of antennas is shown in Figure 4-6 (c). Since, all antennas are placed in the same arrangements so reflection coefficient of antennas is the same, therefore, return loss of one antenna with and without JC-AMC is shown. Figure 4-6 (c) shows that the zigzag antennas are resonating at 30GHz with a reflection coefficient of about -13dB. The return loss is optimized to be the same in case of with and without JC-AMC to show any comparison. The radiation efficiency of antennas is enhanced from 35% to 40%. The transmission coefficients of antennas 2, 3 and 4 with respect to antenna 1 in case of with and without JC-AMC is shown in Figure 4-6 (d). The enhancement of transmission for antenna 2 and 4 with respect to antenna 1 are about 3.3dB and 2.3dB, respectively. Using JC-AMC, the received power at the antenna is almost doubled. This enhancement is beneficial when designing on-chip integrated transceivers which are often restricted to constrain of the signal-to-noise ratio in link-budget. This increases the flexibility of designing integrated communication systems. This enhancement can still be improved by further optimization.

4.4 Challenges when using AMCs the transmission between the antennas and Future work

The idea of using the AMC is very intriguing, however, implementing AMC in a practical situation is not without trade-offs and challenges. In this section, some of the challenges are discussed.

One challenge with AMC layers is for its effective performance, the AMC layer should have many unit cells [98]. Designing and simulating these AMC cells would require a significant amount of computing resources. Second, the design will require more area overhead on-chip. The space available is quite limited to us. Another problem is the antenna in the silicon-dioxide (SiO_2)

layer is very close to the AMC layer just a few micrometers. This affects the performance of the AMC layer.

Moreover, the aim of the work which uses AMCs in literature is mostly to enhance the radiation orthogonal to the AMC layer, however, in this work, the intra-chip and inter-chip wireless transmission occur in the plane of AMC layer. One more problem which occurs when using the AMC layers is the antenna aperture becomes smaller as more elements are added to the antenna. In this way, the antenna with AMC may become a better transmitter, but there is still a question about its receiving capacity since the antenna aperture is quite small. Researchers are overcoming these issues at mmWave frequencies by using novel and innovative AMC designs. Such methods will be explored as future work.

5 Final Discussion and Conclusions

In this work, the transmission between wireless interconnects, implemented as antennas on-chip (AoC), in a wire-bonded chip package are studied using simulation and measurements at 30GHz. The simulations were performed in ANSYS HFSS. The simulated results presented the reflection coefficients along with the transmission coefficients between the on-chip antennas. The results showed that the transmission coefficients between wireless interconnects for inter-chip scenarios range from -45dB to -60dB at 30GHz while sustaining bandwidths up to 7GHz. The results also discussed the simulated electric field distribution across the chip package. After measurements, fabricated antennas showed a shift of resonance to 25GHz. Further simulations were performed where the GSG probe is feeding the zigzag antenna. It was seen that the probes do influence the measurement by shifting the resonance to 1.5GHz. Also, the SOLT calibration is known to show discrepancies at mmWave frequencies. Furthermore, a large-scale channel model for the inter-chip communication scenario between wireless interconnects is presented using the measured results in a wire-bonded package. Moreover, simulation results were provided for the wireless interconnects operating at 60GHz frequencies band in a flip-chip package. It was found that the inter-chip transmission at 60GHz between the different pairs of antennas ranges from -50dB to -55dB.which is satisfactory in such an environment. Due to the complicated flip-chip package, fabrication and measurements of on-chip antennas will be considered as future work.

The transmission coefficients observed in the previous cases can be further improved by using antenna arrays to perform beamforming which can increase the overall system gain. Three types of arrays are designed with different beam angles – broadside, phased and endfire, which are considered in two scenarios that are intra-chip and inter-chip. The antenna elements were fed using delayed-line system to create the desired progressive phase difference for corresponding arrays.

For broadside arrays working at 60GHz, the measured transmission when the beam max was directed in between the array pair for untrimmed-feed for intra-chip scenario varied from -43 to -55dB, and for inter-chip scenario, it varied from -35dB to -40dB. For phased array in the intra-chip scenario, the measured transmission between the arrays with untrimmed-feed varies from -37dB to -42dB at 60GHz. Lastly, the endfire arrays for the intra-chip scenario are also discussed which showed good consistency between the simulation and measured results. For inter-chip scenarios, despite best alignment between the arrays, the measured results are quite lower than the simulated results. This might be due to the fabrication variation. Simulated radiation patterns and electric field density are plotted to show beamforming for all types of designed arrays located at various locations across the chip. These radiation patterns are compared with the radiation patterns in free-space. The simulated beam of the array is distorted by the losses in the silicon substrate and diffraction effects due to the chip structure. The measured transmission coefficients would be useful to find the link budget for the system-level design.

Moreover, innovative techniques like artificial magnetic conductors (AMC) are investigated to improve the transmission between wireless interconnects which are implemented as zigzag antennas on the chip. The simulations are performed to design the Jerusalem-cross (JC) AMC. The results show that the reflection phase is zero at 60GHz. This JC-AMC unit cell is then simulated under the zigzag antenna with a 5x6 planar JC elements. The intra-chip transmission shows an improvement of about 3dB for two of the three intra-chip antenna pairs. This is lower than expected, because of the lower antenna aperture. Further study should be performed to find the optimal number of JC-AMC elements which can provide better transmission between antennas. In the future, more work is required to further analyze and fabricate AMC layers under antennas and arrays.

The proposed antennas and arrays would be operating in 60GHz unlicensed bands because of the availability of large bandwidth. But these bands are also used by other external WiGig devices. Although the transmitted power from the antenna of the on-chip system would be relatively low compared to the external devices which would communicate to devices much farther away. So, the power from on-chip antennas might not affect the external mmWave communication systems. But, the external mmWave communication systems working at 60GHz like WiGig with high transmission power may affect the on-chip wireless system. A comprehensive study is also needed to understand the effects of external 60GHz devices on the antennas and arrays in the MCMC systems. One way to isolate the on-chip system is to use a metal covering around the chip which is commonly known as Faraday cage, however, this metal covering can create problems like multipath interference because the metal covering would reflect antenna radiation. Proper experiments are required when encasing such wireless systems in a Faraday Cage like structure. Another way is to use shared medium access (MAC) mechanisms the same as the external WiGig system to reduce interference. This might require implementation of low-power implementation of the WiGig MAC mechanism on the processor chip. A study is required to evaluate the area overhead required and the power requirement to support such a shared MAC mechanism.

There is also a need to characterize substrate material at 60GHz band mmWave frequencies since there are only a few works available in the literature. A brief overview of the challenges involve in fabrication and measurement is provided in section 2.3.3. Further work is required to understand the difference between simulations and measurements. In this work, the differences between simulations and measurements are observed, to increase the understanding multiple fabrications must be performed to clear the discrepancies between simulation and measurement.

References

[1] “Intel Xeon 9200 CPU series,” 2019. [Online]. Available: https://www.anandtech.com/show/14182/hands-on-with-the-56core-xeon-platinum-9200-cpu-intels-biggest-cpu-package-ever. [Accessed: 31-July-2019].

[2] “AMD EPYC,” 2018. [Online]. Available: https://www.amd.com/system/files/2018-03/AMD-Optimizes-EPYC-Memory-With-NUMA.pdf. [Accessed: 31-July-2019].

[3] Intel Corporation, “Intel ® Xeon ® Processor E7-8800 / 4800 v4 Product Families - Thermal Mechanical Specification and Design Guide,” 2016. https://www.intel.com/content/dam/www/public/us/en/documents/design-guides/xeon-e7-v2-thermal-guide.pdf. [Accessed: 31-July-2019].

[4] E. Perfecto and K. Srivastava, “Technology Trends: Past, Present, and Future,” in *Advanced Flip Chip Packaging*, H.-M. Tong, Y.-S. Lai, and C. P. Wong, Eds. Boston, MA: Springer US, 2013, pp. 23–52.

[5] “Cmos-chip structure in 2000.” [Online]. Available: https://commons.wikimedia.org/wiki/File:Cmos-chip_structure_in_2000s_%28en%29.svg. [Accessed: 31-July-2019].

[6] “Copper Interconnects - IBM.” [Online]. Available: http://www-03.ibm.com/ibm/history/ibm100/us/en/icons/copperchip/. [Accessed: 31-July-2019].

[7] M. Bohr, “Interconnect scaling - The real limiter to high performance VLSI.,” *IEEE Int. Electron Devices Meet.*, pp. 241–244, 1995.

[8] A. M. Ibrahim, “Global (interconnect) warming,” *IEEE Circuits Devices Mag.*, vol. 17, no. 5, pp. 16–32, 2001.

[9] L. Benini and G. De Micheli, “Networks on Chips: A New SoC Paradigm,” *Computer (Long. Beach. Calif).*, vol. 35, no. 1, pp. 70–78, 2002.

[10] “TILE-Gx72 Porcessor” [Online]. Available: http://www.mellanox.com/related-docs/prod_multi_core/PB_TILE-Gx72.pdf. [Accessed: 31-July-2019].

[11] B. Bohnenstiehl *et al.*, "KiloCore: A 32-nm 1000-Processor Computational Array," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 891-902, April 2017.

[12] S. Deb, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Wireless NoC as interconnection backbone for multicore chips: Promises and challenges," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 2, no. 2, pp. 228–239, 2012.

[13] T. Baehr-Jones, T. Pinguet, P. Lo Guo-Qiang, S. Danziger, D. Prather, and M. Hochberg, "Myths and rumours of silicon photonics," *Nat. Photonics*, vol. 6, no. 4, pp. 206–208, 2012.

[14] S. Laha, S. Kaya, D. W. Matolak, W. Rayess, D. DiTomaso and A. Kodi, "A New Frontier in Ultralow Power Wireless Links: Network-on-Chip and Chip-to-Chip Interconnects," in IEEE Trans. Comput.-Aided Design of Integr. Circuits Syst., vol. 34, no. 2, pp. 186-198, Feb. 2015.

[15] M. S. Shamim, N. Mansoor, R. S. Narde, V. Kothandapani, A. Ganguly, and J. Venkataraman, "A Wireless Interconnection Framework for Seamless Inter and Intra-Chip Communication in Multichip Systems," *IEEE Trans. Comput.*, vol. 66, no. 3, pp. 389–402, Mar. 2017.

[16] "FCC: Part 15 Rules for unlicensed operation in 57-64GHz band." [Online]. Available: https://www.fcc.gov/document/part-15-rules-unlicensed-operation-57-64-ghz-band. [Accessed: 31-July-2019].

[17] J. Buechler, E. Kasper, P. Russer, and K. M. Strohm, "Silicon High-Resistivity-Substrate Millimeter-Wave Technology," *IEEE Trans. Electron Devices*, vol. 33, no. 12, pp. 2047–2052, 1986.

[18] K. Kim, H. Yoon, and K. Kenneth, "On-Chip Wireless Interconnection with Integrated Antennas," *Iedm 2000*, pp. 485–488, 2000.

[19] T. Deng and Y. P. Zhang, "On-Chip Antennas," in Handbook of Antenna Technologies, Singapore: Springer Singapore, 2016, pp. 1565–1584.

[20] H. M. Cheema and A. Shamim, "The last barrier: On-chip antennas," *IEEE Microw. Mag.*, vol. 14, no. 1, pp. 79–91, 2013.

[21] K. O. Kenneth et al., “On-chip antennas in silicon ICs and their application,” *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1312–1323, 2005.

[22] J. J. Lin et al., “Communication using antennas fabricated in silicon integrated circuits,” *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1678–1686, 2007.

[23] C. K. Munuswamy, J. Venkataraman, and A. Ganguly, “Design of antennas for 3D wireless Network-on-Chip with micro-fluidic cooling layers,” *2016 IEEE Antennas Propag. Soc. Int. Symp. APSURSI 2016 - Proc.*, pp. 257–258, 2016.

[24] F. Gutierrez, “Design of a Wideband Antenna for Wireless Network-On-Chip in Multimedia Applications,” *J. Low Power Electron. Appl.*, vol. 7, no. 2, 2017.

[25] A. Bronner, F. Schwarze and F. Ellinger, "60 GHz On-Chip BiCMOS Bow-Tie Antenna," *2018 IEEE-APS Topical Conference on Antennas and Propagation in Wireless Communications (APWC)*, Cartagena des Indias, 2018, pp. 769-772.

[26] Zhang, Y. P., Sun, M., & Guo, L. H. (2005). On-ChipAntennas for 60-GHz Radios in Silicon Technology. IEEETransactions on Electron Devices, 52(7), 1664-1668.

[27] Shun-Sheng Hsu, Kuo-Chih Wei, Cheng-Ying Hsu, and Huey Ru-Chuang, “A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18-μm CMOS Technology,” *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 625–627, Jun. 2008.

[28] R. Willmot, D. Kim and D. Peroulis, "A Yagi–Uda Array of High-Efficiency Wire-Bond Antennas for On-Chip Radio Applications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3315-3321, Dec. 2009.

[29] K. T. Chan *et al*., "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," in *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 11, pp. 487-489, Nov. 2003.

[30] R. Wu *et al*., "A 60-GHz efficiency-enhanced on-chip dipole antenna using helium-3 ion implantation process," *2014 44th European Microwave Conference*, Rome, 2014, pp. 108-111.

[31] Y. Baek *et al*., "94-GHz Log-Periodic Antenna on GaAs Substrate Using Air-Bridge Structure," in *IEEE Antennas and Wireless Propagation Letters*, vol. 8, pp. 909-911, 2009.

[32] H. Kuo, H. Yue, Y. Ou, C. Lin and H. Chuang, "A 60-GHz CMOS Sub-Harmonic RF Receiver With Integrated On-Chip Artificial-Magnetic-Conductor Yagi Antenna and Balun Bandpass Filter for Very-Short-Range Gigabit Communications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1681-1691, April 2013.

[33] C. Li and T. Chiu, "Single Flip-Chip Packaged Dielectric Resonator Antenna for CMOS Terahertz Antenna Array Gain Enhancement," in *IEEE Access*, vol. 7, pp. 7737-7746, 2019.

[34] C. Deng, W. Liu, Q. Hao, and Z. Feng, "Micromachined 60 GHz postsupported patch antenna with flip-chip interconnect," *Microw. Opt. Technol. Lett.*, vol. 57, no. 11, pp. 2706–2710, Nov. 2015.

[35] Z. M. Chen and Y. P. Zhang, "Inter-Chip Wireless Communication Channel: Measurement, Characterization, and Modeling," *IEEE Trans. Antennas Propag*., vol. 55, no. 3, pp. 978–986, Mar. 2007.

[36] Y. P. Zhang, Z. M. Chen, and M. Sun, "Propagation mechanisms of radio waves over intra-chip channels with integrated antennas: Frequency-domain measurements and time-domain analysis," *IEEE Trans. Antennas Propag*., vol. 55, no. 10, pp. 2900–2906, 2007.

[37] M. Sun, Y. P. Zhang, G. X. Zheng, and W. Y. Yin, "Performance of intra-chip wireless interconnect using on-chip antennas and UWB radios," *IEEE Trans. Antennas Propag*., vol. 57, no. 9, pp. 2756–2762, 2009.

[38] S. Redfield, S. Woracheewan, H. Liu, P. Chiang, J. Nejedlo, and R. Khanna, "Understanding the ultrawideband channel characteristics within a computer chassis," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, no. February, pp. 191–194, 2011.

[39] T. Kikkawa, "Wireless inter-chip interconnects," *Microelectron. Eng.*, vol. 88, no. 5, pp. 767–774, 2011.

[40] S. Khademi, S. P. Chepuri, Z. Irahhauten, G. J. M. Janssen, and A.-J. van der Veen, "Channel Measurements and Modeling for a 60 GHz Wireless Link Within a Metal Cabinet," *IEEE Trans. Wirel. Commun.*, vol. 14, no. 9, pp. 5098–5110, Sep. 2015.

[41] G. Wang, K. Zhan, T. Kamgaing, R. Khanna, H. Liu, and A. Natarajan, "Measurement-based channel modeling for mmWave wireless links in enclosed server platforms," in *2017 IEEE Radio Wireless Symp. (RWS)*, 2017, pp. 141–143.

[42] D. W. Matolak, S. Kaya, and A. Kodi, “Channel modeling for wireless networks-on-chips,” *IEEE Commun. Mag.*, vol. 51, no. 6, pp. 180– 186, Jun. 2013.

[43] W. Rayess, D. W. Matolak, S. Kaya, and A. K. Kodi, “Antennas and Channel Characteristics for Wireless Networks on Chips,” Wirel. Pers. Commun., vol. 95, no. 4, pp. 5039–5056, 2017.

[44] S. H. Gade, S. S. Ram, and S. Deb, “Millimeter wave wireless interconnects in deep submicron chips: Challenges and opportunities,” *Integration*, vol. 64, no. September 2018, pp. 127–136, Jan. 2019.

[45] I. El Masri, T. L. Gouguec, P. Martin, R. Allanic and C. Quendo, "Electromagnetic Characterization of the Intra-chip Propagation Channel in Ka and V Bands," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*. doi: 10.1109/TCPMT.2019.2930347

[46] H. Nakano, H. Tagami, A. Yoshizawa, and J. Yamauchi, “Communications. Shortening Ratios of Modified Dipole Antennas,” *IEEE Trans. Antennas Propag.*, vol. 32, no. 4, pp. 385–386, 1984.

[47] S. Abadal *et al.*, "Scalability of Broadcast Performance in Wireless Network-on-Chip," in *IEEE Trans. Parallel Distrib. Syst.*, vol. 27, no. 12, pp. 3631-3645, 1 Dec. 2016.

[48] W. Roh *et al.*, “Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results,” *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106– 113, 2014.

[49] S. Abadal, J. Torrellas, E. Alarcón and A. Cabellos-Aparicio, "OrthoNoC: A Broadcast-Oriented Dual-Plane Wireless Network-on- Chip Architecture," in IEEE Trans. Parallel Distrib. Syst., vol. 29, no. 3, pp. 628-641, 1 March 2018.

[50] “Intel Pentium pro – thermal design guide.” [Online]. Available: http://datasheets.chipdb.org/Intel/x86/Pentium%20Pro/24276601.pdf. [Accessed: 05-08-2019]

[51] “Recycle CPU Intel Pentium Pro processor.” [Online]. Available: https://www.youtube.com/watch?v=V-J4XGVksfM. [Accessed: 05-08-2019].

[52] “Gold value in Intel Pentium pro.” [Online]. Available: http://www.chipsetc.com/gold-value-in-computer-chips.html. [Accessed: 05-08-2019].

[53] C. Capps, “Near field or far field?,” Electrical Design News, vol. 46, p. 18, 2001.

[54] K. Kim, W. Bomstad, and K. Kenneth, “A plane wave model approach to understanding propagation in an intra-chip communication system,” *Antennas Propag. Soc. Int. Symp. 2001. IEEE*, vol. 2, pp. 166–169, 2001.

[55] R. S. Narde,’Wireless Interconnects for Intra-chip & Inter-chip Transmission’, Rochester Institute of Technology, 2017.

[56] E. M. Godshalk, J. A. Williams and J. N. Burr, “High-Frequency Probe Tip Assembly,” U.S. Patent 5 506 515, Apr. 9, 1996.

[57] Q. Li and K. L. Melde, “The impact of on-wafer calibration method on the measured results of coplanar waveguide circuits,” *IEEE Trans. Adv. Packag.*, vol. 33, no. 1, pp. 285–292, 2010.

[58] A. C. F. Reniers, Q. Liu, M. H. A. J. Herben, and A. B. Smolders, “Review of the accuracy and precision of mm-wave antenna simulations and measurements,” in *2016 10th Eur. Conf. Antennas Propag. (EuCAP)*, 2016, pp. 1–5.

[59] M. R. Karim, X. Yang and M. F. Shafique, "On Chip Antenna Measurement: A Survey of Challenges and Recent Trends," in *IEEE Access*, vol. 6, pp. 20320-20333, 2018.

[60] A. C. F. Reniers, A. R. Van Dommele, A. B. Smolders, and M. H. A. J. Herben, “The Influence of the Probe Connection on mm-Wave Antenna Measurements,” *IEEE Trans. Antennas Propag.*, vol. 63, no. 9, pp. 3819–3825, 2015.

[61] D. Muller *et al.*, “Electromagnetic field simulation of MMICs including RF probe tips,” *Eur. Microw. Week 2017 “A Prime Year a Prime Event”, EuMW 2017 - Conf. Proceedings; 47th Eur. Microw. Conf. EuMC 2017*, vol. 2017-Janua, pp. 900–903, 2017.

[62] A. Papio Toda and F. De Flaviis, “60-GHz Substrate Materials Characterization Using the Covered Transmission-Line Method,” IEEE Trans. Microw. Theory Tech., vol. 63, no. 3, pp. 1063–1075, Mar. 2015.

[63] T. Rappaport, *Wireless Communications: Principles and Practice*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall PTR, 2001.

[64] S. S. Ghassemzadeh, R. Jana, C. W. Rice, W. Turin, and V. Tarokh, “Measurement and modeling of an ultra-wide bandwidth indoor channel,” *IEEE Trans. Commun.*, vol. 52, no. 10, pp. 1786–1796, 2004.

[65] T. Gupta, “Routing and Reliability,” in *Copper Interconnect Technology*, vol. 1, New York, NY: Springer New York, 2009, pp. 347–403.

[66] S. R. Vangal *et al*., "An 80-Tile Sub-100-W TeraFLOPS Processor in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 29-41, Jan. 2008.

[67] E. G. Friedman, "Clock distribution networks in synchronous digital integrated circuits," in *Proc. IEEE*, vol. 89, no. 5, pp. 665-692, May 2001.

[68] W. S. Song and L. A. Glasser, "Power distribution techniques for VLSI circuits," *IEEE J. Solid-State Circuits*, vol. 21, no. 1, pp. 150-156, Feb. 1986.

[69] R. S. Narde, N. Mansoor, A. Ganguly, and J. Venkataraman, “On-Chip Antennas for Inter-Chip Wireless Interconnections: Challenges and Opportunities,” in *12th European Conference on Antennas and Propagation (EuCAP 2018)*, 2018, pp. 600 (5 pp.)-600 (5 pp.).

[70] A. Ganguly, K. Chang, S. Deb, P. P. Pande, B. Belzer and C. Teuscher, "Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems," in *IEEE Transactions on Computers*, vol. 60, no. 10, pp. 1485-1502, Oct. 2011.

[71] W. Roh *et al*., "Millimeter-wave beamforming as an enabling technology for 5G cellular communications: theoretical feasibility and prototype results," in *IEEE Communications Magazine*, vol. 52, no. 2, pp. 106-113, February 2014.

[72] W. Hong, "Solving the 5G Mobile Antenna Puzzle: Assessing Future Directions for the 5G Mobile Antenna Paradigm Shift," in *IEEE Microwave Magazine*, vol. 18, no. 7, pp. 86-102, Nov.-Dec. 2017.

[73] A. Babakhani, X. Guan, A. Komijani, A. Natarajan and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," in *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2795-2806, Dec. 2006.

[74] K. Sengupta and A. Hajimiri, "A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3013-3031, Dec. 2012.

[75] K. Sengupta, D. Seo, L. Yang and A. Hajimiri, "Silicon Integrated 280 GHz Imaging Chipset With 4$\times$4 SiGe Receiver Array and CMOS Source," in *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 3, pp. 427-437, May 2015.

[76] P. Baniya, A. Bisognin, K. L. Melde and C. Luxey, "Chip-to-Chip Switched Beam 60 GHz Circular Patch Planar Antenna Array and Pattern Considerations," in *IEEE Transactions on Antennas and Propagation*, vol. 66, no. 4, pp. 1776-1787, April 2018.

[77] P. Baniya and K. L. Melde, "Switched-Beam Endfire Planar Array With Integrated 2-D Butler Matrix for 60 GHz Chip-to-Chip Space-Surface Wave Communications," in *IEEE Antennas and Wireless Propagation Letters*, vol. 18, no. 2, pp. 236-240, Feb. 2019.

[78] A. Rashidian, S. Jafarlou, A. Tomkins, K. Law, M. Tazlauanu and K. Hayashi, "Compact 60 GHz Phased-Array Antennas With Enhanced Radiation Properties in Flip-Chip BGA Packages," in *IEEE Transactions on Antennas and Propagation*, vol. 67, no. 3, pp. 1605-1619, March 2019.

[79] D. G. Kam, D. Liu, A. Natarajan, S. K. Reynolds and B. A. Floyd, "Organic Packages With Embedded Phased-Array Antennas for 60-GHz Wireless Chipsets," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 11, pp. 1806-1814, Nov. 2011.

[80] T. Zhang, L. Li, M. Xie, H. Xia, X. Ma and T. J. Cui, "Low-Cost Aperture-Coupled 60-GHz-Phased Array Antenna Package With Compact Matching Network," in *IEEE Transactions on Antennas and Propagation*, vol. 65, no. 12, pp. 6355-6362, Dec. 2017.

[81] Z. Cao *et al.*, "Advanced Integration Techniques on Broadband Millimeter-Wave Beam Steering for 5G Wireless Networks and Beyond," in *IEEE Journal of Quantum Electronics*, vol. 52, no. 1, pp. 1-20, Jan. 2016, Art no. 0600620.

[82] B. Xu et al., "Radiation Performance Analysis of 28 GHz Antennas Integrated in 5G Mobile Terminal Housing," in IEEE Access, vol. 6, pp. 48088-48101, 2018.

[83] J. Park, S. Y. Lee, Y. Kim, J. Lee and W. Hong, "Hybrid Antenna Module Concept for 28 GHz 5G Beamsteering Cellular Devices," *2018 IEEE MTT-S International Microwave Workshop Series on 5G Hardware and System Technologies (IMWS-5G)*, Dublin, 2018, pp. 1-3.

[84] X. Chen, M. Abdullah, Q. Li, J. Li, A. Zhang and T. Svensson, "Characterizations of Mutual Coupling Effects on Switch-Based Phased Array Antennas for 5G Millimeter-Wave Mobile Communications," in *IEEE Access*, vol. 7, pp. 31376-31384, 2019.

[85] M. J. Al-Hasan, T. A. Denidni, A. R. Sebak, "Millimeter-Wave Compact EBG Structure for Mutual Coupling Reduction Applications,"*IEEE Trans. Antennas Propag*., vol. 63, No 2. Feb 2015

[86] C. Balanis, *Antenna Theory*, 3nd ed. Wiley Publications, USA, 2005.

[87] S. Ghosh and D. Sen, "An Inclusive Survey on Array Antenna Design for Millimeter-Wave Communications," in *IEEE Access*, vol. 7, pp. 83137-83161, 2019.

[88] A. Chakraborty and B. Gupta, “Paradigm Phase Shift: RF MEMS Phase Shifters: An Overview,” *IEEE Microw. Mag.*, vol. 18, no. 1, pp. 22–41, Jan. 2017.

[89] S. Shamsadini, I. M. Filanovsky, P. Mousavi and K. Moez, "A 60-GHz Transmission Line Phase Shifter Using Varactors and Tunable Inductors in 65-nm CMOS Technology," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 10, pp. 2073-2084, Oct. 2018.

[90] W. Rayess, D. W. Matolak, S. Kaya, and A. K. Kodi, “Antennas and Channel Characteristics for Wireless Networks on Chips,” Wirel. Pers. Commun., vol. 95, no. 4, pp. 5039–5056, 2017.

[91] J. Wu, A. K. Kodi, S. Kaya, A. Louri and H. Xin, "Monopoles Loaded With 3-D-Printed Dielectrics for Future Wireless Intrachip Communications," in *IEEE Transactions on Antennas and Propagation*, vol. 65, no. 12, pp. 6838-6846, Dec. 2017.

[92] X. Timoneda, A. Cabellos-Aparicio, D. Manessis, E. Alarcon, and S. Abadal, “Channel Characterization for Chip-scale Wireless Communications within Computing Packages,” in *2018 Twelfth IEEE/ACM International Symp. on Networks-on-Chip (NOCS)*, 2018, pp. 1–8.

[93] S. Moghadami, F. Hajilou, P. Agrawal and S. Ardalan, "A 210 GHz Fully-Integrated OOK Transceiver for Short-Range Wireless Chip-to-Chip Communication in 40 nm CMOS Technology," in *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 5, pp. 737-741, Sept. 2015.

[94] M. Saad Khan, F. A. Tahir, A. Meredov, A. Shamim and H. M. Cheema, "A W-Band EBG-Backed Double-Rhomboid Bowtie-Slot On-Chip Antenna," in *IEEE Antennas and Wireless Propagation Letters*, vol. 18, no. 5, pp. 1046-1050, May 2019.

[95] H. M. Cheema and A. Shamim, "The last barrier: On-chip antennas," *IEEE Microw. Mag.*, vol. 14, no. 1, pp. 79–91, 2013.

[96] C. Liu and R. G. Rojas, "V-Band Integrated on-Chip Antenna Implemented With a Partially Reflective Surface in Standard 0.13- μm BiCMOS Technology," in *IEEE Transactions on Antennas and Propagation*, vol. 64, no. 12, pp. 5102-5109, Dec. 2016.

[97] X. Bao, Y. Guo, et alalal, "60-GHz AMC-Based Circularly Polarized On-Chip Antenna Using Standard 0.18 μm CMOS Technology," IEEE Trans. Antennas Propag., vol. 60, no. 5, pp. 2234–2241, 2012.

[98] M. Nafe, A. Syed, and A. Shamim, "Gain Enhanced On-Chip Folded Dipole Antenna Utilizing Artificial Magnetic Conductor at 94 GHz," *IEEE Antennas Wirel. Propag. Lett.*, vol. 16, pp. 1–1, 2017.

[99] H. Vahimian, M. Naser-Moghaddasi and N. Amiri, "Designing Dual and Triple-wideband EBG Structures," *2019 5th Conference on Knowledge Based Engineering and Innovation (KBEI)*, Tehran, Iran, 2019, pp. 072-075.

[100] M. R. Karim, X. Yang and M. F. Shafique, "On Chip Antenna Measurement: A Survey of Challenges and Recent Trends," in *IEEE Access*, vol. 6, pp. 20320-20333, 2018.

[101] A. C. F. Reniers, A. R. van Dommele, A. B. Smolders and M. H. A. J. Herben, "The Influence of the Probe Connection on mm-Wave Antenna Measurements," in *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 9, pp. 3819-3825, Sept. 2015.