

SOLAR CELL DESIGN EMPLOYING A TEXTURED SURFACE

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ABSTRACT

Planar-junction, 1 mm x 1 mm, p+/n/n+ silicon solar cells, both with and without a textured surface, were fabricated in order to study the effects of decreased surface reflectance on cell efficiency. The texturing process was performed through the use of a KOH preferential etchant and an array of 10um x 10um windows to form an oxide masking layer. Inverted pyramids etched to points with final base widths being 13.7 microns due to undercutting of the masking oxide. Completed cells, evaluated at an irradiance of 100 mW/cm², showed greater efficiencies for the textured surface, but outputs of both were limited by series resistance.

INTRODUCTION

Recent advancements in the utilization of solar energy have been made through the creation of high efficiency silicon solar cells. Contemporary designs of concentrator silicon cells with point and planar junctions, high and low resistivity substrates, and a front metal grid have been shown to achieve efficiencies greater than 25% [1]. A technique for accomplishing this increased efficiency is through the use of a textured surface. By patterning the top layer of the substrate to form inverted pyramids, surface reflectance is decreased, and the absorption of light is enhanced [2,3].

Cross-sections of two patterned, silicon solar cells with front metal grids are shown in Figure 1. Design (a) was found to have an efficiency of 26% at 90 suns and was the highest ever reported for a silicon cell having a front metal grid. At 1 sun a 21.8% efficiency was reported. Design (b) had a 21% efficiency between 100 and 200 suns [1] and varies from design (a) through the use of a planar-junction instead of point-junctions. The inverted pyramids are produced through the utilization of a preferential etchant. The angles (54 degrees with the surface) of these pyramids are dependent upon the crystal orientation of the silicon. If the surface of a cell lies parallel to the (100) plane then the intersection of the (111) planes form the sides of the pyramid.

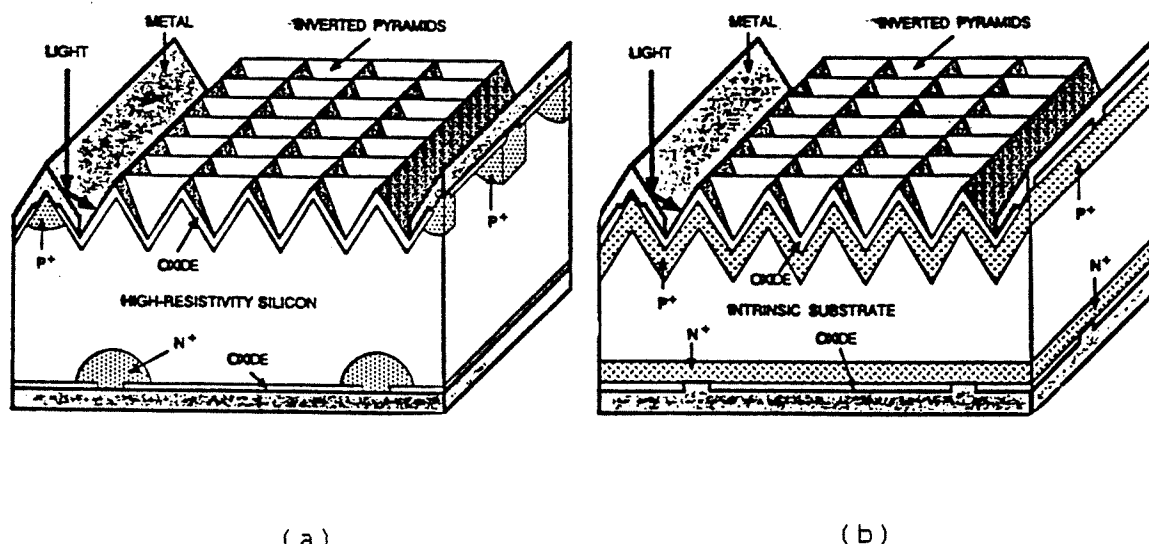


Figure 1: Cross-sectional View of Textured Solar Cells [1].

A light ray incident upon the surface of this cell will make at least two reflections [2,3,4] as shown in Figure 2. At the first point of incidence 33% of the light will be reflected for bare silicon [2]. This reflected light will make a second point of incidence on the opposite side of the pyramid and again 33% will be reflected. The total amount of reflection will be decreased to 11%. A reduction in surface reflectance of two-thirds is, therefore, possible. This percentage can be further reduced to as little as 3% through the use of an antireflective coating [2].

Transmitted light will also be refracted within the solar cell. This will cause the creation of large internal angles reaching the back surface. If the incident angle on the silicon surface is greater than 23 degrees, total internal reflection will take place as shown in Figure 2. Longer-wavelength photons that are allowed to reach the back surface will be reflected back in the direction of the front surface and the absorption of light will be increased [3,4].

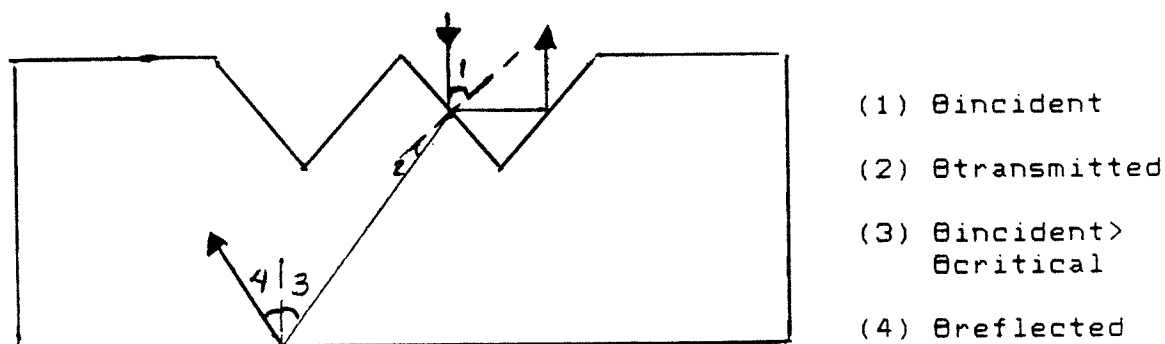


Figure 2: Light Ray Incident on Textured Surface.

The basic operation of the silicon solar cell is through the creation of electron-hole pairs with incident light. An incident photon with an energy greater than the band gap will be absorbed to create an electron in the conduction band and a hole in the valence band. As more photons are absorbed electron-hole formation will increase in the p-type and n-type regions, as well as the depletion region formed at the junction. The field created from the pn junction serves to sweep the electrons from the p-type region to the n-type region where they will be seen as majority carriers. In the same way the n-type region holes diffuse across the junction to add to the majority carriers in the p-type region. If a conductor is connected from the metal grid to the back metal surface a short circuit current, I_{sc} , will flow. An open-circuit voltage, V_{oc} , can also be measured between these connections. These terminal properties are illustrated in Figure 3.

A third parameter called the fill factor, FF, measures the squareness of the output characteristics [2]. Equation (1) shows how the fill factor can be derived using the maximum power voltage, V_{mp} and maximum power current, I_{mp} .

$$FF = V_{mp}I_{mp} / V_{oc}I_{sc} \quad (1)$$

The efficiency, η , of this cell is found as shown in Equation (2), where P_{in} is the total power of the incident light [2].

$$\eta = V_{mp}I_{mp} / P_{in} = V_{oc} I_{sc} FF / P_{in} \times 100\% \quad (2)$$

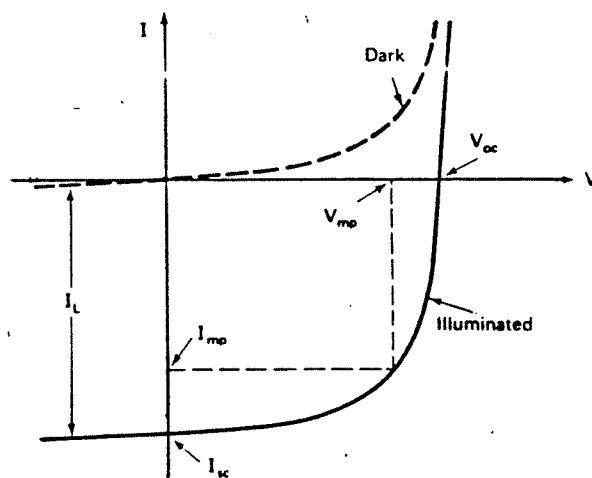


Figure 3: Terminal Properties of an Illuminated Solar Cell [2].

This project investigated the advantages of using a textured surface for optimization of fill factor and efficiency. The design studied was similar to the planar-junction cell of design (b), but with the metal grid covering non-textured plateaus and total area contact made to the back substrate.

EXPERIMENT

Experimental reticles containing 2, 3, 4, 5, 10, and 20 μ m square openings were imaged with KT1820 resist on several <100> wafers covered with 6000 \AA of oxide. The oxide mask was etched in hydrofluoric acid, HF, and the pyramids were etched using a potassium hydroxide solution, KOH, of concentration 5% by weight, held at 40C, to enable process control [5]. Pyramids were allowed to etch completely to points with the time of etch dependent upon pyramid size. In order to determine the optimum opening size and etch time, each sample was examined under a lightfield and darkfield scope at 1000X.

In addition to optimizing the pyramid etch, it was necessary to determine the separation distance between the windows of the mask to allow for undercutting during the etch process. A third experimental reticle containing an array of 10 μ m squares with separation distances of 1 to 15 μ m was imaged on wafers having approximately 2100 and 6000 \AA of oxide. Lightfield and darkfield illumination was used again for spacing determination.

Upon determination of pyramid size and spacing a three level mask system was designed using ICE (Integrated Circuit Editor), a custom CAD tool on the Digital Vax System at RIT. A MANN 3000 pattern generator was used to create a master reticle set on five inch square high resolution photographic plates for use with a GCA 4800 stepper.

The final cell design shown in Figure 4, was 1 square mm. Windows for pyramids were 10 μ m wide separated by 7 μ m. Metal lines were 50 μ m wide, spaced 450 μ m apart, and covered plateau regions between textured areas. Approximate total metal coverage was 19%.

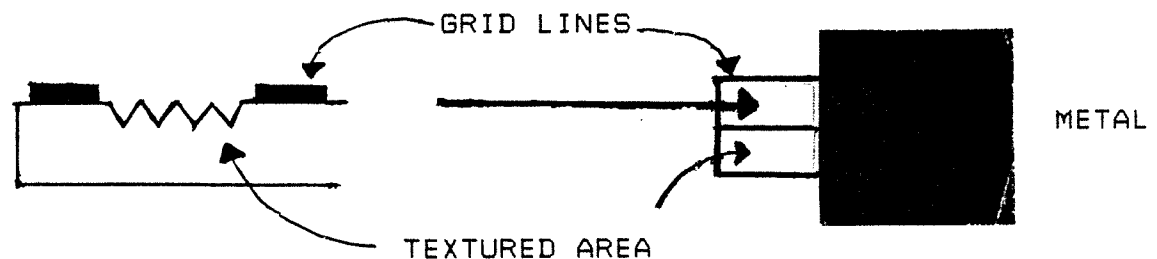


Figure 4: Fabricated Solar Cell Design.

Ten <100> n-type, 5-10 ohm-cm resistivity, device quality wafers were prepared using an RCA cleaning process. An oxide layer of 2400Å was grown to act as masking against the KOH solution. The oxide layer on six of the ten wafers was then patterned with openings for the pyramids. The remaining four wafers were fabricated as non-textured controls. These 10um windows on the frontside were opened with an HF etch while the backside was protected with resist. The pyramids were etched in 5% KOH solution at 40C for an average of 170 minutes. This oxide layer was removed on all wafers and an RCA clean was performed. A new oxide layer of approximately 2300Å thickness was grown to protect the frontside of the wafers from phosphorous diffusion. Diffusion of phosphorous using Emulsitone N-250 spin-on dopant was then performed at 1050C for 10 minutes in dry oxygen and 5 minutes in wet oxygen to form an ohmic contact at the back surface. After diffusion, this masking oxide was removed and an RCA clean was performed. A new masking oxide of approximately 3200Å was grown to protect the backside of the wafers. The p/n junction was formed using Borofilm 100 spin-on dopant for 7 minutes in dry oxygen and 3 minutes in wet oxygen at 1000C for half of the wafers and at 1100C for others to vary junction depth. After diffusion the oxide was removed and an RCA clean was again performed. An antireflective coating of 750Å of oxide was grown on the front side of the wafers. This layer was then patterned with contact cuts. Aluminum was deposited and patterned on the frontside of the wafers and then deposited on the backside. A sinter at 450C took place to complete fabrication.

RESULTS/DISCUSSION

The optimal spacing distance to form upright pyramids, shown in the SEM photo of Figure 5 as the second group of pyramids in the second row, was found to be 7 microns for a masking layer of 2100 Å of oxide. Actual device wafers did not etch to form upright pyramids. Etching time was extended in order to undercut the masking oxide layer, however, the formation of upright pyramids was not achieved. The failure to form upright pyramids may have occurred because of a slight difference in the masking oxide thicknesses of 300 Å, which apparently limited undercutting. After the final diffusion step pyramid bases measured an average of 13.7 microns wide as shown in the SEM photo of Figure 6. The sharp points of the pyramids seen immediately after etch were more rounded following the high temperature diffusion steps. This is most likely due to the consumption of silicon during oxide growth. Etching pyramids after the phosphorous diffusion step would possibly help to eliminate this problem to some degree.

Measurement of I_{sc} and V_{oc} to determine efficiency at an irradiance of 100 mw/cm² was performed on the fabricated cells. Output characteristics prior to die separation showed a large series resistance and leakage current. The fill factors were .25 and the efficiencies were 6% on average. Textured cells did show an increase in short-circuit current over non-textured cells.

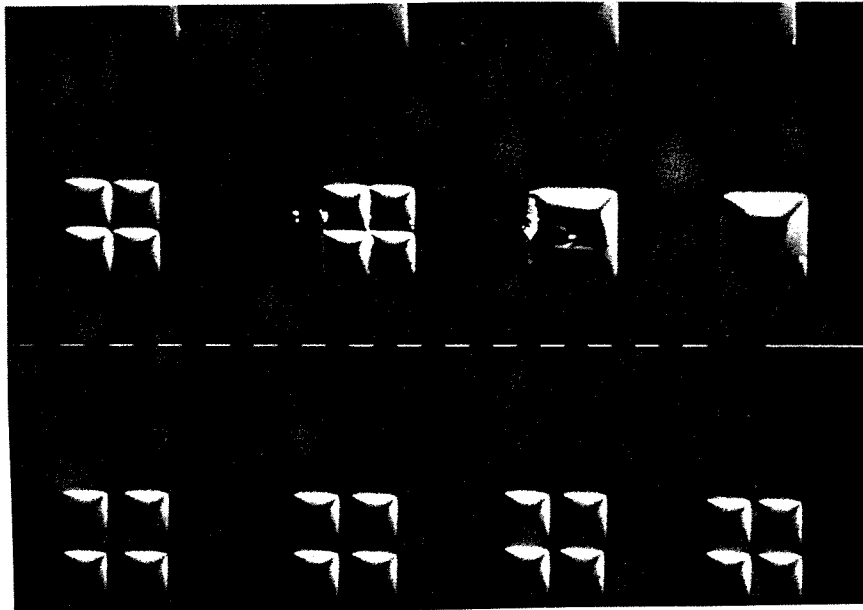


Figure 5: Etched Pyramid Spacing Array.

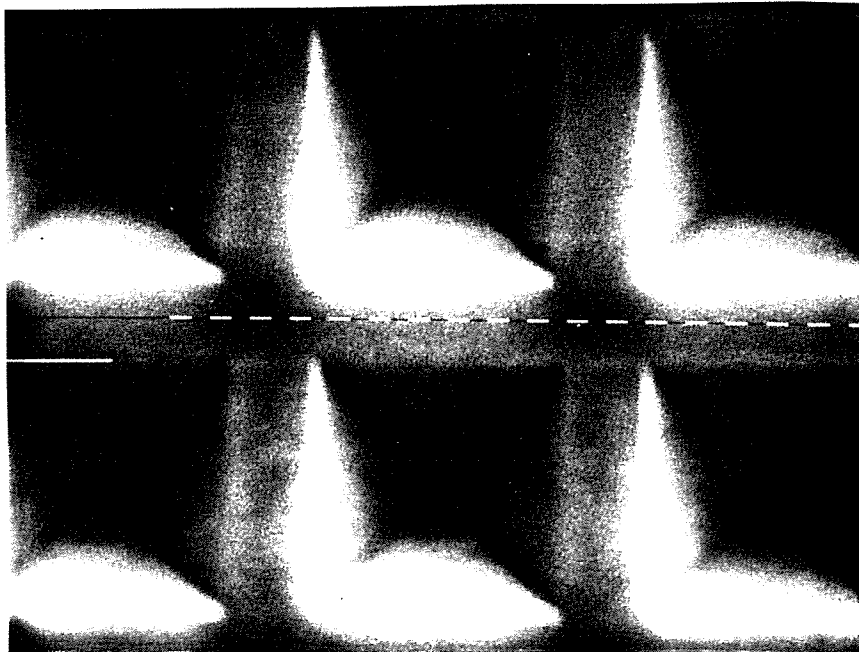


Figure 6: Actual Device Inverted Pyramids.

After die separation the difference in short-circuit current between the textured and non-textured cells was less extreme. Average fill factors and efficiencies of .4 and 9% respectively were observed with improvement attributed to a decrease in leakage current. The short-circuit currents were still larger for the textured cells. Limitations placed on the fill factors

and efficiencies seemed to be due to series resistance created from the p+ diffusion across the entire surface of the cell. This can be shown from the plot of dark and light current for a textured .8um p/n junction cell shown in Figure 7. The characteristic curves downward in the third quadrant instead of remaining fairly level, illustrating series resistance. The deeper, 1.5um junction, lower sheet resistance cells showed higher efficiencies than the shallow, .8um junction, higher sheet resistance cells, again demonstrating the effects of series resistance. A revision of the cell design to create point-junctions would decrease the series resistance created from p+ areas in the textured region and lessen the severity of the problem. The highest fill factor and efficiency of .57 and 12%, respectively, was achieved from the testing of a textured 1.5 micron junction cell. The output characteristics are shown in Figure 8.

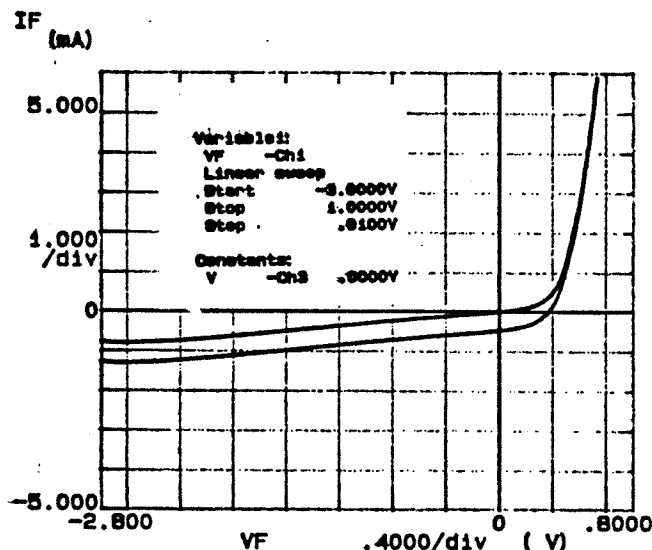


Figure 7: Textured Cell Characteristic Illustrating Series Resistance.

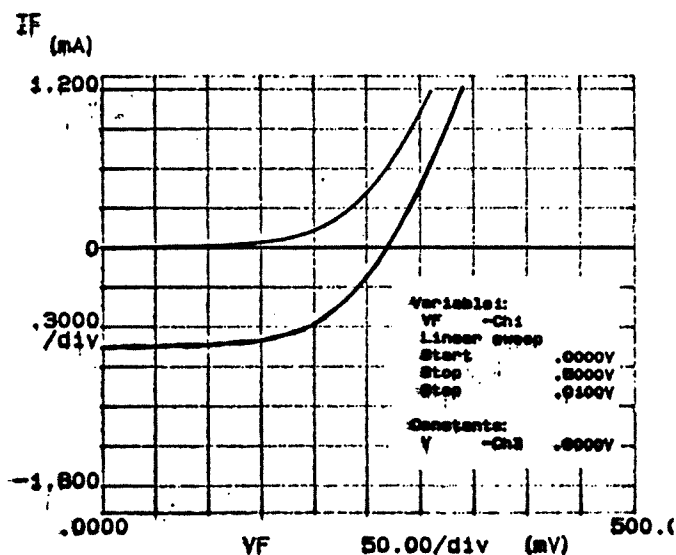


Figure 8: Textured Cell Characteristic with Highest Tested Efficiency.

CONCLUSIONS

Texturing aids in increasing the efficiency of photovoltaic cells. A revision of the design from a planar-junction cell to a point-junction cell would help to eliminate series resistance limitations on fill factor and efficiency, in order to make full use of the advantages of textured surfaces.

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