Evaluation of Polyoxide Capaccitor Edge Effects using ramped I-V Measurements.

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Abstract: Thermally grown oxide on polysilicon has poorer insulator properties than an oxide grown on single crystal silicon. Due to surface roughness of the polysilicon surface the localized oxide electric field is enhanced at the surface bumps and asperities. In order to minimize surface roughness attention has to be given to the polysilicon surface for the steps following deposition. This inludes doping and annealing the polysilicon in order to increase the grain size and using care in cleaning the poly and growing the oxide. By minimizing the surface roughness the polyoxide has better insulating properties due to a decrease in the localized electricc field and this oxide demonstrates a higher barrier height (ϕ_B) and breakdown voltages.

Evaluation of the oxides were done using ramped I-V measurements. The measurements were taken at an area where Fowler-Nordheim tunneling was taking place. That region of the courve was analyzed to find the breakdown voltages and barrier height, ϕ_B. Breakdown voltages were found to be from a low of 37.85v to a high of 43.5v. Barrier heights ranged from 2.1eV to 2.6eV cocmpared to 3.2eV which is the ϕ_B for oxide grown on single crystal silicon. Edge length of the test structures was also evaluated and it was found that the barrier height decreased with increasing edge length indicating an increase in the local electric field along the edge regions.

Theory: Thermally grown oxide on polycrystalline silicon (polysilicon) is a common insulating material that is used in the microelectronics industry. The nature of the surface of the polysilicon determines its electrical characteristics. Due to the enhanced surface roughness caused by the many grains that make up polysilicon the oxide grown on polysilicon is a lesser quality oxide than the oxide that can be grown on single crystal silicon. In previous studies it has been seen that the polyoxide has a lower breakdown voltage as well as greater Fowler-Nordheim leakage. By altering the processing of the polyoxide it is possible to reduce these problems. The grains of polysilion have a certain roughness to the surface that is a variable of grain size. This roughness causes the surface to have a varied electric field which is enhanced in the regions that form bumps of sharp points and this electric field is what causes the oxide to be of poorer quality.

By varying the grain size of the polysilicon it is possible to reduce the enhanced field. As the grain size of the polysilicon is increased the boundaries between the grains are decreased in number thereby reducing the number of regions where the enhanced field would be found. Grain growth an be achieved by annealing the polysilicon film at temperatures above 900-950°C. It has been found that grain growth occcurs to a greater extent if the polysilicon is heavily doped with phosphorous. This increases the grain size drastically. In order to see the drastic improvement it is reccomended that the doping concentration be at or above 7.5E20 cm-2. The grain growth is possible due to the lower activation energies that are seen at the grain boundaries and with the

addition of phosphorous these energies are decreased even further. It has been observed that for temperatures greater than 1000°C the grain size seems to increase as the square root of the annealing time. It can be seen that the grain size of the polysilicon can be increased by heavily doping the poly with phosphorous and then annealing the poly at above 900°C.

Oxide growth that is performed on polysilicon surfaces is a poorer quality oxide than that of oxide grown on single crystal silicon. The rate at which oxide is grown on polysilicon varies due to the many crystal orientations that are found in the polysilicon. Whichever crystal orientation is the dominant orientation will determine the majority of the growth time. As the oxide is grown the grain boundaries cause the dopant to be able to be diffused away from the surface causing the oxide growth rate to decrease as compared to an oxide grown on similary doped single crystal silicon. As the temperature of the oxide growth is decreased below 800°C the growth rate observed at grain boundaries is increased due to the accccumulation of phosphorous at the boundaries. This causes an uneven oxide thickness that is undesirable so low temperature oxide growth over polysilicon is not reccomended.

Current conduction of the oxide grown on the polysilicon (polyoxide) is greater than that of regular silicon dioxide, usually by several orders of magnitude. The polyoxide also has a decreased breakdown voltage as compared to silicon dioxide. The current flow is goverened by the Fowler-Nordheim mechanism:

$$I=A\,K_1\,(\mu E)^2\,\exp(-K_2/\mu E)$$

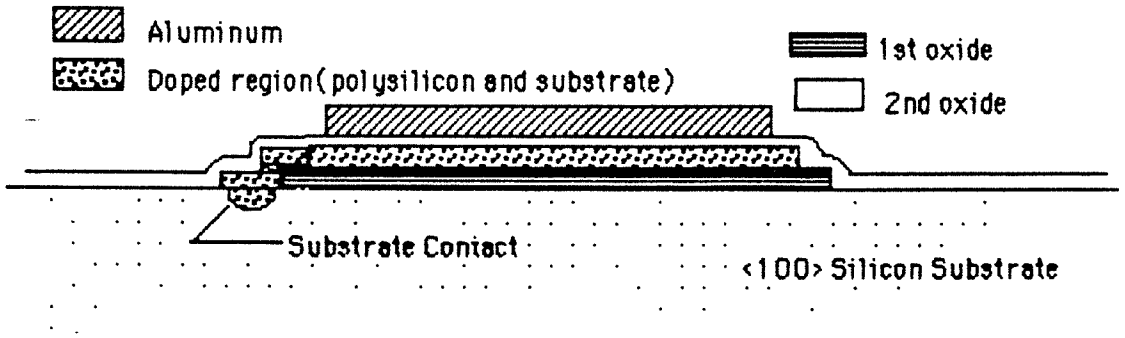
Where I is the current; A the area; K_1 the carrier distribution factor; μ the ratio of the local field to the average field E; E the average field; K_2 the emmision fator related to the energy barrier (ϕ_B=3.2 eV; M*=.4 Mo). As can be seen in this equation the strong dependance on field makes the conduction current very sensitive to small changes in the electric field. Due to the surface roughness the poly surface will have an enhanced local field which is greater than the average field causing the current to be enhanced greatly. Another observance is the dependance on polarity. If the poly plate is made negative the field is increased over the positive polarity bias due to the electron injecton found at the polysilicon roughnesses. Also the higher local electric field is the cause of the lower breakdown voltage found in the oxide. Typical field enhancement over the regular oxide is typically a factor of 3 or 4 which causes an enhancement of the injection current by a factor of around 50. This explains the necessity to try to decrease the surface roughness of the polysilicon.

As can be seen by this discussion it is important that the polysilicon surface is as smooth as possible in order to reduce the localized electric fields and thereby decreasing the injection current. In order to decrease the surface roughness the polysilicon should be heavily doped with phosphorous and then anneales at above 900°C. This should smooth out the polysilicon surface by increasing the grain size. By reduing the grain size the localized field is decreased and thereby dereasing the injection current.

The edges of the capaictor plates also demonstrate inreased electric fields and can contribute to the lowering of the breakdown voltages and ϕ_B.

Experimental:

Device Fabrication: Obtain lightly doped <100> wafers and scribe. RCA clean the wafers. Grow 3000Å of oxide at 1100°C in wet 02. RCA clean again. Etch the oxide using the oxide mask pattern forming pads that the capacitors will be made on. Strip the photoresist in the plasma asher. RCA clean. LPCVD deposit 3000Å of polysilicon. Dope polysilicon using solid source diffusion using the following precautions: Insert wafers at 800°C in a Nitrogen ambient; Ramp up to 1000°C at 5°C/min; 20 minute solid source predeposition at 1000°C; Ramp down to 800°C (or lower) at around -5°C/min in a nitrogen ambient. The wafers are then deglazed in HF acid. Anneal the wafers in nitrogen at 900°C for 45min. The deposition and anneal were done in order to increase the grain size of the polysilicon. Pattern the polysilicon with the poly mask. Etch the polysilion in polysilicon etch, checking the etch rate before etching. The photoresist was removed from the wafers by using miroposit photoresit stripper. Using petri dishes filled with the stripper, place a wafer in one dish of the stripper for 2 minutes and then transfer the wafer to the other dish for an additional two minutes. Ccontinue until all wafers are stripped. If the solution beomes too dirty change the stripper with fresh stripper. After the wafers have gone through the two solutions rinse the wafers in DI water for a time less than 2 minutes so there will not be exessive water in the oxide. Inspect the wafers, if there is remaining photoresist submerge the wafers in the stripper again until the photoresist is removed. The lot is split up at this point. One half the lot is subjeted to a standard RCA clean. The other half of the lot undergoes a pirhanna clean (5:1 Sulfuric Acid:Hydrogen Peroxide) for 15 minutes. After the pirhanna clean the lot undergoes a 10:1 DI:HF dip for 2 minutes. The two lots should be timed so they both are finished around the same time. Spin dry the wafers and immediatly put into the oven for the oxide growth. The oxide growth is done using the following precautions in order to minimize surface roughness: Start oven at 600°C; Push wafers into the oven at 8"/min, under an oxidizing environment(13% dry 02: 87% N2); Ramp up the oven to 1100°C; Grow 1000Å of polyoxide with 100% dry 02(27 min.); Switch the gasses from 02 to N2 and anneal the oxide for15 minutes at 1100°C in N2; Turn power off and let the ovens cool to < 800°C; Remove wafers from oven(8"/min pull). RCA clean the oxide before aluminum is evaporated onto the wafers. Coat the wafers with photoresist and pattern with the metal mask. Etch the metal in Al etch checking the temperature and etch rate before the actual etching. Strip the photoresist in the plasma asher. Sinter the wafers at 450°C in forming gas. The processing should be finished and the following cross section should be observed.



Testing of the finished structures: Testing was done on the test strutures using ramped I-V measurements on a Hewlet Packard 4145B Semiconductor Parameter Analyzer. The curves were tested using a voltage ramp from around 20v up to around 40 to 50 volts where the capacitors broke down. The current was monitored and evaluated at the region where the Fowler-Nordheim leakage current was taking place. Curves of the log of the current vs. the ramped voltage were plotted. From these curves and the Fowler-Nordheim equation it is possible to determine the breakdown voltages of the oxide and the barrier height ϕ_B of the oxide. One contact to the test structures was accomplished via a backside substrate contact and the other contact was made via contacting the aluminum on top. The test structures were designed so that there were complementary structures, one with the aluminum contact being smaller than the polysilicon the complement being the opposite. This was done in order to eliminate biasing due to polarity on the plates. Test structures were also designed such that the area of the capacitor plates is kept the same but the perimiter of the devices is varied to see the effects of edge length on the capacitors.

Results: Test strucctures I, III, and VI have smaller metal plates and test structures II, IV, and V have smaller polysilicon plates. The structures were tested using both a negative and positive bias, the negative bias being where the substrate contact is negativly biased as compared to the positive bias. Curves were generated and from these curves the breakdown voltage and the ϕ_B were calculated. Wafers were also evaluated to see if there was an effect of using the two different kinds of cleans on the polysilicon. The results are as follows:

RCA Clean:

	Barrier Height ϕ_B (eV)		Breakdown Voltage (v)	
	-Bias	+Bias	Mean	Std. Dev.
I	2.10	2.33	37.9	2.34
II	2.33	2.18	39.2	3.56
III	2.18	2.17	38.1	2.00
IV	2.10	2.15	36.2	3.03
V	2.11	2.14	36.9	2.07
VI	2.11	2.19	40.1	2.29

Pirhanna Clean:

	Barrier Height ϕ_B (eV)		Breakdown Voltage (v)	
	-Bias	+Bias	Mean	Std. Dev.
I	2.61	2.41	43.5	2.74
II	2.41	2.29	43.2	1.50
III	2.61	*	42.4	2.80
IV	2.41	*	43.0	1.47
V	2.45	2.61	42.2	2.35
VI	2.41	*	43.5	2.14

* -capacitors broke down before reasonable curves could be generated.

Effects of edge length on barrier height and breakdown voltage:

Edge Length (μM)	Barrier Height ϕ_B (eV)	Breakdown Voltage (v)
894.4	2.22	38.5
1118.0	2.14	37.1
1900.4	2.11	38.5

As can be seen by the results there is a range of breakdown voltages from 36.1 volts to 43.52 volts. Barrier height was found to have a range of 2.1eV to 2.61eV which is comparible to those found in previous studies with values of around 2.78eV and is cocmpared to the ideal barrier height of 3.2 eV which is the value for oxide grown on single crystal silicon. Breakdown voltages are low as compared to polyoxide breakdown voltages of around 80 volts for memory quality polyoxides. The ideal polysilicon capacitor is the one where the polysilicocn plate is larger than the aluminum plate and the polysilicon plate is biased negativly with respect to the aluminum plate. The results from this type of structure is a barrier height of 2.1eV for the pirhanna clean and a value of 2.60 for the RCA clean. Breakdown voltages of the structures are 38 volts and 43 volts respectfully. The results demonstrate that the RCA clean did not damage the surface as much as the pirhanna clean and is demonstrated by the increased barrier height and breakdown voltage that is found in the RCA clean compared to the pirhanna. The results also show that the edge length of the test structures does effect the readings. The barrier height was found to decrease with increasing edge length, a .11eV decrease in the barrier height when the edge length was about doubled. The breakdown voltage did not seem to vary with edge length and ould be a sole factor of the oxide thikness and the polysilicon surface roughness.

Conclusion: From the results of the measurements it can be seen that it is possible to manufacture polyoxide capacitors using the reommended care that is necessary in order to have a smooth enough surface to get a fair barrier height and breakdown voltage. It can also be seen that the processing of the capacitors is a very touchy process and that the polysilicon surface is very suceptable to subsequent proccesses. The cleaning steps that were compared shows that the RCA clean did not damage the surface of the polysilicon as much as the pirhanna clean did. This is evident in the better results obtained with the RCA clean. Edge effects were studied and were found to have an effect on the barrier height but no noticable effect on the breakdown voltage. This leads to the idea that the barrier height is a function of the edge length as well as the polysilicon surface roughness and quality of the oxide. The breakdown voltage seems to be only a factor of the surface roughness and the polysilicon surface as the change of edge length did not seem to vary breakdown voltage. It can be seen in the study that the production of polysilicon capacitors is very subject to the degree of care taken in the processing, and with fine tuning of the processes it should be possible to produce polysilicon capacitors that have the standards that are needed for the production of memory devices. Minimization of the edge length of the device design also will lead to better results in the final product as the minimal edge length gave the minimal barrier height.

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