ALIGNMENT ERROR CHARACTERIZATION USING ELECTRICAL PROBING TECHNIQUES

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ABSTRACT

A technique for electrically measuring alignment errors is described and employed to characterize a GCA 4800 DSW stepper. The experimental accuracy was determined to be +/- 0.05 microns for all line-width measurements. The GCA 4800 stepper's day-to-day performance was determined to fluctuate between 0 and -1 micron in X and between 0 and +2 microns in Y. Average alignment ranges of +/- 0.74 and +/-0.95 microns in X and Y were observed across four samples during the wafer-to-wafer variation testing within one run. These errors were directly related to the accuracy of the "pass-shift" values used by the stepper's control software.

INTRODUCTION

Reductions in the minimum device geometries used by the semiconductor industry can be directly correlated to the overlay errors that occur during lithography. These errors include translations, rotations, and distortions, which can be traced to mechanical, chemical, and environmental factors [1]. The mechanical errors can be induced by lack of stage precision or improper alignment due to operator error. The chemical errors can be caused by pattern shift during a crystalline layer growth process. The temperature and humidity in the vicinity of the lithographic tool can also cause errors due to the heating of stage and optical components. Of the three, the main source of overlay error is caused by mechanical positioning errors which produce wafer-to-reticle misregistration. According to Rottmann, "the reduction of overlay errors should play a decisive role in future lithographic developments [1]."

Overlay errors may be characterized through the use of electrical probing techniques. The overlay information which can be derived from electrical probe data includes pattern linewidths, X and Y alignment translations, local (within a die) and global (across a wafer) rotations, and magnification errors. This method of analysis can be used to evaluate any lithographic tool, but, some of the parameters and calculations do not apply to contact or scanning tools. Comparisons of electrical and optical inspections using a SEM determined the experimental accuracy of each method to be +/-1% and +/-2.5%, respectively. These results indicate a measurement precision of +/-0.01 microns for repeated measurements of a 1.0 micron wide line [2,3,4].

The electrical test structures used for this project were designed to be similar to those used by the Prometrix company for use with their automated LithoMap LM20 probing station [2]. The test devices were doped polysilicon "resistors" on an insulating silicon dioxide layer. The structures included Van der Pauw test cells, optical verniers and special Full-Kelvin linewidth measurement devices. A

Full-Kelvin device is a four (or more) terminal structure which is typically used to measure sheet resistances. In this case, it consisted of four symmetrically positioned, doped polysilicon resistors defined by two separate lithographic exposures and dry etch steps. The first pattern and etch step produced the base levels of each die consisting of the Van der Pauw and Kelvin structures with nominal linewidths of 20 microns. The second lithography and etch step was used to reduce the linewidth of specific regions on the measurement devices. The Van der Pauw and Kelvin structures shown in Figure 1 were used to determine the experimental sheet resistance. That value was then used to determine the linewidths on the measurement structure. Plots of actual devices have been included in Appendix A.

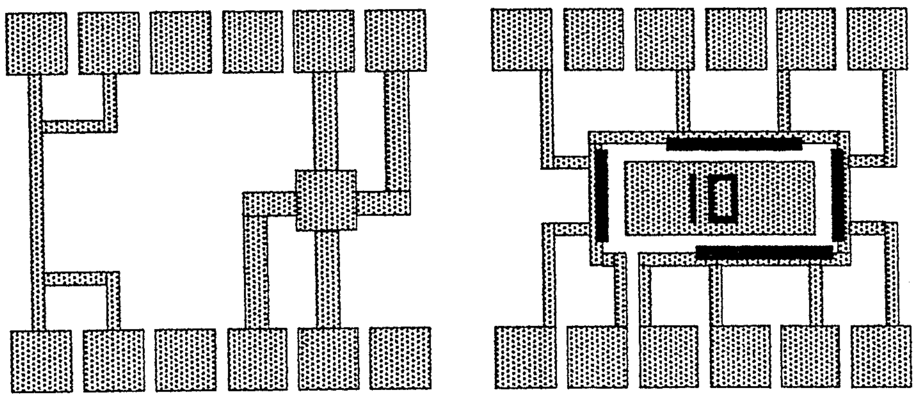

Figure 1: Sample test cells containing a) Van der Pauw and Kelvin sheet resistance structures and b) linewidth measurement device.

A four-point probe determination of the local sheet resistance is made using the Van der Pauw or Kelvin structures. The polysilicon's sheet resistance is computed from the I-V relationship in the following equation:

$$R_S = \pi / (\ln 2)(V / I) \qquad (1)$$

The experimental linewidths are found using the R_S from Equation 1 and measured values of **I** and **V** from a test device in the following equation:

$$W = (R_S)(L)(I / V) \qquad (2)$$

Where **L** is the designed length between the tap-offs (microns) on the measurement devices.

The linewidths on each side of the measurement device are determined by the accuracy of the second alignment. If a translation in the negative x direction occurred during the alignment, the line on the right side will be wider than the line on the left side. The amount of translation is calculated by taking the average of the difference between corresponding linewidths [2, 4]. The same theory applies to the measurement of the lines on the top and bottom of the test device. The diagrams in Figure 2 illustrate how the linewidth measurement techniques are used to determine the experimental translations and where those translations were measured to characterize a wafer.

Table 1 lists the equations which are necessary to completely characterize the alignment errors of a common stepper using the models described by Brunner and Petrillo [2]. The term "local" refers to measurements made within one die and **Dx** and **Dy** refer to the distances indicated in Figure 2. The subscripts **L, R, T** and **B** refer to the wafer locations as shown in Figure 2.

This electrical probe technique has some desirable, inherent advantages over optical evaluations. Some of these reasons are: highly accurate (.01 microns), self-calibrating (localized sheet resistances), non-tool-specific, easy to automate on most equipment and data can be stored in databases for analysis over long periods of time. Some obvious disadvantages are that it is difficult to integrate into most processes and that the processing extends the time to get results.

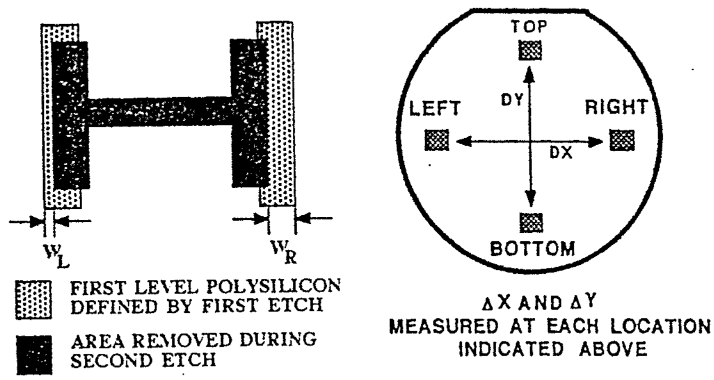

Figure 2: a) Example of measurement principles and b) wafer locations where measurements were taken.

X Error (local)	$\Delta X = (WL - WR)/2$	(3)
Y Error (local)	$\Delta Y = (WB - WT)/2$	(4)
X Translation	$\Sigma \Delta X / n$	(5)
Y Translation	$\Sigma \Delta Y / n$	(6)
X Rotation	$\theta x = (\Delta XT - \Delta XB)/Dx$	(7)
Y Rotation	$\theta y = (\Delta YR - \Delta YL)/Dy$	(8)
X Magnification	$Mx = (\Delta XR - \Delta XL)/Dx$	(9)
Y Magnification	$My = (\Delta YT - \Delta YB)/Dy$	(10)
Rotation (Total)	$\theta Total = (\theta x + \theta y)/2$	(11)
Skew Angle	$\theta Skew = (\theta x - \theta y)/2$	(12)
Magnification (Total)	$MTotal = (Mx + My)/2$	(13)

Table 1: Linear equations for alignment error characterization.

This project applied these electronic measurement methods to a GCA 4800 DSW stepper. A determination of the accuracy and repeatability of the measurement technique was performed. The day-to-day performance was evaluated for two runs of three wafers each. Wafer-to-wafer variation of alignment errors within a run were also investigated.

EXPERIMENT

Twelve 3 inch silicon wafers were scribed with a reference number (1 through 12) and cleaned in 10:1 diluted HF acid. All wafers had approximately 5000 Angstroms of silicon dioxide grown on them in a wet oxygen ambient at 1100 degrees Celsius. Approximately 5000 Angstroms of LPCVD polysilicon was then deposited on all of the wafers. The polysilicon layer was doped using an n-type

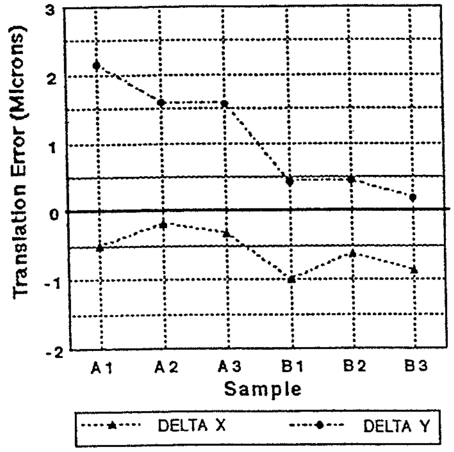

Figure 3: Summary of X and Y translations.

The results from the wafer-to-wafer variation of overlay errors across four wafers at 10 locations on each sample have been summarized in Table 2. (All values below are in microns.) The samples which were evaluated exhibited a range of 1.48 to 1.91 microns in X and Y, respectively, across any sample. This range is considerably higher than expected for a stepper with a stage precision of 0.02 microns. The age and condition of the equipment may be the underlying factors which caused these gross alignment errors.

	Sample 1	Sample 2	Sample 3	Sample 4	Average
Average ΔX	0.60	0.95	0.71	0.73	0.75
Std. Dev. ΔX	0.88	0.46	0.50	0.45	0.57
Range ΔX	2.02	1.43	1.27	1.20	1.48
Average ΔY	1.18	0.65	0.77	-2.33	0.07
Std. Dev. ΔY	0.85	0.64	0.55	0.55	0.65
Range ΔY	2.44	1.86	1.52	1.81	1.91

Table 2: Summary of wafer-to-wafer uniformity testing.

The data was also compiled into histograms for X and Y errors in Figure 4 in order to provide a pictorial view of how the data points were distributed across the four sample wafers. The histogram of X translations shows that most of the overlay errors were concentrated between +0.5 and +2.5 microns with the center of the data occurring around +1.5 microns. Since only a few measurements "stray" from the remainder of the data, the repeatability in the X direction can be considered quite good. On the other hand, the histogram of Y errors shows a different situation. The alignment translations in Y show a bi-humped "random" distribution of data centered about zero. This would suggest that the repeatability in Y cannot be controlled as accurately as the X direction.

"Pass-shifts" are correction factors which are entered into the stepper's control software and are used to compensate for reticle construction and alignment errors. The day-to-day repeatability of the GCA 4800 was determined to be a function of the pass-shift accuracy. The job file on the stepper must be updated for each run by exposing "send-ahead" wafers (or die) and evaluating the accuracy of the pass-shift on a vernier stage microscope. The wafer-to-wafer data which was collected suggests

Allied Signal spin-on (phosphorus) diffusion source.

All wafers were patterned using KTI-820 positive photoresist which was exposed using a dose of 60 millijoules per square centimeter on a GCA 4800 DSW stepper. All wafers were then developed and post-baked. A SF_6 (10.3 sccm) and O_2 (3.3 sccm) dry plasma etch (130 Watts, 1 minute at .650 Torr) was used to pattern the polysilicon. An oxygen plasma ash was used to remove all of the photoresist. The same processing techniques and equipment were used to define the second level on all of the wafers. A final DHF dip was used to clean all samples before going on to the testing area. A summary of actual processing steps has been provided in Appendix B.

The required current and voltage measurements were made using a 12-pad probe card, 2 digital voltmeters and a power supply (used to provide current). The probe card made contact to all of the pads at the same time, and the signals going to the meters were switched using a homemade switch box rather than physically exchanging wires. All pertinent data was recorded and the data was later input into a spreadsheet in order to perform computations and statistics.

RESULTS / DISCUSSION

The twelve wafers were broken into three groups before testing began. The measurement accuracy was determined using a randomly selected cell on wafer 2. Wafers 1, 6, and 12 were used for Group A of the day-to-day testing and wafers 10, 11, and 5 comprised Group B for the same test. Wafers 3, 7, 8, and 9 were probed to determine the wafer-to-wafer variation. The optical verniers were designed to provide readings between +/-2.5 microns, however, the final pattern was distorted by the lithography and etching steps and no confident observations could be made from them.

Twelve measurements on the same Kelvin structure were made to determine the accuracy and repeatability of the electrical probing technique. The data produced an average linewidth of 10.69 microns, with a standard deviation of 0.05 microns. A +/-0.05 micron tolerance was established for all electrical measurements by employing a Studentized t-distribution (t-test) to construct a 99% confidence interval for the linewidths measured. This level of accuracy is lower than reported values, however, it is more accurate than standard optical verniers.

The average sheet resistance of the unpatterned, doped polysilicon was determined to 19.5 Ohms per square. The average sheet resistance measured on a patterned wafer was calculated to be 23.08 Ohms per square. The most probable cause for this difference is the presence of native oxides or probe damage to the polysilicon pads which altered the V/I ratios slightly.

The day-to-day repeatability of the GCA 4800 DSW stepper system was evaluated. The average X and Y translations for Group A were determined to be -0.33 and +1.77 microns, respectively. The data from Group B yielded averages of -0.83 and +0.36 microns for X and Y. The graph in Figure 3 shows the relative errors from the six wafers.

that a pass-shift of -1.5 microns could have been entered for X in order to center most of the data around the origin. However, a pass-shift would not help to correct the Y errors due to their symmetric nature.

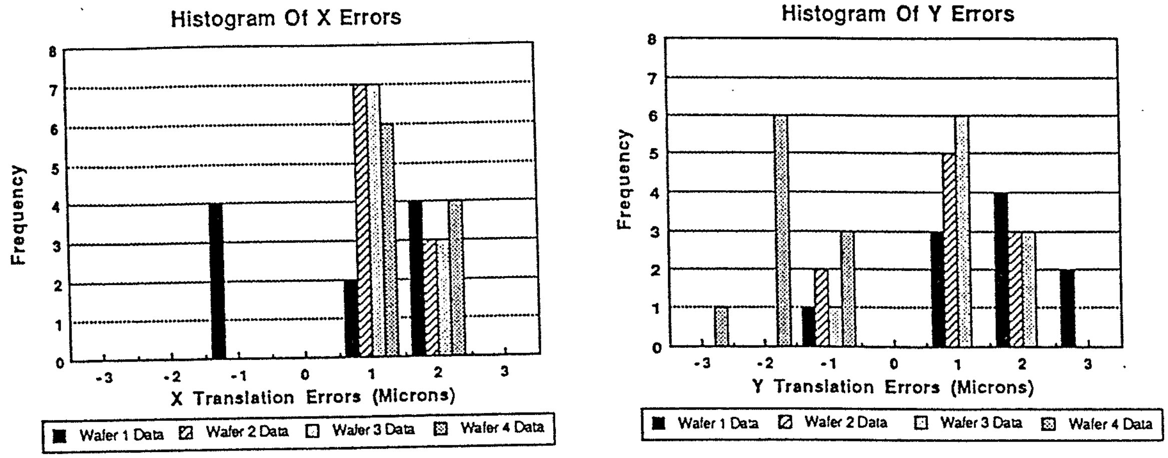

Figure 4: Histogram of X (left) and Y (right) errors.

CONCLUSIONS

The experimental accuracy of the linewidth measurements was determined to be +/-0.05 microns. The GCA 4800 stepper's day-to-day performance ranged from -1 to 0 microns in X and from 0 to +2.3 microns in Y. These errors were determined to be function of the pass shift accuracy. The GCA stepper's alignment varies by as much as 1.91 microns across any wafer and the translations can be reduced by adjusting the pass-shift values in the job file. The data from part 3 suggested that the X errors could be corrected, but the Y errors were symmetric about zero and could not be helped by altering a pass-shift value. All of the observed errors were well below the allowable 10 micron tolerance used for NMOS and PMOS design rules at RIT. In summary, the electrical probe techniques utilized for this experiment have provided an accurate account of the GCA 4800 stepper's performance.

ACKNOWLEDGMENTS

I would like to thank the following individuals for their much appreciated contributions to this project: Mike Jackson, Dr. Richard Lane, Dr. Tim Brunner (IBM), Scott Blondell and Matt Matessa.

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