FULLY RECESSED OXIDE ISOLATION TECHNOLOGY FOR NMOS FABRICATION

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ABSTRACT

Fully Recessed Oxide Isolation Technology (FROIT) and LOCOS methods were both fabricated to verify if the FROIT process provides solutions to two major problems associated with LOCOS, namely the bird's beak formation and surface topography. The FROIT process uses a two step field oxidation and employs a nitride sidewall to recess the oxide and reduce the bird's beak, respectively. The SEM results verified the FROIT process achieved the desired results.

INTRODUCTION

Local oxidation of silicon (LOCOS) has been the primary technique for growing field oxide isolation between active MOSFET's. Conventional LOCOS isolation techniques for fabrication of MOSFETS have two major problems that put constraints on device fabrication and performance. The first problem is the bird's beak and the second is surface topography.

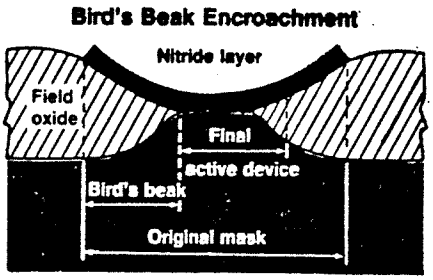


Figure 1: View showing bird's beak on a 1.5 micron active area width [1].

Figure 1 illustrates that during field oxidation, not only does the oxide grows where there is no masking nitride, but some oxidant diffuses laterally at the nitride edges. The oxidant that penetrates the edge of the Silicon Nitride/pad oxide/silicon stack allows oxide to grow under that edge which creates a lateral extension of the field oxide into the active area. Due to its shape it has been termed a bird's beak.

The length of the bird's beak depends on several parameters which include field oxide thickness, oxidation temperature and pressure, pad oxide thickness, and nitride thickness. The thicker the pad oxide, the less edge force provided by the nitride and the more the oxidant can penetrate laterally. The bird's beak could be minimized with increasing nitride thickness, however the major concern becomesis the high tensile stress associated with thicker nitride films. Thick nitride films can generate dislocations in the silicon, which degrade device performance. The pad oxide provides a way to reduce this stress due to its viscous flow. However, pad oxide to nitride thickness ratio to obtain no defects in the silicon is limited to 1:6.

The length of the bird's beak for a typical 0.5 micron oxide thickness is about 0.5 microns per side. From Figure 1 it can be seen that for a 1.5 micron active area, the bird's beak consumes up to two thirds of the original active area as defined by the mask. The result of the creation of the bird's beak is that the packing density of devices and lateral diffusion of the field adjust implant limit device performance.

A limiting factor in processing submicron geometry Integrated Circuits is the small depth of focus of the optical steppers. To get the maximum resolution from these steppers everything in the field of view will have to be kept within the depth of focus. This means the imaging surface needs to be as flat as possible. This leads into the second major problem which concerns the surface topography of LOCOS has. This lack of planarity will cause film coverage problems and limit lithography resolution in later processing steps. This effect can be seen in Figure 2 where the photoresist is thinned over a step, and upon exposure, will be over exposed. Development of the photoresist line will cause narrowing over the step, which is referred to as necking.

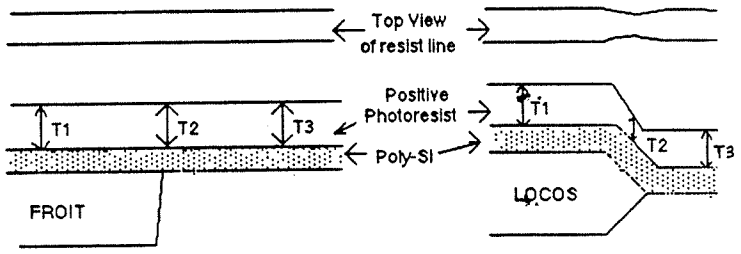


Figure 2: Top view and cross sectional view of a photoresist line over a) FROIT T2 < T1 < T3 and b) LOCOS T2 < T1 < T3.

The Fully Recessed Oxide Isolation Technology (FROIT) [1,2] can solve the two major problems associated with LOCOS. A conventional semirecessed field oxide (LOCOS) is first grown as shown in Figure 3 a-b. This field oxide is then removed with

buffered HF to provide a moat of well controlled depth and sidewall angle as seen in Figure 3c. The silicon surface is now free of any dry etching damage and also has a short nitride overhang. Next, a second thin pad oxide is grown followed by a second CVD nitride that conformally covers all surfaces. A self aligned boron channel stop implant is done (Figure 3d) and the second nitride layer is anisotropically etched so that a sidewall still remains for oxidation masking (Figure 3e). A second field oxide is grown and the result is a defect free, near zero bird's beak, fully recessed oxide with good planarity. Note that the conventional LOCOS processing is just step 3a, followed by the boron implant, followed by step 3b.

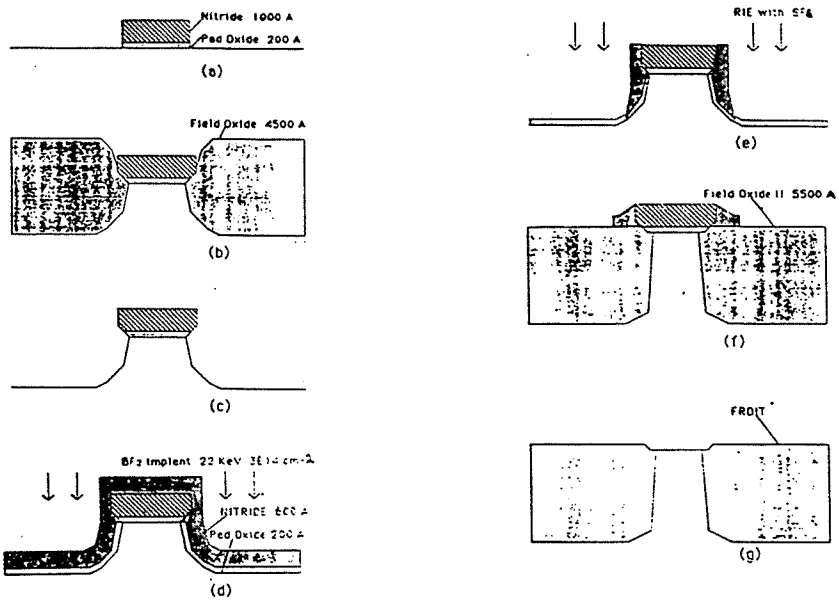
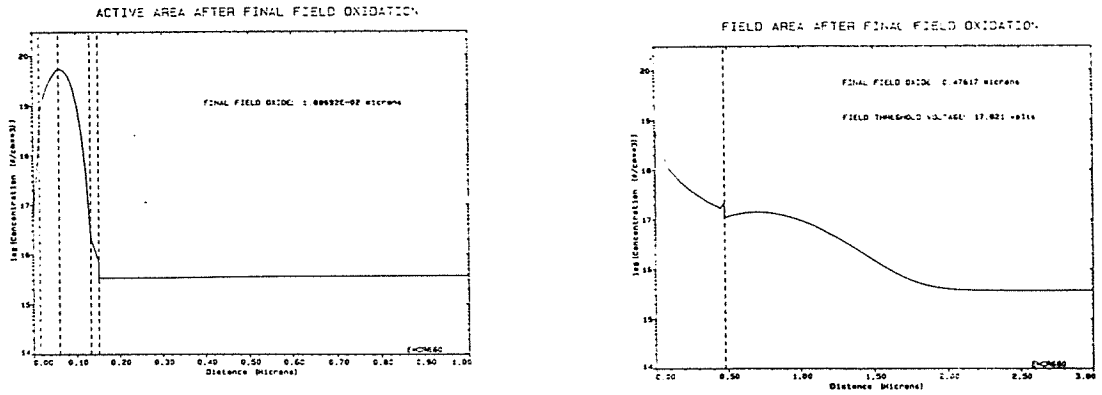


Figure 3: Major processing steps of the FROIT process.

One key parameter to MOS circuit performance is the BF2 implant. Technology modelling Associates version of SUPREM-3 was used to model the implant in the active device area and the field oxide area. The difficult problem here was to optimize the implant dose, energy, and the second nitride thickness so the field area would have a sufficient threshold voltage (greater than 10 volts for RIT designed NMOS circuits) and the active area would be completely masked by the implant and drive in during field oxide growth. The implant parameters determined that met the device processing requirements were a boron dose of 3E14, energy of 22 KeV, and second nitride thickness of 600 Angstroms. The concentration profile for the active area after implant and field oxide growth is shown in Figures 4a. The resultant field oxide thickness was simulated to be 4700 Angstroms and threshold voltage (with aluminum gate) was 17.8 volts. Figure 4b shows the concentration profile of the field area after oxide growth.



(a) (b)

Figure 4: SUPREM III simulations.

This project compared the FROIT process to the LOCOS process to verify if the FROIT solves the problems with LOCOS. Also, an attempt was made to achieve an acceptable field threshold voltage for the FROIT process without implant punchthrough in the device area.

EXPERIMENT

A design layout was done with RIT's Integrated Circuit Editor (ICE), an in house design tool. The design consisted of 3400 micron long lines that represent the active and isolation regions of a device. This design allows for ease of cleaving samples for SEM cross section analysis. The design consisted of 4,7,10 micron wide lines on the mask to define active areas. Field regions of 2,4,6,8, and 10 microns for each active area dimension. The reticle was made on five inch, high resolution emulsion plates, using the MANN 3000 pattern generator.

Thirteen p-type, <100>, 2-7 ohm-cm Silicon wafers were scribed and RCA cleaned. A 200 Angstroms pad oxide was grown in dry oxygen at 950C. At this point the wafers were split to see the effects of two different first nitride thicknesses on the bird's beak. Wafers 1,2,6,7,8 and 9 had 800A of LPCVD nitride deposited, while wafers 3,4,5,10,11,12 and 13 had 1000A deposited. Wafers 6-13 were coated with KTI 820 photoresist and imaged using a GCA 4800 stepper. The wafers were developed in ZX-934 developer and water 1:1. The nitride was patterned by an SF6 RIE plasma etch. The pad oxide was etched using buffered HF and the resist was ashed in O2 plasma. All thirteen wafers were RCA cleaned and a 4200A field oxide was grown in wet oxygen at 1050C for 55 minutes. Wafers 6 and 10 were oxidized for an additional 15 minutes to obtain a oxide thickness of 4800A. These two wafers were then pulled from the process to represent the LOCOS results.

The field oxide was etched in buffered HF to provide a short nitride overhang. A second 200A pad oxide layer was grown, and a second LPCVD nitride layer of 600 Angstroms deposited. After the self aligned BF2 field implant with energy of 22 KeV and dose of 3E14/cm2 on the remaining wafers, except for wafers 2 and 4, the second LPCVD nitride was etched anisotropically. Then the second pad oxide was etched in buffered HF on all remaining wafers except 1,2,3 and 4. Wafers 7 and 11 were removed from processing at this point for SEM cross section analysis. After a RCA clean on all remaining wafers (1-5,8,9,12,13), the second field oxide was grown in wet oxygen at 1100C for 56 minutes to achieve a field oxide thickness of 5500A. The nitride was stripped in 160C phosphoric acid and then the pad oxide was removed in buffered HF for wafers 6, 10,8 and 12. Wafer 5 was split in half, then processed through the additional hot process steps required for NMOS fabrication. The additional processing included 160 minutes at 900C and 100 minutes at 950C. Aluminum was evaporated on wafers 1-5, including both halves of wafer 5. Capacitance voltage measurements were made on wafers 1-5. SEM cross section analysis was done on wafers 6,10,8 and 12 comparing standard LOCOS vs. FROIT.

RESULTS/DISCUSSION

The SEM results of the FROIT vs. LOCOS processes with 1000A nitride over device area during oxidation can be seen in Figures 5 and 6. Figure 5a shows a SEM of FROIT vs. LOCOS for a 2 micron field region mask. The sample was prepared by coating wafers with photoresist, cleaving the wafer and etching SiO2 away in buffered HF. Nominal SEM magnification was 40K X. Knowing oxide thickness from Nanospec measurement, an attempt was made to quantify the extent of the bird's beak. The field oxide thickness was 4800A and the bird's beak was measured to be 0.22 micron/side. Figure 5b is the LOCOS process with 4500A field oxide thickness and 0.27 micron/side bird's beak. Figure 6a is the FROIT process with a 4 micron designed isolation width, 4800 A field oxide thickness and 0.25 micron/side bird's beak. Figure 6b is the LOCOS process with a micron designed isolation width, 4500 A field oxide thickness and 0.32 micron/side bird's beak. Thus the FROIT process was superior to the LOCOS process with respect to reduction of bird's beak. From the SEM results in Figure 5 and 6 it can be seen that the isolation oxide in the FROIT process was fully recessed with respect to the silicon surface. The LOCOS process resulted in the typical semirecessed oxide isolation. The FROIT process also was proved to provide a reduced bird's beak.

The field threshold voltage for the FROIT process was measured to be 15.7 volts. This result differed by 11.8% less than the SUPREM simulated result. The wafer that had the additional processing to simulate the complete NMOS fabrication process had a field threshold voltage of 13.2 volts. These results show that the implant dose and energy chosen were sufficent to provide a threshold voltage greater than 10 volts

for this process. The result of CV measurements on before and after field implant wafers showed a thresold voltage of -0.6 and -0.8 volts. These numbers are basically the same so it is safe to say the implant did not penetrate the thick nitride mask. If it had the threshold voltage would have shifted. Thus, it was verified that the implant did not penetrate through to active device area.

Due to time constraints and the difficulty to prepare the SEM samples the wafers with 800A nitride over the device area during oxidation were not inspected.

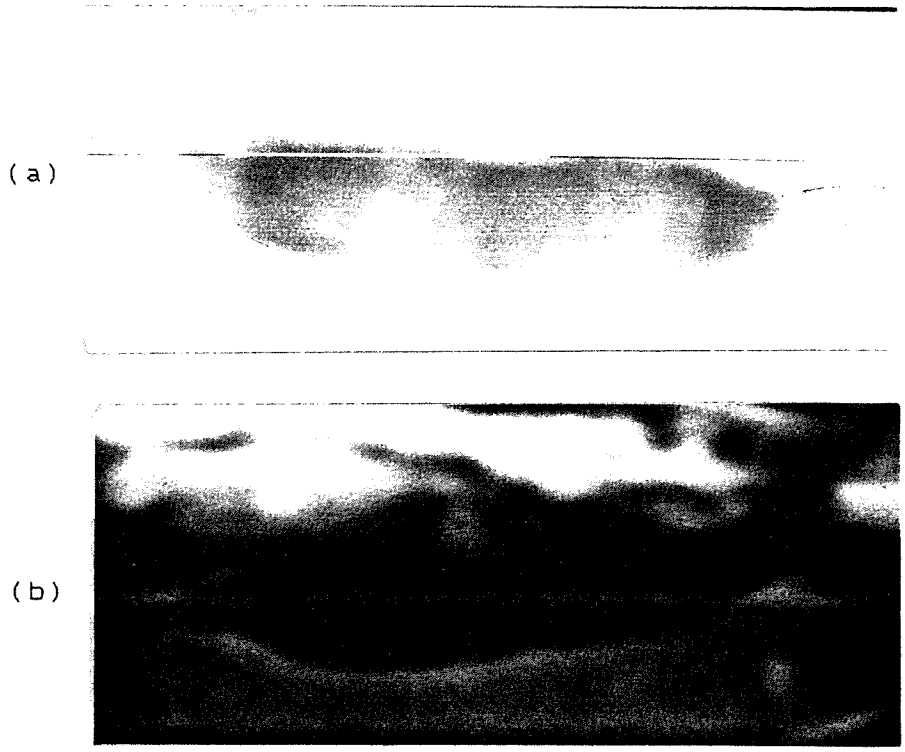


Figure 5: a)FROIT and b)LOCOS with 2 micron designed isolation.

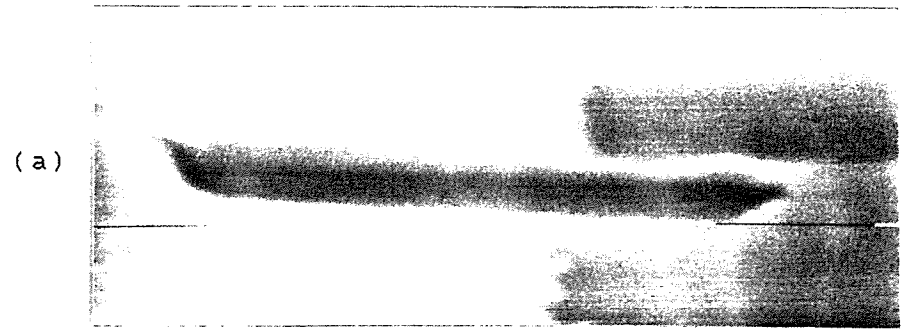


Figure 6: a)FROIT with 4 micron designed isolation.

(b)

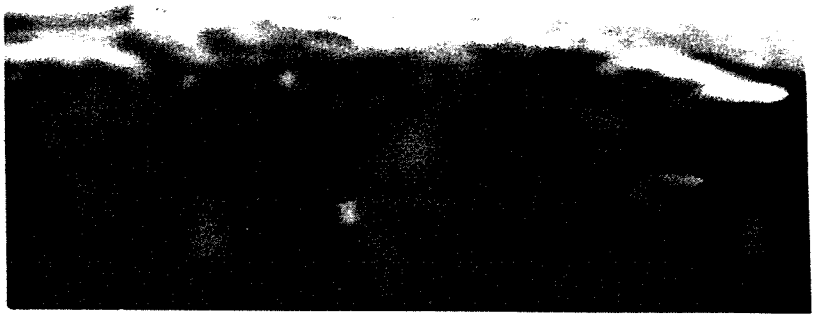


Figure 6: b)LOCOS with 4 micron designed isolation.

CONCLUSION

The FROIT and LOCOS methods for oxide isolation were processed and compared. It was seen the FROIT process provided solutions to the LOCOS process problems with respect to eliminating surface topography. The FROIT process also reduced the bird's beak by an average of 23%. An acceptable field oxide threshold voltage was achieved, 13.2 volts after complete device processing, with the aid of using SUPREM III to make determination of the processing parameters. As intended the BF2 field adjust implant did not penetrate through the active device area. This was true since the CV measurements showed no change in before and after implant threshold voltages.

ACKNOWLEDGMENTS

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