

EVALUATION OF A DOUBLE RESIST PROCESS

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ABSTRACT

A hierarchical analysis of variance was executed on both critical dimension and film thickness data to prove manufacturability of a double layer resist process as compared to an existing device process. Testing was designed to provide estimates of variance on a die-to-die, wafer-to-wafer, and run-to-run basis. Ion implant mask sidewall angle and process repeatability were other concerns investigated. The double resist process displayed improvement in all phases of the process examined except the run-to-run variance of the polysilicon film thickness. More testing is required to determine if the possible cause was related to the process or some outside factor.

INTRODUCTION

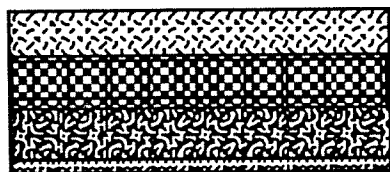
A device process, currently employed in manufacture, includes a double-layer dielectric film. The top layer, dielectric 2, serves as an ion implant mask. However, the deposition of this material is characterized by film thickness non-uniformity, high particle counts, and includes a lengthy furnace operation. Another problem incurred is the poor etch selectivity of the dielectric 2/ dielectric 1 etch to the polysilicon. Because of the dielectric 2 thickness non-uniformity, some over-etching must occur to insure complete cleanout of the dielectric material, resulting in the attack of the poly layer.

In order to minimize these problems, a double layer resist process is proposed. Figure 1 outlines the existing and new processes. The double resist process eliminates the dielectric 2 layer and replaces it with a deep UV (DUV) stabilized, patterned photoresist layer. This new layer would have a dual function: first as an etch mask for the dielectric 1 layer, and second, as part of a medium energy ion implant mask, the same duty as the dielectric 2 level. Another advantage of the double resist process would then be a time savings realized by the reduction in process steps.

EXISTING PROCESS

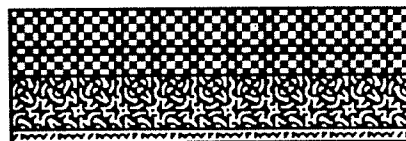
NEW PROCESS

1. Grow oxide and deposit polysilicon dielectric 1 and dielectric 2



DIELECTRIC 2
DIELECTRIC 1
POLY
OXIDE

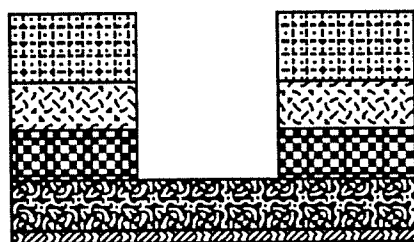
No dielectric 2



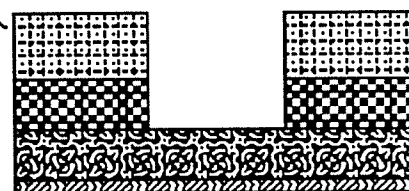
2. Pattern resist for use as dielectric etch mask

3. Etch dielectric 2 and dielectric 1 - 1 step

DUV stabilize resist before etch



— RESIST
— DIELECTRIC 2
DIELECTRIC 1
POLY
OXIDE



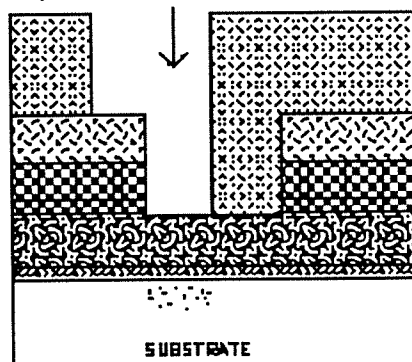
4. Strip resist

No strip

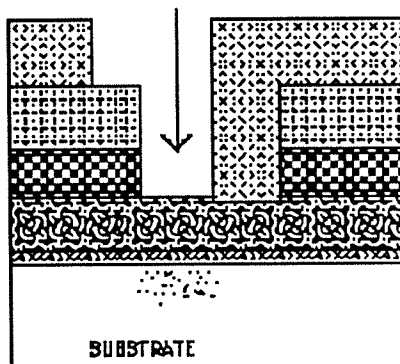
5. Coat and pattern another resist layer for use as an implant mask

Coat second resist layer directly over first layer

6. Implant through poly and oxide



— RESIST 2
RESIST 1
— DIELECTRIC 2
DIELECTRIC 1
POLY
OXIDE



7. Strip resist

Strip both resist layers

8. Remove (etch) dielectric 2

Processes are the same after this step

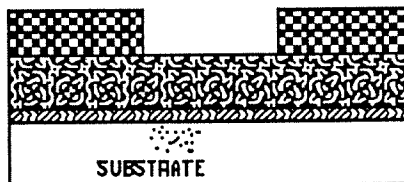


Figure 1: Comparison of process steps.

The crosslinking effects of DUV radiation on novolac-based positive resist was first reported in the early 1980's [1,2,3]. Subsequent work provided results which suggested a bilayer resist process, utilizing the DUV stabilized resist as the underlying layer, was possible [4,5,6,7]. This project will attempt to prove the manufacturability of the double resist process as compared to the existing process. Areas of the processes to be examined are critical dimensions (CDs) before and after the dielectric etch, and the underlying polysilicon film thickness after the dielectric etch. Other areas of concern include the DUV stabilized resist sidewall angle and the repeatability of the double resist process. The role of the stabilized resist as an implant mask is critical, therefore, the sidewall angle can be no less than that of the replaced dielectric 2 layer.

Zone monitoring will be employed to examine the repeatability of both processes. This technique allows the monitoring of only that portion, or zone, of a process which is of interest. The complete device process includes close to 300 steps, but only approximately 50 of those were needed for this study.

EXPERIMENT

A total of 36 four-inch <100> n-type silicon wafers were needed, 18 wafers for each process. The first twenty steps of the processes were identical (up to the dielectric 1 deposition), and all the wafers were processed together to this point. After the polysilicon doping, but prior to the dielectric 1 deposition, the poly film thickness was measured on ten of the wafers in five locations across each wafer. Eighteen wafers comprising the existing process received the dielectric 2 deposition. At this point, the wafers for each process were released in groups of three per run over a three week period. Two of the wafers were used for CD and film thickness measurements, while the other was removed at the implant mask step for sidewall angle measurements on a SEM.

The wafers included in the existing process were patterned with the dielectric etch mask. A double dry etch was performed to delineate the dielectric materials. The resist was stripped, and another resist layer applied for use as the implant mask. Recall that the patterned dielectric 2 material was also part of the implant mask. The resist was stripped and the dielectric 2 layer etched away, having served their purposes.

The wafers which constituted the new process were patterned with the dielectric 1 etch mask but did not receive a conventional postbake. The patterned resist was irradiated using a Microlite 126PC DUV unit manufactured by Fusion Semiconductor Systems. The stabilization process included a temperature ramp to 200°C which insured proper hardening. Following the dielectric 1 etch, a

second resist layer was applied directly over the stabilized material and patterned. Both resist layers were utilized as part of the ion implant mask. The resist layers were stripped simultaneously, and both processes were now at the same point in the overall manufacturing process.

Critical dimensions were measured for the dielectric etch mask resist pattern and the etched dielectric pattern. Measurements were taken with a Philips 545 scanning electron microscope.

Using a Leitz MPV SP automatic film thickness measurement instrument, the polysilicon film thickness was recorded after the dielectric etch in the same approximate wafer location as the initial measurements.

A hierarchical analysis of variance (ANOVA) was performed on both the CD and film thickness data. A hierarchical, or nested experimental design allows estimates of component variances to be made [8]. The testing was designed so that variations could be investigated on a die-to-die, wafer-to-wafer, and run-to-run basis and included the following data points: five die across each wafer, two wafers per run, and six runs for each process. Deducing these component variances aided in determining which portion of the total variance was a result of the process, or was caused by some other factor. Acceptable results for the double resist process would include CD and polysilicon film thickness variances at least matching the existing process. Any CD difference (etch mask vs etched pattern) between processes can be resolved with a change in the mask bias.

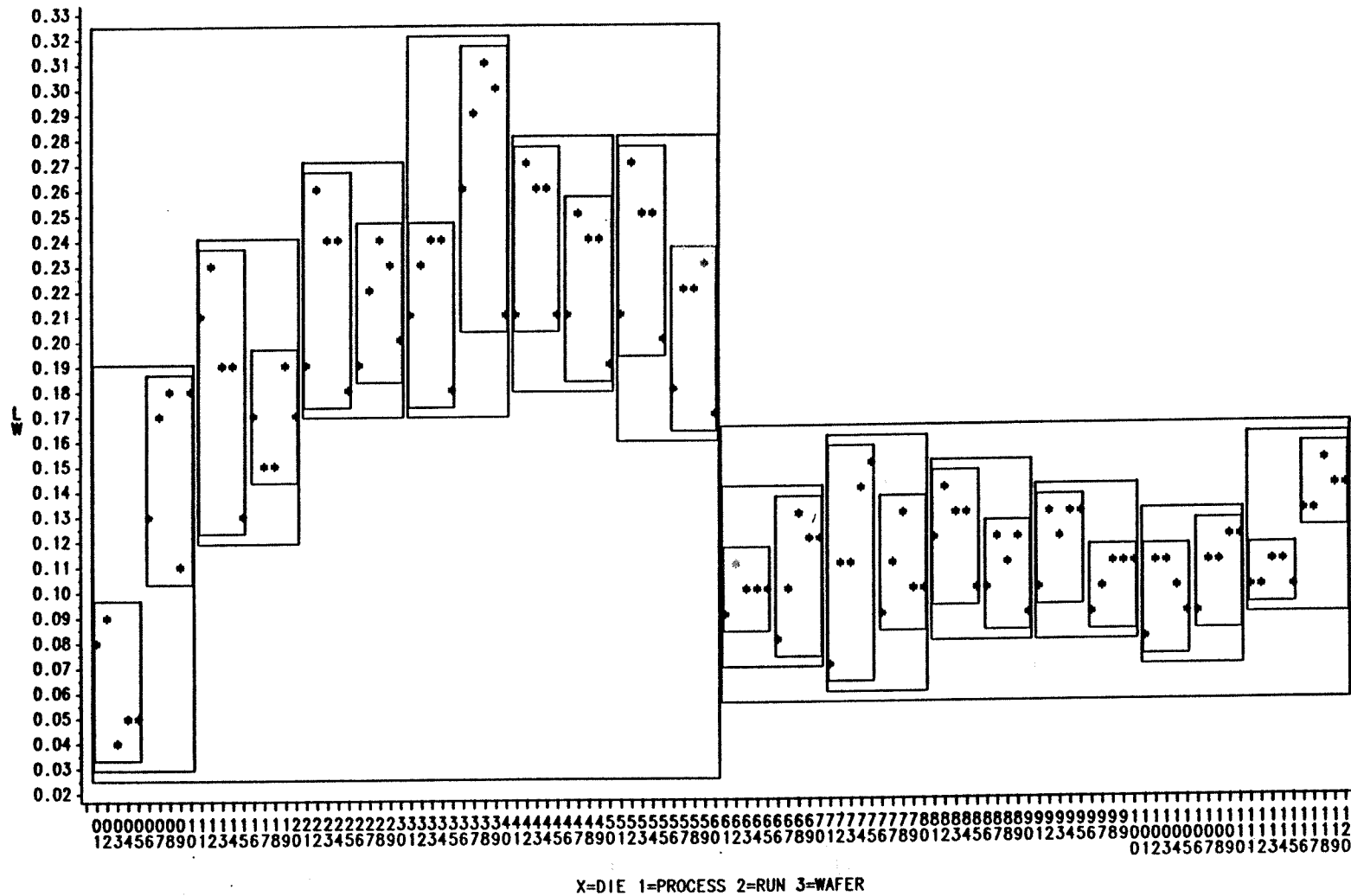
RESULTS/DISCUSSION

The analysis of variance treatment for the CDs is shown graphically in Figure 2. The difference in the etch mask and etched pattern CDs (using the delta eliminated the etch mask linewidth difference between processes) is plotted on the vertical axis, while the horizontal axis represents the data points for each die. The innermost set of boxes show the die values for each wafer. Each die value is an average of three line (actually space) measurements. Their standard deviations were extremely small and did not contribute to any variation. The next set of rectangles represent each run. The largest boxes are labeled with their corresponding process.

Starting within the smallest boxes, or die-to-die variation, the elongated wafer boxes of the existing process indicate a larger variance than the new process. Also, the run boxes enclosing the wafer data are more elongated on the existing process. Finally, the existing process box is much larger, again demonstrating greater variance. Therefore, the CD process variability is less for the new process in all parameters examined.

FIGURE 3. 6P PROCESS
LW DIFFERENCE BETWEEN ETCH MASK AND ETCHED PATTERN

EXISTING PROCESS	NEW PROCESS
1. 6P	1. 6P
2. 6P	2. 6P
3. 6P	3. 6P
4. 6P	4. 6P
5. 6P	5. 6P
6. 6P	6. 6P
7. 6P	7. 6P
8. 6P	8. 6P
9. 6P	9. 6P
10. 6P	10. 6P
11. 6P	11. 6P
12. 6P	12. 6P
13. 6P	13. 6P
14. 6P	14. 6P
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91. 6P	91. 6P
92. 6P	92. 6P
93. 6P	93. 6P
94. 6P	94. 6P
95. 6P	95. 6P
96. 6P	96. 6P
97. 6P	97. 6P
98. 6P	98. 6P
99. 6P	99. 6P
100. 6P	100. 6P



The analysis of variance output for the polysilicon film thickness data is displayed in Figure 3. The vertical axis is the film thickness after the dielectric etch. The remaining parameters are the same as the CD output graph. The data reveals less die-to-die and wafer-to-wafer variation for the new process, but the run-to-run variation was higher. The overall process variation appears to be the same. Figure 4 represents film thickness loss repeatability on a run-to-run basis. More variation is shown in the new process. The run-to-run variation could be attributed to factors other than the process. The grouping of the runs as seen in Figure 4 (the first two runs appear to form a group and the last four runs form another) happens to coincide with a change in personnel at the dielectric 1 etcher.

The SEM photomicrographs in Figures 5 and 6 show the topography profile of the existing and new processes respectively, after the implant mask patterning. The dielectric 1 layer cannot be seen because of a thin deposit. The sidewall angle averaged 83° , with a three sigma value of 1.7° , for dielectric 2, and 83.6° (three sigma of 1.1°) for the DUV stabilized resist.

Two problems were discovered with the double resist process. The first problem encountered pertained to the second resist layer coverage over the DUV stabilized resist. Small v-shaped areas where the resist did not adhere were visible fanning out near the edge of the wafers. There was no resist lifting, in the regions of proper coverage, during the patterning steps, ruling out any full-scale adhesion problems. It could be a matter of step coverage, since the first resist layer is over one micron thick. The photoresist coat process must be investigated for coverage improvements.

The second problem surfaced on the wafer stepper. The ion implant level was aligned to the previous level (dielectric etch mask). The stepper had trouble reading the alignment targets and kept giving a die rotation error. The problem could have been the transfer of the polysilicon surface roughness through the resist in the absence of the Dielectric 2 layer. An adjustment in the stepper auto-alignment algorithm solved the problem.

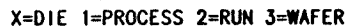
CONCLUSION

The double resist process requires some fine tuning at this point, however, it exhibits promise as a viable alternative to the existing process. Future work would entail a more rigorous evaluation, including full device processing and electrical testing.

ACKNOWLEDGMENTS

The assistance of Mike Jackson, and his time, were greatly appreciated.

AFTER DIELECTRIC ETCH



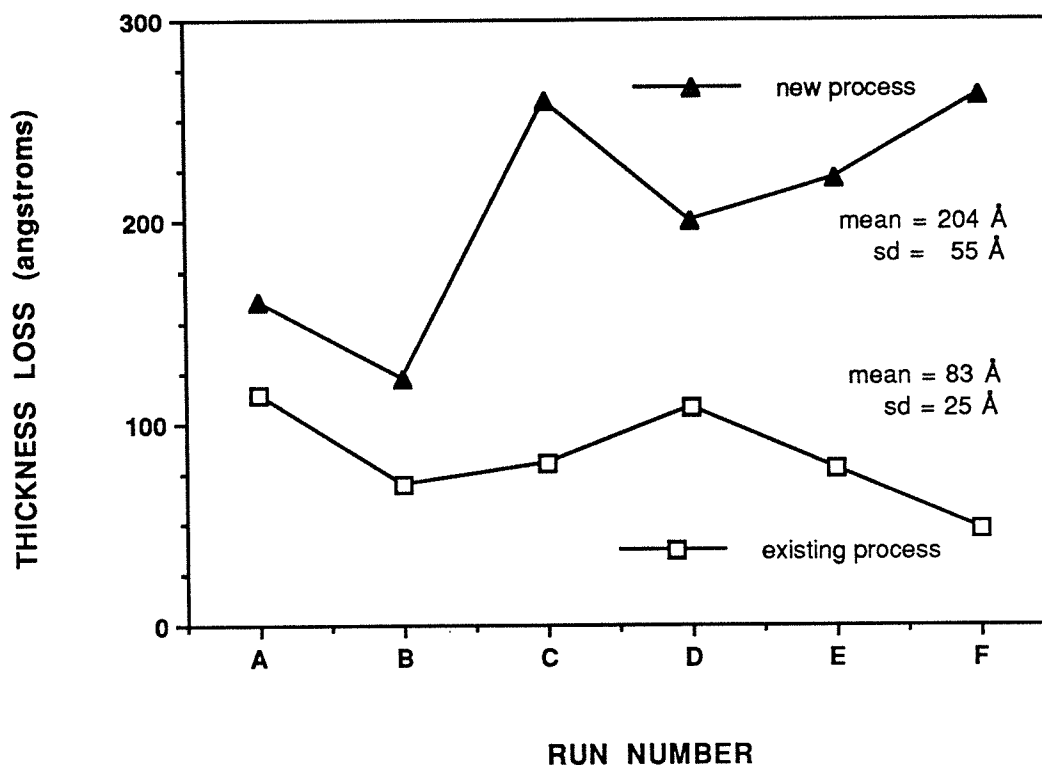


Figure 4: Poly film thickness loss after dielectric etch; run-to-run repeatability.

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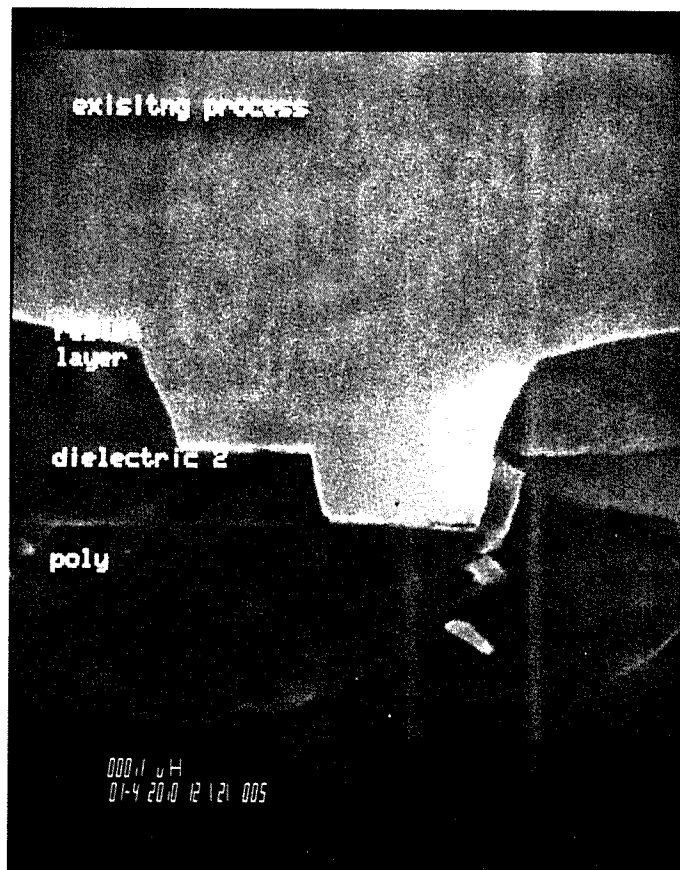


Figure 5: SEM photo of existing resist process.

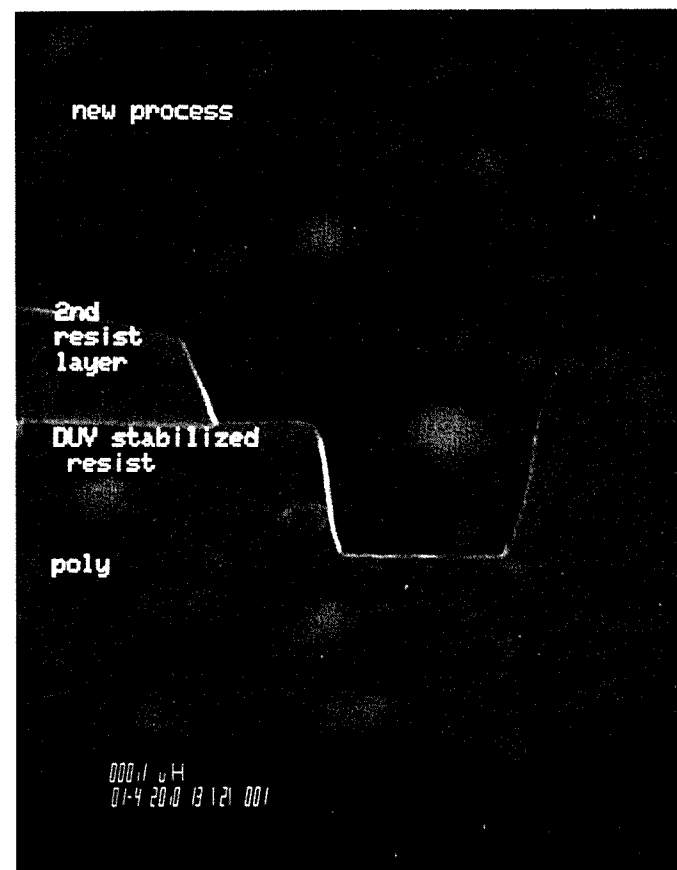


Figure 6: SEM photo of resist process.