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Monolayer Doping for Fabrication of Recessed Channel MOSFETs

Veena Nudnure

November 2019

A Thesis Submitted in Partial Fulfilment of the
Requirements for the Degree of
Master of Science in Microelectronics Engineering

**DEPARTMENT OF MICROELECTRONIC ENGINEERING
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ABSTRACT

Scaling of semiconductor devices has become a challenge with respect to the design, device performance, reliability, integration and fabrication schemes. For over sixty-years now, from the first design of transistor various challenges has been overcome with various integration schemes to shrink the device whilst increasing the device performance. As the devices are shrinking, there is a need to achieve shallow junctions for better performance of non-planar structures such as FinFETs and 3D FETs. The implementation of conventional doping technique ion-implantation can be a hindering process for the shallow junctions as they tend to damage the crystal due to bombardment of high energy beams. Monolayer doping can be an alternative doping technique as the chemicals react with the semiconductor surface enabling a self-assembled and self-limiting process. MLD exploits the surface reaction properties of the crystalline semiconductors to form covalently bonded, self-assembled dopant molecular monolayers on the semiconductor surface with high doping concentrations.

Monolayer doping is implemented to fabricate Recessed Channel MOSFETs which are successful in suppressing the short channel effects by having the channel engineered by implementing the recessed channel grooves which have the potential of reducing the corner barrier effect in comparison to a standard classical planar MOSFET. The subthreshold slope of a 10 μm planar NMOSFET previously fabricated at R.I.T was 150mV/dec, whereas for a 10 μm recessed channel MOSFET fabricated in this work was 117.65mV/dec. The threshold voltage of the 10 μm planar NMOSFET was -0.3V whereas the threshold voltage of the 10 μm recessed channel MOSFETs was 0.2V.

The smallest working Recessed Channel MOSFETs fabricated had a channel length of 1 μm . Various integration schemes can be adopted to further investigate and fabricate recessed channel MOSFETs to show better device performance.

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1. Introduction

Semiconductor industry has moved from planar to non-planar device structures to maintain device scaling, however over years of scaling the devices, it has been found that it is not a linear process and other adjustments are required to maintain the Moore's Law such as changes in design, materials used and process steps.

The junction depths tend to decrease as the devices scales down. Formation of shallow junctions with low resistance is one of the important factors in the device performance and forming shallow junction by widely used doping methods is becoming difficult.

The most commonly used doping technique to introduce dopants into the semiconductor surface is ion implantation which possess various disadvantages such as crystal damage due to bombardment of high energy beam of ions, incompatible with 1D nanostructures and inability to have a range in the nanometre scale i.e., its inability to create shallow junctions. Another doping technique to introduce impurity atoms is thermal diffusion. It is difficult to obtain shallow junctions as impurity atoms are activated at elevated temperatures in thermal diffusion. This elevated temperature pushes the dopant deeper into the substrate. In spin on dopant technique, a uniform layer containing the dopant is coated over the substrate by spinning at different rpms to achieve different thicknesses. The spin coat is followed by a pre-bake step to remove the excess dopant source and desired junction depths are formed by performing diffusion at high elevated temperatures. The disadvantage of this doping technique is not a good control over the deposited dopant film leading to abrupt junction depths. To overcome these disadvantages, a controlled doping technique known as Molecular monolayer doping was developed. The two important parameters of a diffusion profile are junction depth, X_j , and sheet resistance, R_s . The intersection of the background concentration with the diffused dopant impurity profile in the semiconductor is a distance from the surface

of the substrate and is defined as the junction depth. It is important to discern complete dopant activation. For a given dopant dose, ultra-shallow junctions show high sheet resistance.

Figure 1.1 shows the reported data for $R_s \cdot X_j$ for various doping techniques such as ion-implantation following various annealing methods.

Technology Node	Year of introduction	Key Innovation
180nm	2000	Cu interconnect, MOS options, 6metal
130nm	2002	Low-k dielectric, 8 metal layers
90 nm	2003	SOI Substrate
65nm	2004	Strain silicon
45nm	2008	2nd generation strain, 10 metal layers
32nm	2010	High-k metal gate
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers
14nm	2015	FinFET
10nm	2017	FinFETs, double patterning
7nm	2019	FinFETs, quadruple patterning
5nm	2021	Multi-bridge FET

Table 1.1 Summary of developments in technology nodes [1]

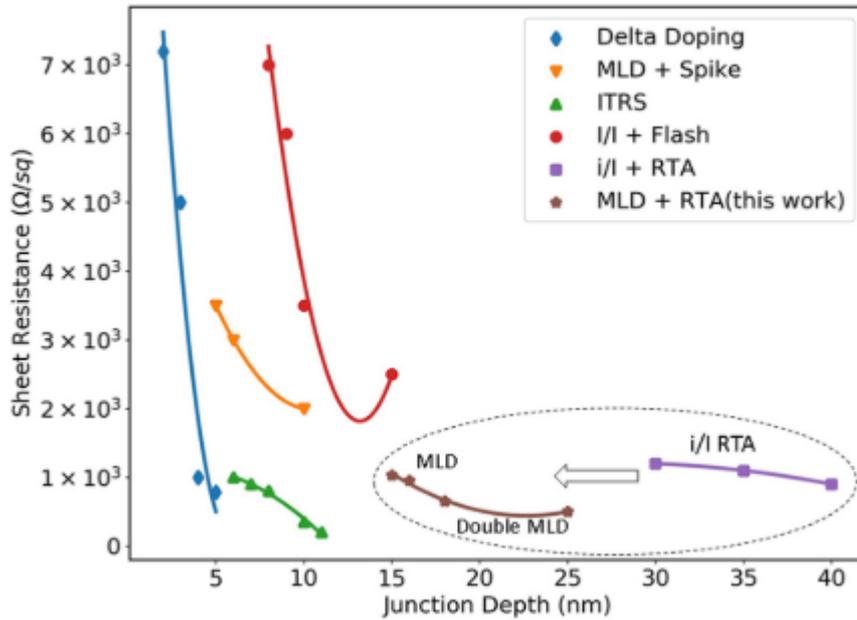


Figure 1.1 Map of literature data for sheet resistance versus junction depths[2]

A summary of the developments in the technology nodes over past 19 years and in future is described in table 1.1.

1.1 Molecular Monolayer doping (MLD)

At University of California, Berkeley, a unique doping technique known as Molecular monolayer doping was established in 2007[3]. Many technological challenges are faced while fabricating well-defined precise structures. Integration of semiconductor surface with chemicals is one of the solutions to achieve well-defined precise structures as it enables a self-assembled and self-limiting process which can be done using Molecular monolayer doping. MLD exploits the surface reaction properties of the crystalline semiconductors to form covalently bonded, self-assembled dopant molecular monolayers on the semiconductor surface with high doping concentrations. This molecular monolayer is the source of dopants, which requires an annealing step for diffusion of dopants into the semiconductor to form shallow junctions[3].

The MLD process is started by immersing the silicon wafer in HF bath, to create hydrogen terminated Si-H sites on the surface. A chemical solution comprising of the solvent and the compound containing the required dopant is prepared in inert nitrogen ambient. The sample is then immersed in the solution for 2.5 hours at 120°C. To ensure an oxygen free environment, the reaction is carried out in a argon filled chamber[3]. This process breaks the C=C molecular sites in the dopant containing compound to form Si-C covalent bonds. During this process, the compound containing dopant from the chemical solution covalently bonds with the hydrogen terminated on the wafer surface. After removal of wafer from the chemistry, silicon-di-oxide is deposited that acts as capping oxide preventing the out-diffusion of dopants from the wafer, which is followed by a high temperature annealing step, that results in diffusion of dopants in the semiconductor forming ultra-shallow junctions. The two important factors that plays major role in the MLD process are the annealing time and temperature as they determine the amount of dopants and the depth of diffusion[4]. The MLD process is demonstrated in Figure 1.2

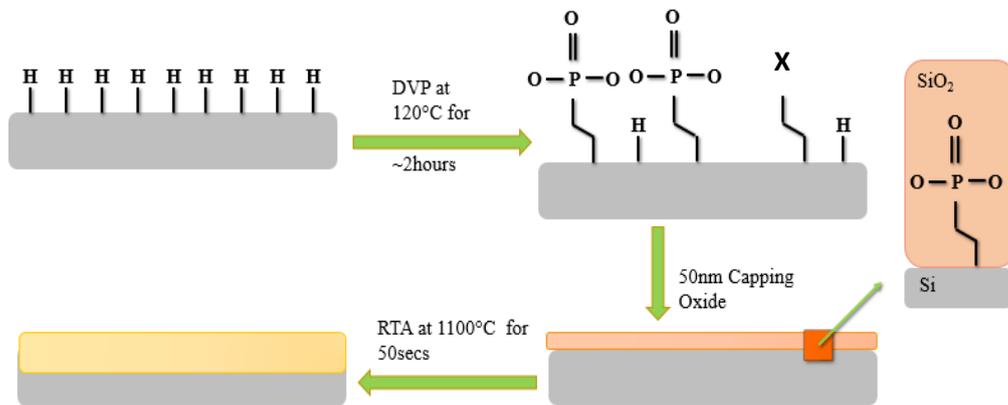


Figure 1.2 MLD Process flow

In the Figure 1.2. X represents the compound containing dopant molecule. Conventional doping technologies such as ion implantation cannot be effectively implemented in high aspect ratio FinFETs as it causes random dopant fluctuations and a non-uniform doping profile in high aspect ratio fin structures. This results in an increase in the parasitic series

resistance and leads to film amorphization due to bombardment of high energy beam. There are chances of lateral dopant encroachment in the channel region which results in high off-state leakage currents. As the channel length scales down to nanometre range, it will be difficult to overcome these major issues.

MLD depends on the Hydrosilylation process to form covalent bonds with hydrogen-terminated surfaces. The dopant containing molecules usually contains a terminal alkene C=C or terminal alkyne C≡C that forms the bond. To dope the surface with boron, allylboronic acid pinacol ester (ABAPE) can be used which has a terminal alkene, whereas to dope phosphorus, diethyl-vinyl phosphonate (DVP) is used which has a terminal alkene. Diethyl 1-propylphosphonate (DPP) has shown results in doping phosphorus regardless of lack of terminal alkene and alkyne terminals. The mechanism of bond formation for DPP is quite not understood but it is reported by various researchers that it forms monolayer similar to other dopant containing molecules [3].

Hydrosilylation process is initiated by immersing the hydrogen-terminated substrate in solution bath heated to 150-200°C which then proceeds by a radical-chain mechanism as shown in Figure 1.3.

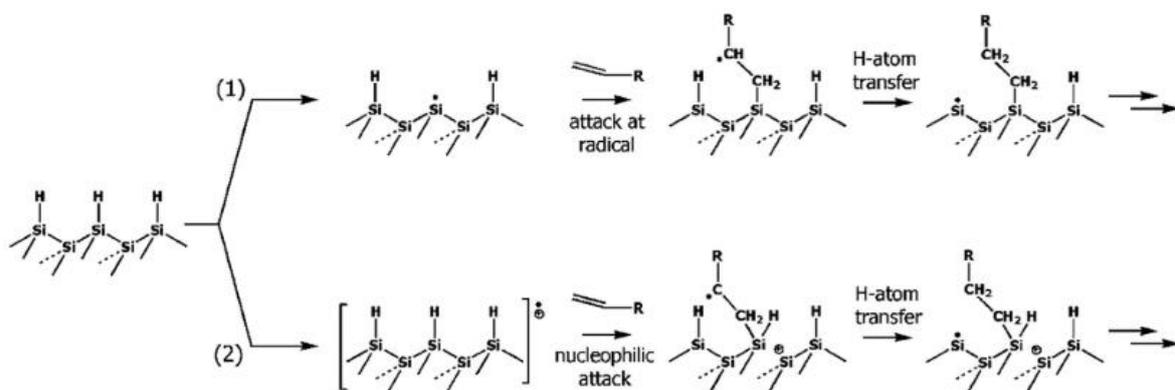


Figure 1.3 Hydrosilylation process

There are two ways of forming covalent bonds as described by path 1 and 2 in figure 1.3. Mechanism shown in path 1 is in the presence of UV light whereas mechanism shown in path

2 is under thermal conditions or room temperature under visible light. In both the mechanisms, a silyl radical is formed that reacts with terminal alkene or alkylene and the reaction chain continues until islands of closely packed monolayers are formed on the surface. It is important to understand the percentage of covalent bonds formed. A study performed on the packing density of monolayers showed a packing of density of 69% relating to the differences in the molecular sizes of alkyl chains and the density of hydrogenated silicon sites present on the silicon surface [5]. Practically, experiments performed showed a packing density of 50% [6]. For DPP molecule, a packing density of $8 \times 10^{14} \text{ cm}^{-2}$ is found. Thus, higher amounts of dopants can be introduced in the substrate by performing MLD multiple times or using a different dopant molecule [7].

1.2 Motivation and MLD work at RIT

At RIT, work on MLD is extensively researched and various devices are fabricated. Novak designed and developed an MLD chamber capable of uniformly doping 6 inch wafers to produce ultra-shallow junctions with high surface dopant concentration[8]. The work mainly focused on doping p-type silicon wafers with n-type dopant such as phosphorus. Diethyl 1-propylphosphonate (DPP) is used as the dopant source with Mesitylene as the solvent. The ratio of the dopant source to the solvent is set to 1:25 volume/volume.

Tapriya and Novak performed a comparative study on various pieces and 6 inch wafers with different annealing time and temperatures and it was concluded that the sheet resistance decreases as annealing time and annealing temperature increases[8][9].

Tapriya investigated and fabricated N+P diodes and transmission line measurement (TLM) structures for realizing their application in shallow emitters and for reducing the contact resistivity in metal semiconductor junctions. The process flow for the fabrication of diodes are shown in Figure 1.4.

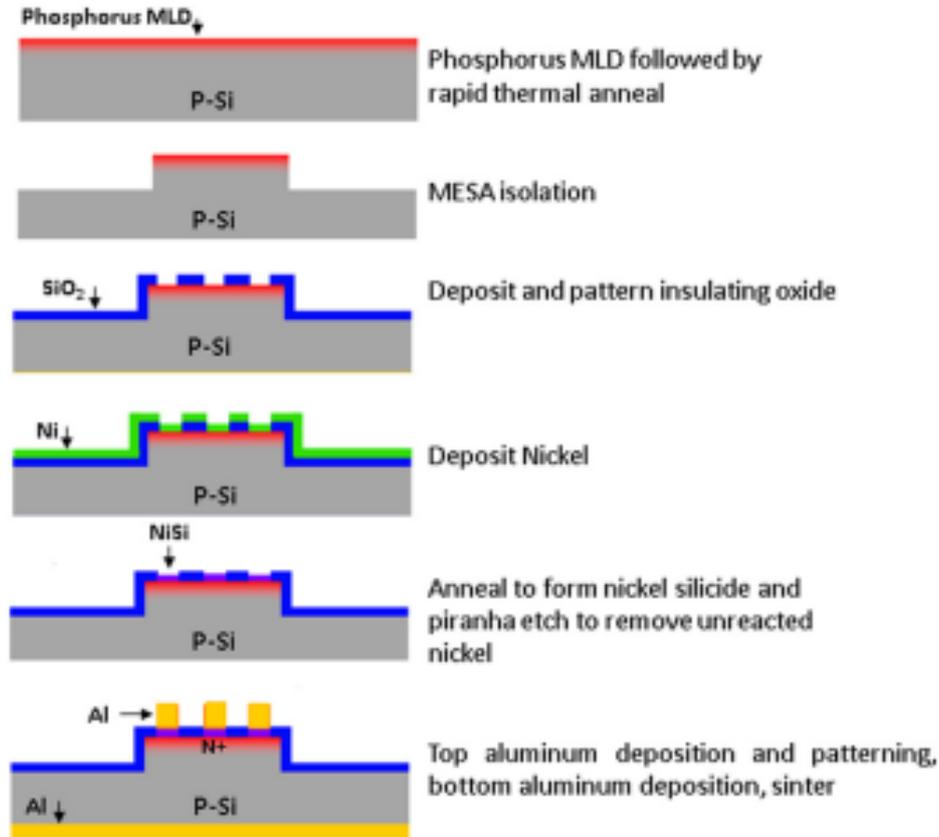


Figure 1.4. Process flow for fabrication of N+P diodes and TLM structures followed by Tapriya[10]

The N+P diode indicates, n regions in p-type silicon substrate. The n-type impurity atoms are introduced by Diethyl 1-propylphosphonate (DPP) compound. The first level of photolithography was MESA isolation, followed by a contact cuts level and metal level. A 7 nm nickel was sputtered on the targets after defining the contact cuts such that nickel is deposited on the doped silicon regions. Nickel silicide is formed by a rapid thermal annealing process and the unreacted nickel is etched in piranha solution.

In the work, the substrate surface with the phosphorus monolayer was analysed using X-ray photoelectron spectroscopy (XPS) for the presence of various elements such as silicon, silicon-carbide, phosphorus and silicon dioxide. It was found that the ratio of carbon to phosphorus on the surface was 1:6 which is like the ratio in the DPP compound.

A secondary ion mass spectroscopy (SIMS) was generated for the substrate encountered with double MLD. The surface concentration was found to be $5.6 \times 10^{21} \text{ cm}^{-3}$.

A dose of $1 \times 10^{15} \text{ cm}^{-2}$ is found for single MLD and is expected to be double of this value for a double MLD process. The sheet resistance obtained for a single MLD was $1130 \text{ } \Omega/\text{sq.}$ and $670 \text{ } \Omega/\text{sq.}$ for double MLD [9].

The current density versus voltage diode characteristics are shown in Figure 1.5 [9], with a parasitic resistance of $264 \text{ } \Omega$ extrapolated from the resistive region of the linear characteristics.

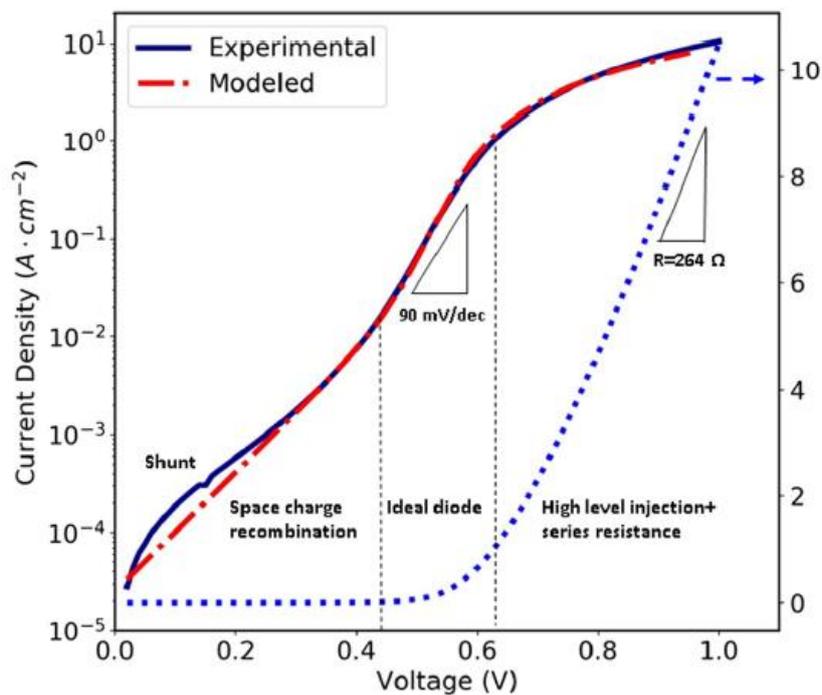


Figure 1.5 Current density versus voltage diode characteristics with parasitic resistance of $264 \text{ } \Omega$ for the fabricated diode[9]

The diode characteristics were consistent in the neutral region, whereas variations in the depletion-region recombination's and the high level/series resistance regions were found. The characteristics are compared and is in close approximation with an unified diode model [9]. Specific contact resistivity of $10^{-5} \text{ } \Omega\text{cm}^2$ are obtained making them an attractive process for selective emitters [9].

Doran fabricated successful n type field effect transistors at SMFL RIT using MLD. Previously designed MLD chambers at RIT has some issues with doping the substrates, so Doran designed

and developed the MLD chamber and was successful in doping 6inch substrates. Two different dopant containing compounds were utilized namely, diethyl propyl phosphonate (DPP) and diethyl vinyl phosphonate (DVP). Various measurement techniques were used to verify the results of MLD. First measurement technique was four-point probe, to measure the sheet resistance of doped samples after single MLD and double MLD. It was found that the sheet resistance dropped be almost 300 $\Omega/\text{sq.}$ from single MLD to double MLD. Also, DVP showed reduced sheet resistance values compared to DPP and hence was used for subsequent processing.

An experiment was conducted to verify the MLD process reaction timings. In this experiment, different pieces were immersed in the MLD chemistry solution with DPP for different time intervals such as 5, 10, 20, 30, 45, 60, 90, 120, 180 and 240 minutes with the other processing steps remaining same. Sheet resistance versus the immersion reaction time intervals are plotted in Figure 1.6 [2].

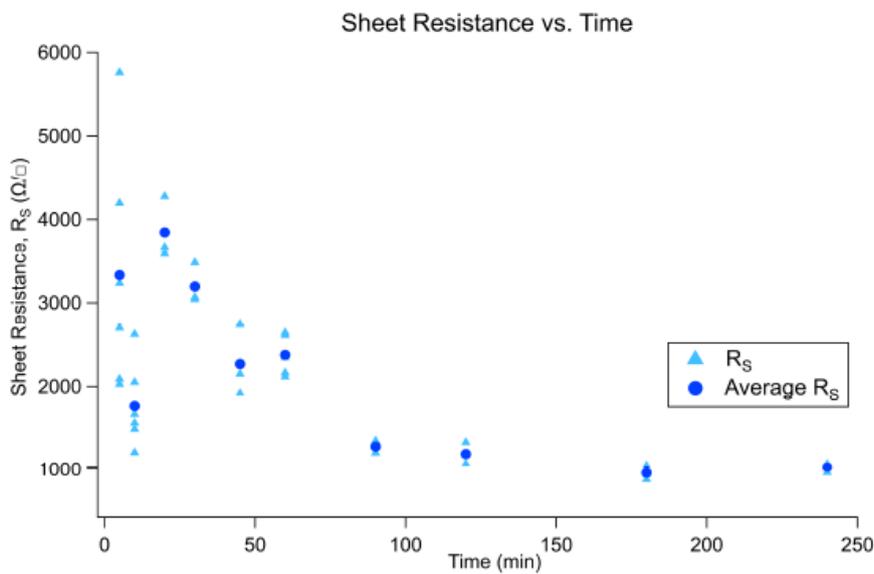


Figure 1.6 Sheet resistance versus reaction time intervals[2]

It was observed that sheet resistance of the samples exponentially decreases with the increase in reaction time intervals with small changes in the sheet resistance after 90 minutes reaction time. After a period of 150 minutes, the distribution becomes tighter, indicating the formation

of a uniform monolayer on the surface and it was concluded that reaction time of 120 minutes is enough to form uniform dopant monolayer on the substrate.

SIMS was performed on a single MLD substrate doped with DVP and DPP to analyse the surface concentration of phosphorus dopants versus the depth in the p-type silicon having a background concentration of $1 \times 10^{15} \text{ cm}^{-3}$. The substrate doped with DPP had a peak concentration of $1.3 \times 10^{20} \text{ cm}^{-3}$ with a junction depth of 140nm, whereas the substrate doped with DVP had a peak concentration of $3.3 \times 10^{20} \text{ cm}^{-3}$ with a junction depth of 200 nm, relating to the results obtained before where DVP showed a lower sheet resistance in response to higher peak concentration with a deeper junction depth compared to DPP.

Another study was conducted to study the patternability of MLD using silicon dioxide as a hard mask. A 750 nm thick silicon dioxide was thermally grown, patterned using photolithography step and etched to expose silicon regions for the doping process. After doping, the oxide is completely etched, and a thin oxide is regrown at 900 °C for 30 minutes. Figure 1.7 shows a visible difference in the oxide growth over doped regions versus undoped regions.

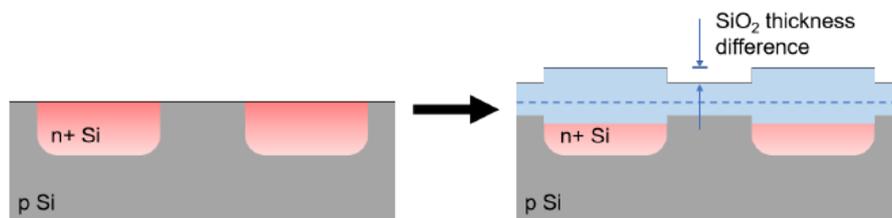


Figure 1.7 Difference in oxide growth on a doped silicon substrate

To verify, if MLD could dope features using silicon dioxide as hard mask, the layout design for various features were overlaid with the microscopic image of the patterned doped features with thin oxide and no difference was found in the overlaid image with respect to the layout design. Hence, it was proved that MLD could dope features using silicon dioxide as a hard mask.

The regular NMOSFET was fabricated with a thin gate oxide of 30nm with various gate lengths and widths. The transfer characteristics of a NMOSFET with gate length of 10 μm and a gate width of 110 μm plotted in both linear and log scale is shown in Figure 1.8[2].

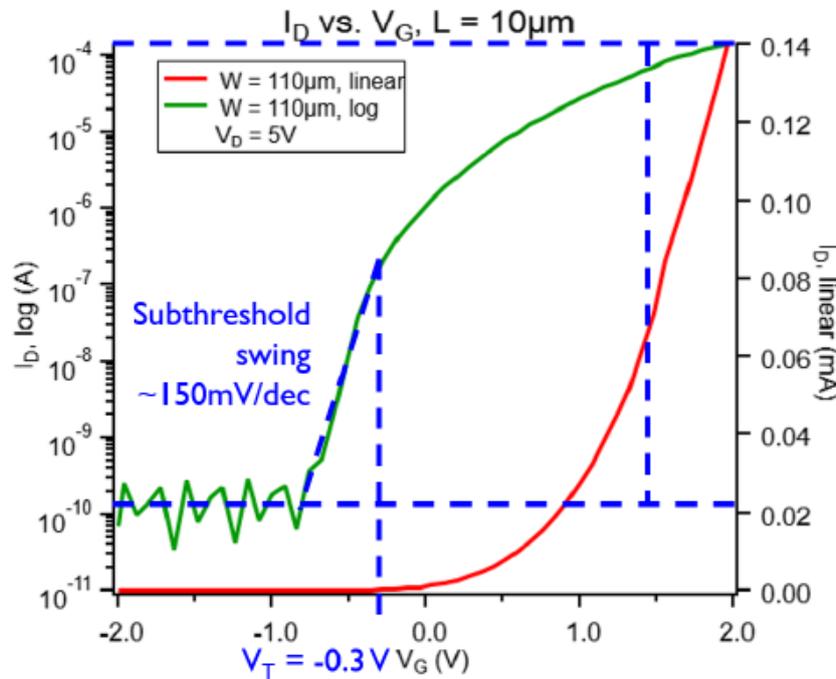


Figure 1.8 Transfer characteristics of NMOSFET with gate length 10 μm

The threshold voltage of the device is -0.3 V with a subthreshold swing of 150 mV/dec and an on/off current ratio in 3 orders of magnitude. From the characteristics plot of other devices, it was observed that as the gate width increases the current increases in a linear fashion. The only drawback observed in the regular MOSFET devices was the absence of nickel-silicide, which created non-ohmic contacts which was identified in the SEM and TEM cross-section images. As a result of the absence of nickel, a interfacial layer of silicon dioxide was formed on the silicon in the contact cut region during the piranha etch performed to etch unreacted nickel as per the process flow[2].

The mask layout mainly consisted of four levels hence had four photolithography steps. The first level defined the region for the monolayer formation. Second level defined the trench

regions. Third level defined the contact cut regions and the fourth level defined the metal regions.

1.3 Applications of Molecular Monolayer Doping

Properties of the widely used semiconductor material, Silicon, can be easily tuned by forming H-terminated silicon surfaces with monolayer doping technique, which makes MLD applicable in many integrated circuits and many photovoltaics industries as it can form junctions less than 10nm [11]. One of the many advantages is forming ultra-shallow junctions in planar and 3D devices such as FinFETs. Selective emitters can be fabricated using MLD thus increasing the efficiency of solar cells in photovoltaics industry.

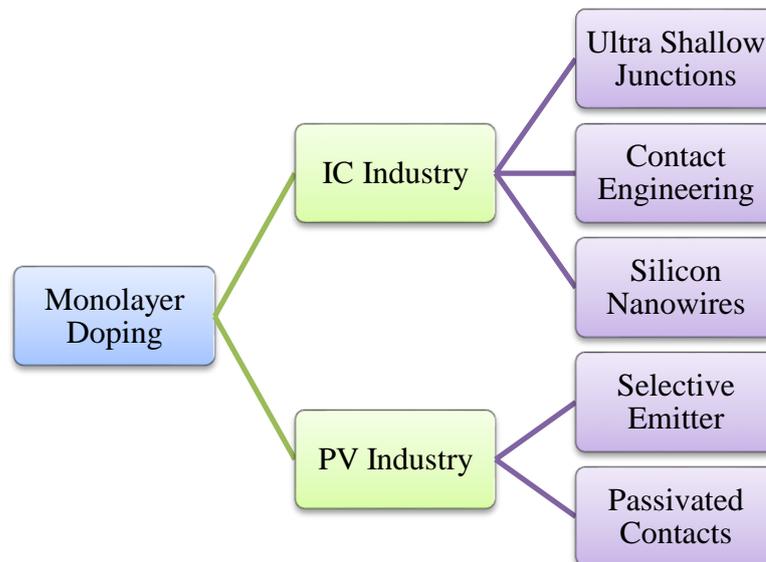


Figure 1.9 Applications of MLD

Devices with ultra-shallow junctions and low sheet resistance perform better compared to a high sheet resistance ultra-shallow junction device as it results in short-channel effects such as surface scattering, drain induced barrier lowering, impact ionization and hot electrons and velocity saturation. Scaling of channel length usually modifies the threshold voltage of the device and the restrictions due to electron drift characteristics leads to a lower device performance. Control over the gate dielectric thickness can help overcome the short channel

effects but lowering the thickness also increases the power consumption along with leakage current. Another method to overcome these problems is to form shallow junctions which can be formed using MLD.

MLD has shown positive results in doping III-V compound semiconductors which has lower bandgap compared to silicon, which makes it more vulnerable to high junction leakage, thus there is a need to form damage-free junctions in III-V compound semiconductors. InGaAs III-V substrates were doped with sulphur, using ammonium sulfide solution. A sheet resistance of 164 Ω/sq with maximum dopant activation of $3 \times 10^8 \text{ cm}^{-3}$ was achieved. X-ray diffraction was performed on the samples before annealing and after annealing with increasing temperatures. No differences were found in the spectra before and after annealing even after increasing the temperature which indicated that MLD did not damage the crystal structure [12].

In 2011, at CNSE, Albany, MLD was used to fabricate a FinFET with a fin width of 20 nm and a gate length of 40 nm to create an ultra-shallow junction of 5 nm. It is also shown that MLD can be used to form defect less doped fin with uniform silicide as it is one of the important to reduce the junction spiking while giving a low parasitic fin resistance as compared to a ion implanted fin which usually has lot of defects due to implant damage which forms irregular non-uniform silicide along the dislocation paths. Important aspects about Ni-Si formation is presented and compared between a Schottky source and drain versus a diffused source and drain. In a Schottky sourced and drain, the Ni-Si is greater than the junction formed. This possess major issues as a high thermionic emission leakage increasing the hole current during the off-state operation as a result of fermi level of Ni-Si being closer to the valence band. The other issue experienced is the performance of on-current which is restricted by the high electron Schottky barrier height. To overcome these issues, it is necessary to ensure the thickness to Ni-Si to be within the shallow junction formed as it results in a diffused source and drain enabling ideal transistor characteristics such as high on state current and low off start current[13].

Molecular monolayer doping has shown significant results in introducing impurity atoms such as arsine in germanium substrates in a similar manner as the silicon substrate as shown in figure 1.1. The only difference between the doping process in germanium and silicon would be the annealing temperature as germanium has a lower melting point compared to silicon. The annealing temperature was engineered to be 650 °C for different annealing times such as 1secs, 10 secs and 100 secs which introduced same amount of dopant dose but creating different concentration profiles with different junction depths. The same peak concentration irrespective of different annealing times indicates the limit of solubility of arsenic in germanium has reached at 650 °C[14].

MLD was demonstrated on undoped 20-100 nm InGaAs that was epitaxially deposited on GaA/InP heterostructure grown on silicon substrates using various sulphate chemistries [15].

MLD plays an efficient and important role in doping solar cells. Electric energy in solar cells are generated when electrons and holes are efficiently separated at the p-n junction hence controlled doping in solar cells plays an important role in fabricating solar cells. Fabricating nanometre scale structures in solar cells with higher surface to volume ratio and larger areas allocated to p-n junctions can increase the efficiency of the solar cells as these structures can absorb more light thus separating the electron-hole concentration more effectively.

1.4 Recessed Channel FETs

Power MOSFETs can be categorized into five main groups. The first group includes MOSFET structures consisting of co-planar source, gate and drain electrodes having aluminium metal. The device structure is horizontal and is constantly doped to create the channels. The second group of MOSFET structure consists of co-planar source, gate and drain electrodes. This structure has a horizontal channel region designed and fabricated implementing the double-diffusion technique. The third group of MOSFET structures include non-planar electrodes

having a uniformly doped horizontal conducting channel region. The fourth type of MOSFETs include non-coplanar source, gate and drain electrodes. These devices have source and gate fabricated at the top of device and the drain region at the bottom of the device. These devices are fabricated using double-diffusion technique implementing multi-cell configuration. The fifth group of MOSFETs are classified as Recessed Channel MOSFETs with trenches etched in the silicon between source and drain to define the channel region. In 1969, the first high-voltage power MOSFET was developed implementing a V-Groove etched MOSFET. In this work, Recessed Channel MOSFETs are fabricated using Monolayer doping, which inherits the idea of etching trenches to define the channel region. The figure 1.10, shows the first V-groove Recessed Channel MOSFET.

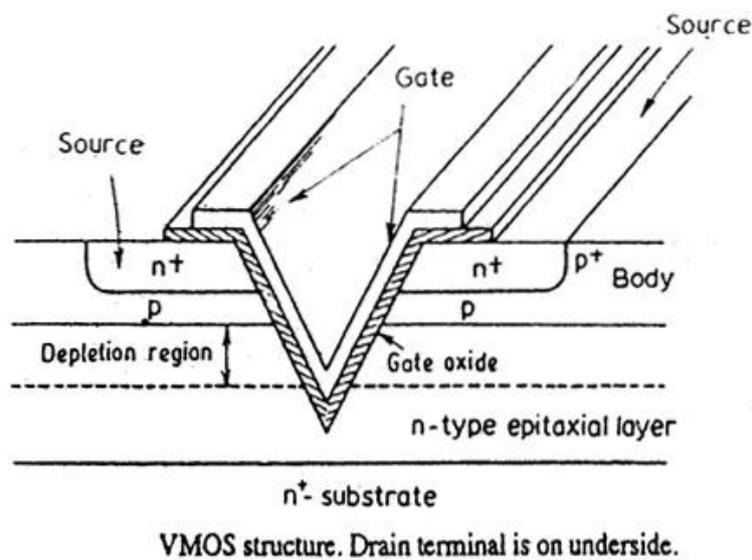


Figure 1.10 VMOS structure with V-shaped Recessed Channel [16]

A two dimensional Recessed channel Silicon-On-Insulator MOSFETs with rectangular channel is analysed and are successful in suppressing the short channel effects by having the channel engineered by implementing rectangular grooves[17]. It was proved that having the rectangular groove reduced the corner potential barrier. Silicon on insulator offers great advantages in suppressing the short channel effects, and hence was a great candidate for this work. Silicon on insulator comprises of buried oxide acting as insulator, which ensures

isolation between the active part and the substrate. It offers low junction capacitance reducing the power consumption of the device, increasing the device performance. The main advantage of having a groove between the drain and source is the depletion region formed around the drain is not extended towards the source region reducing the short channel as well as punch-through effect. Four different type of Recessed Channel FETs have been simulated using 2D ATLAS Device simulator to understand the device performance and the devices simulated comprises of different dual gate material and multi-gate material integrated with the Recessed Channel FETs on a Silicon on insulator substrate[17]. The devices were simulated with a channel length of 102 nm, oxide thickness of 4 nm, buried oxide thickness of 100 nm and n-type source and drain heavily doped with $1 \times 10^{17} \text{ cm}^{-3}$. The substrate of the devices was p-doped with a concentration of $1 \times 10^{20} \text{ cm}^{-3}$. From the simulation results it was observed that the Multi-Layer Dual Material RC SOI FET showed better device performance in terms of a higher drain current, as it had an improved control of the gate region over the high mobility and the channel of the device. The Multi-Layer Dual Material RC SOI FET also showed better transconductance in comparison to other devices mainly due to the fact that the channel had a low doping concentration due to incorporation of Multi-Layer and had a low electron velocity peak near the source region due to the incorporation of Dual Gate Material[17]. An analytic model of the threshold voltage of a Recessed Channel FETs with U shaped groove was modelled in 2010 [18]. The Recessed channel FETs in shown in figure 1.11. The model can be obtained and derived in a way like a classic planar MOSFET implementing the charge sheet approximation and the gradual channel approximation. For a classic planar MOSFET, the equations of V_{DS} are expanded in power series, but due to the distribution of depletion charge over the recessed channel in RC-FET, analytical calculation of threshold voltage is difficult.

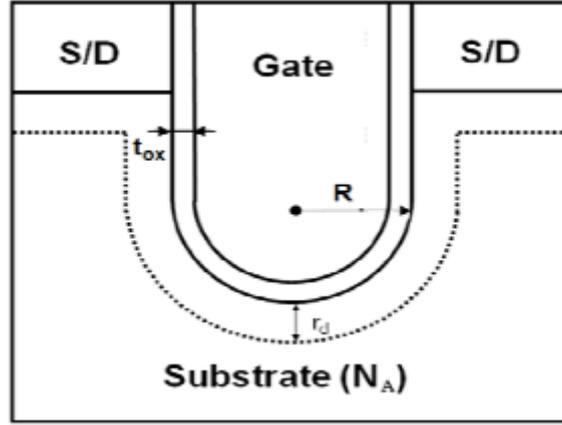


Figure 1.11 Recessed Channel FET with U shaped groove [18]

The proposed drain current is in equation 1.1.

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} \left[\left(V_g - V_{fb} - 2\phi_f - g(2\phi_f) - \frac{V_{DS}}{2} \right) V_{DS} \right] \quad (1.1)$$

and the threshold voltage as shown in equation 1.2.

$$V_{th} = V_{fb} + 2\phi_f + \frac{\sqrt{2qN_a\epsilon}}{C_{ox}} \sqrt{2\phi_f} \left(1 - \frac{\epsilon}{qN_a} \frac{2\phi_f}{3R^2} \right) + \frac{2\epsilon}{C_{ox}} \frac{2\phi_f}{3R} \left(1 + \frac{\epsilon}{qN_a} \frac{2\phi_f}{2R^2} \right) \quad (1.2)$$

In this analytic model, the threshold voltage is also dependent on a parameter R, which is the radius of the U-shaped groove. The threshold voltage is directly dependent on the doping concentration and indirectly proportional to the radius of the groove, which indicates the threshold voltage of the device decreases as the doping concentration of the device decreases and the radius of the groove increases. Hence, for the devices without U-shape the term R can be equated as zero, and the threshold voltage equation can be derived.

In a simulation study the classic planar MOSFET and the recessed channel FET are studied using Monte Carlo Simulation and drift diffusion technique [19].

For long channel devices, the threshold voltage is the voltage required to invert the channel region to enable charge flow, whereas in short channel devices, the channel depletion region is affected by the drain and source junctions and depletion widths and the threshold voltage is then dependent on the effective channel length and the shape of the channel.

The gate corner effect is demonstrated in figure 1.12. The figure shows a plot of surface potential across the silicon-silicon dioxide interface versus the distance from source junction for both planar and Recessed Channel MOSFET.

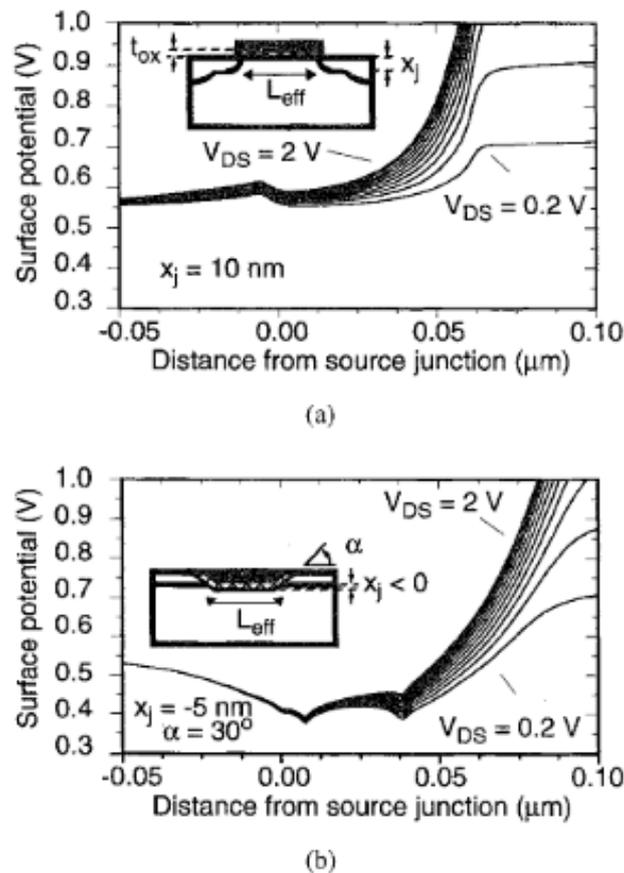


Figure 1.12 Surface potential along the Si/SiO₂ interface for (a) Planar MOSFET (b) Recessed Channel MOSFET[19]

Recessed Channel FETs has the capability to reduce the short channel effects due to the strong potential barrier produced at the corners of gate that are eventually suppressed due to the device structure. It is observed that for a planar MOSFET the surface potential is strongly affected by the drain voltage whereas for the Recessed Channel FET, the surface potential is hardly affected by the drain voltage indicating the corner effect acting against the DIBL effect.

The presence of threshold voltage roll-off in a planar MOSFET is prominent due to the influence of junction depth created in drain region into the channel region, whereas in a

Recessed Channel MOSFET, the threshold voltage is almost same irrespective of different gate lengths and gate oxide thickness [19].

In a study performed to understand the electrical behaviour of planar MOSFET and Recessed Channel MOSFETs, Monte-Carlo Simulation are executed. The mean electron velocity along the silicon-silicon dioxide interface for a planar MOSFET with a x_j of 10 nm and a Recessed Channel FET with a x_j of 0 nm is plotted in figure 1.13.

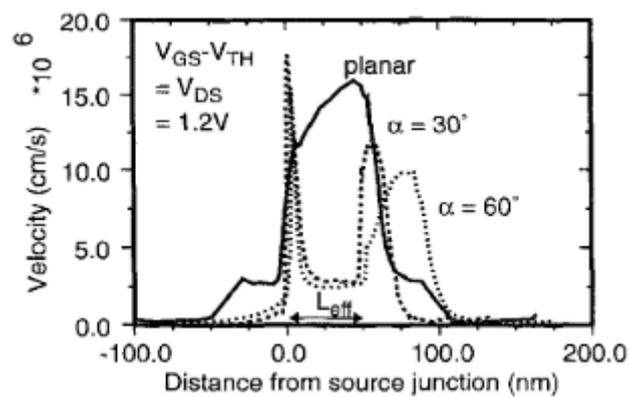


Figure 1.13 Mean Velocity along the silicon-silicon dioxide interface for planar and Recessed devices[19]

As observed in the figure 1.13., for the planar device, a peak is observed in the channel as well as drain region indicating the presence of the electron velocity, whereas in the Recessed Channel FETs, the peak demonstrating the non-stationary transport is observed only in the drain region, specifically near the oxide corners.

The presence of the electron transport in the channel region is less compared to a planar MOSFET ensuring better reliability of the device and the hot carrier effects. The mechanism of flow of drain current in Recessed Channel MOSFET can be studied by the electric field profiles shown in figure 1.14. The electric field lines across the silicon-silicon dioxide interface for different channel lengths are plotted having a x_j of 0 nm.

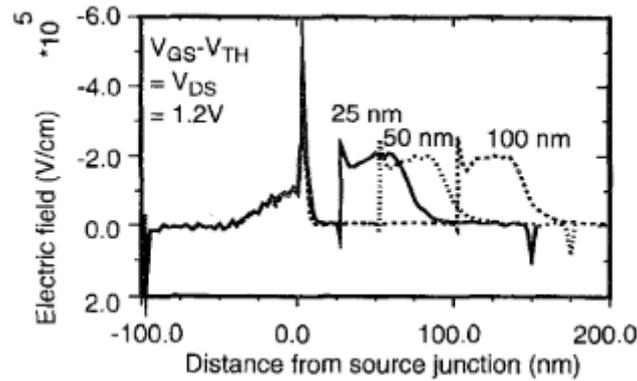


Figure 1.14 Electric field lines parallel to the Silicon-Silicon dioxide interface [19]

As observed the lateral electric field is protected by the corner effect in the channel region. The electric field around the source oxide corner of the Recessed channel FETs is large and has a narrow peak whereas it's the amount and shape of electric field around the drain oxide corner is almost unaffected but changes according to the channel length. Thus, it is proved through simulations that the electric field and electron transport properties are dependent on the channel to oxide geometry.

1.5 Scope of this work

In this work, molecular monolayer doping (MLD) is implemented to fabricate Recessed Channel Field Effect Transistors (FET).

The first objective of the work performed is to demonstrate the efficiency of the MLD chamber for doping various substrates such as Bulk-Silicon and Silicon-On-Insulator. The detailed information is discussed further in Chapter 2.

The second objective is to improve the annealing conditions such as annealing temperature and annealing time. In the previous work at RIT, an annealing temperature of 1000 °C for 5 minutes was performed. The key feature of rapid thermal processing is the low time process. Thus, experiments will be performed on pieces of different substrates at different annealing

temperatures and times to reduce the overall time of the fabrication process and to provide shallow junctions. These are discussed in Chapter 4.

The third objective is to complete the fabrication of Recessed Channel MOSFETs and test the devices for electrical performance and to check the liability of MLD for shallow trench MOSFETs. The detailed information about the mask design and fabrication steps are presented in Chapter 5 and the details on electrical performance and testing results of the FETs are explained in Chapter 6.

2. Doping Silicon-On-Insulator (SOI)

Scaling of bulk-Silicon devices down to 20 nm gives rise to many problems such as decrease in carrier mobility due to impurity scattering, an increase in p-n junction leakage due to shallower junctions and an increase in gate tunnelling current due to reduction in gate dielectric thickness. Due to these issues, the operating voltage of the device needs to be set to a higher value than the expected value to achieve the desired device performance and speed. A new technology enabled fabricating MOSFETs on the silicon-on-insulator (SOI) substrates, as the buried oxide layer in the SOI-MOSFETs offered many advantages over the bulk-silicon MOSFETs.

The various advantages offered by SOI-MOSFETs are negligible drain to substrate capacitance, steep subthreshold characteristics, negligible floating body effects with small short channel effects, reduced junction leakage current, high speed operation due to its low capacitance, and high temperature withstand ability. [20]

The presence of the buried silicon dioxide layer (BOX) under the top silicon layer distinguishes the bulk-silicon substrate from the SOI substrate. The widely used methods of forming the buried oxide layer is by oxidation of silicon and by oxygen implantation into the silicon. The thin silicon film on the buried oxide layer can also be referred as the top-silicon layer or the SOI layer. The thickness of this SOI layer is usually set to one third of the effective channel length to prevent the punch through current. The devices fabricated in a single crystalline SOI layer are called as SOI devices whereas the devices fabricated in a polycrystalline SOI layer are called as thin film transistors. [20]

2.1.Literature Review of MLD on SOI

Recently in 2018, MLD has been demonstrated on SOI substrates [21]. In the experimental setup, the SOI substrates were placed in a 2% HF solution to enable hydrogen-terminated silicon dangling bonds. Following the treatment, the samples were placed in Schlenk apparatus to avoid the re-oxidation of the surface. A 100 μL of Allyldiphenyl phosphine (ADP) used as the phosphorus dopant containing compound is mixed with 5mL of mesitylene as the chemistry solution used to dope the samples. The reaction is carried out for 3 hours, although no information about the reaction temperature is provided. A 50 nm of SiO_2 is sputtered as the capping oxide prior to annealing steps. The SOI samples were annealed at a temperature of 1050 $^\circ\text{C}$ for 5 seconds.

Atomic force microscopy (AFM) was carried out to measure the surface quality before and after MLD on the SOI samples. The surface roughness prior to MLD was less than 0.2 nm which increased to approximately 0.3 nm after MLD processing which may be due to the remains of capping oxide after etch removal process[21].

An active carrier concentration of $2 \times 10^{19} \text{ cm}^{-3}$ was found using the electrochemical capacitance voltage technique that studies the concentration of dopants versus the depth.

Two samples were used in the experiment, 13 nm and 66 nm. Hall measurements were used to measure the presence of active dopants in SOI samples by calculating mobility and carrier properties of the samples. It measures voltage and resistance by applying current and magnetic field to the samples. It was found that the sheet carrier concentration, namely the dose values for both the samples were same as it limited by the concentration of ADP on the surface but the carrier concentration on the 66 nm sample is less due to higher volume, because of which it has higher mobility.

A study was conducted, to analyse the surface oxidation of the surface after the HF treatment and the chemical reaction process. During the MLD process, extensive care was taken to avoid any re-oxidation by carrying out the experiment in Schlenk line which is an inert chamber. Regardless of these steps, it was found that small amount of silicon dioxide was formed during the chemical reaction process which inhibits the diffusion of phosphorus in those areas. The results of the XPS analysis carried out is shown in Figure 2.1[21].

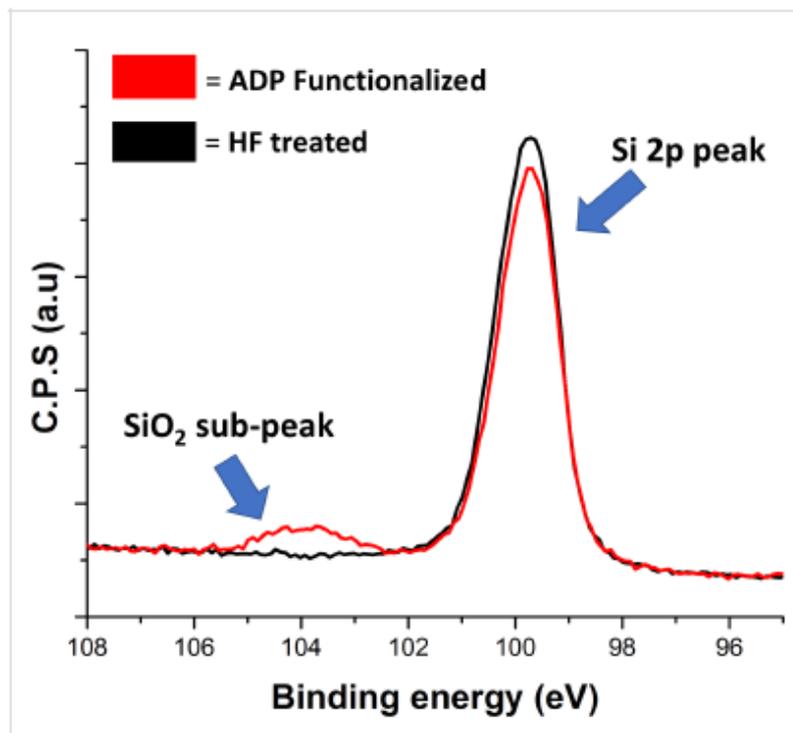


Figure 2.1 XPS analysis to measure the presence of SiO₂ [21]
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Secondary ion mass spectroscopy (SIMS) analysis was also performed to analyse the distribution of dopants in the SOI substrate. A spike in the phosphorus concentration is observed at the silicon-oxide interface indicating the dopant trap at the interface. It may also indicate the slower diffusion rate of phosphorus in the silicon dioxide compared to bulk silicon. The SIMS performed by these researchers are shown in Figure 2.2 [21].

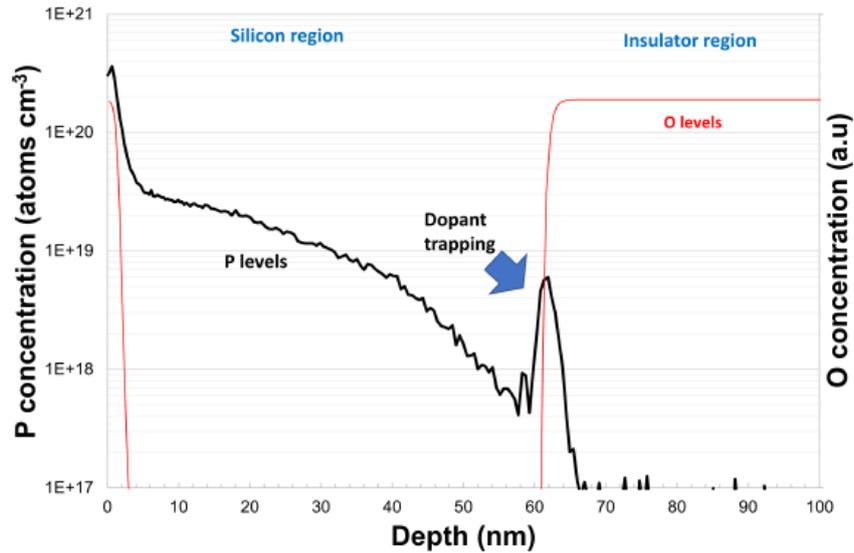


Figure 2.2 SIMS analysis performed on the MLD doped SOI substrate [21]
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A unique conformal doping technique was introduced in 2018 by a research group from Korea introduced to the semiconductor industry as initiated-CVD process. iCVD technique involves depositing dopant containing polymer layers onto substrate by free radical polymerization. A reactor with initiators and vaporized monomers is used. Thermal dissociation of initiators generated radicals leading to chain reaction forming polymers. A post bake at 230 °C annealed the film followed by deposition of 50 nm of capping oxide to protect the polymer film. A rapid thermal processing at 1100 °C for 5 secs to activate and diffuse the dopants.

Fourier transformed infrared spectroscopy (FTIR) analysis performed on the deposited polymer films, poly (boron allyl oxide) (pBAO) and poly (triallyl phosphate) (pTAP) acting as the dopant source for boron and phosphorus respectively is shown in Figure 2.3.

The analysis shows polymers of boron allyl oxide and triallyl phosphate indicating successful polymerization reaction. Poly (boron allyl oxide) polymer showed exhibited hygroscopic characteristics which indicates easy decomposition of B-O-C bonds in exposure to ambient air.

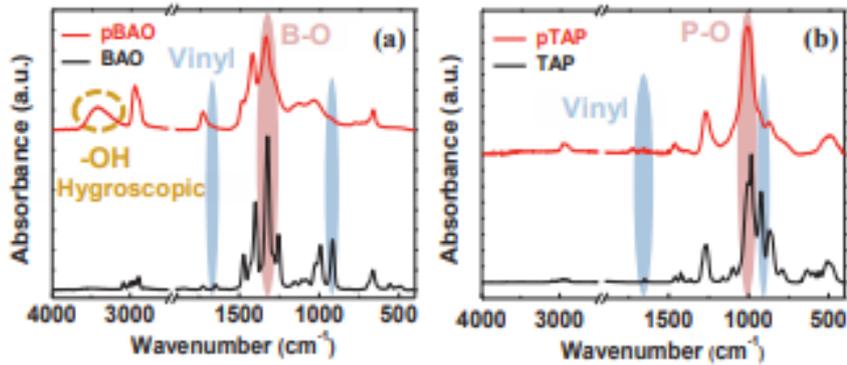


Figure 2.3 FTIR analysis spectra of pBAO and pTAP polymer film [21]
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To study the effectiveness of the deposited polymer films and the concentration of the dopant profiles transmission electron microscope (TEM) and electron energy loss spectroscopy (EELS) analysis were performed on the deposited polymer stacks after the rapid thermal annealing step performed at 1100 °C for 10 seconds. A total thickness of 40 nm of polymer was deposited as the dopant source. Figure 2.4(a) shows the existence of 8.3 nm of remaining polymer layer with 50 nm of capping oxide. From the Figure 2.4(b) showing the EELS spectra, growth of a thin oxide layer can be observed on the silicon substrate effecting the dopant enhancement.

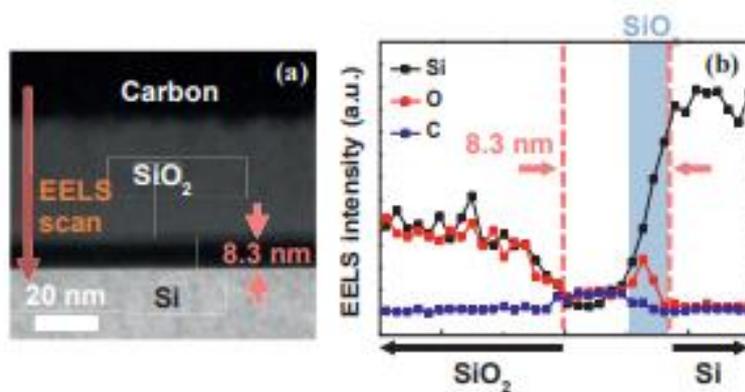


Figure 2.4(a)TEM image of the stack after RTA (b)EELS spectra [21]
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Different thickness of poly (Boron allyl oxide) were deposited on the silicon substrate as and SIMS analysis were performed on these polymer films to study the dopant profiles in the

substrate as shown in Figure 2.5. Boron concentration is observed to decrease along with the junction depth as the polymer thickness decreases. For polymer thickness less than 10 nm, a surface concentration of less than $1 \times 10^{19} \text{ cm}^{-3}$ is observed.

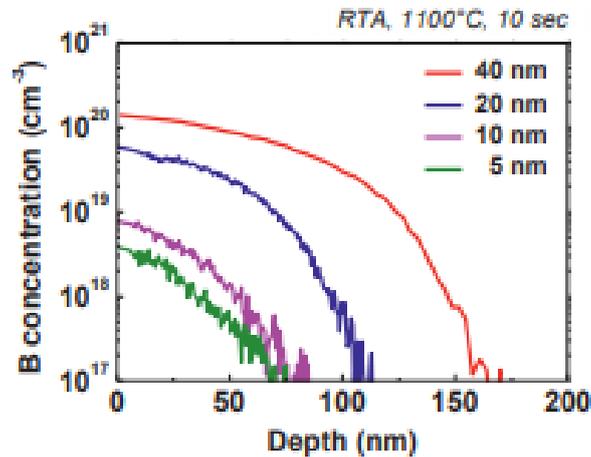


Figure 2.5 SIMS profile for different polymer thicknesses [21]
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To enhance the dopant concentration for polymer thicknesses less than 10 nm, integration with copolymer step was studied. For both boron and phosphorous polymer films, a passivation step and double deposition step is performed respectively. In both the steps, another layer of polymer is deposited by the iCVD deposition process flow. An experiment performed with a polymer thickness of 8nm and a polymer thickness of 5 nm with a copolymer thickness of 3 nm, showed an enhancement in boron dopant concentration as shown in SIMS profile in Figure 2.6. Integration with copolymer resulted in ultra-shallow junction of 50 nm with high dopant concentrations of $1 \times 10^{20} \text{ cm}^{-3}$.

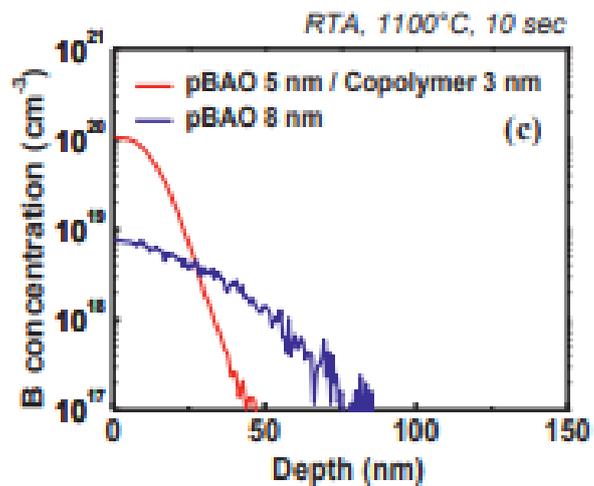


Figure 2.6 SIMS profile for integrated copolymer versus polymer [21]
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3. Mono Layer Doping Process

The main step for the formation of monolayer doping is selection of the dopant containing compound among the available compounds. The dopant containing compound must be capable of forming chemical bonds with the hydrogenated silicon bonds to form self-assembled monolayers. To form self-limiting monolayers containing phosphorus, n-type dopant compounds such as diethyl-vinyl phosphonate (DVP) and diethyl 1-propylphosphonate (DPP) are explored in this work. Dopant dose depends on the density of formed monolayers, which depends on the footprint of the dopant containing compound.

Diethyl-vinyl phosphonate (DVP) and diethyl 1-propylphosphonate (DPP) have footprints of 0.1 nm [3] having similar compound structure differing by one functional group.

This section elaborates on the process of formation of hydrogenated silicon bonds, formation of monolayers and the MLD process for creation of ultra-shallow junctions.

3.1.Preparation of Solution

The first step in the monolayer formation is the preparation of monolayer solution. An argon filled glove bag is used as the deoxygenated chamber to mix the chemical solutions. The necessary supplies such as dopant containing compound, solvent, graduated cylinder, parafilm, Erlenmeyer flask and pipettes are set down in the glove bag prior to sealing it. In order to ensure a completely deoxygenated chamber, inert gas such as argon is filled in the glove bag followed by evacuating it using vacuum. This process step is performed three times. Finally, the glove bag is filled with argon and sealed with all the necessary supplies.

Erlenmeyer flask is used to mix the dopant containing compound with the solvent in a 1:25 volume to volume ratio. DVP or DPP can be used as the dopant containing compound and mesitylene is used as the solvent. The solution is prepared in the deoxygenated chamber as the

dopant compound can catch fire in presence of oxygen in ambient air. After the preparation of solution, the solution is removed from the bag and is sparged for 15 minutes with argon to ensure deoxygenated solution.

3.2. Formation of hydrogenated silicon bonds

In this work, n-type MOSFETs are fabricated on a 650-700 μm thick 6" p-type silicon wafers with resistivity of 10-40 ohms. The hydrogenated silicon bonds are formed on bare silicon wafers by immersing the wafer in a 10:1 solution of buffered oxide etch (BOE). Buffered oxide etch is a mixture of 40% ammonium fluoride to 49% hydrofluoric acid.

The wafers are immersed in the BOE for 15 seconds followed by a rinse in deionized (DI) water for 5 minutes to ensure the HF acid from the wafer is completely removed. The wafer is then dried in spin-rinse-dryer, placed in a wafer carrier and carried to the chemistry lab for the monolayer formation.

3.3. Formation of self-assembled monolayers

The monolayers are formed in a deoxygenated reaction chamber with continuous argon inflow and outflow, that evenly transfers heat across the chamber, condenses the monolayer solution internally, has the capability to completely immerse the wafer in the solution for uniform formation of self-assembled monolayers.

The reaction chamber setup is illustrated in Figure 3.1. The stainless-steel vessel is the reaction chamber with a lid consisting of two holes. One hole is connected to an argon inlet pipe and the other to the argon outlet pipe. To transfer heat evenly across the reaction chamber, a layer of sand is placed in the vessel. Two Pyrex dishes are used, one with a slanted slope to completely immerse the wafer in the solution and the other Pyrex dish used as the lid. During

the reaction mechanism, the solution tends to evaporate and condenses on the sidewalls which are collected back in the slanted Pyrex dish and the mechanism continues.

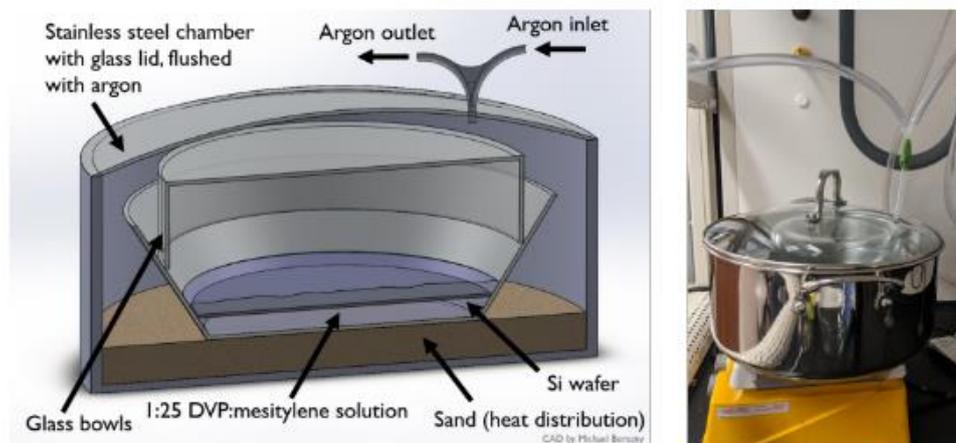


Figure 3.1 Illustration of the reaction chamber

The temperature of the reaction chamber is set to 120 °C. Once the temperature readout is 120 °C, the solution is poured in the Pyrex dish, and the wafer with the hydrogen terminated bonds is immersed in the dish. The reaction chamber is closed with the lid and the argon is flowed continuously across the chamber through the inlet for 2 hours for the monolayer reaction leading to formation of self-assembled Phosphorus monolayers.

Following the 2 hours, monolayer reaction time, the wafer is removed from the Pyrex dish and is rinsed with three different solvents with increasing polarity to rinse any unwanted unreacted solution from the wafer surface. The wafer is first rinsed with toluene, followed by acetone, methanol and finally rinsed with deionized water.

3.4. Protection of monolayers and dopant diffusion process

The self-assembled monolayers are formed from the dopant containing compound which is a mixture of atoms such as carbon, oxygen, hydrogen and dopant atom. These atoms easily decompose during the high temperature annealing step. Hence, a capping oxide is deposited on the monolayer to protect them. A 50 nm silicon-di-oxide film is deposited via the plasma enhanced chemical vapour deposition step.

After the deposition of the capping oxide layer, the wafer is processed through a rapid thermal processor to anneal, diffuse and drive-in the dopants. The wafer is annealed at 1100 °C for 50 seconds in nitrogen ambient.

The 50 nm capping oxide layer is further etched in the 10:1 buffered oxide etch solution for 15 seconds.

4. Evaluation of Monolayer Doping

To analyze the effectiveness and efficiency of Monolayer Doping at R.I.T, various experiments were conducted and studied. The first experiment involved improving the MLD chamber, reactions and RTA process conditions. The second experiment involved performing monolayer doping on various substrates such as Silicon and Silicon-On-Insulator pieces. Dynamic Secondary Ion Mass Spectrometry (SIMS) analyses are performed on SOI pieces by analysing the secondary ions emitted from the SOI pieces upon bombardment with primary ions. SIMS analysis is beneficial in providing information about the elemental and molecular composition of the uppermost SOI layers. Additionally, the analysis can provide bulk-composition and in-depth classification of the trace elements of the SOI doped piece.

4.1. Studies to improve MLD process conditions

Annealing time and temperature play an important role in the process conditions for Monolayer doping. To quantify the time and temperature conditions required to obtain low sheet resistance suitable for fabricating shallow junction transistors, experiments were performed on silicon pieces at varying time and temperatures. In the first experiment, 3 identical sized silicon pieces were placed in the MLD chamber used for doping 4" and 6" silicon wafers. The silicon samples were doped in the MLD chamber using Diethyl 1-propylphosphonate (DPP). The samples were capped with 50nm of TEOS oxide to protect the monolayer. The samples were annealed at three different temperature conditions of 1000 °C, 1050 °C and 1100 °C at a constant time of 300 seconds. The oxide was etched in the HF bath and the sheet resistance was measured using the ResMap. The results of the experiment are tabulated in table 4.1.

Annealing Temperature (°C)	Sheet Resistance (Ω/sq.)
1000	2083
1050	1485
1100	1176

Table 4.1 Results shows sheet resistance for various annealing temperatures

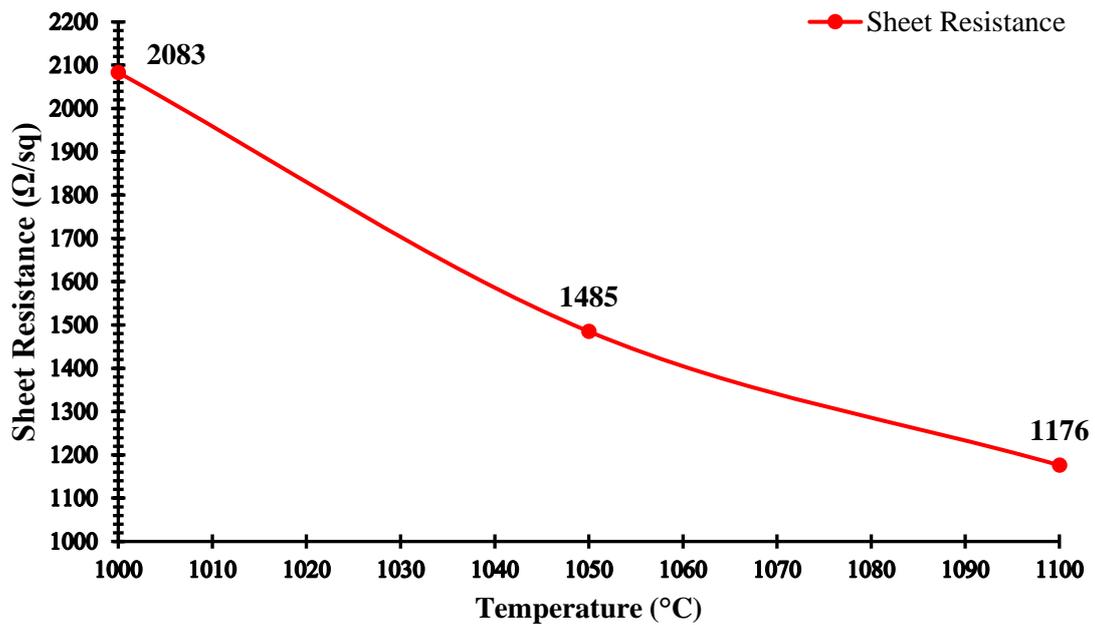


Figure 4.1 Plot illustrating sheet resistance versus temperature

From the results, it is evident that as the temperature increases the sheet resistance decreases, resulting in diffusion of more dopants increasing the dopant concentrations in the samples. As the melting temperature of silicon is 1400 °C, from the results of experiment, it can be concluded that 1100 °C can be used for doping the silicon samples.

In the second part of the experiment variation of time on the single-MLD as well as double-MLD process was studied. In a single-MLD the process of doping, depositing oxide layer, annealing and etching the oxide is performed once, whereas in double-MLD the process is performed twice, as double-MLD increases the dose of dopant by double lowering the sheet

resistance. For this experiment, 4 identical sized silicon pieces were placed in the MLD chamber used for doping 4” and 6” silicon wafers. The silicon samples were doped in the MLD chamber using Diethyl 1-propylphosphonate (DPP). The samples were capped with 50 nm of TEOS oxide and annealed at 1100 °C for varying time intervals of 50 seconds, 100 seconds, 150 seconds and 200 seconds. The oxide was etched in the HF bath followed by measuring the sheet resistance using the ResMap. The experiment results are tabulated in table 4.2.

Time (Secs)	MLD1	MLD2
	Sheet Resistance ($\Omega/\text{sq.}$)	
50	585	1120
100	788	1081
150	520	1044
200	460	896

Table 4.2 Results shows sheet resistance for various annealing time

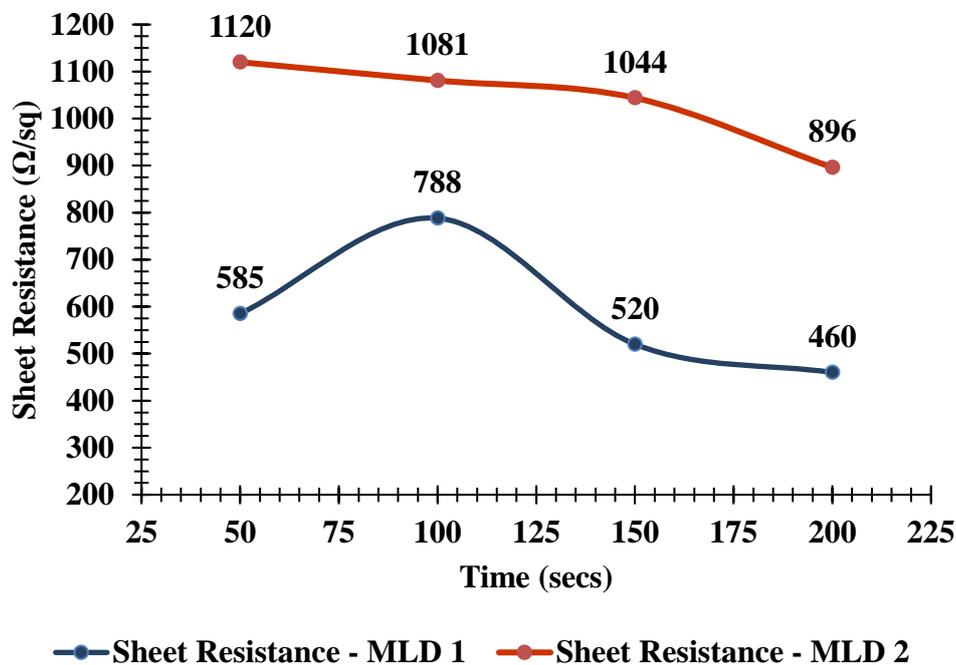


Figure 4.2 Plot illustrating sheet resistance versus annealing time

The experiment concludes two facts about sheet resistance. A correlation can be observed in the sheet resistance and the number of MLDs performed. By performing double-MLD, double the amount of dopant dose was introduced in the sample resulting in reducing the sheet resistance by half after the double-MLD process and can be confirmed across various time intervals. Secondly, as the time interval increases, the sheet resistance decreases, since ample time is given for the dopants to diffuse and increase the dopant concentration. To adhere to the industry standards, the lower the time used for annealing the semiconductor materials the better it is for the process controllability, hence the silicon samples were annealed at 50 seconds.

There is an irregularity observed in the sheet resistance for annealing time of 100 seconds post MLD2. The sheet resistance was measured for small sized silicon piece approximately 2" in size using ResMap. The probe of the ResMap has a tip radius of 40 μm with a spacing of 1mm and uses a force of 100 g. The ResMap is used to measure various film, hence there may be chances of mismeasurement and can be neglected for analysis.

4.2.Doping SOI

A smart cut 8" SOI wafer obtained from IBM was broken into many pieces to conduct the experiment. In the fabrication of smart-cut SOI wafer, a bare silicon wafer is oxidized, followed by a heavy-dose hydrogen ion implantation. The hydrogen implant peak should be at a depth between the final desired SOI thickness and below the oxidized silicon surface. This implanted wafer is bonded with another silicon oxidized wafer. A low-temperature annealing is performed resulting in the formation of hydrogen bubbles separating the top silicon layer at this location. Finally, to improve the bond between the two silicon layers, a high temperature annealing is performed.

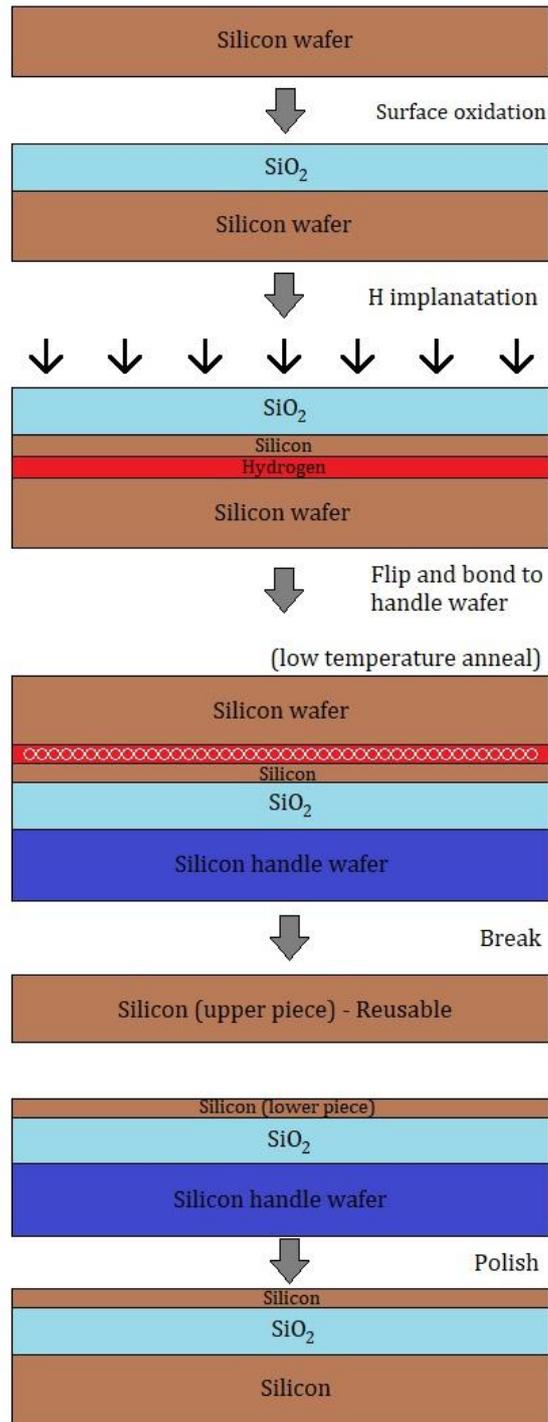


Figure 4.3 Smart-Cut SOI process [22]

The SOI had a 145 nm thick undoped buried oxide layer and a 55 nm top silicon insulating layer. The silicon insulating layer measured a resistivity 10 Ω -cm and was p-type boron doped

with a concentration of $1 \times 10^{15} \text{ cm}^{-3}$. The measured sheet resistance of the SOI piece before MLD was measured and showed a very high value.

The theoretical initial calculated sheet resistance of the SOI piece is very high, shown in equation in 4.1

$$R_S = \frac{\text{Resistivity}}{\text{Thickness}} = \frac{\rho}{t} = \frac{10 \Omega \text{cm}}{55 \times 10^{-7} \text{cm}} = \text{very high} \quad (4.1)$$

The sheet resistance was measured using the automated CDE Res Map available at R.I.T SMFL, which is capable of measuring resistivity across pieces as well as wafers.

The doping of SOI pieces involved two parts. In the first part, the SOI pieces were immersed in the MLD bath for 2 hours, followed by Rapid thermal annealing at $1100 \text{ }^\circ\text{C}$ for 300 seconds. The sheet resistance after the first MLD was $1600 \text{ } \Omega/\text{sq}$. In the second part, the same piece was immersed in the MLD bath for 2 hours. A 50 nm thickness capping oxide was deposited on the SOI piece to protect the MLD layer. To diffuse the dopants in the SOI piece, a rapid thermal annealing was performed at $1100 \text{ }^\circ\text{C}$ for 300 seconds. The final sheet resistance was measured to be $996.9 \text{ } \Omega/\text{sq}$.

SIMS analysis was performed on this SOI piece at IBM T.J. Watson, NY. The phosphorus doping concentration versus the depth in SOI is plotted in Figure 5.2. The plot verifies the presence of the electrical active dopants after 5 nm into the top silicon insulating layer.

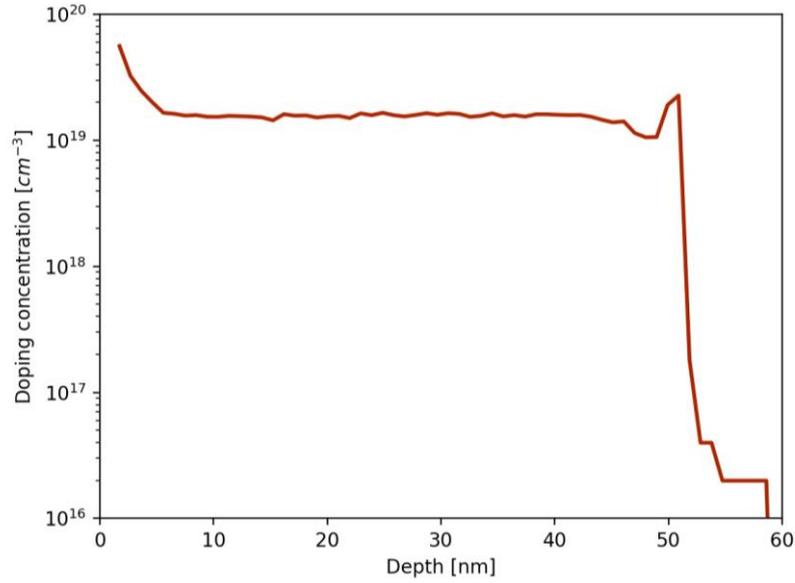


Figure 4.4 Smart-Cut SOI process

The plot shows a sharp decrease in the phosphorus dopant concentration near the silicon surface which is an artefact of the SIMS measurement and are considered as invalid measurement data points. A mean phosphorus doping of $1.6 \times 10^{19} \text{ cm}^{-3}$ is obtained. The spike observed near the interface of the top silicon insulating layer and the buried oxide layer is due to dopant trapping due to the slower diffusion rate of phosphorus in buried silicon-dioxide compared to the diffusion rate in silicon. The SIMS profile also displays the kink effect, the rapid decrease in the high surface concentration due to the dissociation of phosphorus and vacancy pair.

The measured phosphorus doping is $1.6 \times 10^{19} \text{ cm}^{-3}$. The N-type resistivity is $4.06 \times 10^{-3} \Omega \text{ cm}$.

The calculated sheet resistance assuming all the dopants are ionized is $727 \Omega/\text{sq}$. as shown in equation 4.2

$$R_s = \frac{\text{Resistivity}}{\text{Thickness}} = \frac{\rho}{t} = \frac{4.06 \times 10^{-3} \Omega \text{ cm}}{55 \times 10^{-7} \text{ cm}} = 727 \Omega/\text{sq} \quad (4.2)$$

The dose after double MLD can be calculated by multiplying the phosphorus doping after MLD with the thickness of the top silicon insulating layer, which is as shown in equation 4.3.

$$\text{Dose after double MLD} = 1.6 \times 10^{19} \text{ cm}^{-3} \times 55 \times 10^{-7} \text{ cm} \quad (4.3)$$

$$\text{Dose after double MLD} = 8.8 \times 10^{13} \text{ cm}^{-2}$$

The maximum possible dose is $6.7 \times 10^{14} \text{ cm}^{-2}$. The packing density of 0.065 can be obtained using this MLD process in a smart-cut SOI piece and can be calculated as shown in equation 4.4.

$$\text{Packing density} = \frac{\text{Double dose after MLD}}{2 \times \text{Maximum possible dose}} \quad (4.4)$$

$$\text{Packing density} = \frac{8.8 \times 10^{13} \text{ cm}^{-2}}{2 \times 6.7 \times 10^{14} \text{ cm}^{-2}}$$

The packing density defines the number of bonds formed out of 100 bonds. Thus, 6-7 bonds out of 100 bonds can be formed using the above MLD process.

5. Fabrication Process for Recessed Channel MOSFETs

Recessed Channel MOSFETs can provide low on-resistance due to the absence of pinching resistance present in planar MOSFETs and increased cell packaging densities in comparison to planar MOSFETs. The main difference between the planar MOSFET and the Recessed Channel MOSFET is the trench etched in the silicon substrate to isolate the source and drain of the MOSFETs creating the gate region using the advanced microelectronics fabrication methodologies such as dry-etch or ion-milling. The challenging part about the fabrication process is the creation of smooth textured trenches in the substrate. Dry etch as well as focus ion beam milling may lead to surface roughness affecting the electron mobility. Studies conducted by Kuribayashi H. et al. [23] indicated annealing in H₂ atmosphere results in smooth surfaced silicon trenches.

The performance of Recessed Channel MOSFETs depends heavily on the quality and smoothness of etched trench in the silicon substrate and the quality of insulating gate oxide deposited in the trench that ensures high breakdown voltage.

The key factors influencing the fabrication of a successful Monolayer doped Recessed Channel MOSFETs are formation of smooth even surfaced silicon trenches, stable and healthy monolayer doping process conditions, extension of deposited gate oxide over the doped regions, adhering to the thermal budgets and reducing the possibility of junction spiking at the contacts.

5.1. Recessed Channel FET Mask Design

The masks for the fabrication of Recessed Channel MOSFETs were designed and taped out at R.I.T SMFL. Mentor Graphics Pyxis software was used to design the mask layout and then fabricated using Heidelberg DWL 66 Laser Writer.

The mask consisted of 4 layers. First layer will define the source, gate and drain regions by patterning the field oxide. Second layer will define the trench gate region. Third layer will define the contact cut regions and fourth layer will define the electrical connections by patterning the deposited metal.

A mask designed to fabricate the devices needs to meet the requirements of circuit designers as well as process engineers. Circuit designers require tighter, high performance smaller designs whereas process engineers require manufacturable, reproducible high yield processes. Following the basics of design rules enables one to resolve tighter smallest features using advanced lithography and etch processes. For this thesis work, lambda (λ) based design rules are followed. In lambda-based design rules, lambda describes the minimum allowable feature size with other features scaled in terms of lambda. The Recessed Channel MOSFET mask is designed using the following design rules:

1. The contact cuts are drawn by a λ by λ .
2. The contact cuts are placed at λ .
3. The distance between the contact cuts and edges of source and drain regions are a λ .
4. The metal lines are separated by λ .
5. The metal lines extend over the contact cuts by λ and over source and drain regions by λ .
6. The active area mask will not go beyond the source and drain regions.

The above design rules are demonstrated in Figure 5.1 in the mask design of a Recessed Channel MOSFET transistor.

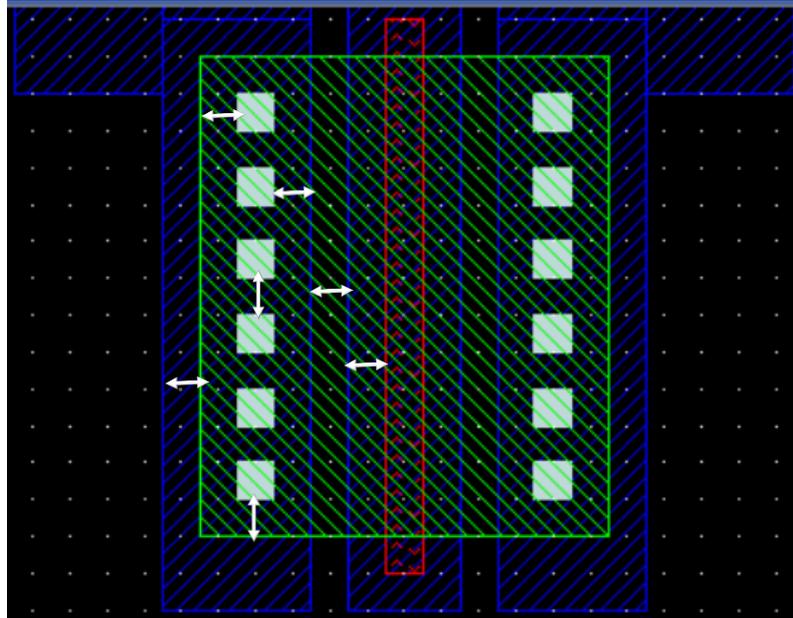


Figure 5.1 Mask Design for Recessed Channel MOSFET

The first layer defining source and drain are indicated by the green region, second layer defining the active i.e., gate region is indicated by the red region, the third layer defining the contact cuts are indicated by the white colour and the fourth layer defining the metal aluminium region are indicated by the blue coloured region.

The field type of design layers defining the diffusion layer, gate region and the contact cuts are dark field type, which means the features or the pattern on the masks are surrounded by the chrome/opaque region. Whereas, the field type of the design layer defining the metal regions are clear field type, which means the features or the pattern on the masks are made up of chrome/opaque region.

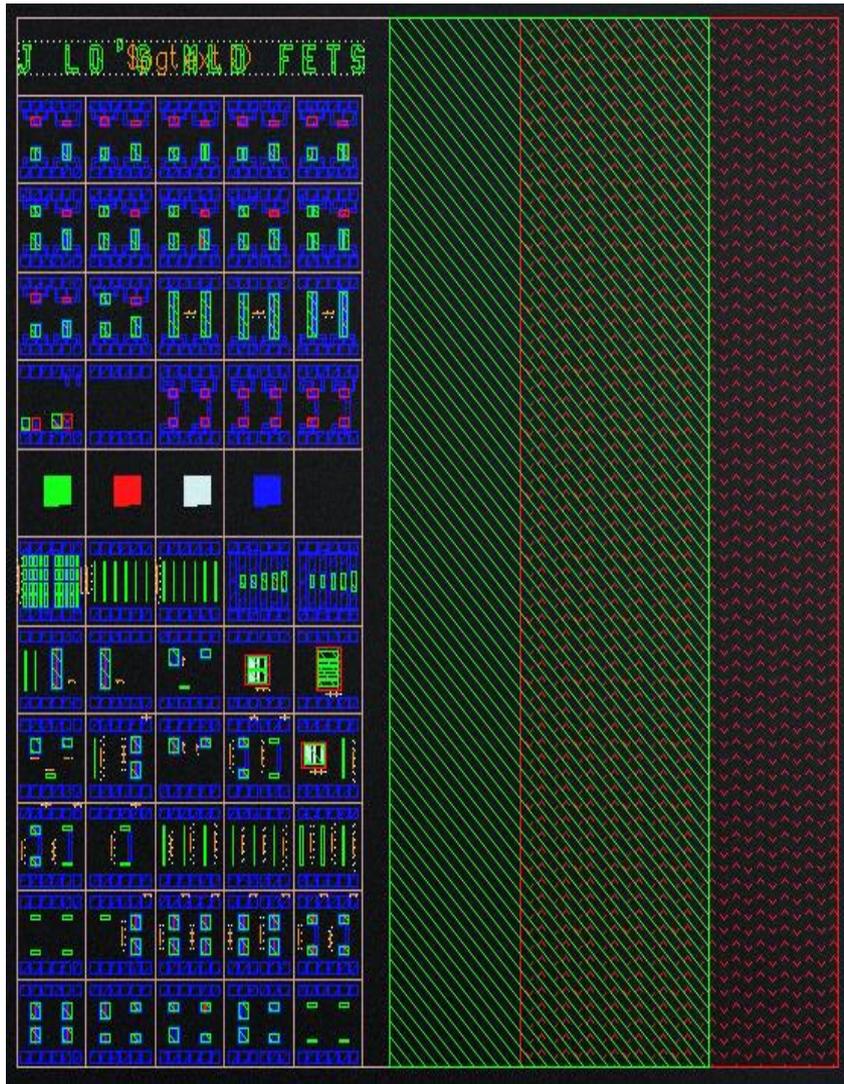
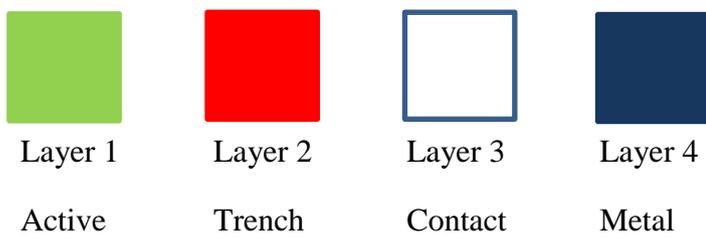


Figure 5.2 Entire Mask Design



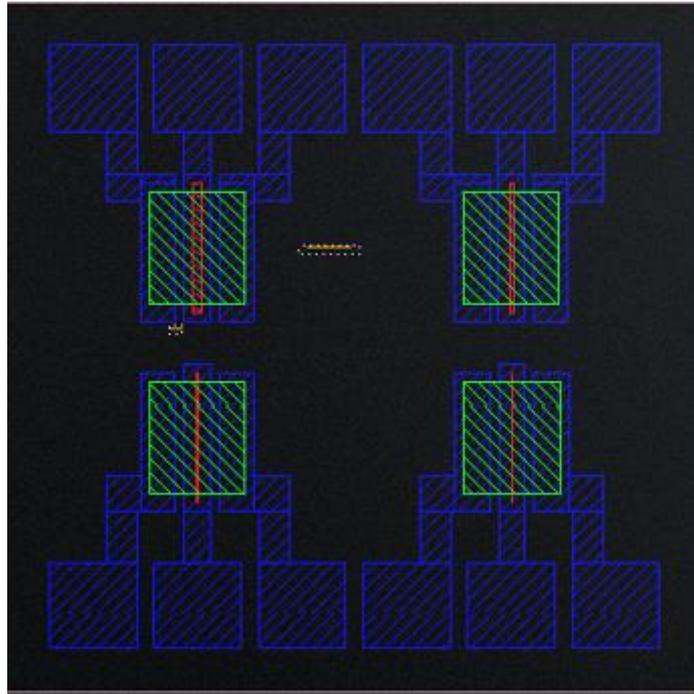


Figure 5.3 One field of the mask

In this mask design, the λ is chosen to be $10\ \mu\text{m}$. The gate length is not defined by λ , hence in this work Recessed Channel FET transistors with varying gate lengths such as $1, 2, 5$ and $10\ \mu\text{m}$ and varying widths such as $30, 70$ and $130\ \mu\text{m}$ are fabricated. If there are error in design rules, the device will fail. Contacts should be completely covered by metal. Depending on the alignment sequence to avoid misalignment, the contact must be at a minimum of λ from the doped source/drain region.

The entire mask design can be divided into two designs. The top portion of the design consists of standard planar MOSFETs, whereas the bottom portion of the design consists of Recessed Channel MOSFETs.

5.2. Fabrication Process Flow for Recessed Channel MOSFET

In this work, the process flow followed to fabricate n-type MOSFETs at SMFL R.I.T is briefly described. The final cross-section of the Recessed Channel MOSFET is described in the figure 5.13 and the fabrication process flow is illustrated from figure 5.4 to figure 5.8.



Figure 5.4 (a) p-Si with patterned Field Oxide (b) MLD



Figure 5.5 (c) PECVD Capping Oxide (d) Rapid Thermal Annealing



Figure 5.6 (e) Active area etch and deposition of Nickel (f) Formation of Nickel Silicide



Figure 5.7 (g) Formation of V Shaped Recessed Channel (h) Deposition of PECVD Gate oxide



Figure 5.8 (i) Formation of Contact Cuts (j) Deposition and patterning of Aluminium metal

NMOSFETs are fabricated on a p-type 6" <100> oriented silicon wafer with resistivity of 4-6 Ω -cm. RCA clean is performed on the wafers to decontaminate the wafers. RCA method is performed to chemically clean the surface of the wafer with a series of acid and rise baths. In the process, organic contaminants are first removed followed by removal of inorganic and metal contaminants. The RCA clean consists of Standard Clean 1 bath (SC1), a Hydrofluoric acid dip, and a Standard Clean 2 bath (SC2). The SC1 contains ammonium hydroxide and hydrogen peroxide. The SC2 contains hydrochloric acid and hydrogen peroxide. Hydrogen peroxide reacts with the exposed silicon wafer forming a chemically grown oxide that protects the wafer from being etched in the strong acid or base. The ratio of water, hydrogen peroxide and ammonium peroxide or hydrochloric acid is 15:3:1.

After the clean procedure, silicon alignment marks need to be etched into the silicon wafers to be used by the stepper to align between various mask layers. The alignment marks are etched using the DryTek Quad tool. The wafers are cleaned again post the resist strip process to remove all the resist residues. A thick 5000 Å of silicon-dioxide is thermally grown on the wafers forming the field oxide. The purpose of the field oxide is to electrically isolate the devices fabricated on the wafer. The field oxide is thermally grown using the Bruce furnace tube 1. The thermal oxide is patterned and etched using 10:1 BOE buffered oxide etch for 10 minutes, with a etch rate of 586 Å/min, to expose the source, gate and drain regions.

The wafers are then doped using the Monolayer doping process. The solution used for doping is DPP. The wafers are immersed in the doping solution for 2 hours 15 minutes at a temperature of 125 °C. The wafers are then deposited with capping oxide of thickness 50 nm using P5000 tool used to protect the dopant layers formed on the wafers. Rapid thermal annealing is performed on the wafers using the RTP chamber to diffuse the dopants into the wafer forming the source and drain regions. The RTP is performed at 1000 °C for 300 seconds. The capping oxide are etched in the 10:1 BOE for 20 seconds. A second MLD is performed the wafer using the same procedure and MLD conditions.

A thin layer of 7nm Nickel is deposited on the wafers using PE4400 tool. Rapid thermal annealing is performed on the wafers with the deposited nickel to form a 15 nm layer of Nickel Silicide. The RTP is performed at 550 °C for 30 seconds in the RTP chamber. The deposition of nickel can be confirmed by the formation of yellow stripes on the wafer confirming the formation of nickel silicide. Nickel silicide is formed in the regions with nickel in contact with silicon, that is, the source and drain regions with the possibility of junction spiking. Junction spiking occurs when silicon from the source and drain regions are diffused into the deposited aluminium metal in the contact regions at high temperature processes. Due to this process,

voids are formed in the silicon which are filled with aluminium causing junction spiking. Devices with junction spiking are not reliable devices as the spikes can result in shorting the junctions or causing excess device leakages. Hence, a barrier metal can be deposited in the contact regions, where the metal is directly deposited over the bare silicon to avoid junction spiking. Nickel has been used in the work due to its various advantages such as low silicon consumption, being able to process at low temperatures.

The unreacted nickel is etched using the Piranha solution. A piranha solution is a 2:1 ratio of sulphuric acid H_2SO_4 to hydrogen peroxide H_2O_2 . In this work, 300 mL of H_2SO_4 to 150 mL of H_2O_2 is used. The wafers are immersed in the piranha bath at 85-90 °C for 5 minutes.

To form the Recessed Channels defining the gate regions, trenches of depth 200 nm are to be etched in the silicon dividing the source and drain region forming the gate region. The trenches were formed using ion-milling at Veeco instruments company.

The wafers are cleaned using RCA before the deposition of gate oxide to have a clean decontaminated surface. The thin gate oxide of 30 nm is deposited using P5000 tool. The wafers are in the deposition chamber of 3 seconds at very low temperature following to the no high temperature process post the monolayer doping. The gate oxide is densified using the Bruce Furnace Tube 4. The gate oxide is densified to remove any trapped charges in the film improving the electrical characteristics of the gate oxide.

The gate oxide is patterned and etched to form contact cuts of the MOSFET. The wafers are cleaned again using the RCA before the deposition of aluminium. Aluminium of 3000 Å is sputter deposited on the wafers using the CVC 601 Sputter tool. The metal is patterned and etched forming the metal regions. The wafers are loaded into the Bruce Furnace to sinter the aluminium metal lines at a temperature of 400 °C in the presence of forming gas. Sintering is performed to improve the aluminium to silicon contact and to reduce any interface charges.

6. Recessed Channel MOSFETs Device Performance Results

6.1. Electrical Analysis of Recessed Channel MOSFETs

The Recessed Channel MOSFETs fabricated in this work are electrically tested to verify its device performance capabilities. The MOSFETs are tested using HP4145 parametric analyser at the Testing Lab at R.I.T. The electrical data obtained from the analyzer are used to plot various device characteristics.

6.1.1. Transfer Characteristics of Recessed Channel MOSFET

Transfer characteristics plots the response of drain current I_D to the gate to source voltage V_{GS} . As the gate of the device is electrically isolated, the gate current, I_G is ideally zero and hence is not considered as part of the device characteristics. To find the field-effect behaviour of the fabricated Recessed Channel MOSFET, the source voltage of the device is set to ground indicating zero voltage, the drain voltage of the device is set to a high voltage of 5 V sweeping the gate voltage and measuring the drain current for a range of gate voltages. The transfer characteristics should ideally show a very low current for gate voltages less than the threshold voltage, while increasing exponentially for gate voltages more than threshold voltage of the device.

The figure 6.1. shows transfer characteristics for the Recessed Channel MOSFET with a gate length of 10 μm and the gate width of 130 μm plotted at low drain voltage of 0.1 V. The characteristics is plotted on both log and linear scale.

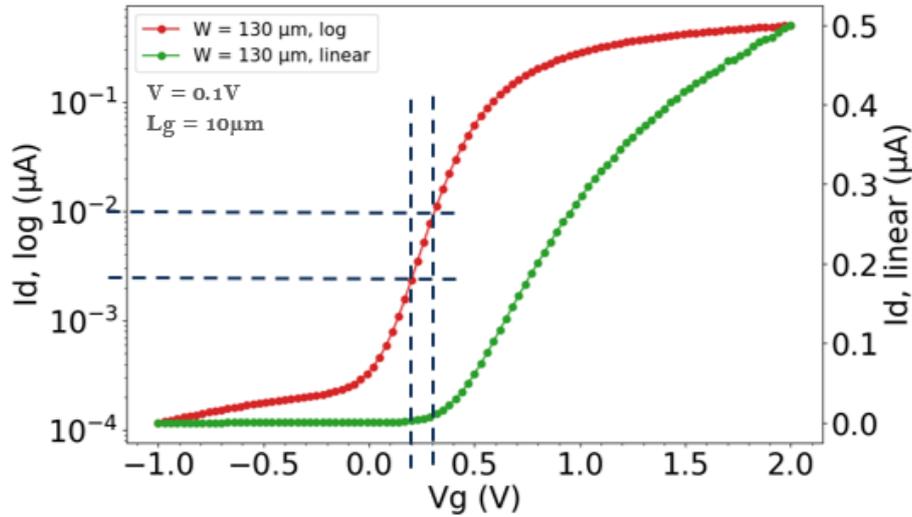


Figure 6.1 Transfer characteristics at low drain voltage for 10 μm device

From the transfer characteristics of the MOSFET, the subthreshold slope is calculated as 117.7 mV/dec. The device shows a very low ratio of on current to off current of approximately 3 orders of magnitude. Subthreshold slope is an important parameter of a MOSFET as it relates to the change in voltage required to bring an effective in drain current by a certain ratio. A device with low subthreshold slope will have high on/off ratio indicating an equivalent difference in V_{GS} decreases the drain current by more orders of decades and requiring low gate voltage to turn on the device. A device with high subthreshold slope will show low on current to off current ratio and high gate voltage to turn on the device which can be observed from the results of the fabricated device.

In this work of fabricating recessed channel MOSFETs, recessed channels are etched to define sharp V-trench recessed channels. The sharp edges of these V-recessed channels accumulate and attract high electric fields. The gate oxide is deposited along these V-recessed channels. Thus, due to high electric field at high operating temperatures, there is a tendency of the atomic bonds between Silicon and silicon dioxide surface to break down and introduce oxide charges. These oxide charges will result in threshold voltage shift.

The subthreshold slope of the device is extracted from the linear portion of the log scale of the transfer characteristics and is calculated as shown in equation 6.1,

$$\text{Sub threshold slope} = 1000x \frac{(0.2 - 0.3)}{(-2.85) - (-2.0)} = \frac{117.7mV}{\text{dec}} \quad (6.1)$$

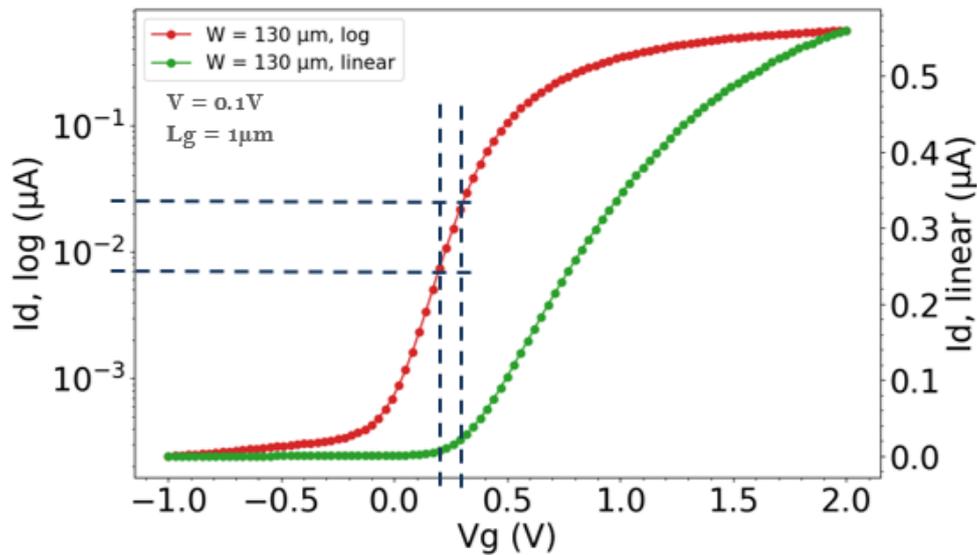


Figure 6.2 Transfer characteristics at low drain voltage for 1 μm device

Recessed Channel MOSFETs as small as gate lengths measuring 0.5 μm, 1 μm and 2 μm were also fabricated. The smallest working MOSFET fabricated in this work measured a gate length of 1 μm. Hence, it is proved that Recessed channel MOSFETs of gate lengths as small as 1 μm can be successfully fabricated using Monolayer Doping.

The transfer characteristics of recessed channel MOSFET for a gate length of 1 μm are plotted in figure 6.2. From the transfer characteristics, it is observed that the device has a threshold voltage of 0.15 V with a subthreshold slope of 166 mV/dec. The subthreshold slope exponentially raises with the increase in gate to source voltage V_{GS} .

The subthreshold slope of the 10 μm is greater than the subthreshold slope of the 1 μm device, which indicates that the 10 μm recessed channel MOSFET has better turn-on characteristics

and will perform better. Subthreshold slope depends on various parameters such as substrate doping, gate oxide thickness, temperature and substrate biasing. Low values of subthreshold slopes can be obtained by reducing the gate oxide thickness and increasing the substrate biasing. A higher subthreshold slope is resulted by increased substrate doping and operation temperature. By reducing the substrate doping a thick region of depletion layer can be obtained reducing the depletion capacitance resulting in a reduced subthreshold slope.

The 1 μm device shows high subthreshold slope which may be due to the heat dissipation nature of the device, resulting in the operation of the device at a high temperature environment. The other parameters such as substrate doping, gate oxide thickness and substrate biasing are kept constant for all the fabricated Recessed Channel MOSFETs. Thus, 10 μm device shows a reduced I_{OFF} due to smaller subthreshold slope.

The linear scale characteristics confirms that the fabricated Trench MOSFET shows field-effect behaviour. The threshold voltage of the device is 0.2 V, which is extracted from the linear scale of the characteristics. The threshold voltage is the value when the device starts conducting and flowing current across the channel and can be calculated theoretically using equation 6.2.

$$V_{th} = V_{FB} + 2\phi_f + \frac{qN_A x_{DT}}{C_{ox}} \quad (6.2)$$

where,

ϕ_f stands for the semiconductor potential and can be calculated using equation 6.3,

N_A stands for channel doping and n_i stands for intrinsic concentration

x_{DT} is the junction depth

C_{ox} is the gate oxide capacitance

V_{FB} stands for flat-band voltage and can be calculated using equation 6.4,

$$\phi_{Fp} = \frac{kT}{q} \cdot \ln\left(\frac{N_A}{n_i}\right) = 0.33 \text{ V} \quad (6.3)$$

$$V_{FB} = \phi_{MS} - \left(X + \frac{E_g}{2q} + \phi_{Fp}\right) = -0.94 \text{ V} \quad (6.4)$$

ϕ_{MS} is the work function of metal to semiconductor and is 4.05 V.

x_{dT} is the maximum depletion width and can be calculated using equation 6.5

$$x_{dT} = \sqrt{\frac{4\epsilon_0\epsilon_r Si \phi_{Fp}}{qN_A}} = 0.92 \mu m \quad (6.5)$$

The gate oxide capacitance can be calculated using equation 6.6,

$$C_{ox} = \frac{\epsilon_0\epsilon_r SiO_2}{t_{ox}} = 1.15 \times 10^{-7} \text{ F/cm}^2 \quad (6.6)$$

Thus, substituting all the values in equation 6.2, we obtain a value of 0.28 V for the theoretically calculated threshold voltage, as shown in equation 6.7.

$$V_{th} = -0.94 + 2(0.33) + \frac{(1 \times 10^{15} \text{ cm}^{-3})(1.6 \times 10^{-19})(.92 \times 10^{-6})}{1.15 \times 10^{-7} \text{ F/cm}^2} = 0.28 \text{ V} \quad (6.7)$$

The theoretical threshold voltage is 0.28 V, which is close to the calculated threshold voltage. Various parameters such as increased oxide-interface charges, health of the milled trench including the parameters such as the depth, roughness of the sidewalls of the trench, the steepness of V-groove and the junction depth might have affected the threshold voltage of the fabricated Recessed Channel MOSFETs.

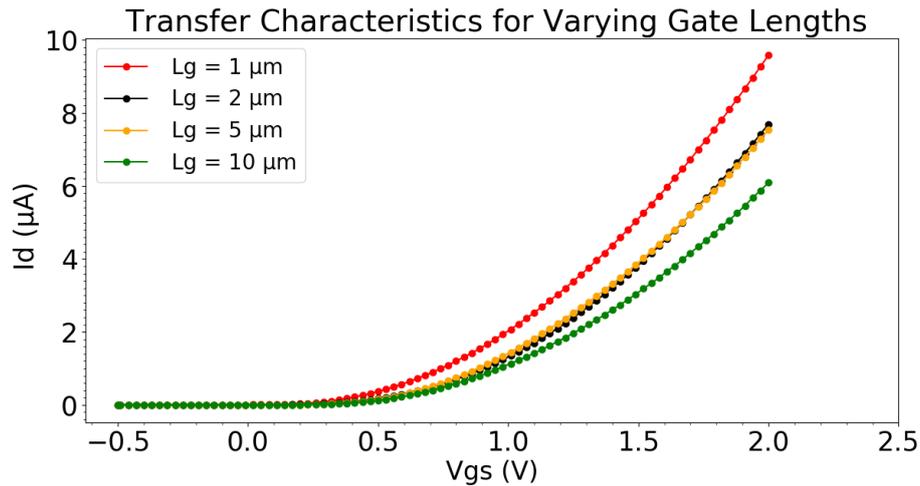


Figure 6.3 Transfer characteristics for varying lengths

The transfer characteristics plotted in the figure 6.3 represents the characteristics for transistors for a constant gate width of 130 μm versus varying gate lengths of 1 μm , 2 μm , 5 μm and 10 μm . The characteristics shows a linear scale plotted at high drain voltage.

The drain current of an NMOSFET can be described and calculated using equation 6.8. The drain current of the device is inversely proportional to the channel length, thus to obtain higher amount of current flow through the device, the channel length of the device should be decreased. This behaviour can be explicitly observed from the transfer characteristics plotted in figure 6.3. It can be observed that as the device shrinks, the amount of current the device can flow across the channels between source and drain increases prominently.

Scaling of gate lengths has an adverting effect on the threshold voltage and performance of the device. The channel depletion width decreases as the device is scaled down in size resulting in a threshold voltage needed to turn on the device. The threshold voltage of a device is directly proportional to the square root of the gate length, as shown in equation 6.8.

$$V_{th} = V_{gs} - \sqrt{\frac{2 I_{dsat} L}{\mu_n C_{ox} W}} \quad (6.8)$$

The threshold voltage of 1 μm device is 0.15 V, 2 μm device is 0.18 V, 5 μm device is 0.19 V and 10 μm is 0.2 V. Thus, threshold voltage of the device decreases as the gate length reduces as observed in the performance of different gate length fabricated Recessed channel MOSFETs. The threshold voltage of the Recessed Channel FETs for varying channel lengths does not vary similar to a planar MOSFET and are comparable to the results of the simulated Recessed Channel FETs from the literature study [19]. This is mainly due to the increased potential barrier between the source and the drain region due to the V shaped groove of the gate.

The linear mobility of the 10 μm Recessed Channel MOSFET can be calculated from the slope of the linear characteristics curve of $I_d(\mu\text{A})$ plotted against V_{gs} (V) as shown in Figure 6.4.

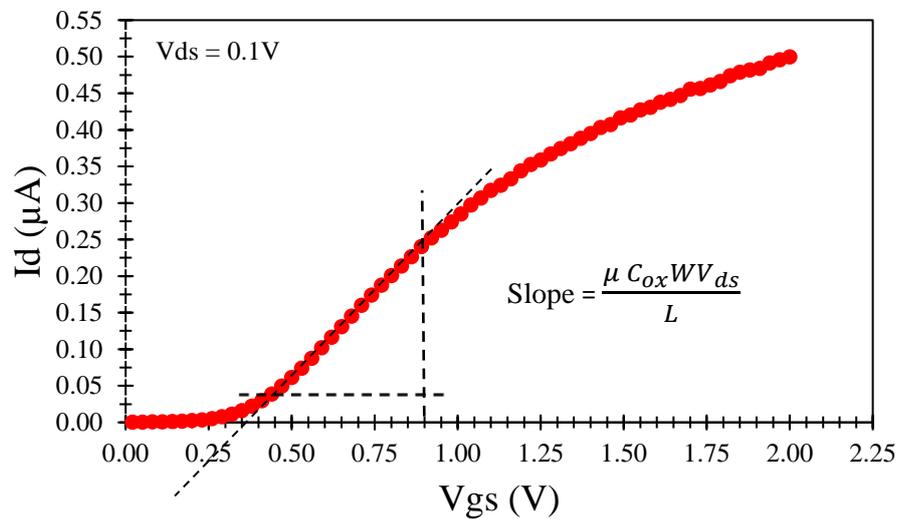


Figure 6.4 Linear Characteristics of 10 μm device

The slope of the plot is equal to 0.458 $\mu\text{A}/\text{V}$ which gives a linear mobility of 3.065 cm^2/Vs .

The saturation mobility of the 10 μm Recessed Channel MOSFET can be calculated from the slope of the saturation characteristics curve of $I_D(\mu\text{A})$ plotted against V_{GS} (V) as shown in Figure 6.5.

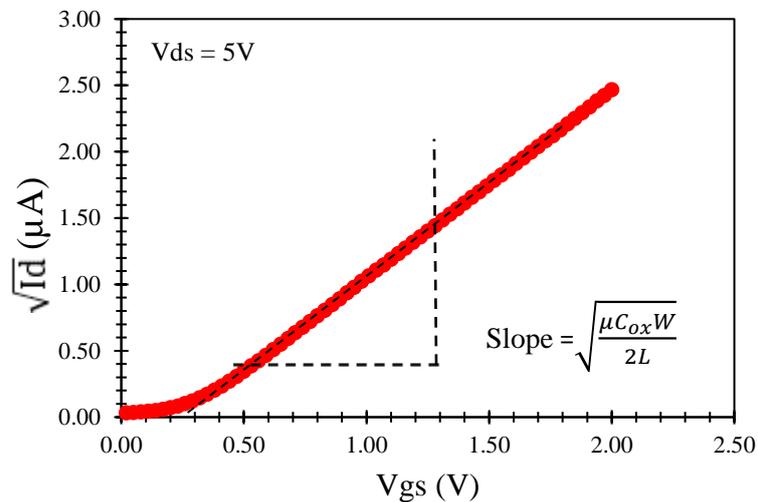


Figure 6.5 Saturation Characteristics of 10 μm device

The slope of the plot is equal to $1.43 \sqrt{\mu\text{A}}/\text{V}$ which gives a linear mobility of $2.735 \text{ cm}^2/\text{Vs}$.

6.1.2. Output Characteristics of Recessed Channel MOSFET

The characteristics of the transistor plots drain current I_D versus the drain to source voltage V_{DS} for varying gate to source voltage V_{GS} . The output characteristics for a Recessed Channel MOSFET of gate length 10 μm and a gate width of 130 μm are plotted in figure 6.6.

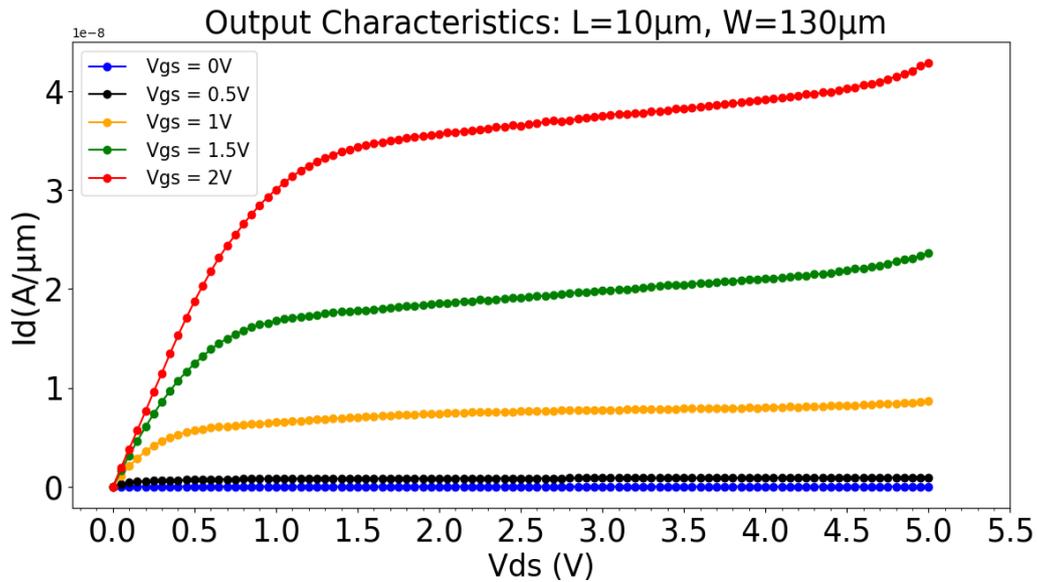


Figure 6.6 Output characteristics for 10 μm MOSFET

The characteristics clearly indicates the transistor behaviour, showing an increase in drain current with the increase in gate voltage across drain to source voltages. Channel length modulation effects are observed in the characteristics.

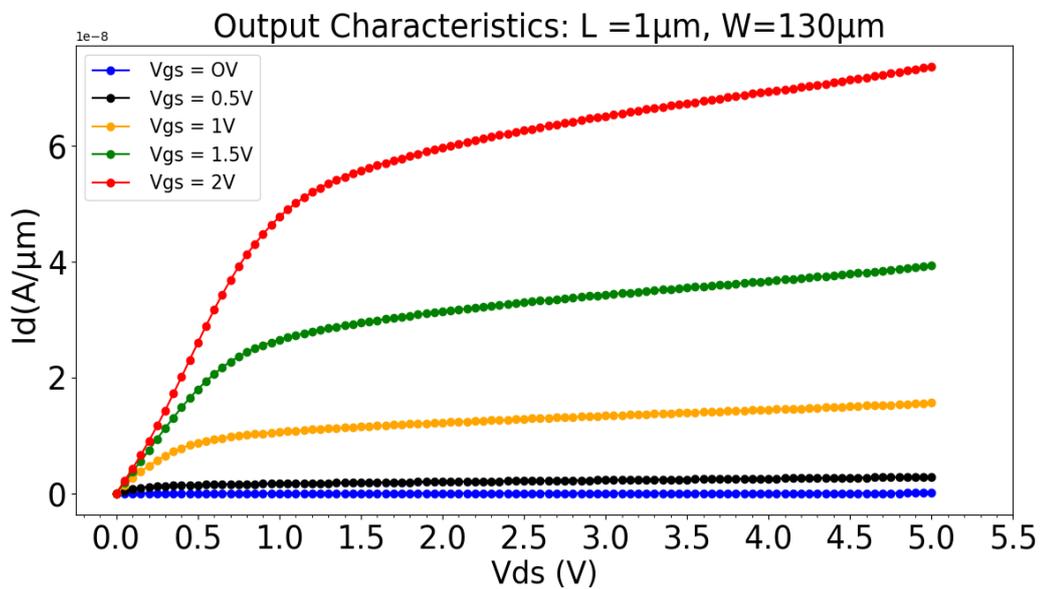


Figure 6.7 Output characteristics for 1 μm MOSFET

From the output characteristics of 1 μm MOSFET from figure 6.7, it is observed that as the drain to source voltage increases more current flows through the device at high gate voltages

in comparison to the flow of current for the 10 μm MOSFET. Whereas, an ideal short-channel device flows less amount of current. This indicates the flow of a very high leakage current through the short channel 1 μm MOSFET. These leakage currents can be a result of the roughness of the milled trench of such short dimension and the result of accumulation of high electric field at the trench.

In Recessed Channel MOSFETs, the conduction channel is formed along the sidewall of the milled V-shaped trench thus decreasing the on-state resistance increasing the carrier mobility. This profile also allows increased flow of current due to a longer channel. But, the huge disadvantage of V-shaped trench MOSFETs are the increase in the accumulation of electric-field lines around the V-milled trench, resulting in low-breakdown voltage. Hence, there is a need to smoothen the shape of the milled trench from V- shape to U-shape to spread the distribution of electric field lines evenly across the trench.

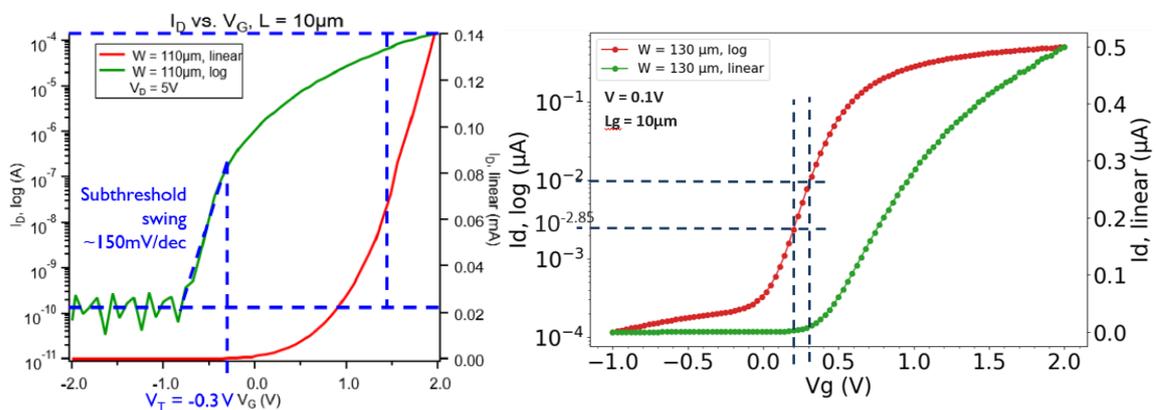


Figure 6.8 Comparison of transfer characteristics (a) MOSFET (b) Recessed channel MOSFET

Previously, at R.I.T, planar NMOSFETs were fabricated using Monolayer doping. Figure 6.8 shows the transfer characteristics of planar NMOSFETs and Recessed Channel MOSFETs. The transfer characteristics are plotted for gate length of 10 μm devices. The recessed channel MOSFET is strongly comparable to the planar NMOSFET as the subthreshold slope of planar

NMOSFET was 150 mV/dec, whereas for recessed channel MOSFET it was 117.7 mV/dec. The threshold voltage of the planar NMOSFET was -0.3 V whereas the threshold voltage of the recessed channel MOSFETs was 0.2 V. Both the devices have an on current to off current ratio in 3 orders of magnitude. Hence, recessed channel MOSFETs shows good device characteristics and performance using Monolayer doping and can be investigated further. Due to the bend nature of the groove, the saturation drain current in the Recessed Channel FETs is less than a standard MOSFET. The groove channel forms potential barrier due to high electric field at the sharp edge of groove which is enhanced as the groove radius decreases and is responsible in reducing the short channel as well punch through effects in Recessed Channel FETs which is not possible in standard MOSFET due to absence of the groove.

6.2.Device Characterization

Focused Ion beam is a characterization technique widely used in semiconductor industry as an analysis method. FIB is similar Scanning Electron Microscope, SEM but unlike SEM, FIB uses focused beam of ions to analyze the given sample. FIB can image the samples at low currents and can sputter and mill the sample at high current values.

Beam of Gallium ions are used as the primary source to target the sample to be characterized. The ion beam introduced to the surface ejects materials from the sample surface which leaves the sample as secondary ions or neutral atoms. The gallium ion beam also develops secondary electrons. This process of beam of ions hitting the sample continues till the signals from secondary ions forms an image of the sample to be analysed.

In this work, FIB analysis is carried out by deposition of tungsten material through the ion beam induced deposition method. The FIB deposition is performed in a vacuum chamber in the presence of tungsten hexacarbonyl ($W(CO)_6$), that will chemisorb on the Recessed Channel transistor samples. When an area of the sample is scanned with the beam, the precursors of

tungsten hexacarbonyl such as tungsten will be deposited on the transistor samples as non-volatile components and can be observed on the sample images.

The FIB deposition technique is advantageous as the deposited non-volatile tungsten will act as a protective sacrificial layer, protecting the underlying Recessed Channel MOSFETs from the destructive ion beam sputtering.

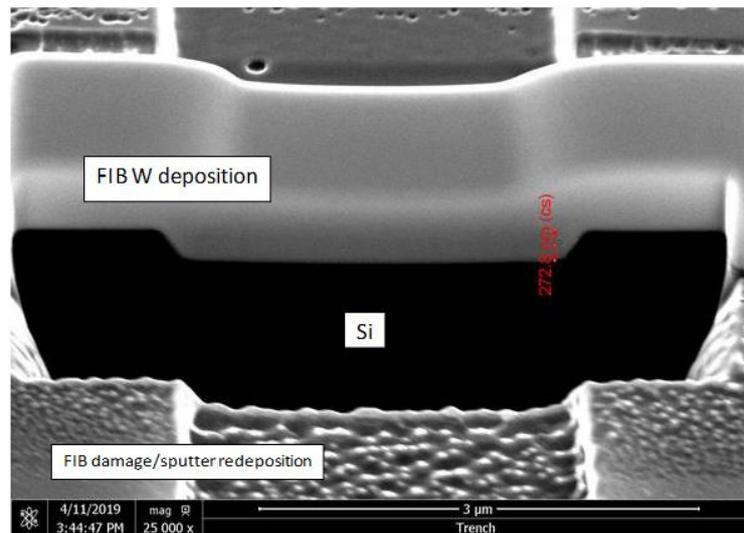


Figure 6.7 Cross-section of the Recessed Channel MOSFET

The cross-section image showed in figure 6.7 is obtained from the FIB deposition analysis. FIB analysis is performed in the presence of tungsten hexacarbonyl, which resulted in the deposition of the precursor tungsten material as a non-volatile component on the trench MOSFET, as observed in the figure 6.7.

The FIB analysis also shows a trench milled into the trench MOSFET of depth 272.8 nm, whereas, the process is designed for a trench of depth of 200 nm, which indicates that high beam currents were used, resulting in deeper trench recessed channel.

Nanovea ST400 3D Non-contact Profilometer is used to characterize and generate the 3D profile of the fabricated Recessed Channel MOSFET as shown in figure 6.8. It allows us to view the distribution of the fabricated surface and the morphology of the fabricated device from different angles. The profile gives various information including the surface depth, step height and peak of the various regions of the device. Here, the deposited aluminium metal is used as the reference layer and thus is indicated by the blue regions defining 0% depth. All the other regions are having a step height with respect to the deposited metal layer.

In the device, metal is deposited over the source, gate and the drain region excluding the contact cut region, giving an elevation to the profile in comparison to the contact cuts which is at a lower depth, and this profile is observed in the green coloured region referring to a depth in comparison to the top elevated metal. The contacts are a lower height in the device and hence is indicated by the red colour indicating the lowest depth in comparison to the metal layer.

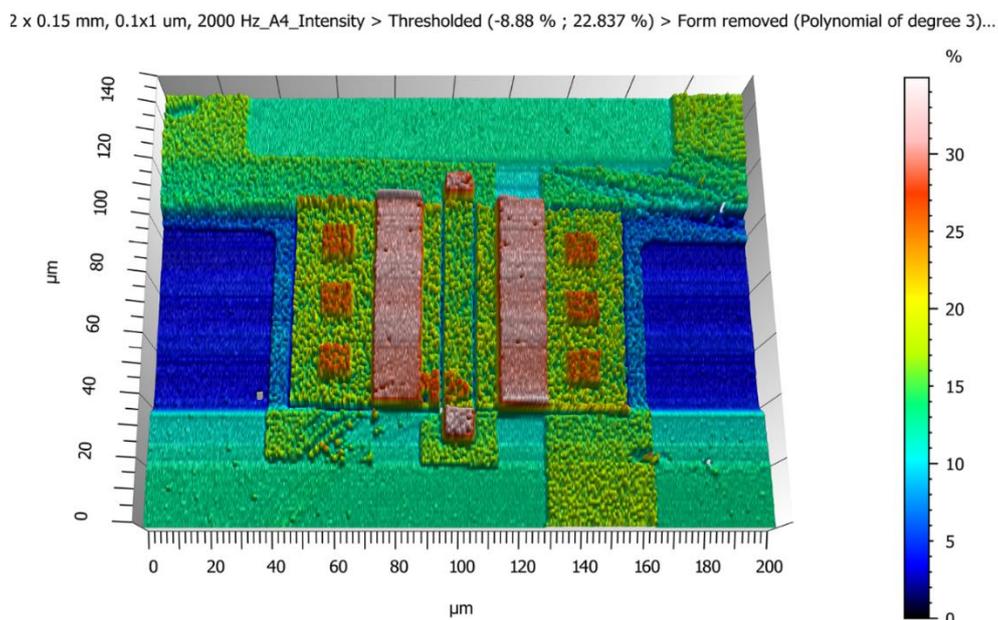


Figure 6.8 3D Profile of the fabricated Recessed channel MOSFET

The profile generated by the Profilometer can also give information on the surface roughness and the device dimensions accurately. The Trench MOSFET was fabricated based on the λ

design rule, with λ defining 10 μm . The 3D Profile is generated from a device having a gate length of 10 μm and a gate width of 70 μm . The dimensions of the contact cuts can also be verified which is equal to λ of 10 μm .

7. Conclusions and Future work

Recessed Channel MOSFETs using Monolayer Doping are successfully fabricated in this work. A gate oxide thickness of 30nm is deposited for the Recessed Channel FETs. The subthreshold slope of the fabricated device with a channel length of 10 μm is 117.7 mV/dec. The device shows a very low ratio of on current to off current of approximately 3 orders of magnitude. The measured threshold voltage of the 10 μm device is 0.2 V whereas the calculated threshold voltage is 0.28 V. High electric fields are formed along the sharp edges of these V-recessed channels. Thus, due to high electric field at high operating temperatures, there is a tendency of the atomic bonds between Silicon and silicon dioxide surface to break down and introduce oxide charges. These oxide charges have resulted in threshold voltage shift.

Various channel lengths Recessed Channel MOSFETs are fabricated and the smallest working MOSFET fabricated in this work measured a gate length of 1 μm . It is observed that the device is having a threshold voltage of 0.1 V with a subthreshold slope of 166 mV/dec.

Hence, it is proved that Recessed channel MOSFETs of gate lengths as small as 1 μm can be successfully fabricated using Monolayer Doping.

In Recessed Channel MOSFETs, various parameters affecting the threshold voltage of the device can be the depth, roughness of the sidewalls of the trench, the steepness of V-groove and the junction depth might have affected the threshold voltage.

The fabricated Recessed Channel MOSFET is comparable to the classic planar MOSFET in terms of device performance. The subthreshold slope of a 10 μm planar NMOSFET was 150 mV/dec, whereas for a 10 μm recessed channel MOSFET it is 117.7 mV/dec. The threshold voltage of the 10 μm planar NMOSFET was -0.3 V whereas the threshold voltage of the 10 μm recessed channel MOSFETs is 0.2 V. Both the devices have an on current to off current

ratio in 3 orders of magnitude. Hence, recessed channel MOSFETs shows good device characteristics and performance using Monolayer doping and can be investigated further with advanced integration schemes.

In the work, it is proved that Silicon-On-Insulator can be doped using Monolayer doping. From the study performed to understand the role of temperature in doping process, it is observed that as the temperature increases the sheet resistance of the doped SOI decreases, resulting in diffusion of more dopants increasing the dopant concentrations in the SOI samples. In the second study performed to study the role of multiple MLDs, it is observed that by performing double-MLD, double the amount of dopant dose was introduced in the sample resulting in reducing the sheet resistance by half after the double-MLD process and can be confirmed across various time intervals. Secondly, as the time interval increases, the sheet resistance decreases, since ample time is given for the dopants to diffuse and increase the dopant concentration. Thus, it is proved that MLD can be implemented to dope Silicon on Insulator to develop an integration mechanism to fabricate Recessed Channel FETs on Silicon on Insulator substrates.

Thinner and uniform gate oxide can be deposited for achieving better device performance. When silicon di oxide is used as gate oxide as thin as 1.5 nm can be deposited since lesser than 1.5 nm can easily introduce leakage currents in the devices affecting the device performance drastically.

High-k dielectrics such as HfO_2 can be introduced in the device fabrication as an alternative to SiO_2 . HfO_2 has various advantages such as a high dielectric constant, approximately equal to a value of 24 making it 6 times larger than SiO_2 . Thus, a deposition of 1nm SiO_2 is equivalent to depositing 6nm of HfO_2 resulting in same value of oxide capacitance. Another advantage of

HfO₂ is an increased tunnelling barrier to the electrons and holes resulting in a very low leakage current in comparison to SiO₂.

The milled V-shaped trench tends to accumulate electric field lines along its sharp edge resulting in introduction of electrons into the oxide region shifting the threshold voltage of the MOSFET. Thus, for further investigation, U-shaped trenches can be milled as it has been proved that Recessed Channel MOSFETs as small as 1 μm can be doped using Monolayer Doping to form shallow junctions and have a working MOSFETs with subthreshold-slopes.

Recessed channel FETs on silicon on insulator can be fabricated as both have their own advantages as shown in the above work. By combining both the devices short channel effects, V_{th} roll-off, punch through effects, DIBL and hot carrier effects can be reduced, and a better device can be implemented. The combination can also be successful in having a device with lower subthreshold slope to have less leakage current. Further implementation can be performed by having multi-gate material, which will enable high carrier flow in the gate channel region leading to high on current and a reduction in the leakage current.

Multi-Layer gate oxide can be integrated with the FETs as it has the capability to control the gate in an improved manner over the device charge carriers and can also have better sub-threshold characteristics.

8. References

- [1] K. Mistry *et al.*, “Introducing 14-nm FinFET technology in Microwind To cite this version : HAL Id : hal-01541171 Introducing 14-nm FinFET technology in Microwind,” *Proc. 49th Des. Autom. Conf. - DAC '12*, vol. 637371, no. 3, p. 37, 2017.
- [2] J. L. Doran and J. L. Doran, “Self-Assembled Monolayers for Phosphorus Doping of Silicon for Field Effect Devices Self-Assembled Monolayers for Phosphorus Doping of Silicon for Field Effect Devices,” 2018.
- [3] Z. Fan, Z. A. Jacobson, J. C. Ho, A. Javey, R. L. Alley, and R. Yerushalmi, “Controlled nanoscale doping of semiconductors via molecular monolayers,” *Nat. Mater.*, vol. 7, no. 1, pp. 62–67, 2007.
- [4] A. Javey *et al.*, “Wafer-Scale, Sub-5 nm Junction Formation by Monolayer Doping and Conventional Spike Annealing,” *Nano Lett.*, vol. 9, no. 2, pp. 725–730, 2009.
- [5] A. B. Sieval, B. Van den Hout, H. Zuilhof, and E. J. R. Sudhölter, “Molecular modeling of covalently attached alkyl monolayers on the hydrogen-terminated Si(111) surface,” *Langmuir*, vol. 17, no. 7, pp. 2172–2181, 2001.
- [6] L. Scheres, M. Giesbers, and H. Zuilhof, “Organic monolayers onto oxide-free silicon with improved surface coverage: Alkynes versus alkenes,” *Langmuir*, vol. 26, no. 7, pp. 4790–4795, 2010.
- [7] E. Arduca *et al.*, “Synthesis and characterization of P δ -layer in SiO₂ by monolayer doping,” *Nanotechnology*, vol. 27, no. 7, 2016.
- [8] B. Novak, “Large Area Monolayer Doping Development,” no. May, pp. 1–4, 2017.
- [9] A. Tapriya, “Ultra-Shallow Phosphorous Diffusion in Silicon using Molecular

- Monolayer Doping,” 2017.
- [10] A. Tapriya, B. Novak, S. Williams, and S. Kurinec, “Shallow Si N + P junction diodes realized via molecular monolayer doping,” *Microelectron. Eng.*, vol. 193, pp. 1–6, 2018.
- [11] L. Ye, M. P. de Jong, T. Kudernac, W. G. van der Wiel, and J. Huskens, “Doping of semiconductors by molecular monolayers: monolayer formation, dopant diffusion and applications,” *Mater. Sci. Semicond. Process.*, vol. 57, no. January, pp. 166–172, 2017.
- [12] J. Barnett, R. Hill, W. Y. Loh, C. Hobbs, P. Majhi, and R. Jammy, “Advanced techniques for achieving ultra-shallow junctions in future CMOS devices,” *IWJT-2010 Ext. Abstr. - 2010 Int. Work. Junction Technol.*, vol. 78741, no. 512, pp. 132–135, 2010.
- [13] K. W. Ang *et al.*, “300mm FinFET results utilizing conformal, damage free, ultra shallow junctions ($X_j \sim 5\text{nm}$) formed with molecular monolayer doping technique,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 837–840, 2011.
- [14] B. Long *et al.*, “Molecular Layer Doping: Non-destructive doping of silicon and germanium,” *Proc. Int. Conf. Ion Implant. Technol.*, pp. 1–4, 2014.
- [15] W. Y. Loh *et al.*, “300mm wafer level sulfur monolayer doping for III-V materials,” *2015 26th Annu. SEMI Adv. Semicond. Manuf. Conf. ASMC 2015*, pp. 451–454, 2015.
- [16] R. Kaur, “A Review on Power MOSFET Device Structures,” *Int. J. Res. Appl. Sci. Eng. Technol.*, vol. V, no. X, pp. 208–218, 2017.
- [17] M. Singh, S. Mishra, S. S. Mohanty, and G. P. Mishra, “Performance analysis of SOI MOSFET with rectangular recessed channel,” *Adv. Nat. Sci. Nanosci. Nanotechnol.*,

vol. 7, no. 1, 2016.

- [18] Y. Kwon, Y. Kang, S. Lee, B. G. Park, and H. Shin, “Analytic threshold voltage model of recessed channel MOSFETs,” *J. Semicond. Technol. Sci.*, vol. 10, no. 1, pp. 61–65, 2010.
- [19] P. H. Bricout and E. Dubois, “Short-channel effect immunity and current capability of sub-0.1-micron MOSFET’s using a recessed channel,” *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1251–1255, 1996.
- [20] T. D. Takayasu Sakurai, Akira Matsuzawa, *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications - Takayasu Sakurai, Akira Matsuzawa, Takakuni Douseki - Google Books. .*
- [21] N. Kennedy *et al.*, “Phosphorus monolayer doping (MLD) of silicon on insulator (SOI) substrates,” *Beilstein J. Nanotechnol.*, vol. 9, no. 1, pp. 2106–2113, 2018.
- [22] N. Alfaraj, “SIMOX vs . Smart-Cut : A brief overview of the silicon-on- insulator technology,” no. January, 2018.
- [23] H. Kuribayashi, R. Hiruta, R. Shimizu, K. Sudoh, and H. Iwasaki, “Investigation of shape transformation of silicon trenches during hydrogen annealing,” *Japanese J. Appl. Physics, Part 2 Lett.*, vol. 43, no. 4 A, 2004.

9. Appendix

Process flow for the fabrication of the recessed channel FETs

	Step	Tool	Process
1	RCA Clean	General RCABench	Standard
2	Coat Photoresist	SVG Track 2	
3	Litho 0	ASML Stepper	0 level reticle - use MEMS770_4x stepper job
4	Develop Photoresist	SVG Track 2	
5	Etch Si(alignment marks)	Trion III Etcher	
6	Resist Strip	Gasonics Aura 1000 Asher	FFF
7	RCA Clean	General RCABench	Standard
8	Thermal Field Oxide Growth	Bruce Furnace Tube 1	5000Å, 350recipe
9	Coat Photoresist	SVG Track 2	
10	Litho 1 (S/D)	ASML Stepper	MLD Mask, level 1
11	Develop Photoresist	SVG Track 2	
12	Oxide Etch	BOE & HF Wet Bench	~ 13mins in 10:1 ? Check Etch rates
13	Resist Strip	Gasonics Aura 1000 Asher	FFF
14	HF Dip	BOE & HF Wet Bench	10-15secs
15	MLD	Dr. Williams Lab	120°C, 2hrs
16	Capping Oxide dep	P5000	TEOS_1KA_LS, dep time - 6secs
17	RTA	AG 610 RTP	
18	Capping Oxide etch	BOE & HF Wet Bench	~ 30secs in 10:1 ? Check Etch rates
19	HF Dip	BOE & HF Wet Bench	10-15secs
20	MLD	Dr. Williams Lab	120°C, 2hrs
21	Capping Oxide dep	P5000	TEOS_1KA_LS, dep time - 6secs
22	RTA	AG 610 RTP	
23	Capping Oxide etch	BOE & HF Wet Bench	~ 30secs in 10:1 ? Check Etch rates
24	Nickel deposition	PE4400	~2 rotations for 7nm(~20secs)
25	Nickel Silicide formation	AG 610A RTP	400mL H2SO4:200mL H2O2

26	Etch Unreacted Nickel	General RCABench	Piranha clean
27	Coat Photoresist	SVG Track 2	
28	Litho 2 (Active Area)	ASML Stepper	MLD Mask, level 2
29	Develop Photoresist	SVG Track 2	
30	Trench Etch	VeeCo	
31	Resist Strip	Gasonics Aura 1000 Asher	FFF
32	RCA Clean	General RCABench	Standard
33	Gate Oxide (PECVD) 30nm	P5000	TEOS_1KA_LS, dep time - 3secs
34	TEOS Densification	Bruce Furnace Tube 4	Recipe 59, Doran_TEOS
35	Coat Photoresist	SVG Track 2	
36	Litho 3 (Contact cut)	ASML Stepper	MLD Mask, level 3
37	Develop Photoresist	SVG Track 2	
38	Gate Oxide etch	BOE & HF Wet Bench	~ 1mins in 10:1 ? Check Etch rates
39	Resist Strip	Gasonics Aura 1000 Asher	FFF
40	RCA Clean	General RCABench	Standard
41	Al dep	CVC 601 Sputter	~350nm, 2000W, 12min (~300Å/min)
42	Coat Photoresist	SVG Track 2	
43	Litho 4 (Metal)	ASML Stepper	MLD Mask, Level 4
44	Develop Photoresist	SVG Track 2	
45	Al etch	Al Wet Bench	~2min? 250nm/min, wait until visibly clear
46	Resist Strip	Gasonics Aura 1000 Asher	FFF
47	Sinter	Bruce Furnace Tube 2	99, sinter 400