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Fabrication of Al:HfO₂ Gate Dielectric MOSFETs

GEORGE MCMURDY

Fabrication of Al:HfO₂ Gate Dielectric MOSFETs

GEORGE MCMURDY

Fall 2019

A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

R·I·T | KATE GLEASON
College of ENGINEERING

Department of Electrical and Microelectronic Engineering

Fabrication of Al:HfO₂ Gate Dielectric MOSFETs

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Acknowledgments

I would first like to thank my advisor, Dr. Santosh Kurinec, for her tremendous guidance and support through this project. I would also like to thank my committee members, Dr. Robert Pearson and Dr. Michael Jackson, for their time and efforts in shaping and revising this work. Thank you to Dr. Sean Rommel as well for supporting and guiding me through this process to the end.

I would also like to thank our collaborators at RIT. Dr. Kai Ni for his many useful conversations on ferroelectricity, Dr. Bruce Kahn and Dr. Scott Williams for their help with SEM and EDX measurements, and Dr. Kristen Repa for assistance with XRR analysis.

Thank you to our outside collaborators at Innovion for ion implantation, Veeco Instruments for ion milling, NaMLab for alternate film depositions, and Micron for TEM analysis. Thank you to Dr. Nathaniel Cady and Jubin Hazra at SUNY Polytechnic Institute for their collaboration on ferroelectric device analysis.

Thank you to the entire SMFL staff and the many students that helped me get to this point. This includes Jordan Merkel, Jackson Anderson, and Pooja Chandrashekar Patil.

Finally, I would like to thank all those who have supported me throughout my graduate career. Thank you to the McMurdy's, the Wagner's, the Lussier's, and the DeJohn's. Thank you to my loving girlfriend, Abby DeJohn, for I could not have made it here without her.

Above all else, the greatest inspiration for my work is my mother, Jayne Wagner. Thank you for everything.

This work was sponsored in part by Semiconductor Research Corporation GRC Project 2825.001.

Abstract

Replacing the traditional SiO₂ gate oxide in a MOSFET with ferroelectric HfO₂ creates a 1T memory device referred to as a FeFET. The bi-stable polarization states cause a retained threshold voltage shift known as the memory window. Ferroelectric HfO₂ offers a number of material and electrical advantages over perovskite based ferroelectrics such as PZT or SBT. Due to its use as a high-k dielectric, the ALD capability and etch characteristics of hafnium oxide are well documented. Ferroelectric HfO₂ has been shown to be thermally stable up to 1000°C, making gate first FeFET processes feasible. Electrically, HfO₂ is capable of achieving much larger memory windows due to a high coercive field, on the order of 1-2 MV/cm. This property also allows for much thinner films (<30 nm) without degradation of the memory window, and the potential for finFET applications.

This work focuses on the integration of aluminum doped HfO₂ into a standard RIT FET process. Previous work at RIT has led to the development of an ALD recipe and subsequent anneal to induce the ferroelectric crystal phase in Al:HfO₂. In this work, n-channel MOSFETs with aluminum gate/20nm Al:HfO₂/p-Si have been designed and fabricated. Etching of Al:HfO₂ has been investigated using chlorine based plasma etching. The devices show a subthreshold slope of 75 mV/dec. Pulse testing reveals significant threshold voltage shift due to electron charge trapping commonly observed in Hf based dielectrics. I-V characteristics show mobility degradation, which is caused by Coulomb scattering as a result of trapped charges. For the devices to exhibit ferroelectric behavior with high on-state current, measurement and mitigation of charge trapping need to be further investigated.

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List of Symbols

Term	Description	Units/Value
C_{FE}	Ferroelectric capacitance per unit area	F/cm ²
C_{ox}	Oxide capacitance per unit area	F/cm ²
d_{FE}	Ferroelectric film thickness	nm
E_{loc}	Local electric field	V/cm
E_c	Coercive field	MV/cm
E_C	Energy at the conduction band edge	eV
E_V	Energy at the valence band edge	eV
N_a	Acceptor concentration	cm ⁻³
n_i	Intrinsic carrier concentration	cm ⁻³
P_r	Remnant Polarization	$\mu\text{C}/\text{cm}^2$
P_s	Saturation Polarization	$\mu\text{C}/\text{cm}^2$
q	Elementary charge	1.602×10^{-19} C
V_c	Coercive voltage	V
V_b	Body voltage	V
V_s	Source Voltage	V
V_d	Drain voltage	V
V_g	Gate voltage	V
V_{TH}	Threshold voltage	V
ϵ_r	Relative permittivity	F/cm
ϕ_s	Surface potential	V
ϕ_t	Thermal potential	eV

List of Acronyms

Term	Description
DRAM	Dynamic Random Access Memory
FeFET	Ferroelectric Field Effect Transistor
NV-RAM	Non-Volatile Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
NDRO	Nondestructive Read-Out Device
MW	Memory Window
FeRAM	Ferroelectric Random Access Memory
PZT	Lead Zirconate Titanate
SBT	Strontium Bismuth Tantalate
GIXRD	Grazing Incidence X-ray Diffraction
HKMG	High-k Metal Gate
SIMS	Secondary Ion Mass Spectroscopy
TEM	Transmission Electron Microscopy
EDX	Energy-Dispersive X-ray Spectroscopy
DHM	Dynamic Hysteresis Measurement
PUND	Positive-Up Negative-Down
LM	Leakage Measurement
MLD	Monolayer Doping

Chapter 1

Fundamentals of Ferroelectricity

Discovered in 1921, ferroelectricity has long been known to imply two stable electric polarization states, $+P$ and $-P$, in a material. However, it was not until the late 1990s that these polarization states were successfully engineered to represent the 1 and 0 of Boolean algebra. In Dynamic Random Access Memory (DRAM), ferroelectric capacitors offer large dielectric constants ($\epsilon_r = 100$ to 1000) enabling a proportional decrease in capacitor area. Additionally, ferroelectric field effect transistors (FeFETs) may be used in Non-Volatile Random Access Memories (NV-RAM), in which they serve as a memory element itself. In this architecture, stored information is retained even after the power is turned off [1].

At the time of its conception in the 1970s, NV-RAM was represented by Electrically Erasable Programmable Read-Only Memory (EEPROM) which were devices that utilized a control gate and hot carrier injection to accumulate charge on a second floating gate. Low yield and reliability issues led to its downfall [2], but the theoretical basis of floating gate technology formed what is today's flash memory.

Ferroelectric NV-RAM has the additional benefit of being a Nondestructive Read-Out Device (NDRO), meaning that information is retained during read operations. By monitoring the source-drain current in a FeFET, the polarization of the film can be read without disrupting the written state. This chapter will elaborate on what ferroelectricity is and how it can be used to achieve a working memory device.

1.1 Defining a Ferroelectric Material

Dielectric materials, often regarded as being electrical insulators, also exhibit an important phenomenon known as electrical polarization. Under the influence of an electric field, there are three known contributors to polarization: Electronic, Ionic, and Dipole Reorientation [3]. Figure 1.1 shows a microscopic view of these effects. In

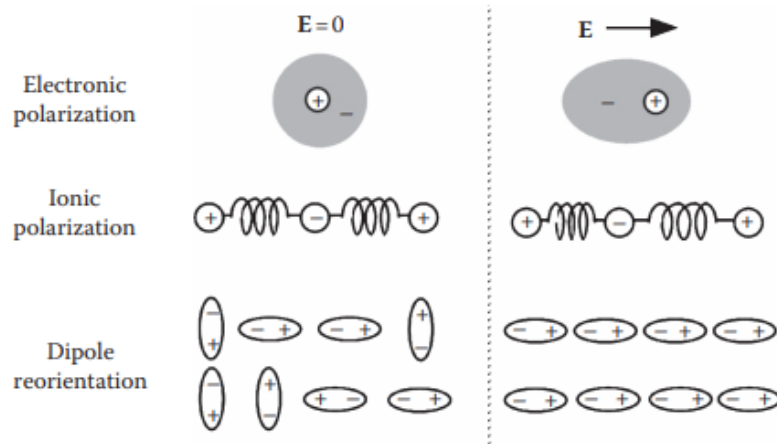


Figure 1.1: Microscopic view of contributors to electric polarization [3].

electronic polarization, an applied electric field causes a displacement of the negatively charged electron cloud relative to the positively charged nucleus, forming electric dipoles. Ionic polarization occurs due to electrostatic interaction between ions and their corresponding cathode/anode, again inducing dipoles. Lastly, under an electric field, existing dipoles will preferentially reorient themselves along the direction of that field. The total polarization of a material depends upon the sum of all electric dipoles from each of these contributors.

In some dielectrics, the crystal structure is asymmetrical in such a way that ionic polarization occurs even without the application of an electric field. This effect is known as spontaneous polarization and it is only observed in non-centrosymmetric crystal point groups. Of the 32 classified point groups, 21 of them do not have a center of symmetry. Of these 21, 20 of them are piezoelectric, meaning they exhibit

charge generation under mechanical stress. These crystallographic classifications are highlighted in Figure 1.2 [3]. Beneath the piezoelectrics there are 10 point groups

Polarity	Symmetry	Crystal System										
		Cubic		Hexagonal		Tetragonal		Rhomboidal		Orthorhombic	Monoclinic	Triclinic
Nonpolar (22)	Centro (11)	$m\bar{3}m$	$m\bar{3}$	$6/mmm$	$6/m$	$4/mmm$	$4/m$	$\bar{3}m$	$\bar{3}$	mmm	$2/m$	
	Noncentro (21)	432	23	622	$\bar{6}$	422	$\bar{4}$	32		222		
Polar (pyroelectric) (10)				$6mm$	6	$4mm$	4	$3m$	3	$mm2$	2 m	1

Figure 1.2: Crystallographic classification by crystal symmetry (highlighted groups are piezoelectric) [3].

which are pyroelectric. With these materials in particular, the spontaneous polarization itself is dependent upon temperature. This leads to different levels of charge generation as temperature is varied. If the spontaneous polarization of a pyroelectric material can be reversed by the application of an electric field, then it is ferroelectric. Further characteristics of polarization in a ferroelectric material will be discussed in later sections, but first it will be useful to describe how spontaneous polarization occurs in non-centrosymmetric crystals.

1.2 Origins of Spontaneous Polarization

We can define a crystal unit cell to have a center of symmetry if a vector drawn from one charge through the origin arrives at a like charge. If this vector arrives at an opposite charge, the point group is non-centrosymmetric. This can be exemplified by looking at a simplistic model of the cubic structure (centrosymmetric), and the hexagonal structure (non-centrosymmetric), shown in Figure 1.3. Although the two structures have differences in symmetry, it is apparent that the centers of mass for

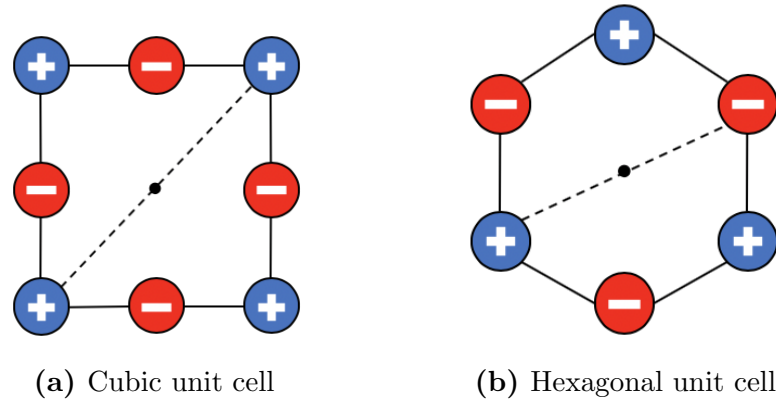


Figure 1.3: Depiction of the central point of symmetry in a unit cell.

negative and positive charges coincide at the origin for both the cubic and hexagonal lattice. However, this is not the case if their ions are displaced in any way. For example, Figure 1.4 shows what can occur to each unit cell under an applied stress. In

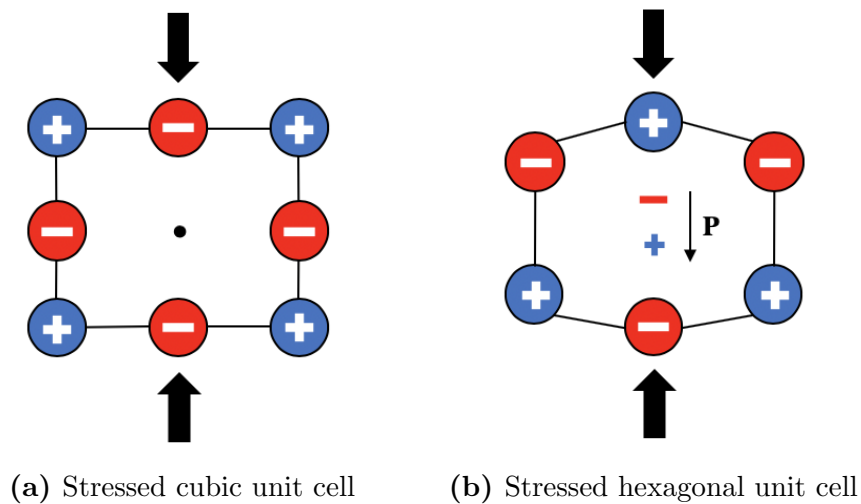


Figure 1.4: Effect of stress upon different crystal symmetries.

the centrosymmetric structure the centers of mass remain at the same point, producing no net dipole. The lack of such symmetry in the hexagonal unit cell shifts both centers of mass away from each other resulting in a net dipole [4]. It is then the total dipole moment per unit volume that is known as the spontaneous polarization, P_S .

The above example represents the piezoelectric effect and is observed in the 20 aforementioned piezoelectric point groups. The 10 pyroelectric point groups that

branch out from those are polar materials, meaning there is a natural displacement of charges even in the absence of an applied stress or electric field. In such a system of surrounding polarization, P , there exists a proportional local field, E_{loc} . Because the dipole moment of the unit cell also depends on P , the associated potential energy is proportional to P^2 and is given by Equation 1.1 [3].

$$U_{dip} \propto -P^2 \quad (1.1)$$

Furthermore, displaced charges will add to the elastic energy of the system. Equation 1.2 gives this contribution as a function of the displacement, d .

$$U_{elas} = N\left[\left(\frac{k}{2}\right)d^2 + \left(\frac{k'}{4}\right)d^4\right] \quad (1.2)$$

Where N is the number of atoms per unit volume, and k/k' are the first/second order force constants. Using Equation 1.3 we can substitute for d in Equation 1.2.

$$P = Nqd \quad (1.3)$$

The total potential energy of this system will be the sum of these two contributions, U_{dip} and U_{elas} . Figure 1.5 best shows this result. It is clear that there are two energetically favorable states at some $+P$ and $-P$ in polar point groups. To be able to switch between these two states a particle must gain sufficient kinetic energy, hence the temperature dependence of the polarization in a pyroelectric material. Lastly, if a polarization state can transition via the application of an electric field, then that material is ferroelectric. In this case, the applied bias would tilt the energy profile towards one minimum leaving one energetically favorable state. A subsequent bias in the opposite direction would leave the adjacent minimum as the lone favorable state [5].

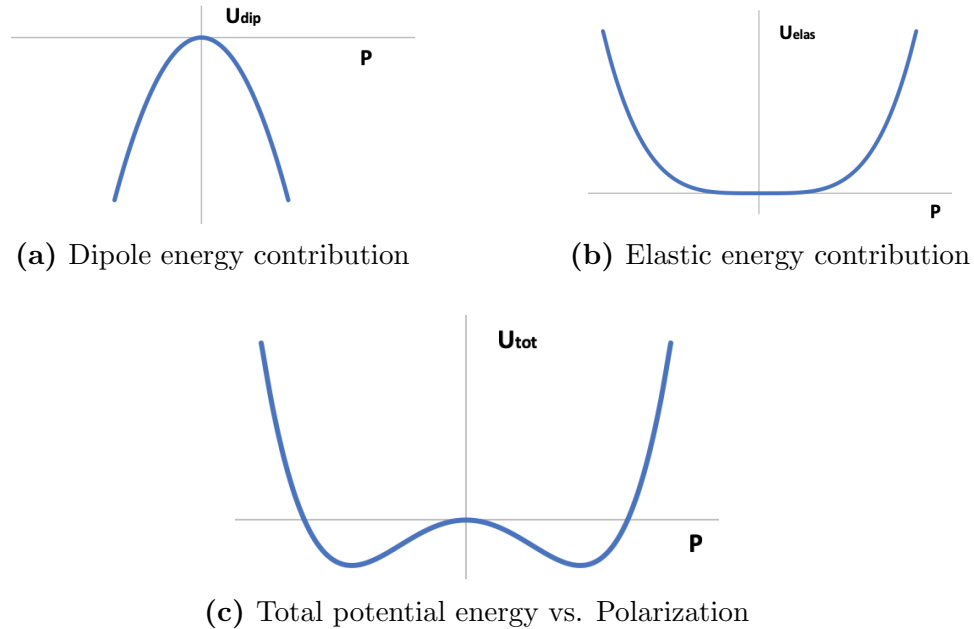


Figure 1.5: Potential energy as a function of polarization for a polar point group.

1.3 Mathematical Model of Ferroelectric Behavior

Once the origins of ferroelectricity are understood, it then becomes important to be able to characterize one ferroelectric material from another. The key measures of a ferroelectric film are remnant polarization, P_r , and coercive field, E_c . Remnant polarization refers to the polarization charge remaining at 0 bias, whereas the coercive field is the bias necessary to induce a change between the two polarization states. As the field is ramped from negative to positive values, the polarization exhibits hysteresis, as shown in Figure 1.6. In a bulk film, the ferroelectric material may consist of multiple ferroelectric domains that may have slightly different coercive fields. When all domains align under an applied bias, the polarization reaches a maximum value known as the saturation polarization, P_s , typically larger than P_r .

In 1990, Miller *et al* developed a model to describe the hysteretic behavior of Figure 1.6 using the above parameters. It is assumed that the positive and negative branches of the hysteresis curve are symmetrical [7]. The positive field sweep is then

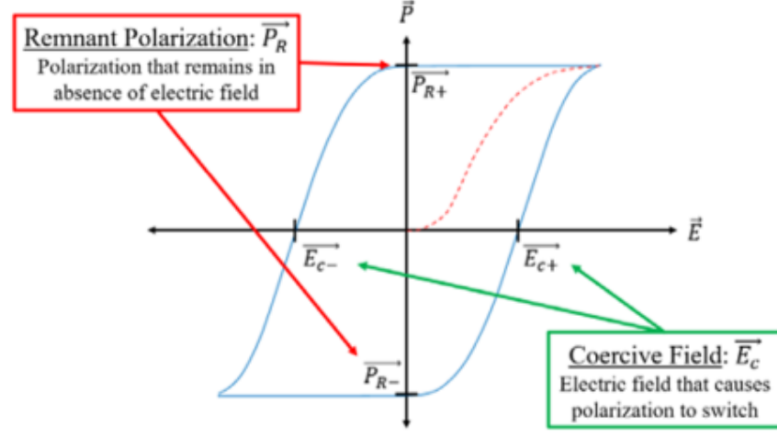


Figure 1.6: Polarization vs. Voltage characteristics for a ferroelectric material [6].

defined by Equation 1.4.

$$P^+(E) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) \quad (1.4)$$

where,

$$\delta = E_c \left[\log\left(\frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}}\right) \right]^{-1} \quad (1.5)$$

Here δ is defined such that $P^+(0) = -P_r$. Under the assumption of symmetry, the negative field sweep, $P^-(E)$, is related to $P^+(E)$ by,

$$P^+(E) = -P^-(-E) \quad (1.6)$$

Such a model can be used to fit a measured hysteresis loop in order to extract the material parameters P_r , P_s , and E_c .

1.4 Ferroelectric Device Physics

In ferroelectric non-volatile memory, the two key structures are the ferroelectric capacitor and the FeFET. The capacitor is more often used as a data storage element in FeRAM, however this is not a NDRO device. Information may be stored via a volt-

age pulse in order to set the direction of polarization, but another voltage pulse must be applied in order to read that direction by observing the corresponding switching current. In fact, during this read process data becomes volatile as the bit must be reprogrammed after each read pulse [8]. It is here that the FeFET offers a significant advantage. By replacing the gate dielectric of a traditional MOSFET with a ferroelectric, a voltage pulse on the gate sets the polarization and in turn effects the threshold voltage of the transistor. In this way, the drain current becomes programmable to define two logic states.

In order to implement this idea into a real world device, it is pertinent to model the electrical performance as it relates to fundamental physical quantities. This section will follow the derivations of Miller and McWhorter, formulated in 1992, to establish the connection between gate voltage, V_{gb} , and surface potential, ϕ_s , in a ferroelectric capacitor. From there, familiar current equations can be modified to describe the FeFET. The structure to be modeled is based on a p-type silicon substrate and is schematically presented in Figure 1.7.

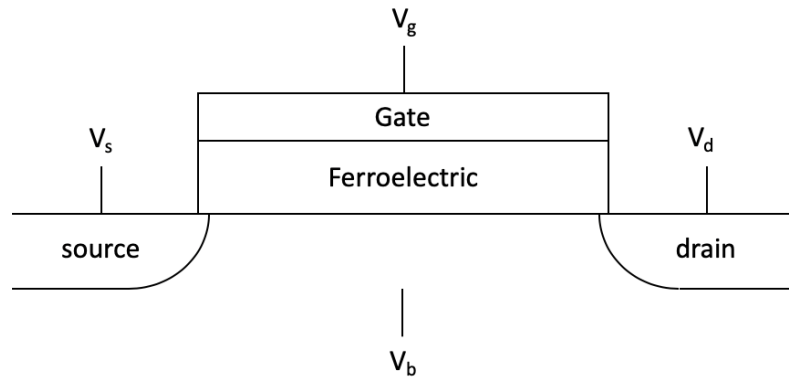


Figure 1.7: Simple FeFET structure.

1.4.1 Ferroelectric Capacitor

Following Kirchhoff's Voltage Law, the voltage drop across the components of the device must equal the applied voltage, V_{gb} . For Figure 1.7, the voltage drop will

be across the ferroelectric layer and the silicon surface potential. The ferroelectric layer has both a linear dielectric contribution and a polarization contribution due to switching dipoles under an applied bias. Equation 1.7 gives this result [8].

$$V_{gb} = \phi_s - \frac{\sigma_s}{C_{FE}} - P(E) \frac{d_{FE}}{\epsilon_0 \epsilon_{FE}} \quad (1.7)$$

where σ_s is the silicon surface charge and C_{FE} is the ferroelectric capacitance given by $\epsilon_0 \epsilon_{FE} / d_{FE}$. $P(E)$ has already been defined in Equations 1.4 and 1.6. Note that due to the inclusion of the $P(E)$ term, the relationship between V_{gb} and ϕ_s depends on the electrical history of the device.

The capacitance term in Equation 1.7 could be amended to account for a total series capacitance in a stack of multiple dielectrics if the device was designed as such. However, no matter what the structure is above the surface, σ_s remains unchanged as a function of ϕ_s and is of the familiar form given by Equation 1.8 [8].

$$\sigma_s(\phi_s) = -SGN(\phi_s) \sqrt{2} \frac{\epsilon_0 \epsilon_s}{\beta L_B} \sqrt{(e^{-\beta \phi_s} + \beta \phi_s - 1) + \left(\frac{n_i}{N_a}\right)^2 (e^{\beta \phi_s} - \beta \phi_s - 1)} \quad (1.8)$$

where β is $1/\phi_t$ and L_B is the Debye length given by Equation 1.9. Here, ϵ_s is the relative permittivity of silicon and N_a is the acceptor dopant concentration for a p-type substrate.

$$L_B = \sqrt{\frac{\epsilon_0 \epsilon_s}{\beta q N_a}} \quad (1.9)$$

1.4.2 Ferroelectric Transistor

Due to varying contributions from drift and diffusion along the length of the channel, the current of a FET is typically written as a function of the quasi-Fermi level ϕ_{Fn} , seen in Equation 1.10 [9].

$$I = -Wq\mu N_I \frac{d\phi_{Fn}}{dx} \quad (1.10)$$

Where W is the transistor width, μ is the carrier mobility, and N_I is the inversion charge. Given that N_I and ϕ_{F_n} both depend upon σ_s [8], the total current shows dependence on $P(E)$ via Equation 1.7.

As a memory device, a FeFET utilizes the two stable polarization states of a ferroelectric to produce a shift in threshold voltage known as the Memory Window (MW). The change in threshold voltage is brought about due to additional charge accumulated or depleted in the channel depending on the gate bias. In an nFET, if the gate bias is higher than the coercive voltage, V_c , the polarization will deplete positive charges in the channel and lower the threshold voltage. If the gate bias is lower than $-V_c$, the polarization will accumulate positive charges from the substrate and raise the threshold voltage. Figure 1.8 shows this effect on a basic FeFET.

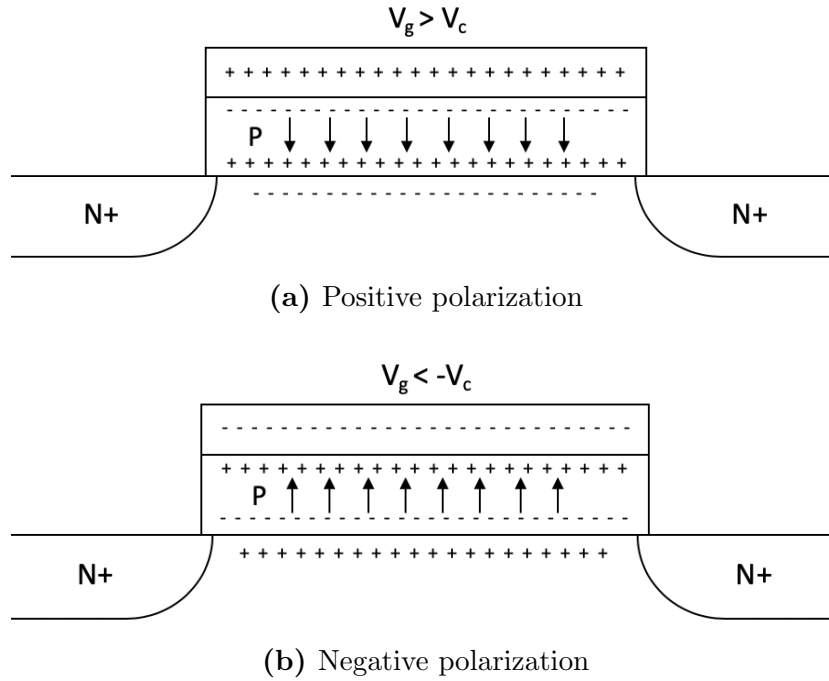


Figure 1.8: Origin of the threshold voltage shift in a FeFET.

The MW of a FeFET is often cited as a figure of merit and is given by Equation 1.11.

$$MW_{max} = 2V_c = 2E_c d_{FE} \quad (1.11)$$

1.5 Hafnium Based Ferroelectrics

In the early 2000s, perovskite based ferroelectrics led the way in commercial applications of FeRAM. Lead zirconate titanate (PZT) was deemed more suitable for scaled capacitors due to its high switching current. For low voltage applications, strontium bismuth tantalate (SBT) was the material of choice due to a lower coercive field [10]. However, in FeFET applications, perovskite materials presented a number of CMOS integration challenges. Below the 100 nm node, charge differences between read-out states became too low in scaled capacitors. Additionally, the interface between PZT/SBT and silicon required thick buffer layers to prevent Bi and Pb diffusion, and the low coercive fields necessitated a thick gate dielectric [5]. These inherent difficulties inspired the search for a ferroelectric material with more CMOS compatible properties.

1.5.1 Doped Hafnium Dioxide

Hafnium oxide, HfO_2 , commonly exists in three phases: monoclinic, tetragonal, and cubic. The monoclinic phase is stable at normal pressure and room temperature and exhibits a transformation to the tetragonal phase at 1720 °C, and the cubic phase at 2600 °C [11]. In thin film deposition, nucleation of HfO_2 tends to begin in the tetragonal phase due to Ostwald's rule, stating that it is the least stable polymorph which crystallizes first [12]. After initial nucleation, the crystal undergoes a martensitic transformation to the monoclinic phase. In this diffusionless transformation, a phase change is brought about by small, synchronized atomic displacements rather than long range atomic diffusion [13].

In 2011, Böscke *et al* reported that doping HfO_2 with silicon (Si:HfO_2) at 3 mol. % was capable of stabilizing the tetragonal phase when paired with a top electrode which serves as a mechanical encapsulation layer [14]. This stabilization occurs at a

lower silicon content than previously reported (4-10 mol. %), where the tetragonal phase has been shown to increase the dielectric constant [15]. Böscke *et al* also showed that if crystallized via a high temperature anneal, a transformation from this metastable tetragonal phase to an orthorhombic phase can take place, shown in Figure 1.9. Grazing incidence x-ray diffraction (GIXRD) measurements reveal that this particular phase is of the polar $mm2$ point group referenced in Figure 1.2. More specifically, the phase was found to belong to the ferroelectric $Pbc2_1$ space group [14], a further classification of crystal symmetry. Additional dopants that have been confirmed to induce the ferroelectric phase in HfO_2 include Al, Gd, La, Sr, and Y [16]. In 2015, Polakowski and Müller reported ferroelectricity in undoped HfO_2 as well, suggesting the intrinsic nature of this property [17].

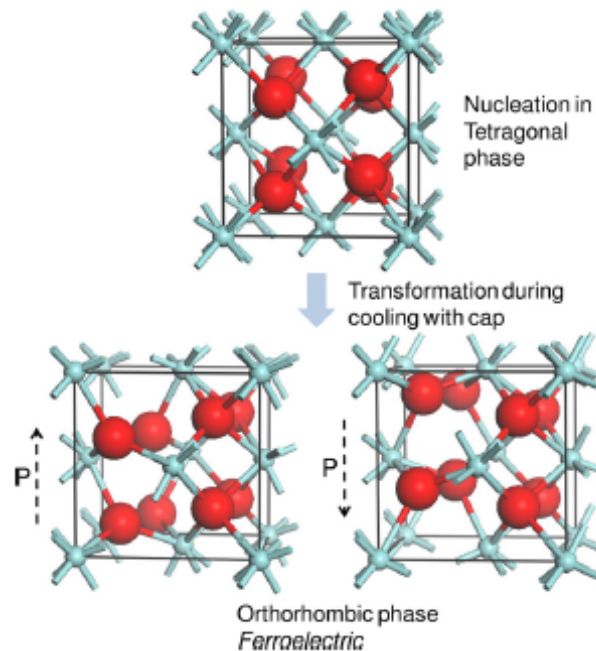


Figure 1.9: Orthorhombic phase transition in Si:HfO₂ [14].

The material advantages of ferroelectric HfO₂ over perovskites are both quantitative and qualitative. Because of a significantly larger coercive field (1-2 MV/cm), film thicknesses can be reduced to the single nanometer range while maintaining a viable memory window. A thinner film also has the effect of reducing the internal depolar-

ization field thus improving reliability. In terms of CMOS compatibility, doped HfO₂ is thermally stable at temperatures up to 1000 °C [18], has more mature ALD capability for a high quality interface, and is stable in BEOL processes. These advantages along with other material comparisons are summarized in Table 1.1 [16].

Table 1.1: Comparison of material properties and compatibilities of HfO₂ to common perovskite ferroelectrics [16].

	SBT	PZT	HfO ₂
Film Thickness	>25 nm	>70 nm	5-30 nm
Annealing Temp.	>750 °C	>600 °C	450 °C-1000 °C
P_r	<10 $\mu\text{C}/\text{cm}^2$	20-40 $\mu\text{C}/\text{cm}^2$	1-40 $\mu\text{C}/\text{cm}^2$
E_c	10-100 kV/cm	~50 kV/cm	1-2 MV/cm
Dielectric Constant	150-250	~1300	~30
ALD Capability	limited	limited	mature
CMOS Compatibility	Bi and O ₂ diffusion	Pb and O ₂ diffusion	stable
BEOL Compatibility	H ₂ damage	H ₂ damage	stable

1.5.2 Hafnium Zirconium Oxide (HZO)

A particular disadvantage of doped hafnium oxide films such as Si:HfO₂ is the high crystallization temperature (1000 °C). Due to similarities in crystal structure between HfO₂ and ZrO₂, it has been shown that the aforementioned tetragonal phase can be controlled in the Hf_{0.5}Zr_{0.5}O₂ system as well. This is particularly advantageous as the integration of both compounds is already well understood in high-k dielectric processes and high-k metal gate (HKMG) applications. The primary benefit of the HZO film is the low crystallization temperature reported by Müller *et al* of 450 °C. Capacitors were fabricated with film thickness of 7.5 nm and 9.5 nm and a TiN encapsulation layer. After annealing at 450 °C, a P_r of 16 $\mu\text{C}/\text{cm}^2$ and E_c of 1 MV/cm were extracted from P-V hysteresis measurements [19]. The high remnant polarization is beneficial to ferroelectric capacitors due to a subsequent high switching current, while the large coercive field should give an appreciable memory window in a FeFET by Equation 1.11. Lastly, the lower thermal budget is a significant advantage

over doped HfO_2 in the context of CMOS process integration.

1.6 Summary

A ferroelectric material exhibits two stable electrical polarization states, capable of being retained when power is removed. This phenomena can be engineered into physical devices such as capacitors and transistors in order to form non-volatile and non-destructive read out memory. Due to the recent discovery of ferroelectricity in HfO_2 , the FeFET has the capability to become more CMOS compatible thus more useful in commercial applications. For this reason, this work focuses on the integration of doped HfO_2 as the gate dielectric for silicon MOSFETs.

Chapter 2

Characterization of Ferroelectric Films

2.1 Materials Characterization

This section will give an overview of various methods used to analyze the structure of thin films. The techniques discussed include Secondary Ion Mass Spectroscopy (SIMS), Grazing Incidence X-ray Diffraction (GIXRD), Transmission Electron Microscopy (TEM), and Energy-Dispersive X-ray Spectroscopy (EDX). GIXRD will also be discussed in the context of identifying the ferroelectric orthorhombic phase in HfO_2 .

2.1.1 Secondary Ion Mass Spectroscopy (SIMS)

Secondary Ion Mass Spectroscopy is a useful tool for analyzing the elemental composition of a sample with a detection limit as low as the parts per billion level. It involves bombarding a sample with a primary ion beam thus ionizing a fraction of the emitted particles, known as secondary ions. These secondary ions are analyzed via a mass spectrometer, in which a magnetic or electric field separates ions of unique mass or charge towards a detector. There are two typical classifications of SIMS analysis: static and dynamic. Static SIMS concentrates on the top monolayer of a sample and provides mostly molecular characterization. In dynamic SIMS, bulk composition and depth distribution of elements can be analyzed. A depiction of the incident primary

ion beam and subsequent ejection of secondary ions is shown in Figure 2.1 [20].

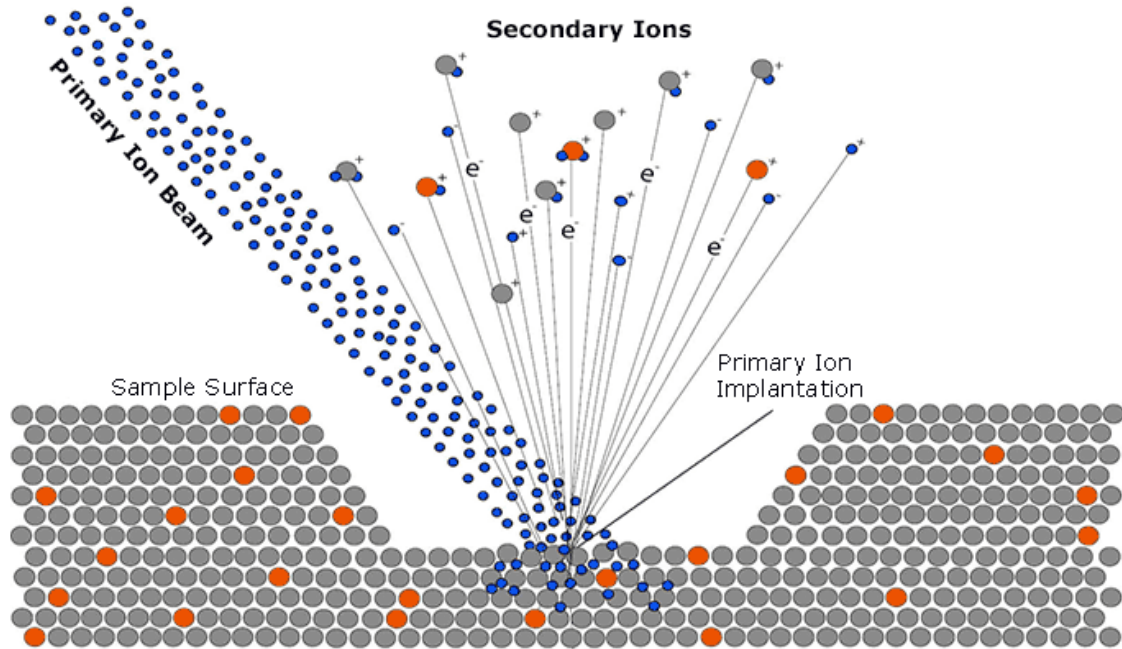


Figure 2.1: Depiction of a sample under SIMS analysis [20].

2.1.2 Grazing Incidence XRD (GIXRD)

X-ray diffraction is a frequently used method to characterize the crystal structure of a material or sample. This technique utilizes Bragg diffraction of incident x-rays reflected by atomic planes. Interference maximums occur as a function of atomic spacing, wavelength, and incident angle. In GIXRD, this incident angle is limited to a few degrees in order to reduce x-ray penetration depth and reduce background scattering from the substrate beneath a thin film [21].

In the study ferroelectric HfO_2 , GIXRD is often used to confirm the formation of the orthorhombic phase. Figure 2.2 shows the results of TiN capped and uncapped Si:HfO₂ GIXRD measurements by Boscke *et al.* This figure highlights the differences between a sample dominated by the monoclinic phase and one properly transformed to the orthorhombic phase. The single peaks just above 30° and 60° suggest that no monoclinic phase was formed in the capped sample. Additionally, the triplet

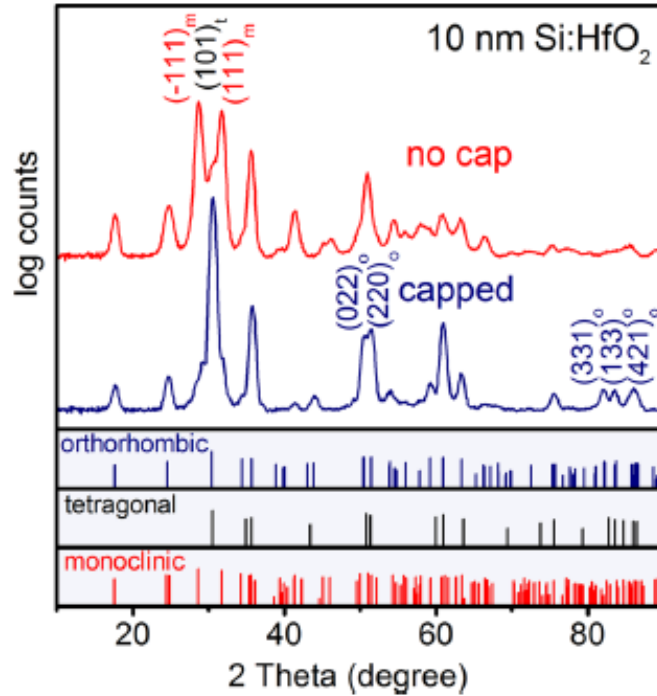


Figure 2.2: GIXRD comparison between capped and uncapped Si:HfO₂ [14].

of peaks at 83° are not typical for the tetragonal phase and indicate the presence of a lower symmetry phase. Similar diffraction patterns have been associated with the noncentrosymmetric orthorhombic phase in Mg:ZrO₂ and due to similar crystal structure this is thought to be the case for HfO₂ as well [14].

2.1.3 Transmission Electron Microscopy (TEM)

In transmission electron microscopy, a high energy beam of electrons is passed through a thin film sample. The interactions between these electrons and the atoms in the sample generate an image in a manner similar to an ordinary optical microscope. Since the de Broglie wavelength of electrons is smaller than the wavelength of visible light, the resolution of a TEM image is much higher and can be as small as a single column of atoms. Therefore, TEM can be used to identify dislocations, grain boundaries, and thicknesses of individual layers in a film stack. The general layout of a transmission electron microscope is shown in Figure 2.3 [22].

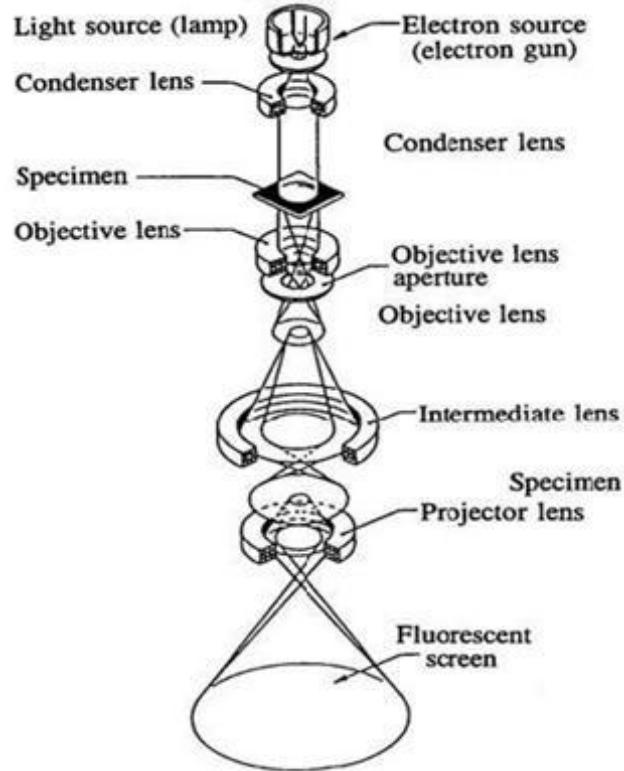


Figure 2.3: Diagram of a Transmission Electron Microscope [22].

2.1.4 Energy-Dispersive X-ray Spectroscopy (EDX)

Energy-Dispersive X-ray spectroscopy is an analysis technique used alongside scanning electron microscopy. In EDX, the sample is bombarded by the electron beam of an SEM and electrons from the sample are subsequently ejected. The resulting vacancies are filled by electrons from a higher state within the sample, causing the emission of an x-ray [23]. The energy of the emitted x-ray is characteristic of the elemental composition of the sample. By detecting the relative counts of a particular x-ray energy, EDX can determine a percent composition for different elements in the sample.

2.2 Electrical Characterization

This section will cover three essential measurements used to electrically characterize a ferroelectric film. This includes the dynamic hysteresis measurement, the positive-up negative-down measurement, and the leakage current measurement. The descriptions of each measurement will be in the context of using the aix-ACCT TF-1000 ferroelectric parameter analyzer.

2.2.1 Dynamic Hysteresis

The dynamic hysteresis measurement (DHM) results in the fundamental signature of a ferroelectric material: the hysteresis curve. In this test, the device is first cycled by a pre-polarization pulse in an attempt to align the ferroelectric domains into a known state. For the final measurement, a voltage pulse is applied to switch the ferroelectric film to one state, and then the other. This process can be repeated in the opposite direction and the measured loops can then be averaged together. A typical DHM result is shown in Figure 2.4 [24]. From the hysteresis curve, P_r , P_s , and E_c can be

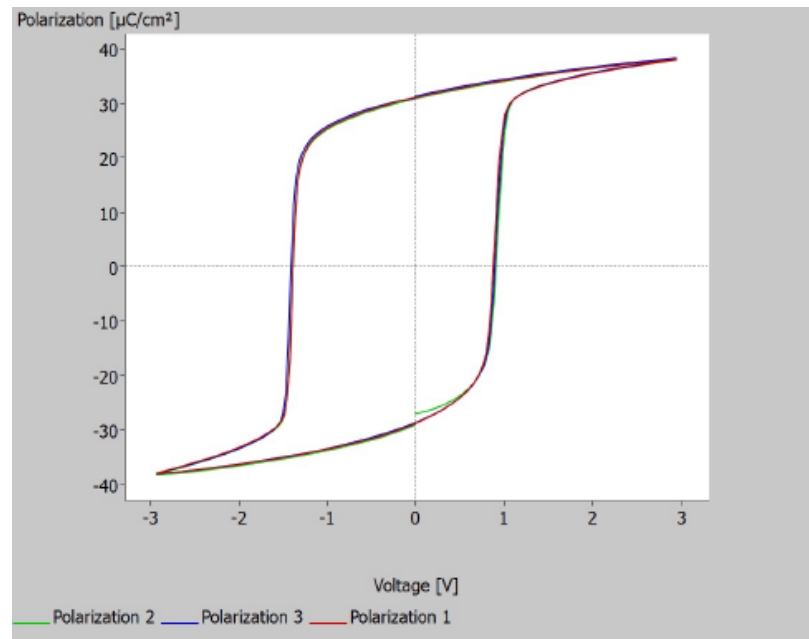


Figure 2.4: Typical DHM graph measured on the TF-1000 [24].

found.

The TF-1000 instrument measures polarization by integrating current with respect to time. However, the current measured through the ferroelectric film is a combination of the displacement current (i_c), leakage current (i_l), and the desired ferroelectric switching current (i_{fe}). For this reason the applied voltage waveform is triangular, as shown in Figure 2.5, which provides a constant $\frac{dV}{dt}$. This allows the switching current to be more easily extracted as i_c becomes constant. With this voltage pulse, a typical

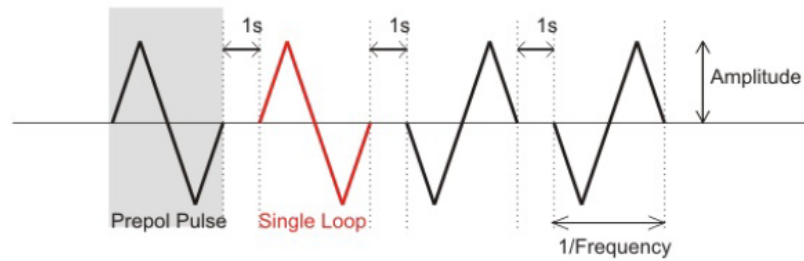


Figure 2.5: DHM triangular waveform voltage pulse [24].

current vs. voltage plot is shown in Figure 2.6 [5].

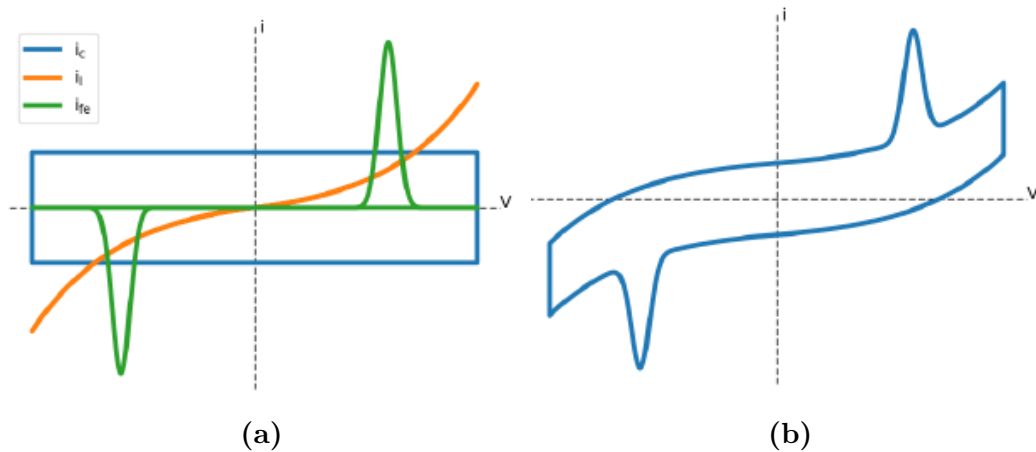


Figure 2.6: Individual current contributions of i_c , i_l , and i_{fe} (left) and total measured current for a hysteresis measurement (right) [5].

Lastly, the DHM can be used to monitor the loss of remnant polarization or coercive field over time. A fatigue measurement will cycle the sample in between a

series of hysteresis measurements in order to extract the degradation of ferroelectric parameters over the lifetime of a film.

2.2.2 Positive-Up Negative-Down (PUND)

It is often stated that hysteresis in polarization is not enough to determine whether or not a material is ferroelectric, as similar behavior can be observed from leakage effects and charge trapping [25]. The Positive-Up Negative-Down (PUND) measurement utilizes a voltage pulse sequence of two positive and two negative consecutive pulses in order to characterize the switching and non-switching characteristics of the film. In this manner, hysteresis can be confirmed to be due to ferroelectric switching behavior. The pulse sequence shown in Figure 2.7 uses a trapezoidal waveform, but can be done

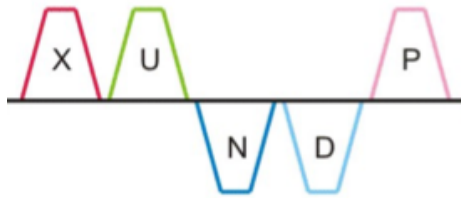


Figure 2.7: Trapezoidal PUND voltage pulse sequence [24].

with a triangular waveform similar to the DHM [5]. A typical PUND measurement is shown in Figure 2.8, with each segment of the curve color-coordinated to the individual pulses in the sequence. For a ferroelectric material the non-switching pulses (green and cyan) should trace from P_r to P_s and back, while the switching pulses (purple and blue) trace the positive and negative branches of the hysteresis curve. This characteristic ensures that polarization domains did indeed switch, and that a true remnant polarization remains at zero bias.

2.2.3 Leakage Current

From Figure 2.6 it is clear that leakage current can have a significant effect on the overall hysteresis of a measured sample. Using the leakage measurement (LM) can

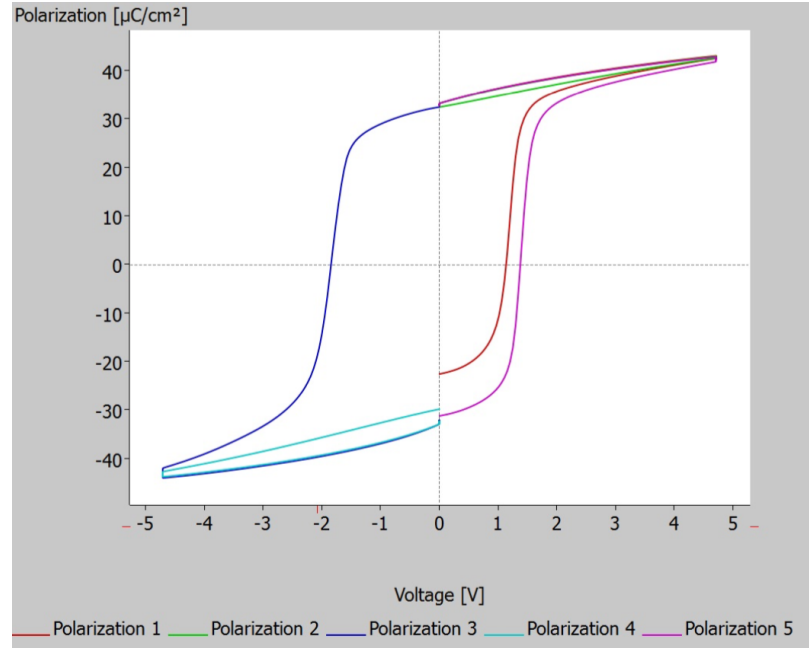


Figure 2.8: Typical PUND measurement curve [24].

therefore be useful in analyzing the effect of this current component on its own. In this measurement, the voltage waveform increases from V_{min} to V_{max} in a series of defined steps with an adjustable time duration. For smaller capacitors, two seconds is typically enough to allow for several time constants to have passed [24]. After this time has passed, the displacement current decays to zero and the measurement is taken, representing only i_t .

2.3 Summary

Various forms of elemental composition analysis such as SIMS and EDX are significant to this work as ferroelectricity in doped HfO_2 often depends on a precise concentration of dopant. GIXRD has been defined as a useful tool to determine which processing conditions will result in the correct ferroelectric crystal phase. Lastly, the electrical measurements needed to quantify the material properties of the films in this work have been described in the context of the TF-1000 parameter analyzer used at RIT.

Chapter 3

Fabrication of HfO₂ FeFETs

3.1 History and Development of the FeFET Process

Work on the FeFET process at RIT began in 2016 following studies of Si:HfO₂ capacitors deposited by NaMLab in Germany [26]. The process was originally designed to use as many mature fabrication steps from RIT's sub-CMOS process as possible [27]. Additional work required the development of an HfO₂ dry etch recipe using a chlorine based plasma. In 2017, RIT acquired the Ultratech S200 G2 Savannah ALD system used in this work. This led to the development of an in-house recipe for the deposition [28] and subsequent anneal [29] of Al:HfO₂. The first attempt at FeFETs with this film was unsuccessful due to improper source/drain formation [6], so this work seeks to attempt to successfully integrate the film into a FET process. The remainder of this section will cover details of the subsequent deposition, anneal, and etch of Al:HfO₂ as well as several process modifications for this work. The complete FET process flow is given in Appendix A.

3.1.1 ALD Deposition and Anneal

ALD of Al:HfO₂ was done using the hafnium precursor tetrakis(dimethylamido)-hafnium (TDMAHf) and the aluminum precursor trimethyl aluminum (TMA) at 200°C [28]. H₂O was used as the oxygen source rather than O₃ as this is the more

established method to ensure good step coverage and favorable electrical properties [30]. It has also been shown that the low deposition temperature of 200°C provides the best step coverage and lowest impurity levels for H₂O-based films. In O₃-based films, a deposition temperature of 320°C was needed to achieve comparably low carbon and hydrogen impurity levels [31].

In the deposition recipe, the hafnium precursor is pulsed first and reacts on the surface of the silicon substrate. Byproducts are purged before an H₂O pulse, which reacts with the now bonded hafnium atoms. The complete growth cycle produces 0.94Å of HfO₂ and is shown in Figure 3.1. The recipe used in this work repeats

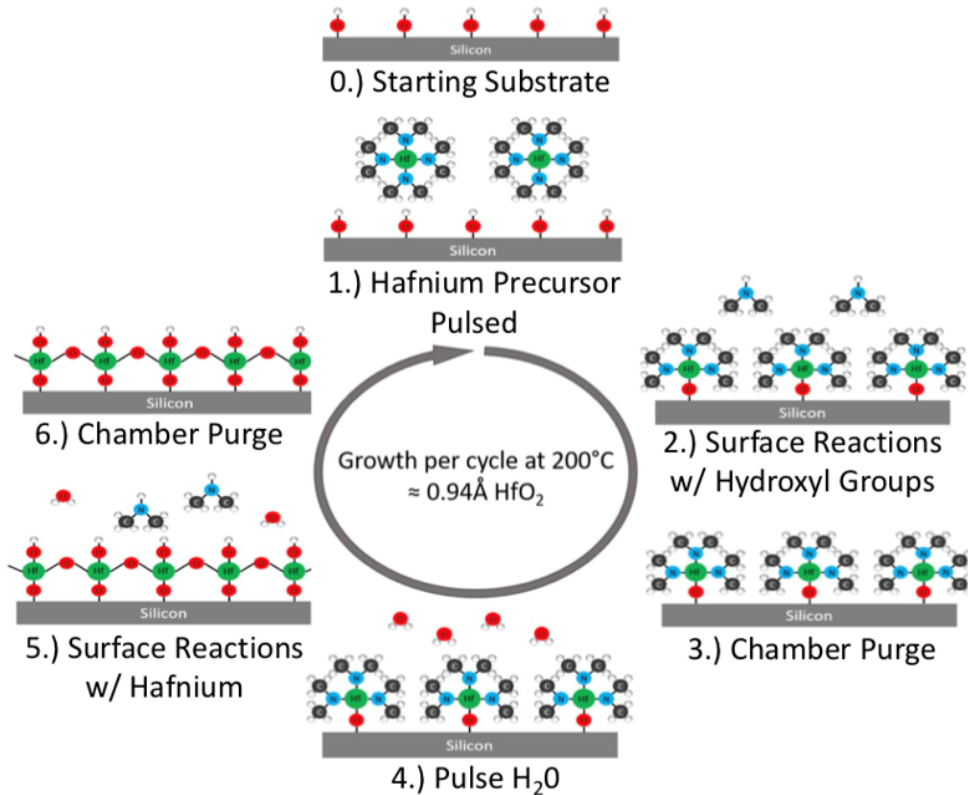


Figure 3.1: Growth cycle of ALD HfO₂ [28].

the cycle from Figure 3.1 along with intermittent pulses of TMA to dope the film. In total, there are 180 HfO₂ cycles and 5 Al cycles, thus it is believed to produce 2.7% Al:HfO₂. The film thickness is consistently between 20-22 nm as verified by ellipsometry. However, X-ray Reflectometry (XRR) measurements show a thickness

of 16 nm. The TEM image in Figure 3.2 shows a thickness of 20 nm.

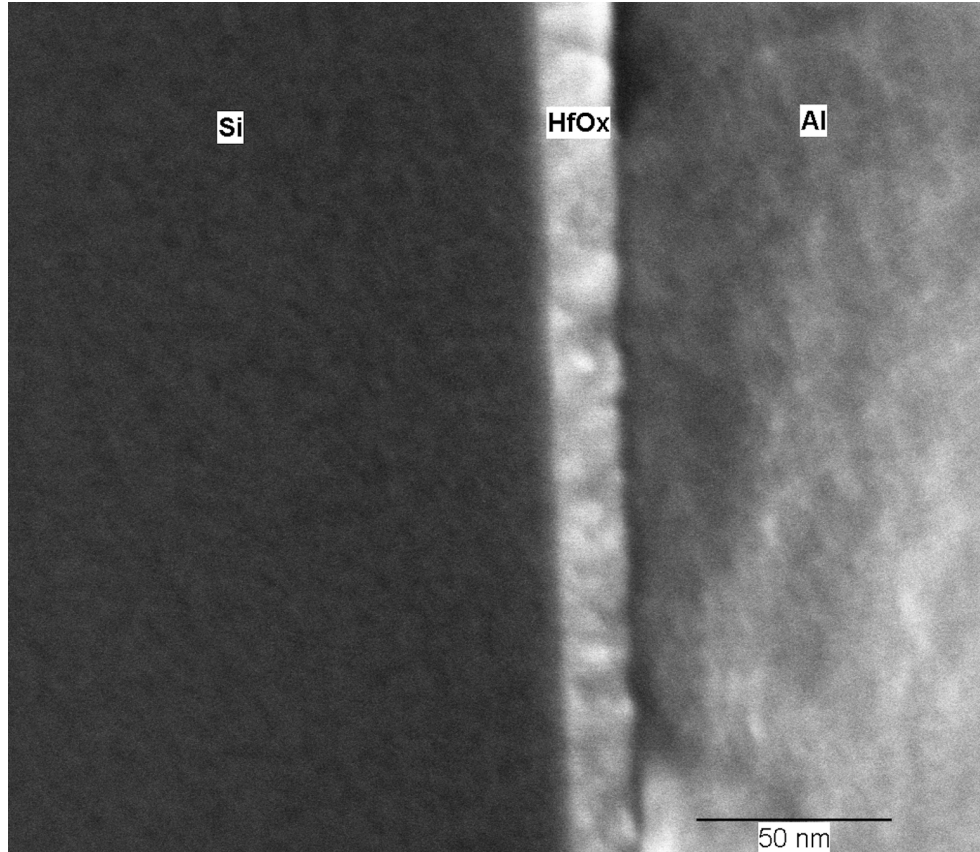


Figure 3.2: TEM image of deposited Al:HfO₂ film.

Immediately after deposition, the films were annealed via rapid thermal annealing at 1000°C for 60 seconds. Past studies of this deposition recipe have shown that these annealing conditions yield the highest P_r of 5.8 $\mu\text{C}/\text{cm}^2$ compared to lower temperatures or shorter anneal times. It has also been shown that the addition of a TiN capping layer to this recipe prior to annealing failed to yield ferroelectricity [29]. Mechanical encapsulation is generally believed to inhibit the shearing of the unit cell upon annealing, allowing the transformation to the orthorhombic phase [14]. However, some doped HfO₂ films have been shown to exhibit ferroelectricity without a capping layer, at the expense of a relatively lower P_r [32].

Various dopants are known to stabilize the tetragonal phase of HfO₂ upon nucleation, but some stress must be applied to the unit cell in order to transition to the

ferroelectric orthorhombic phase. Based on the lattice parameters of both phases, the a- and b-axes require a compressive stress while the c-axis requires a tensile stress. Several factors other than a capping layer have been reported to cause such an anisotropic stress, including the surface energy effect, island coalescence, and thermal expansion mismatch [33]. For small grain sizes, surface energy has been shown to stabilize the orthorhombic phase even in undoped HfO₂ [17]. However, at film thicknesses beyond 10 nm this effect becomes minimal and P_r becomes greatly reduced due to a higher fraction of the monoclinic phase. Park *et al* found that the coalescence stress can be as large as 30 GPa just before islands of HfO₂ and ZrO₂ coalesce to form HZO [34], well above the stress reported to induce the orthorhombic phase (4-14 GPa) [33]. Lastly, the coefficients of thermal expansion of the tetragonal phase in Mg:ZrO₂ have been shown to be anisotropic ($1.43 \times 10^{-5} \text{ K}^{-1}$ along the c-axis and $1.01 \times 10^{-5} \text{ K}^{-1}$ along the a- and b-axes) [35]. Thus, it follows that for similar materials such as HfO₂, the associated anisotropic stress upon cooling may be a factor in orthorhombic phase stabilization. However, these stresses are often considered too small to be a significant cause [33]. Ultimately, the mechanism for ferroelectric phase stabilization in HfO₂ is not completely understood. But there are certainly a number of reported contributing factors, with the capping layer being the most common.

3.1.2 HfO₂ Dry Etch

A reactive ion etch recipe was first developed in 2016 for the LAM 4600 using a chlorine based plasma [27]. The details of the recipe used in this work are shown in Table 3.1. The reaction mechanism that etches HfO₂ in this recipe begins with ion bombardment to break both Hf-O bonds. Exposed Hf sites are then passivated by Cl to produce HfCl_n (n=1-4) which becomes volatile under further ion impact. Electron impact dissociation of BCl₃ produces BCl₂⁺ which can form volatile products with O such as B₂OCl₃, B₂OCl₄, BOCl, (BOCl)₃, and B₃O₂Cl₅. Another point of note is

that these species have been shown to inhibit Si etching by the formation of a BCl_n polymer on top of Si-B bonds. Thus, the addition of BCl₃ is key to good selectivity of the etch. A low power was chosen at the expense of a fast etch rate in order to increase this selectivity, as higher energy ions may act to sputter etch this passivation layer [36]. The gas ratios of Cl₂/BCl₃/Ar were chosen to closely match that which were found to maximize selectivity to Si and SiO₂ [37].

Table 3.1: HfO₂ dry etch recipe.

Step	1	2	3	4	5
Pressure (mTorr)	120	120	120	120	0
RF Top (W)	0	0	0	0	0
RF Bottom (W)	0	150	0	150	0
Gap (cm)	3.0	3.0	3.0	3.0	5.3
O ₂ (sccm)	0	0	0	0	0
N ₂ (sccm)	20	20	50	20	20
BCl ₃ (sccm)	21	21	0	21	0
Cl ₂ (sccm)	11	11	0	11	0
Ar (sccm)	84	84	0	84	0
CFORM (sccm)	0	0	0	0	0
Complete	Stabl	Time	Time	Time	Time
Time (s)	15	250	75	250	15

Due to both a thicker film and a slower etch rate than in the past, the total etch time was increased from 150 seconds to 500 seconds. Previously, a 10 nm film showed an initial etch rate around 6 nm/min, slowing to 2 nm/min by the end of the recipe due to elevated substrate temperature [27]. However, during the past etch rate study the sample was brought to ambient after 60 seconds and the thickness was remeasured at that point. This was repeated several times until the film was etched and at that point the decrease in etch rate was observed. It was noted that this could have been due to chlorine corrosion in between each etch. To reestablish the etch rate, multiple samples of the same thickness were prepared and each sample was etched for a different time. The results are shown in Table 3.2. The etch rate is shown to decrease only slightly, and after a much longer time than in the initial

Table 3.2: HfO₂ etch rate characterization.

Time (s)	Thickness (nm)	Etch Rate (nm/min)
0	21.8	-
110	15.6	3.4
220	9.1	3.5
440	2.1	2.7

study. Therefore, it is likely that the increased substrate temperature decreases the etch rate but to a much smaller degree than previously thought.

3.1.3 Additional Process Changes

The FET process was changed from 4 photomask levels to 5 with the addition of a contact cut. Device isolation was accomplished via Local Oxidation of Silicon (LOCOS) and in prior work a Kooi oxide was etched away completely before proceeding to HfO₂ deposition. As seen in Figure 3.3, this led to exposed regions of silicon between the S/D metal and the gate metal. As a potential source of leakage, this was improved by keeping the Kooi oxide and adding contact cuts for the metal layer. Additionally, a channel stop implant was added for all nFETs. The aluminum etch was also changed to a wet etch to limit the amount of plasma processes in fabrication after the HfO₂ was deposited.

In addition to the contact cut level, the mask design was edited to bring the S/D metal closer to the channel of all transistors in an effort to reduce series resistance. Figure 3.4 shows the complete layout with the upper half dedicated to transistors of various sizes, ranging from L=1 μ m to L=40 μ m, and capacitors. The lower half of the mask includes several test structures (Van der Pauw and TLM), antiferroelectric and negative capacitance device designs, resolution markers, and alignment verniers. Figure 3.5 shows a closer look at the transistor and capacitor designs.

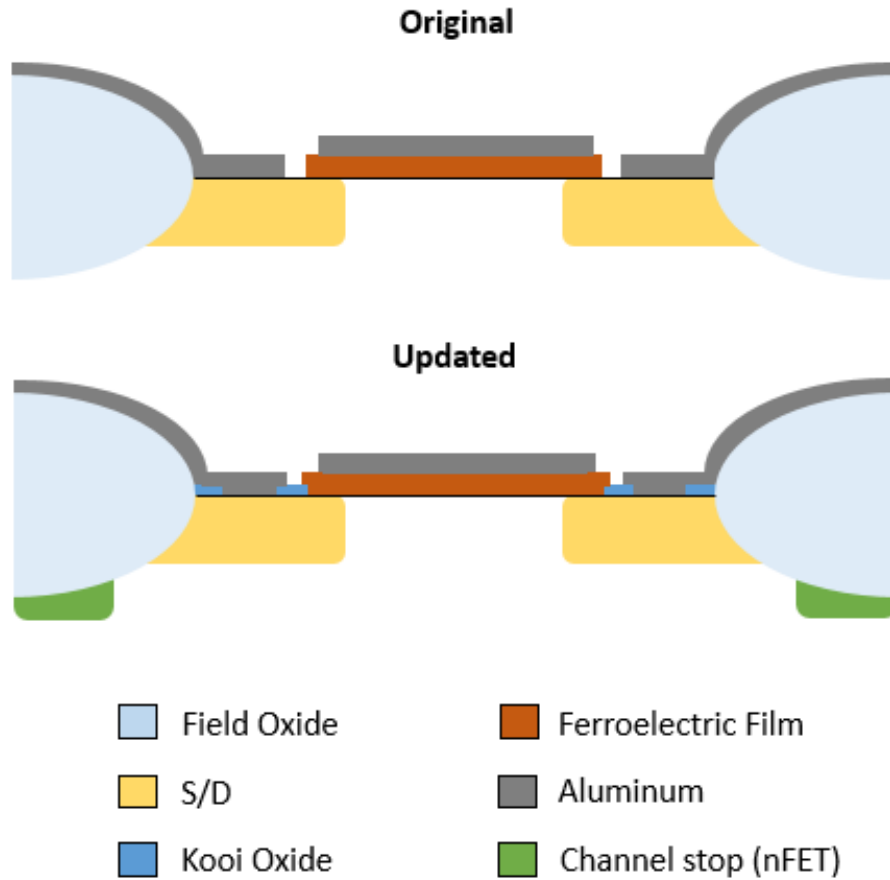


Figure 3.3: FET cross section before and after process changes.

3.2 Description of Fabricated Devices

The process was carried out on both p-type and n-type wafers with 10 Ω -cm resistivity. 20 nm Al:HfO₂ was deposited at RIT without a capping layer and 10 nm Al:HfO₂ was deposited at NaMLab with a TiN capping layer for comparison. Also, 10 nm and 15 nm HZO films were deposited at NaMLab with a TiN capping layer. The dry etch recipe in Table 3.1 and ion milling were done on the RIT deposited films for comparison. Lastly, one nFET did not use ion implantation as outlined in Appendix A for the S/D doping. Instead, a monolayer doping (MLD) process developed at RIT was implemented into the process without the need for an additional masking layer.

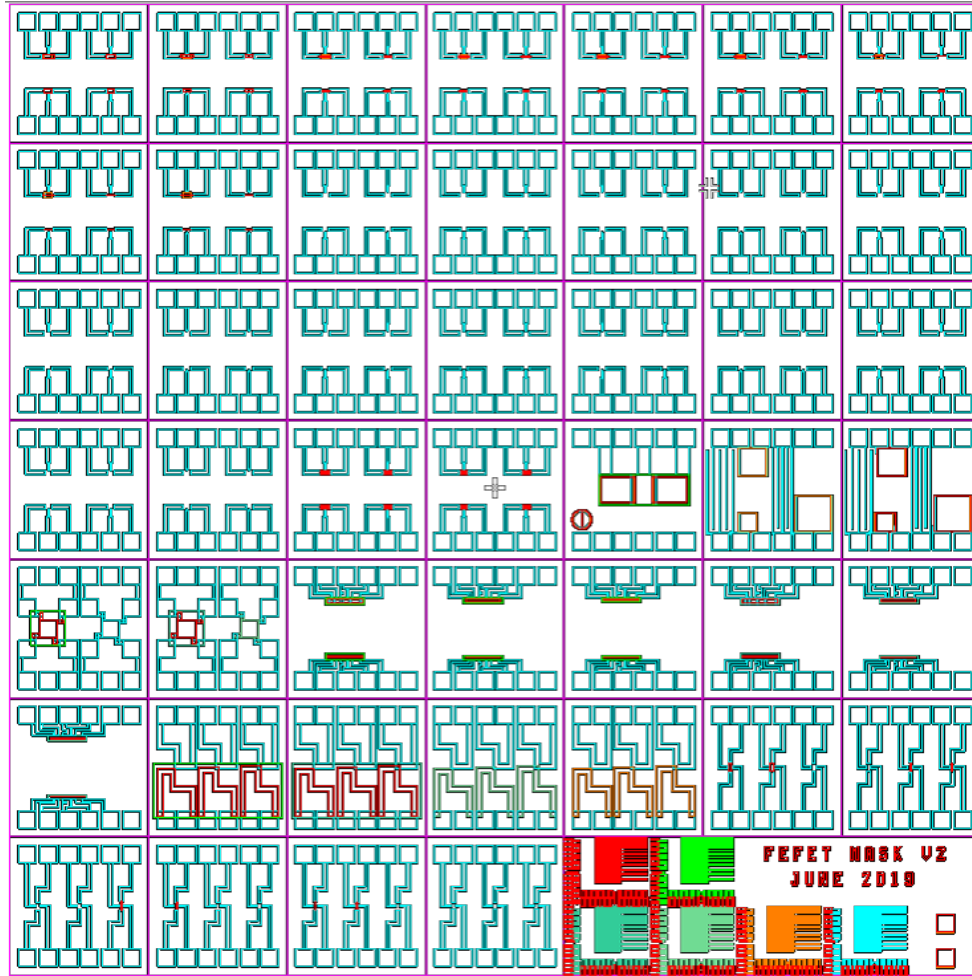
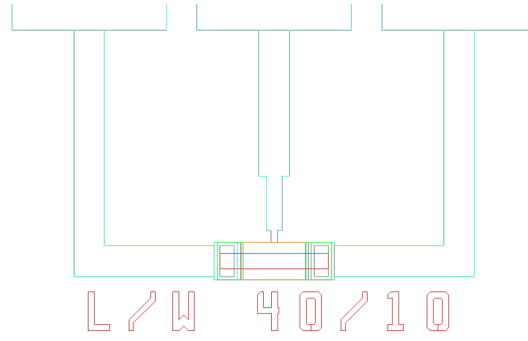


Figure 3.4: Updated FeFET mask layout.

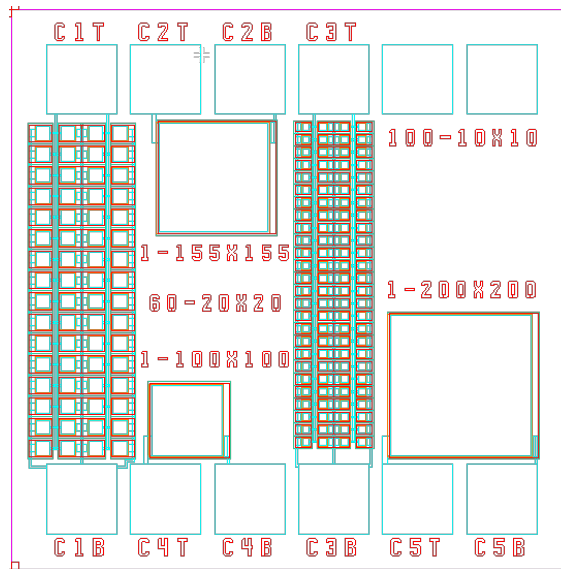
3.3 Implementation of Monolayer Doping

Monolayer doping is the use of a dopant-containing compound to form a self assembled monolayer as the source of dopant atoms with the aim of an ultra-shallow junction. In this work, Diethyl Vinyl Phosphonate (DVP) was used as the phosphorus containing compound for n-type doping of the S/D. Typically, an oxide capping layer is deposited after the monolayer is formed to prevent decomposition during the subsequent drive-in anneal. The anneal is done via rapid thermal anneal at 1100°C for 50 seconds.

Past work has implemented MLD using field oxide device isolation, with initial openings only over the S/D region rather than the entire active region of the device.



(a) Layout of a L/W 40/10 transistor



(b) Layout of MFM capacitors

Figure 3.5: Transistor and capacitor structure design.

This allowed self-assembly of the S/D region as SiO₂ is shown to block the monolayer deposition [38]. Because this work used LOCOS isolation, a different integration technique was necessary. The S/D mask was used to create openings in the Kooi oxide prior to MLD deposition. A capping layer of 1000Å was deposited via PECVD. After the anneal, sheet resistance was measured via 4-point probe on a bare silicon piece processed along side the wafer. The sheet resistance increased from 40 Ω/sq. to 290 Ω/sq. after MLD.

Due to the capping layer, a passivating oxide still remains over the active region of the device. Therefore, the original contact cut mask can still be used to create

openings for the gate and contact metal. The only difference being that there will be roughly 2000Å of oxide over the gate region (capping oxide + Kooi oxide) and just 1000Å over the S/D regions from the capping oxide.

3.4 Integration Challenges of HfO₂

Ultimately, functioning devices were only seen on the nFET wafer with RIT deposited Al:HfO₂ and etched with the Cl plasma from Table 3.1. The wafers etched using ion milling show transfer characteristics that represent no gate control over the channel of the transistor. For example, the results of an nFET with a channel length of 6 um etched using ion milling are shown in Figure 3.6.

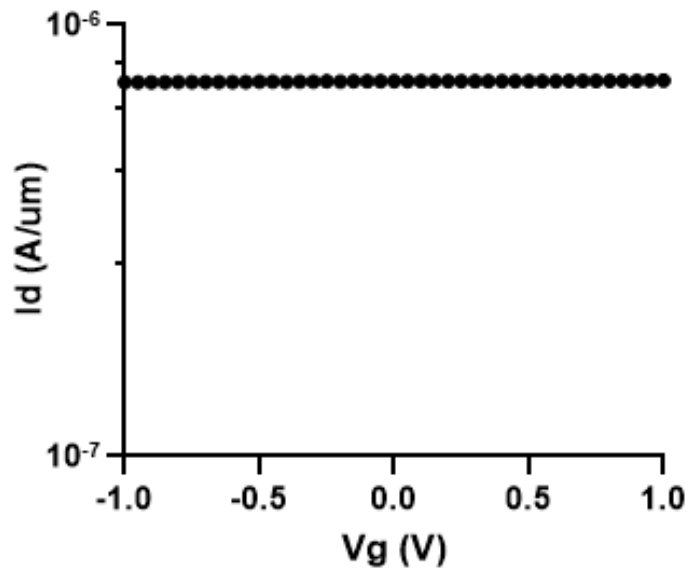


Figure 3.6: Transfer characteristic of an L=6 um device etched using ion milling.

The ion milling process hardened the photoresist protecting the gate region during the etch such that it had to be removed via ashing. Since this was the only process change between the ion milled wafers and the Cl plasma etched wafers, it was originally proposed that this may have removed the HfO₂, causing failure. This was tested using a silicon piece with 20 nm of Al:HfO₂ deposited. The piece was broken into 4 further pieces to test if any process steps that follow the gate etch effected the

film. The process steps studied were the Al wet etch, the BOE dip, and the resist ash. EDX measurements on each piece show the remaining elemental composition after each process step, shown in Table 3.3. It does not appear that any of the process steps significantly effect the composition of the film when compared to the EDX measurement of the piece measured immediately after deposition and anneal.

Table 3.3: EDX Measurements on Al:HfO₂ film after various processing steps.

Process Step	Hf atomic %	Si atomic %	O atomic %
Film deposition and anneal	2.14	92.94	4.91
Al Etch	2.09	92.73	5.18
BOE dip	2.11	93.19	4.70
Resist Ash	2.28	91.79	5.93

It was then thought that ion milling did not properly remove the HfO₂, leading to the characteristic seen in Figure 3.6. To test this, EDX area scans were performed on both a working device and a non-working device. The regions of interest are shown in Figure 3.7. Hafnium should only remain in the gate region (defined in the image

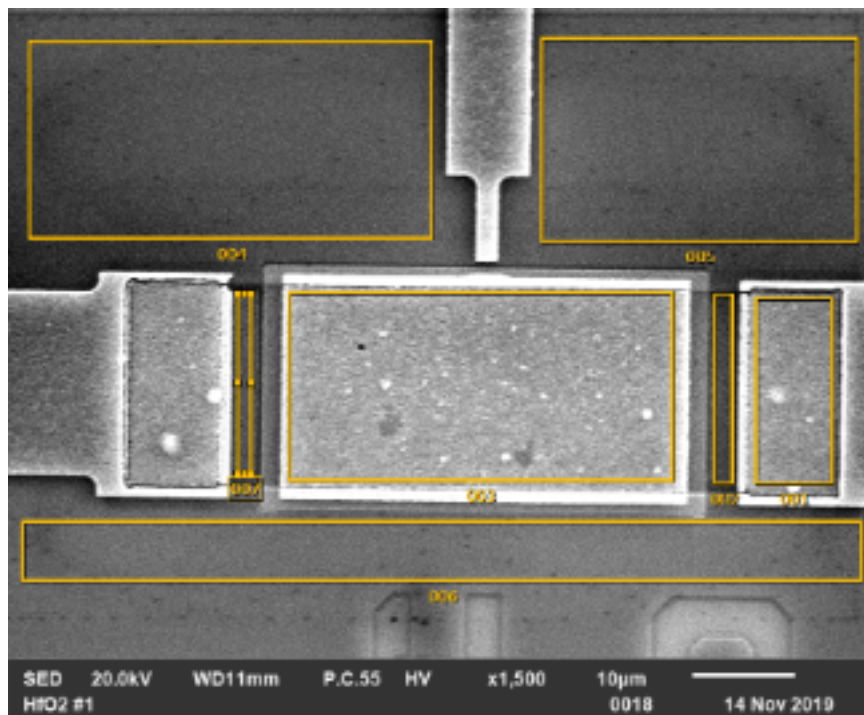


Figure 3.7: Transistor regions scanned by EDX to test Hf concentration.

as area 003) after the gate etch/ion milling. However, on the ion milled devices, the concentration of hafnium in all specified regions was on average 2.3%, nearly equal to the concentration measured on the silicon piece directly after deposition and anneal. On the other hand, the hafnium concentration in the non-gate regions on the plasma etched devices showed an average of 0.05%, a negligible amount. This seems to prove that ion milling did not remove the HfO₂ while the plasma etch did.

3.5 Summary

The details of the deposition and anneal for ferroelectric Al:HfO₂ fabricated at RIT have been discussed. Processing changes from past work, such as leaving the Kooi oxide as a passivating oxide and the addition of a contact cut masking layer are shown. The monolayer doping process is shown to be capable of being implemented without the addition of a new masking level. The evaluation of failed devices shows that ion milling did not properly remove the HfO₂ film across the wafer, leading to no apparent gate control over the channel of the devices.

Chapter 4

Analysis of Fabricated Devices

4.1 FET Analysis

Device measurements were done using an HP-4145 parameter analyzer with a 12 pad probe card. All Id-Vg measurements were taken with Vds=0.1 V. Among the various transistor channel lengths, the highest on/off current ratio was seen in the 6 um device. Below 6 um, series resistance effects became apparent in the Id-Vd measurement. The transfer characteristics for a 6 um and 4 um device are shown in Figure 4.1. The 6 um device has an on/off current ratio ranging 5 orders of magnitude versus only 3 in the 4 um device. Additionally, the off current is an order of magnitude lower in the 6 um device. The 6 um and 4 um devices show subthreshold slopes of 75 mV/dec and 73 mV/dec, respectively. Using Equation 4.1 for subthreshold slope, the density of interface traps can be calculated.

$$SS = 2.3 \frac{kT}{q} \left[\frac{C_{ox} + C_D + C_{it}}{C_{ox}} \right] \quad (4.1)$$

Where C_{ox} is the oxide capacitance, C_D is the depletion layer capacitance, and C_{it} is the interface trap capacitance. From the above equation, the density of traps is calculated to be $1.55 \times 10^{12} \text{ cm}^{-2}$. This is consistent with the number of traps seen in HfO_2 [39].

In Figure 4.3, series resistance effects become more apparent. A possible source

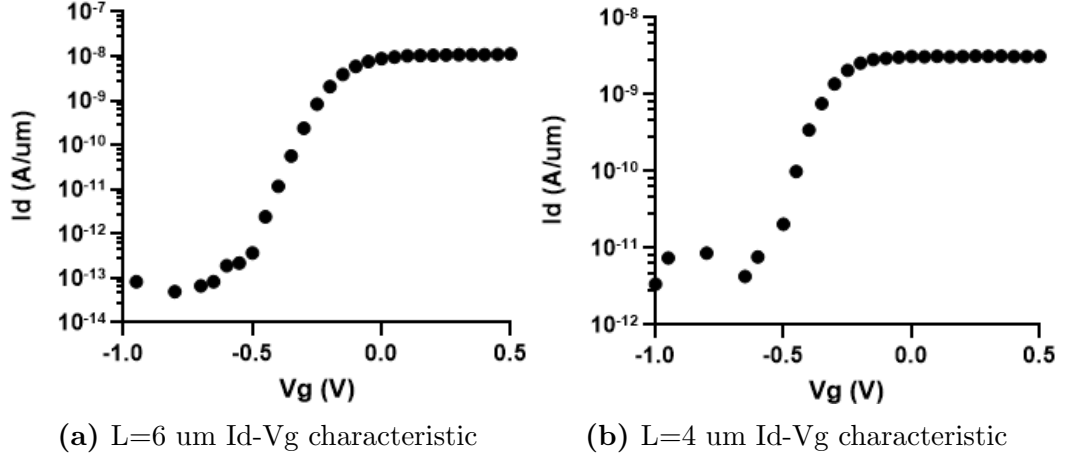


Figure 4.1: Transfer characteristics of L=6 um and L=4 um transistors.

for this added resistance could be an incomplete contact cut etch, but it is more likely to be due to remaining HfO_2 over the S/D regions. It was not possible to record the etch time that would result in a thickness of 0 nm using ellipsometry, so the etch time of 500 seconds was determined by the thickness remaining after 440 seconds (2.1 nm) in conjunction with the slowest measured etch rate (2.7 nm/min) as given in Table 3.2. EDX measurements showed 3% Hf concentration on silicon pieces with HfO_2 etched for both 440 seconds and 500 seconds. It was concluded that this was the floor for this measurement as the electron beam is capable of measuring beneath the silicon surface and some Hf may have diffused during the anneal. However, if there was HfO_2 remaining between the S/D and contact metal, there would certainly be resistive losses.

Terada-Muta analysis was performed using devices of channel length 3 um, 5 um, and 20 um. Gate voltages of -0.2 V, -0.1 V, 0 V, and 0.1 V were used to obtain a resistance value for each device. The results are plotted in Figure 4.2. The intersection of the four gate voltages show a source-drain resistance of $0.2 \text{ M}\Omega$ and an effective channel length reduced by ΔL equal to 1.5 um.

Below 4 um, transistors of channel length 3 um and 2 um still showed good transfer characteristics. However, their performance was so degraded by these resistive losses

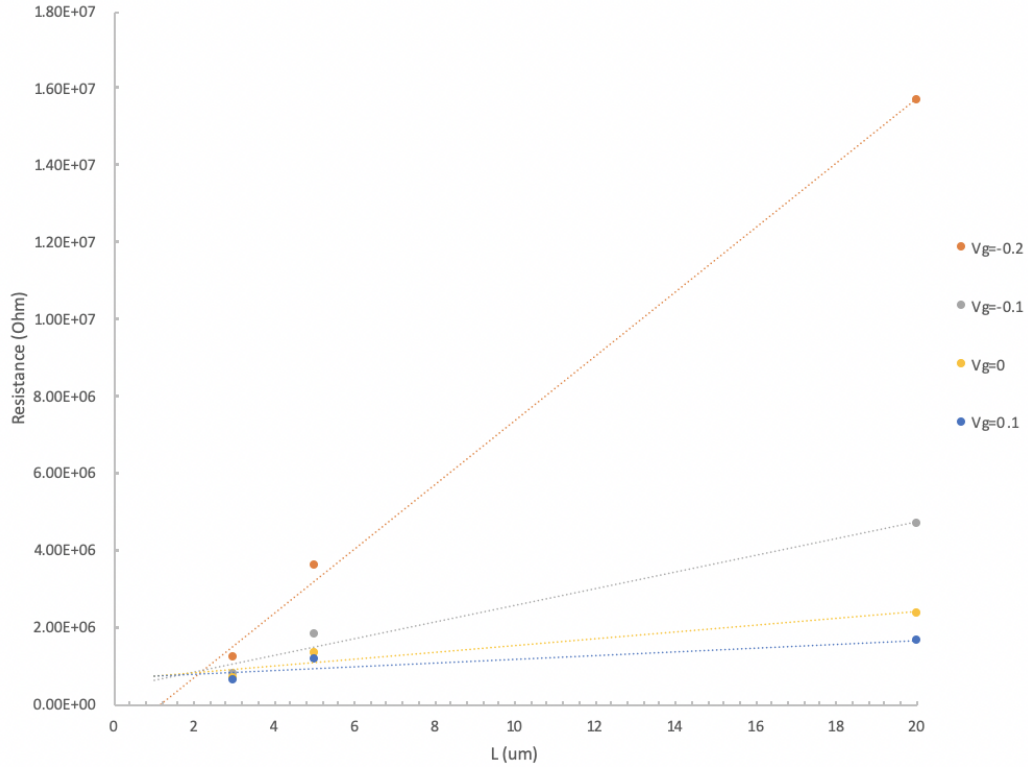


Figure 4.2: Terada-Muta analysis of fabricated devices.

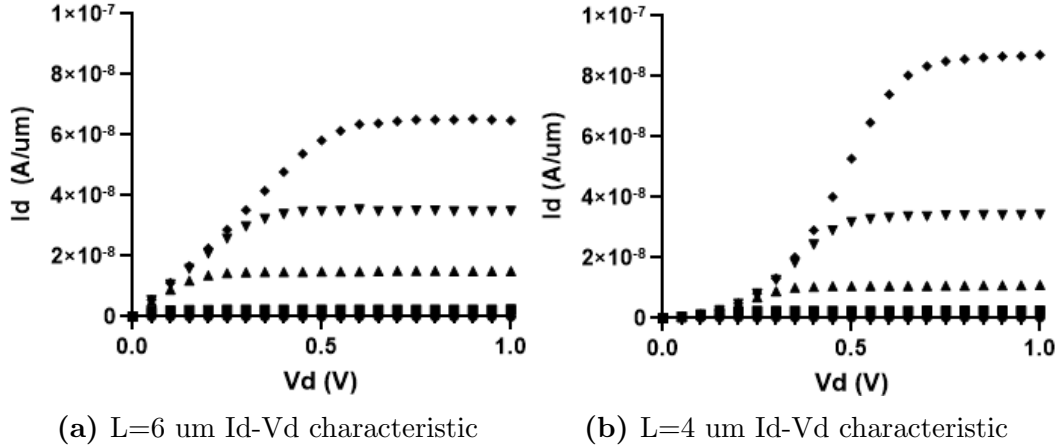


Figure 4.3: Id-Vd characteristics of L=6 um and L=4 um transistors. $V_g = 0.4$ V, 0.2 V, 0 V, -0.2 V, -0.4 V.

that they reached saturation only at much higher drain voltages compared to the 6 um or even 4 um device. At these higher drain voltages, the short channel devices began to exhibit characteristics of channel length modulation. The results of both devices are presented in Figure 4.4. The 3 um and 2 um devices each show a subthreshold

slope of 75 mV/dec.

The devices exhibit low on-state current likely due to reduced mobility. For example, the maximum transconductance for the L=6 um device was found to be 2.4×10^{-7} A/V. Using Equation 4.2, mobility was calculated to be $2.7 \text{ cm}^2/\text{Vs}$. Although mobility degradation is common in high-k dielectrics due to coulombic scattering by interface or trapped charges, this mobility value suggests additional defects [40]. The lack of a deposited interlayer between the silicon surface and high-k HfO₂ may have led to a poor interface.

$$g_m = \frac{W\mu C_{ox}}{L} V_{ds} \quad (4.2)$$

From the above results, we will consider the L=6 um transistor for further device analysis.

4.2 Threshold Voltage Shift Analysis

A gate sweep from -V_g to +V_g, then back to -V_g should result in a negative threshold voltage shift for a ferroelectric nFET. This occurs as -V_g acts to negatively polarize the HfO₂ film, accumulating positive charge in the channel thus increasing V_{TH}. Then, +V_g positively polarizes the film, depleting positive charge in the channel and decreasing V_{TH}. If such a gate sweep were to cause a positive threshold voltage shift, then the effect of charge trapping is dominating. These shifts can be visualized by Figure 4.5 [41].

An Id-V_g measurement was done with the gate voltage sweep out to 4 V on an L=6 um device. The subsequent threshold voltage shift, shown in Figure 4.6, resembles the effects of charge trapping rather than ferroelectric polarization. Furthermore, this positive shift in V_{TH} is shown to increase for higher stress amplitudes in Figure 4.7. This is evidence of an increasing amount of trapped charge and is typical in high-k

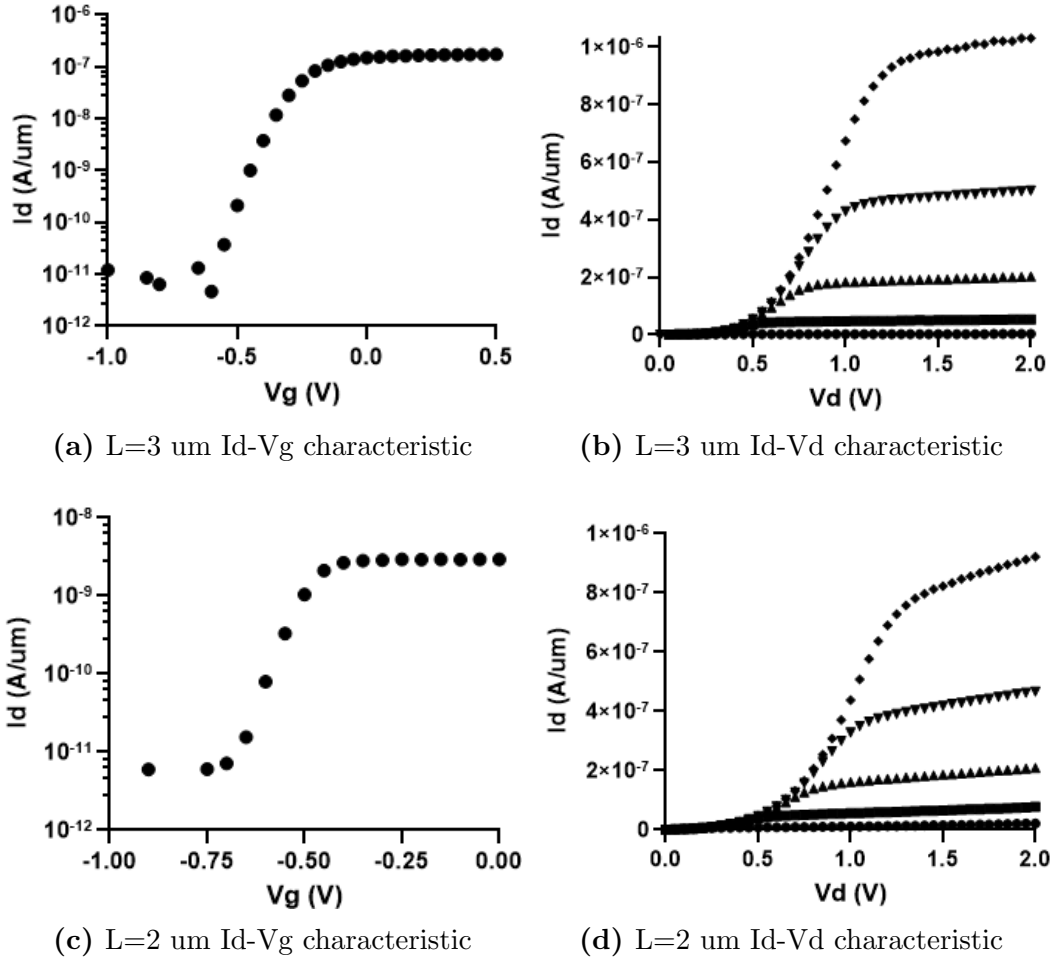
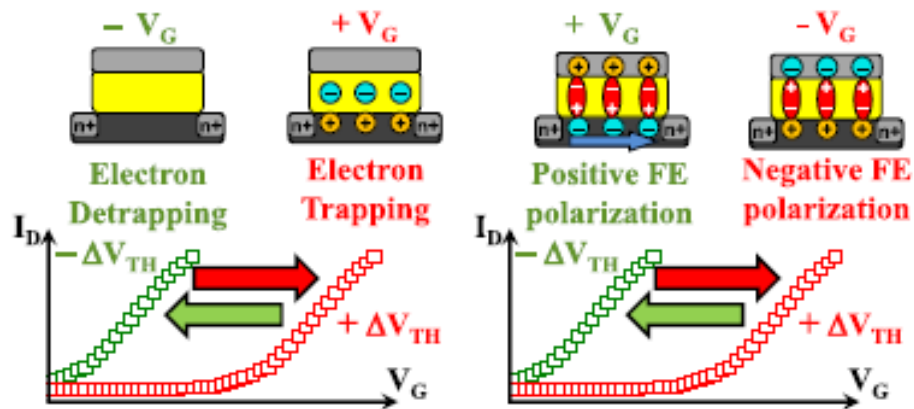


Figure 4.4: Characteristics of L=3 um and L=2 um transistors. For Id-Vd, $V_g = 0.4$ V, 0.2 V, 0 V, -0.2 V, -0.4 V.



dielectric charge trapping mechanisms [42]. The level of trapped charge for each pulse

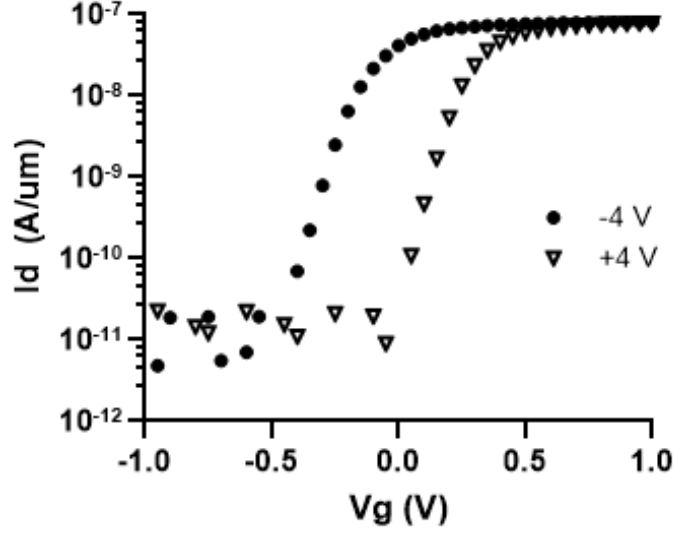


Figure 4.6: Threshold voltage shift of an $L=6 \text{ um}$ device after -4 V and $+4 \text{ V}$ gate pulses.

amplitude can be calculated using Equation 4.3.

$$\Delta V_{TH} = \frac{Q_{trap}}{C_{ox}} \quad (4.3)$$

At 4 V , the 0.4 V threshold voltage shift corresponds to a trapped charge level of $2.2 \times 10^{-12} \text{ cm}^{-2}$. At 5 V , the shift increases to 0.9 V which equates to a trapped charge level of $4.9 \times 10^{-12} \text{ cm}^{-2}$. At 6 V , there is an inconsistency in the shift of the I_d - V_g characteristic at higher gate voltages but it is apparent that the threshold voltage shift has saturated.

4.3 Charge Trapping in HfO_2

Transition metals such as hafnium present the electronic property of occupied d-shell electron states. In high-k dielectrics like HfO_2 , this property has the consequence of inducing a high number of defect states, on the order of 10^{12} - 10^{14} cm^{-2} [39]. These defects act as trap sites for electrons and holes, and have been shown to inhibit CMOS devices that attempt to integrate HfO_2 such as the FeFET. Among the issues these traps may present are mobility degradation, threshold voltage instability, and reduced

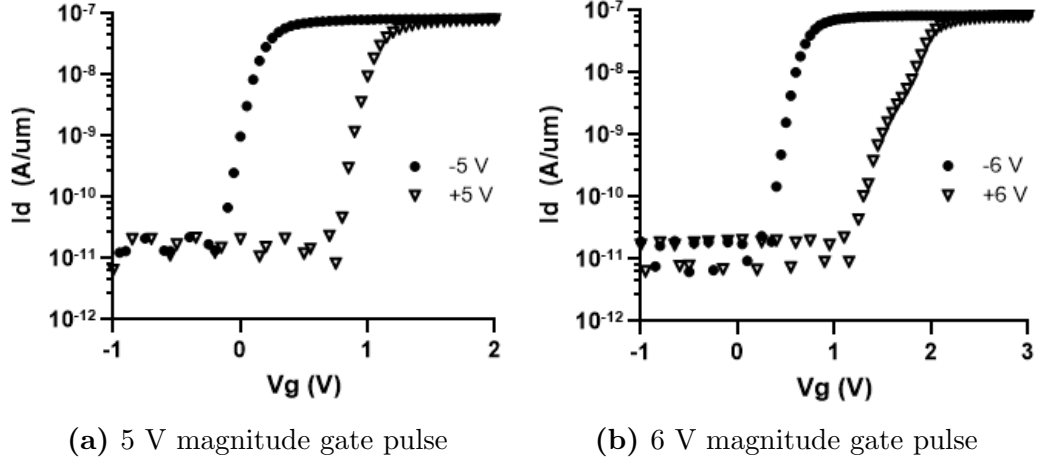


Figure 4.7: Threshold voltage shift increase with higher pulse amplitude.

endurance [41].

Oxygen transport across the gate dielectric interface is responsible for the generation of oxygen vacancies in HfO_2 which can further increase the amount of carrier traps. Estimations of oxygen trap levels have been reported as 1.2 eV and 2.5 eV below the conduction band in ZrO_2 for unoccupied and occupied vacancies, respectively. Due to similarities in electronic structure, the same is expected for HfO_2 . Because these trap levels are so close to E_C and E_V of silicon, they can easily trap carriers in a MOS device and result in threshold voltage instability [43].

Extended thermal annealing after deposition can enhance the oxygen diffusion and lead to unwanted silicate interfacial layer formation [44]. To prevent oxygen transport and increase threshold voltage stability, chemical oxide formation prior to HfO_2 deposition has been shown to be effective. Young *et al* demonstrated that as the thickness of an SiO_2 interlayer increases, the threshold voltage shift due to charge trapping decreases. A thickness of 1.9 nm showed a negligible amount of shift due to charge trapping in an HfSi_xO_y gate stack [45].

4.4 Charge Trapping in HfO₂ FeFETs

In ferroelectric HfO₂, it has been shown that there is an interplay between ferroelectric polarization and charge trapping such that the two effects are competing over the net threshold voltage shift. In fact, it has been observed that at gate pulse amplitudes lower than that necessary to facilitate ferroelectric switching, there is almost no charge trapping [41]. This is true for the devices in this work as well. In the past, the Al:HfO₂ film used here gave the hysteresis characteristics in Figure 4.8, with V_c of over 2 V [29]. In Figure 4.9, with a gate stress amplitude of 2 V, there is almost no threshold voltage shift due to either charge trapping or polarization, highlighting the correlation of the two effects.

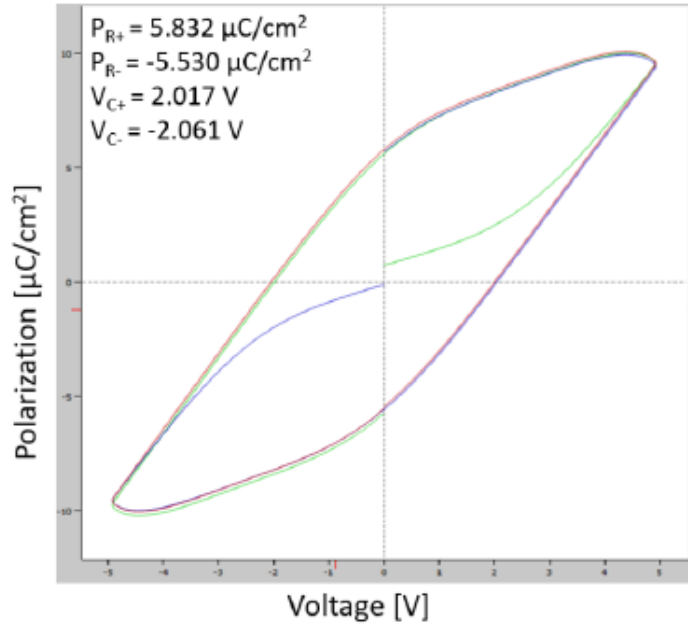


Figure 4.8: Hysteresis characteristic of Al:HfO₂ film [29].

Energy band simulations by Yurchuk *et al* reveal that charge injection through an SiO₂ interlayer is enhanced by ferroelectric polarization due to an altered effective thickness of the tunneling barrier. Under positive polarization, electron injection from the Si into HfO₂ is enhanced. While under negative polarization, hole injection into HfO₂ and back tunneling of trapped electrons into Si also show an increased

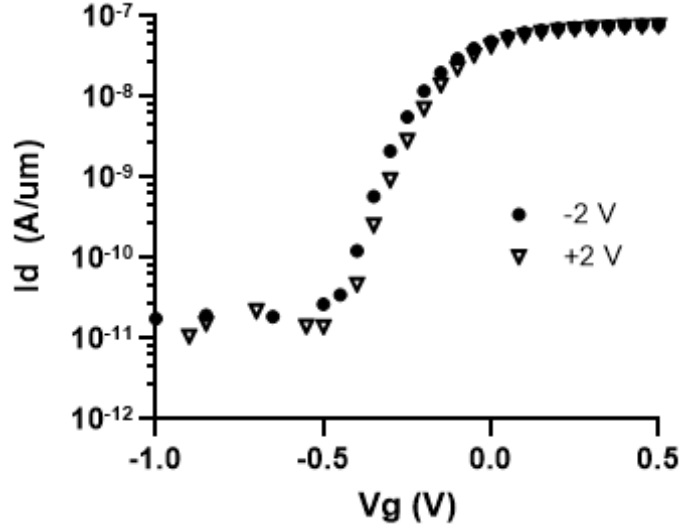


Figure 4.9: Lack of threshold voltage shift due to charge trapping below V_C .

probability [41]. These simulations show that even with the addition of an interlayer, there is an increased level of charge trapping/detrapping inherent to the ferroelectric properties of the film. In order to analyze these two effects separately, a different pulse and measurement technique is necessary.

4.5 Single Pulse Id-Vg

The single pulse Id-Vg measurement is often used to characterize trapping/detrapping mechanisms in high-k materials as it is capable of providing nanosecond scale time resolution [46]. The idea of the measurement is to record Id-Vg characteristics at the rising and falling edges of a gate pulse in order to eliminate lost charge between stressing and sensing. The drain current is commonly measured using an oscilloscope to sense the changing voltage on the drain during the stress pulse.

In an experiment with Si:HfO₂, Yurchuk *et al* utilized the single pulse technique to characterize threshold voltage shifts in 28 nm FeFETs. They first applied a pulse of -6 V to negatively polarize the film, and followed with two consecutive single pulses of +4 V with pulse widths of 0.5, 1, and 10 μ s. The two positive pulses had a delay

of one minute in order to give time for a detrapping mechanism to take place. For all pulse widths, it was found that there was a positive threshold voltage shift on the falling edge of the first pulse relative to the rising edge. This is consistent with charge trapping as previously described. After the one minute delay, there was a negative threshold voltage shift on the rising edge of the second pulse relative to the rising edge of the first pulse. This effect occurs because ferroelectric switching takes place concurrently with charge trapping during the first pulse. During the delay, charge detrapping takes place and the threshold voltage shift is then dominated by polarization [41]. The same test was carried out for pulse amplitudes ranging from 2 to 5 V and pulse widths from 0.1 to 100 μs . It was found that the positive threshold voltage shift due to charge trapping would increase as these parameters increased, while the negative shift due to polarization saturated at high pulse amplitudes and long pulse widths.

4.6 Additional Effects of Charge Trapping on the FeFET

For nonvolatile memory applications, the interplay between ferroelectric polarization and charge trapping must be considered. Because the two effects are coupled, device operation parameters must be tailored to mitigate the damage caused by trapped charge. Specifically, charge trapping has been shown to have an effect on both the retention and endurance of HfO₂ FeFETs.

As seen previously, an increased program/erase amplitude will increase the threshold voltage shift due to charge trapping, thus further countering the opposite shift due to polarization. This reduces the memory window of a FeFET by Equation 1.11. However, the retention characteristics of the device, or the time of which the memory window is sustained, has been shown to increase for these higher program/erase amplitudes. Here, the additional trapped charge compensates the ferroelectric remnant polarization thus decreasing the internal depolarization field, leading to more stable

retention [41].

The ability to maintain a steady memory window as a function of the number of program/erase cycles is referred to as the film's endurance. Continuous charge transport has been shown to reduce the endurance of ferroelectric HfO₂ through degradation of the interlayer between the film and Si [47]. In continuous cycling of Si:HfO₂ films, memory window degradation was reduced using longer delay times between program and erase pulses. This is because if the erase pulse occurs before charge detrapping has taken place, trapped charges move across the interlayer with higher energy due to the applied bias, leading to more significant degradation [48]. With a delay time of 100 ms, trapped charge had sufficient time to become detrapped and resulted in an increase in endurance from 10⁴ to 10⁵ program/erase cycles without significant decline in memory window [41].

4.7 Summary

With the pulse methodology available to the HP-4145 parameter analyzer, observed charge trapping effects are dominant in the Al:HfO₂ films deposited in this work. The effects observed are consistent with charge trapping mechanisms in terms of the direction of threshold voltage shift, and the increase in magnitude of this shift for higher stress amplitudes. Charge trapping is a common effect in high-k dielectrics due to a high level of intrinsic defects, and is especially common in HfO₂ films due to oxygen diffusion into Si. To reduce trap states caused by oxygen vacancies, a thin interlayer deposited prior to ALD of HfO₂ can be employed. To properly analyze the characteristics of charge trapping, a new methodology with a finer time resolution is necessary. It is significant to fully understand these effects as the retention and endurance of FeFETs are correlated with charge trapping, along with the memory window.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This work has focused on the implementation of Al:HfO₂ as a ferroelectric material for FeFET memory devices. Using an ALD recipe and annealing conditions developed at RIT, Al:HfO₂ was successfully utilized as the gate dielectric in an n-channel FET. A chlorine plasma etch was also developed and tailored to etch the 20 nm Al:HfO₂ film, as confirmed by EDX measurements. In an effort to compare the results of this etch with ion milling, it was discovered that ion milling was not successful in removing HfO₂.

Of the successful nFET devices, it was found that below a channel length of 6 μm , parasitic resistance effects led to degraded device performance. However, the devices did show an average subthreshold swing of 75 mV/dec. Using this value, the level of interface traps was calculated to be $1.55 \times 10^{12} \text{ cm}^{-2}$.

Under pulse testing, it was found that the threshold voltage shift was positive for positive bias on the gate. This characteristic is indicative of charge trapping rather than ferroelectricity, where the threshold voltage shift should be negative for positive bias on the gate. Furthermore, it was shown that the threshold voltage shift would increase at higher pulse amplitudes. Calculations show that the level of trapped charge saturated at a 5 V pulse amplitude with a value of $4.9 \times 10^{12} \text{ cm}^{-2}$.

5.2 Future Work

The most significant process improvement to consider is the addition of a thin interlayer between the silicon surface and Al:HfO₂ gate dielectric. This has been shown to reduce the effects of charge trapping due to the elimination of oxygen transport from the HfO₂ into silicon [45]. The densification of the SiO₂ naturally formed on a silicon surface has been shown to function as an interlayer as well [49]. Additionally, the annealing conditions should be reevaluated to induce the ferroelectric phase with the application of a capping layer. This will ensure the transition to the orthorhombic phase of HfO₂ [14].

The capping layer may also prevent damage to the HfO₂ gate dielectric occurring at processing steps after deposition and anneal. Although Table 3.3 shows that there was no change in Hf concentration after the Al wet etch, there was some visible damage to the piece studied in that experiment. Furthermore, the high power Al sputter directly onto the HfO₂ may be a source of damage as well. Lastly, sintering of the Al may cause diffusion into the ferroelectric film in the absence of a proper capping layer.

An additional point of future work is the simulation of devices fabricated with the Al:HfO₂ film. Work has recently began using Silvaco ATLAS and ATHENA along with the ferro package to simulate ferroelectric capacitors. Further study is needed to fully implement the package into a FeFET model. Lastly, a modified FeFET process as described above will allow for the design of more advanced ferroelectric devices such as Ferroelectric Tunnel Junctions (FTJs) and memristor crossbar arrays for neuromorphic computing applications.

References

- [1] J. Scott, *Ferroelectric Memories*. Springer Series in Advanced Microelectronics, 2000, vol. 3.
- [2] S. L. Moskowitz, *Advanced Materials Innovation: Managing Global Technology in the 21st Century*. John Wiley & Sons, Inc., 2016.
- [3] K. Uchino, *Ferroelectric Devices*. Marcel Dekker, 2000.
- [4] S. Kasap, *Principles of Electronic Materials and Devices*. McGraw-Hill, 2006.
- [5] J. Anderson, “Measurement of ferroelectric films in mfm and mfis structures,” Master’s thesis, Rochester Institute of Technology, 2017.
- [6] J. Merkel, “Fefet process integration and characterization,” in *37th Annual Microelectronic Engineering Conference*, 2019.
- [7] S. Miller, R. Nasby, J. Schwank, M. Rodgers, and P. Dressendorfer, “Device modeling of ferroelectric capacitors,” *Journal of Applied Physics*, vol. 68, no. 12, pp. 6463–6471, 1990.
- [8] S. Miller and P. McWhorter, “Physics of the ferroelectric nonvolatile memory field effect transistor,” *Journal of Applied Physics*, vol. 72, no. 12, pp. 5999–6010, 1992.
- [9] J. Brews, “A charge-sheet model of the mosfet,” *Solid State Electronics*, vol. 21, pp. 345–355, 1978.
- [10] Y. Arimoto and H. Ishiwara, “Current status of ferroelectric random-access memory,” *MRS Bulletin*, vol. 29, no. 11, pp. 823–828, 2004.
- [11] J. Wang, H. Li, and R. Stevens, “Hafnia and hafnia toughened ceramics,” *Journal of Materials Science*, vol. 27, pp. 5397–5430, 1992.

REFERENCES

- [12] R. van Santen, “The ostwald step rule,” *Journal of Physical Chemistry*, vol. 88, pp. 5768–5769, 1984.
- [13] D. Porter and K. Easterling, *Phase Transformations in Metals and Alloys*. Chapman and Hall, 1992, vol. 2.
- [14] T. Boscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger, “Ferroelectricity in hafnium oxide thin films,” *Applied Physics Letters*, vol. 99, no. 102903, pp. 1–3, 2011.
- [15] K. Tomida, K. Kita, and A. Toriumi, “Dielectric constant enhancement due to si incorporation in hfo₂,” *Applied Physics Letters*, vol. 89, no. 142902, pp. 1–3, 2006.
- [16] J. Muller, P. Polakowski, S. Mueller, and T. Mikolajick, “Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects,” *ECS Journal of Solid State Science and Technology*, vol. 4, no. 5, pp. 30–35, 2015.
- [17] P. Polakowski and J. Muller, “Ferroelectricity in undoped hafnium oxide,” *Applied Physics Letters*, vol. 106, no. 232905, pp. 1–5, 2015.
- [18] J. Muller, P. Polakowski, J. Paul, S. Riedel, R. Hoffmann, M. Drescher, S. Slesazeck, S. Muller, H. Mulaosmanovic, U. Schroeder, T. Mikolajick, S. Flachowsky, E. Erben, E. Smith, R. Binder, D. Triyoso, J. Metzger, and S. Kolodinski, “Integration challenges of ferroelectric hafnium oxide based memory,” *ECS Transactions*, vol. 69, no. 3, pp. 85–95, 2015.
- [19] J. Muller, T. Boscke, D. Brauhaus, U. Schroder, U. Bottger, J. Sundqvist, P. Kucher, T. Mikolajick, and L. Frey, “Ferroelectric hf_{0.5}zr_{0.5}o₂ thin films for nonvolatile memory applications,” *Applied Physics Letters*, vol. 99, no. 112901, pp. 1–3, 2011.

REFERENCES

- [20] Introduction to sims. [Online]. Available: <https://www.cameca.com/products/sims/technique>
- [21] Grazing incidence x-ray scattering and diffraction on thin films. [Online]. Available: <https://www-ssrl.slac.stanford.edu/materialscatter/scatter-grazing.html>
- [22] Transmission electron microscopy (tem). [Online]. Available: <https://warwick.ac.uk/fac/sci/physics/current/postgraduate/regs/mpagswarwick/ex5/techniques/structural/tem/>
- [23] Energy dispersive x-ray spectroscopy (eds). [Online]. Available: <https://www.mee-inc.com/hamm/energy-dispersive-x-ray-spectroscopyeds/>
- [24] aixACCT Systems GmbH, *aixPlover Software Manual for TF Analyzer 1000*, 2014.
- [25] J. Scott, “Ferroelectrics go bananas,” *Journal of Physics: Condensed Matter*, vol. 20, no. 021001, pp. 1–2, 2008.
- [26] K. Florent, “Ferroelectric hfo₂ for emerging ferroelectric semiconductor devices,” Master’s thesis, Rochester Institute of Technology, 2015.
- [27] J. McGlone, “Ferroelectric hfo₂ thin films for fefet memory devices,” in *34th Annual Microelectronic Engineering Conference*, 2016.
- [28] C. Gonta, “Atomic layer deposition of ferroelectric hfo₂,” in *35th Annual Microelectronic Engineering Conference*, 2017.
- [29] J. Eschle, “Annealing study of ald deposited ferroelectric aluminum-doped hafnium oxide,” in *36th Annual Microelectronic Engineering Conference*, 2018.
- [30] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskela, “Atomic layer deposition of hafnium dioxide films from hafnium tetrakis(ethylmethanamide) and water,” *Chemical Vapor Deposition*, vol. 8, no. 5, pp. 199–204, 2002.

- [31] X. Liu, S. Ramanathan, A. Longdergan, A. Srivastava, E. Lee, T. Seidel, J. Barton, D. Pang, and R. Gordon, "Ald of hafnium oxide thin films from tetrakis(ethylmethyamido)hafnium and ozone," *Journal of the Electrochemical Society*, vol. 152, no. 3, pp. 213–219, 2005.
- [32] M. Park, Y. Lee, H. Kim, Y. Kim, T. Moon, K. Kim, J. Muller, A. Kersch, U. Schroeder, T. Mikolajick, and C. Hwang, "Ferroelectricity and antiferroelectricity of doped thin hfo₂ based films," *Advanced Materials*, vol. 27, no. 11, pp. 1811–1831, 2015.
- [33] Z. Fan, J. Chen, and J. Wang, "Ferroelectric hfo₂ based materials for next generation ferroelectric memories," *Journal of Advanced Dielectrics*, vol. 6, no. 2, pp. 1–11, 2016.
- [34] M. Park, H. Kim, Y. Kim, T. Moon, and C. Hwang, "The effects of crystallographic orientation and strain of thin hf_{0.5}zr_{0.5}o₂ film on its ferroelectricity," *Applied Physics Letters*, vol. 104, no. 072901, pp. 1–5, 2014.
- [35] E. Kisi, "Influence of hydrostatic pressure on the t to o transformation in mg psz studied by in situ neutron diffraction," *Journal of the American Chemical Society*, vol. 81, no. 3, pp. 741–745, 1998.
- [36] J. Shoeb and M. Kushner, "Mechanisms for plasma etching of hfo₂ gate stacks with si selectivity and photoresist trimming," *Journal of Vacuum Science and Technology*, vol. 27, no. 6, pp. 1289–1302, 2009.
- [37] Y. H. Joo, J. C. Woo, X. Yang, and C. I. Kim, "Temperature dependence on dry etching of hafnium oxide using an inductively coupled plasma," *Ferroelectrics*, vol. 406, no. 1, pp. 176–184, 2010.
- [38] J. Doran, "Self-assembled monolayers for phosphorus doping of silicon for field effect devices," Master's thesis, Rochester Institute of Technology, 2018.

- [39] G. Bersuker, J. Sim, C. S. Park, C. Young, S. Nadkarni, R. Choi, and B. H. Lee, "Mechanism of electron trapping and characteristics of traps in hfo₂ gate stacks," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 138–145, 2007.
- [40] S. Mathew, L. Bera, N. Balasubramanian, M. Joo, and B. Cho, "Channel mobility degradation and charge trapping in high-k/metal gate nmosfets," *Thin Solid Films*, vol. 462, pp. 11–14, 2004.
- [41] E. Yurchuk, J. Muller, S. Muller, J. Paul, M. Pesic, R. van Bentum, U. Schroeder, and T. Mikolajick, "Charge trapping phenomena in hfo₂ based fet type non-volatile memories," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3501–3507, 2016.
- [42] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumot, and F. Martin, "Characterization and modeling of hysteresis phenomena in high-k dielectrics," *IEDM Technical Digest*, pp. 737–740, 2004.
- [43] H. Takeuchi, H. Y. Wong, D. Ha, and T. J. King, "Impact of oxygen vacancies on high k-gate stack engineering," *IEDM Technical Digest*, pp. 829–832, 2004.
- [44] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima, and T. Arikado, "Oxygen vacancy induced substantial threshold voltage shifts in the hf based high-k misfet with p+poly si gates," *Japanese Journal of Applied Physics*, vol. 43, no. 11, pp. 1413–1415, 2004.
- [45] C. Young, R. Choi, J. Sim, B. Lee, P. Zeitzoff, Y. Zhao, K. Mathews, G. Brown, and G. Bersuker, "Interfacial layer dependence of hfsi_xo_y gate stacks on v_T instability and charge trapping using ultra short pulse iv characterization," *43rd Annual International Reliability Physics Symposium*, pp. 75–79, 2005.

- [46] C. Young, Y. Zhao, M. Pendley, B. H. Lee, K. Matthews, J. H. Sim, R. Choi, G. Brown, R. Murto, and G. Bersuker, “Ultra short pulse current-voltage characterization of the intrinsic characteristics of high-k devices,” *Japanese Journal of Applied Physics*, vol. 44, no. 4S, pp. 2437–2440, 2005.
- [47] E. Yurchuk, S. Mueller, D. Martin, S. Slesazek, U. Schroeder, and T. Mikolajick, “Origin of the endurance degradation in the novel hfo₂ based 1t ferroelectric non-volatile memories,” *IEEE International Reliability Physics Symposium*, pp. 2E.5.1–2E.5.5, 2014.
- [48] A. Kerber and E. Cartier, “A fast four-point sense methodology for extraction of circuit-relevant degradation parameters,” *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 912–914, 2010.
- [49] B. Dorvel, B. Reddy, J. Go, C. Guevara, E. Salm, M. Alam, and R. Bashir, “Silicon nanowires with high-k hafnium oxide dielectrics for sensitive detection of small nucleic acid oligomers,” *ACS Nano*, vol. 6, no. 7, pp. 6150–6164, 2012.

Appendix A: FeFET Process Flow

Process Step	Tool - Description
1	RCA Clean
2	Zero Level Litho
3	LAM 490 - Zero Level Etch
4	LAM 490 - Resist Ash
5	RCA Clean
6	FURNACE04 - Pad Oxide Growth (tgt 50 nm)
7	LPCVD - Nitride Deposition (tgt 150 nm)
8	SVG/ASML - Level 1 Litho (Active)
9	LAM 490 - Nitride Etch
10	Channel Stop Implant - B ¹¹ , 8x10 ¹³ cm ⁻² @ 100 keV
11	LAM 490 - Resist Ash
12	RCA Clean
13	FURNACE01 - Field Oxide Growth (tgt 650 nm)
14	Hot Phos - Nitride Etch
15	10:1 BOE - Pad Oxide Etch
16	FURNACE01 - Kooi Oxide Growth (tgt 100 nm)
17	SVG/ASML - Level 2 Litho (S/D)
18	S/D Implant - B ¹¹ /P ³¹ , 2x10 ¹⁵ cm ⁻² @ 60 keV/100 keV
19	LAM 490 - Resist Ash
20	RCA Clean
21	FURNACE01 - S/D Anneal (900°C in N ₂ , 30 min)
22	SVG/ASML - Level 3 Litho (Contact Cut)
23	10:1 BOE - Kooi Oxide Etch
24	Solvent Bath - Resist Strip
25	RCA Clean
26	ALD - Al:HfO ₂ Deposition (tgt 20 nm)
27	RTP - Al:HfO ₂ Anneal (1000°C, 60 sec)
28	SVG/ASML - Level 4 Litho (Gate)
29	LAM 4600 - Al:HfO ₂ Etch
30	Solvent Bath - Resist Strip
31	10:1 BOE Dip
32	CVC 601 - Al Sputter (tgt 400 nm)
33	SVG/ASML - Level 5 Litho (Metal)
34	Al Wet Etch
35	Solvent Bath - Resist Strip
36	Freckle Etch
37	FURNACE02 - Al Sinter (450°C in H ₂ /N ₂ , 20 min)