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Implant Activated Source/Drain Regions for Self-Aligned IGZO TFT

RAHNUMA RIFAT CHOWDHURY
November 2019

A Thesis Submitted
In Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

RIT | Kate Gleason College of Engineering

Department of Electrical and Microelectronic Engineering

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Rahnuma Rifat Chowdhury

A thesis submitted in partial fulfillment of the requirements for the degree of
Master of Science in Microelectronic Engineering

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ABSTRACT

In this work, amorphous Indium-Gallium-Zinc-Oxide (IGZO) TFTs with channel lengths scaled as small as L = 1 μm are presented which demonstrate excellent electrical characteristics, however the traditional metal-contact defined source/drain regions typically require several microns of gate overlap in order to provide ohmic behavior with minimal series resistance and ensure tolerance to overlay error. In addition, further scaling the channel length by simply reducing the source/drain metal gap is not feasible. The focus of this study is to investigate techniques to realize self-aligned (SA) IGZO TFTs that are not subject to gate-source/drain misalignment due to overlay error or process bias. Top gate (TG) co-planar and bottom gate (BG) staggered TFTs are fabricated using plasma immersion and ion implantation to selectively form conductive IGZO regions, with the channel region blocked by a gate-defined mask. Among the investigated treatments, oxygen plasma activation and ion implanted activation via $^{11}B^{+}$ and $^{40}Ar^{+}$ has been successfully demonstrated. Due to metal gate charging during ion implantation of SA-TG devices, the characteristics show a significant left-shift whereas SA-BG devices do not show this behavior. Electrical results suggest a defect-induced mechanism is involved with $^{40}Ar^{+}$ implant activation of the S/D regions. However, $^{11}B^{+}$ implant activation is attributed to the formation of an electrically active donor species involving chemical bonding. Both boron and argon demonstrate pronounced degradation in charge injection at higher dose treatments. Finally, a novel lithographic strategy which utilizes top-side flood exposure rather than a back-side through-glass exposure has also been explored, which would enable SA-BG devices on non-transparent substrates.

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Chapter 1. INTRODUCTION

There has been a tremendous upsurge in the display industry over last few decades in the growth of Active Matrix Liquid Crystal Display (AMLCD) for Flat-panel Displays (FPDs) due to the increasing demand for displays with higher resolution, faster response rate and better quality. The active-matrix FPDs use a backplane consisting of Thin-Film Transistors (TFTs) that connects the pixels to the addressing lines to create an image on the front surface of display. This section provides an overview of the display and TFT technologies currently being used in the FPD industry.

1.1 LIQUID CRYSTAL DISPLAY

Liquid crystal displays (LCDs) have widespread applications in several hardware products and is projected to increase. They use a backlight to illuminate the display panel. The backlight used to be generated using Cold-Cathode Fluorescent Lamps (CCFLs) but recently Light-Emitting Diodes (LEDs) are being used for their higher efficiency. The glass panel installed over the diffuser consists of multiple layers. Two polarization filters oriented at 90° to each other where, the first filter polarizes the unpolarized incident light from the source and the second filter blocks out the light as it is rotated by 90° with respect to the upper filter.

A liquid crystal is used in between the two polarizers to rotate the initially polarized light from the first polarizer by 90° in order to pass through the second polarization filter. LCD, such as the one depicted in Figure 1.1, generally uses a twisted-nematic liquid crystal structure which twists

the molecules 90° upon applying a voltage across the crystal which is controlled using a thin-film transistor (TFT). This enables rotation of the polarized light and allows it to pass through the second polarizer to the front surface of the display.

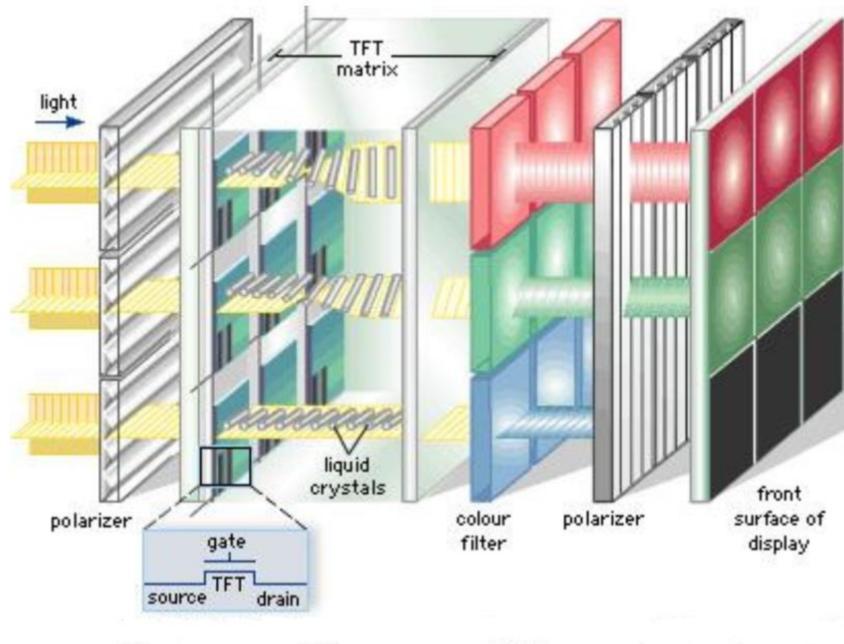
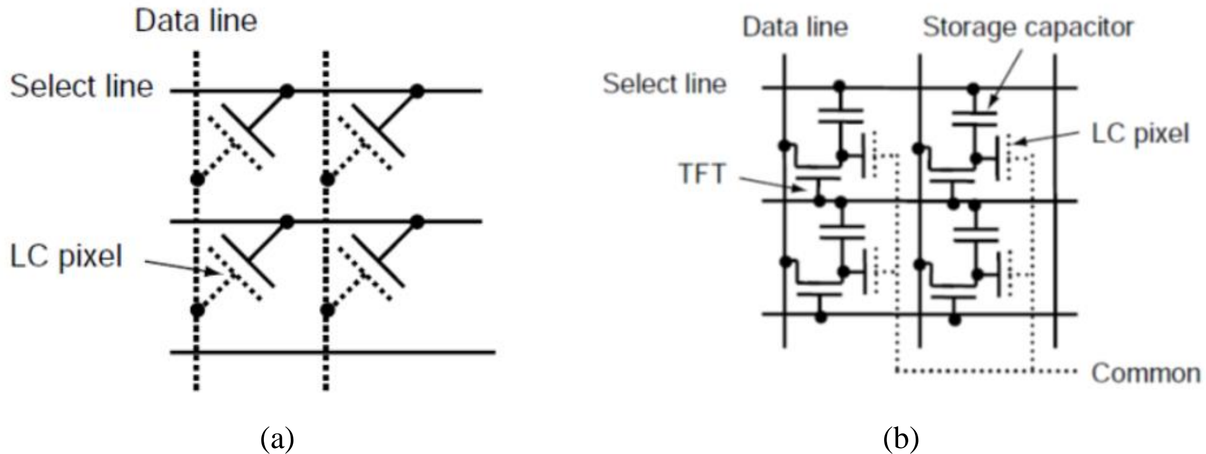


Figure 1.1: Structure of LCD panel with TFT. Adapted from [1].

1.2 PIXEL ADDRESSING

There are mainly two types of display structures for pixel addressing: Passive-matrix and Active-matrix. For passive-matrix display, a grid is created using horizontal and vertical wires. At the intersection of each grid an LCD is connected which translates to a pixel. The wires are connected to integrated circuits that control the charge to each pixel. To turn on a pixel, the integrated circuit sends voltage to the corresponding column and the corresponding row is grounded to complete the circuit. This mechanism involving direct addressing of the pixel is degraded by two main issues: slow response time and poor voltage control. As a result of poor

voltage control, adjacent pixels would also be partially turned on when addressing a particular pixel causing Mura effect.



(a) (b)

Figure 1.2: Circuit diagram for pixel addressing in a) passive matrix LCD and b) active matrix LCD.

The active-matrix display provides an improved mechanism by using a thin-film transistor to address each pixel and refresh the screen more frequently. Active-matrix displays consist of a switching TFT and a storage capacitor. In order to address a pixel, the voltage is sent to the appropriate transistor controlling the pixel. The capacitor is then able to retain the charge until the next refresh cycle resulting in a faster response time. By using TFT to control each individual liquid crystal, it allows a faster on-off of the electrical signal. An example of a simple schematic of both mechanisms is shown in Figure 1.2.

1.3 CURRENT TFT TECHNOLOGY AND LIMITATIONS

With the advancement in display technology, more stringent manufacturing and performance requirements are necessary. Large area uniformity, low-temperature compatibility, transparency to visible lights etc. are some of the major concerns. Several challenges emerge with the growing

requirements of next generation displays. They are more observable in high pixel density display and fast switching speed applications. Both of them require TFTs with high mobility semiconductor for an improved current drive to minimize delay times [1]. A common problem faced by the display industry is large area uniformity with the increasing demand for larger displays. Figure 1.3 illustrates the trend towards larger display panels in the FPD industry. Since display panels are advancing towards FPD panel size dimension of 3370 × 2940mm for Gen10+ which is 180% larger than Gen 8.5, electrical uniformity becomes essential when fabricating TFTs under such circumstances [2].

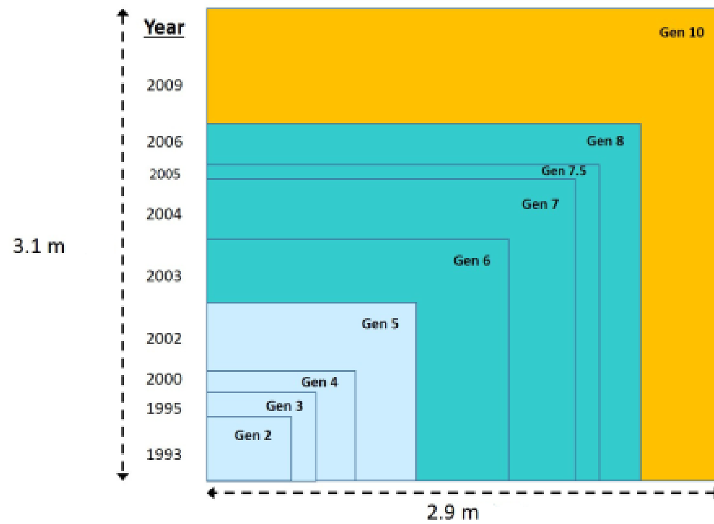


Figure 1.3: Substrate generations of flat-panel display. Adapted from [3].

As TFTs are typically fabricated on glass substrates which have a thermal tolerance of around 600 °C, another challenge is to ensure the fabrication process used for TFTs manufacturing is low temperature compatible. Additionally, to offer better resolutions, pixel density needs to be increased which lowers the aspect ratio between the pixel and the driving TFT. In such cases, it helps if the TFT used is also transparent to visible light.

Amorphous hydrogenated silicon (a-Si:H) has been used as an attractive candidate for the TFT material as it ensures excellent large area uniformity due to its amorphous structure over last few decades. Additionally, hydrogenation helps saturate the dangling bonds and thereby have a lower defect density and increased conductivity as doping is made possible. Moreover, it is low-temperature compatible and can be deposited at temperatures under 350 °C using plasma-enhanced chemical-vapor deposition (PECVD). It is also a low cost and a very well understood material to manufacture and characterize.

Table 1.1: Comparison of properties between different TFT channel materials.

Semiconductor	μ_{FE} **(cm²/Vs)**	**Large Scale Uniformity**	**Transistor Type**
a-Si:H	<1	Good	NMOS
LTPS	>100	Poor	CMOS
a-IGZO	10-20	Good	NMOS

However, due to the low mobility ($\mu_{FE} < 1$ cm^2/(Vs)) of a-Si:H which restricts high frequency response for backplanes, search for alternate materials that can accommodate the increasing demand for large displays with better resolution, higher refresh rates and low power consumption continues. Two most probable candidates for flexible and transparent display application are low temperature polycrystalline silicon (LTPS) and amorphous Indium Gallium Zinc Oxide (a-IGZO) as shown in Table 1.1. Although LTPS shows better field-effect mobility (μ_{FE}) than IGZO due to its grain boundaries in crystalline structure, the electrical uniformity is inferior compared to IGZO. As shown in Figure 1.4, IGZO TFT has received significant attention in a variety of applications such as televisions, mobile phones, flexible displays, etc. owing to its material properties.

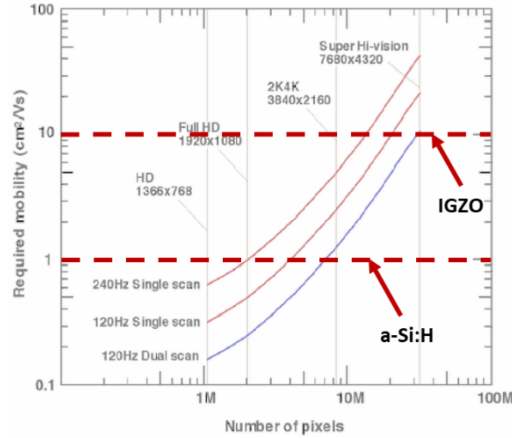


Figure 1.4: Mobility requirements for next-generation displays. Adapted from [4].

1.4 IGZO PROPERTIES

IGZO which is an amorphous oxide semiconductor (AOS) has been considered due to its high mobility and large-scale uniformity. It also offers low-temperature compatibility, low voltage operation, low off-state leakage, low fabrication cost and transparency to visible light. A-Si has highly directional sp^3 hybridized orbitals which introduces structural randomness (defects) and greatly degrades orbital overlap as shown in Figure 1.5a. Carrier transport is controlled by hopping between localized tail-states in a-Si. In IGZO, the conduction path is mainly comprised of s-orbitals ($(n-1)\ d^{10}ns^0$) contributed by heavy metal cations which has large radii and spherically symmetry as shown in Figure 1.5b. The large overlap between neighboring s-orbitals makes them insensitive to bond distortion and allows electrical transportation through band conduction, even in an amorphous material [5].

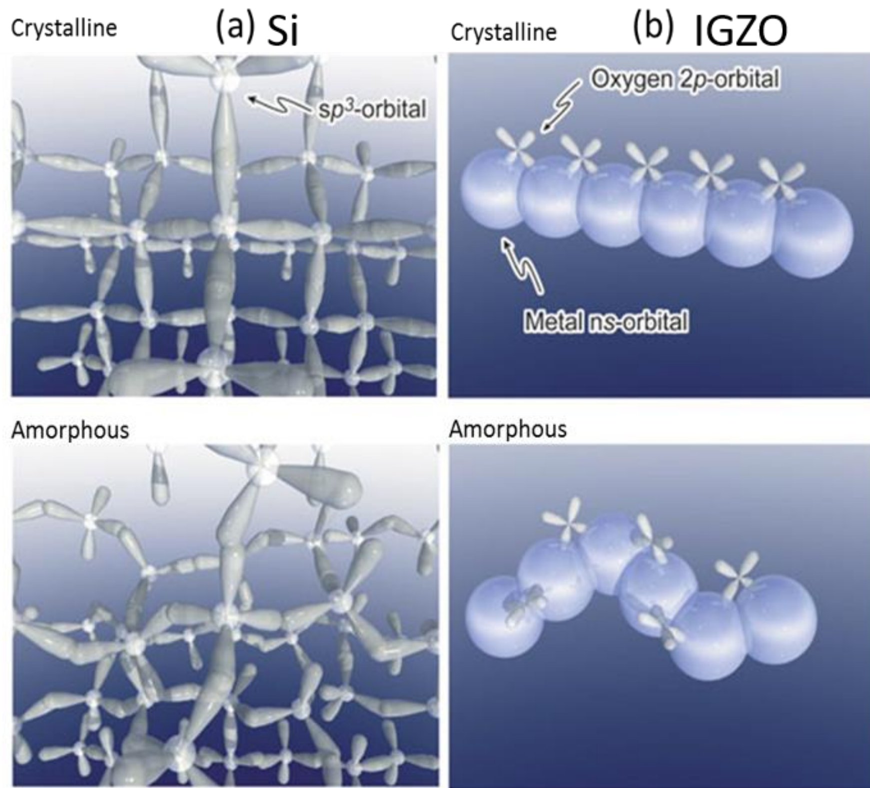


Figure 1.5: Schematic representation of overlapping orbitals. Adapted from [5]

The first report on transparent and flexible TFTs using a-IGZO was published in 2004 [5] as shown in Figure 1.6. Since then, it has become the most promising candidate to be adopted in the next generation displays. The conductivity of IGZO is attributed to oxygen vacancies and hydrogen since both serves as a donor in IGZO [6]. Although people have used different composition of IGZO, $InGaZnO_4$ is most widely used because of the improved stability over other compositions [7].

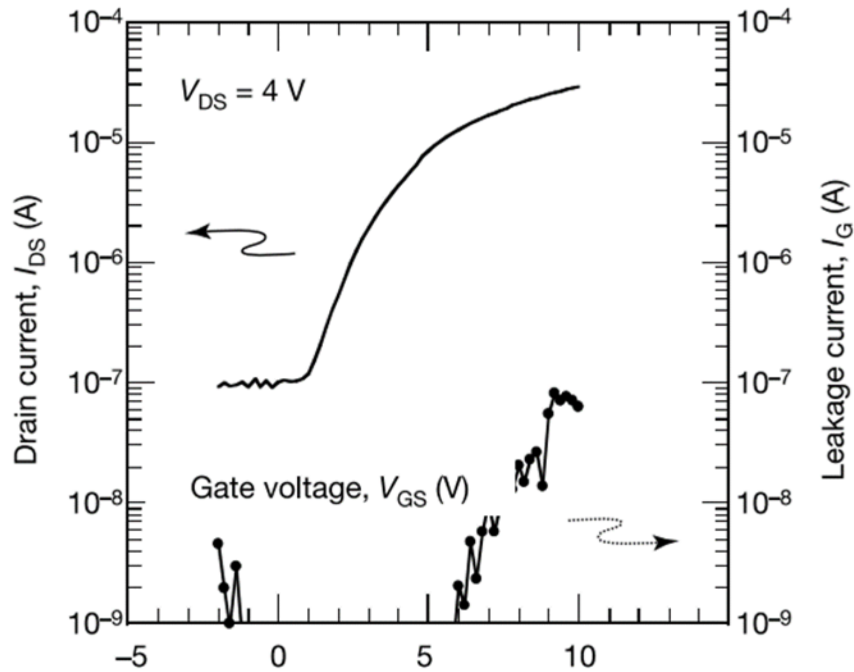


Figure 1.6: Electrical characteristics of first reported IGZO TFT. Adapted from [5].

1.5 GOALS & OBJECTIVES

The goals of this study are to investigate plasma immersion and ion implantation as methods for source/drain (S/D) activation in self-aligned (SA) IGZO TFTs, develop an integration strategy for the traditional bottom gate (BG) staggered TFT, and understand the associated mechanism of activation. The objectives are as follows.

1. Experiments with activation-last treatments on self-aligned top gate (SA-TG) devices. The SA-TG devices are convenient samples available for preliminary study to establish treatment settings (design space) which provides meaningful electrical characteristics.

2. Develop a process for SA-BG devices on silicon and glass substrates.

3. Refined experiments on SA-BG devices which will further optimize treatment combination conditions and clarify the interpretation of electrical behavior.
4. Materials analysis which is needed to support the interpretation of electrical characteristics.

1.6 DOCUMENT OUTLINE

Chapter 1 summarizes the recent developments in the display industry and the role of TFT in the structure of an active matrix display device. Different materials adapted for thin film transistors have been summarized and the advantages of a-IGZO over the other materials have been discussed. The conduction mechanism in IGZO along with its electrical and material properties have also been discussed. Emphasis is given to the goal and objectives of the study.

Chapter 2 describes the motivation behind the fabrication self-aligned (SA) IGZO TFTs with different electrode configurations. It also sheds light on several different techniques i.e., DUV irradiation, plasma treatment, ion implantation that have been adopted so far to realize SA devices.

Chapter 3 discusses the detailed fabrication process for IGZO TFTs which exhibit excellent characteristics for both double gate (DG) and bottom gate (BG) electrode configurations. However, limitations of the device electrostatics begin to give way to short channel behavior as the devices are scaled to shorter channel lengths. To maintain long-channel operation on scaled devices, various process parameters are changed based on TCAD simulation results that shows how these parameters and gate electrode configuration influences short-channel behavior. This chapter discusses electrical characteristics of the scaled IGZO devices along with the thermal and the bias stress stability. Finally, electrical performance of IGZO TFTs fabricated on glass substrate have been discussed.

Chapter 4 discusses the processes to fabricate SA-TG and SA-BG devices by utilizing pseudo SA-BG devices for proof of concept. S/D activation treatments i.e., plasma and ion implantation have been used for making IGZO selectively conductive. Boron and argon implanted devices result in ohmic contact behavior with TFT results showing DC operation comparable to metal-overlapped devices. SA-BG devices are also fabricated using backside flood exposure on glass substrate. This chapter also proposes a novel method for integration of a SA-BG process using a topside flood exposure under optimal exposure conditions.

Chapter 5 provides a summary of the investigation on the techniques that have been utilized towards the realization of SA IGZO TFTs.

Chapter 2. ***BACKGROUND***

Different TFT electrode configurations (BG, TG and DG) has been utilized for suitable applications. Scaling the channel length (L ≤ 2 µm) and integrating the devices on glass or flexible substrates has shown major impact on the display industry. To achieve submicron IGZO TFTs, self-aligned strategy is being explored where the channel length is not defined by the metal S/D distance but the gate dimension. It offers the ability to scale down to smaller channel lengths without the associated limitations of a channel length defined by the S/D contact regions. Non-SA TG coplanar TFTs typically exhibit inferior performance due to high parasitic capacitance induced by the overlap between gate and source/drain electrodes (RC delay). Also, a decrease in gate capacitance at the edges of the channel adjacent to the S/D is observed in such structure as shown in Figure 2.1a. SA coplanar TFTs exhibit superior performance because overlap between gate and source/drain electrodes can be eliminated which reduces the parasitic capacitance as shown in Figure 2.1b.

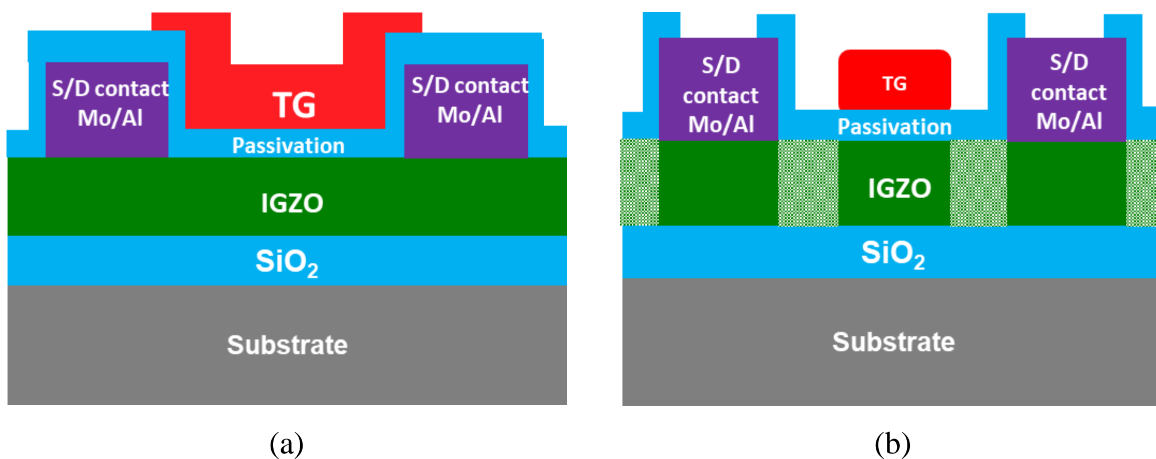


Figure 2.1: Cross sectional image of (a) non-SA TG TFT and (b) SA-TG TFT.

SA structure has many other advantages like better channel length scalability, and better process controllability over standard structure which makes it desirable especially for high-resolution applications [8]. Fabrication of self-aligned IGZO TFTs requires the formation of a homojunction between the highly conductive IGZO serving as the S/D regions and the semiconducting IGZO serving as the channel region. Among the several different of ways to form such a highly conductive IGZO layer, DUV irradiation [9], plasma treatments [10]–[14] and ion implantation [15], [16] are the methods that are currently being used which will be discussed briefly in the next few sections.

2.1 DEEP UV IRRADIATION

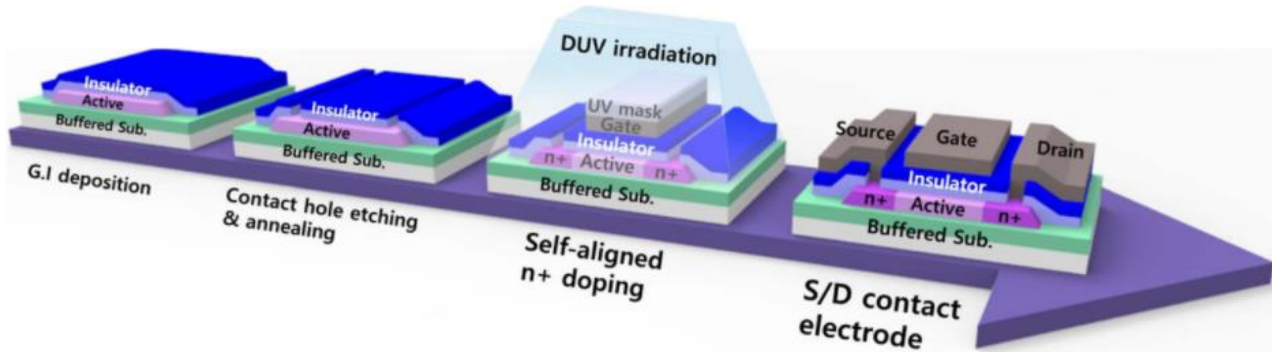
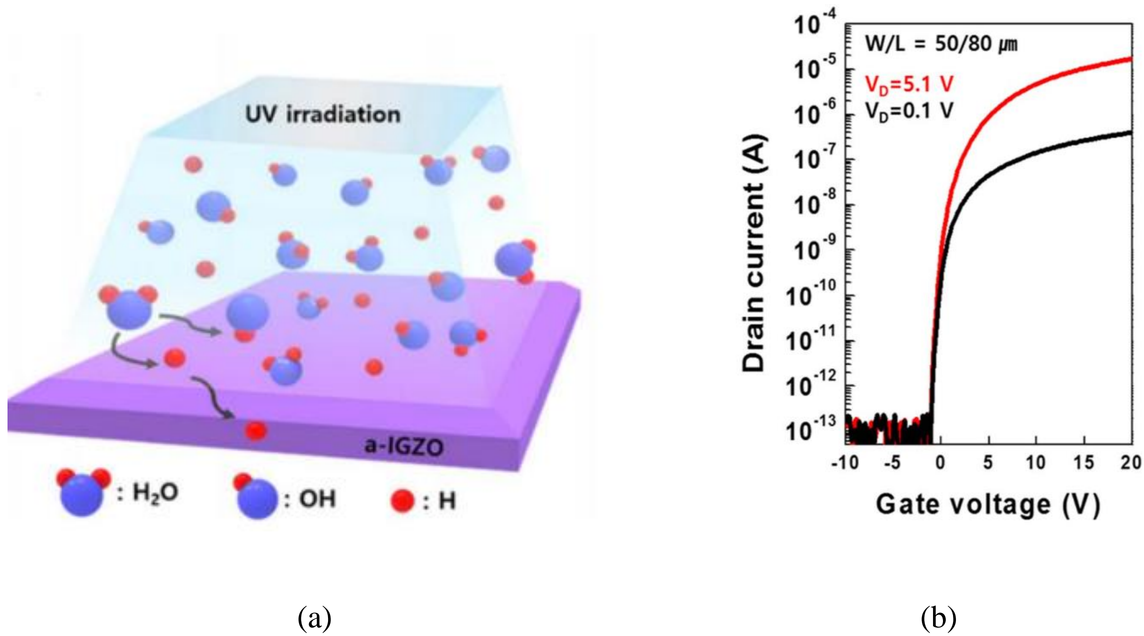


Figure 2.2: Process flowchart for a coplanar SA-TG a-IGZO TFT with S/D regions formed by DUV irradiation energy of 30 J/cm^2. Adapted from [9].

This technique uses deep ultraviolet (DUV) irradiation to define the source/drain (S/D) region of SA coplanar IGZO TFTs. Here, the gate mask pattern acted as a DUV shield layer to define the source/drain regions for selective DUV irradiation at wavelengths of 185 nm and 254 nm and an energy of 30 J/cm^2 as shown in Figure 2.2. DUV irradiation-induced increase in oxygen deficiencies in IGZO thin film indicates an increase in carrier concentration in the film. The water

molecule bond dissociation energy is 497.1 kJ/mol or 5.1 eV [17]. The energies of DUV light of 185 and 254 nm wavelength are 6.7 and 4.9 eV, respectively. Therefore, 185 nm wavelength DUV is likely to decompose the water molecules into H and OH radicals through photochemical water dissociation as shown in Figure 2.3a. As a result, the hydrogen can donate electrons in the a-IGZO thin film increasing the conductivity of the film.



(a) (b)

Figure 2.3: (a) Photochemical dissociation of water caused by DUV irradiation at 185 nm and (b) transfer characteristics of SA-TG a-IGZO TFT with DUV irradiation energy of 30 J/cm^2. Adapted from [9].

However, this technique is not compatible for SA-BG devices with top exposure or for SA-BG devices via through-glass exposure. Also, H-incorporation during DUV irradiation may lead to degraded thermal stress stability as hydrogen can rapidly diffuse into the a-IGZO thin films. The electrical properties of the device show field-effect mobility (μ_{FE}) of 13.2 cm^2/Vs, subthreshold swing (SS) of 0.32 V/decade and threshold voltage (V_T) of 3.2 V [9].

2.2 **PLASMA TREATMENT**

2.2.1 Hydrogen Plasma

Plasma treatment using H_2, O_2, Ar etc. can be an effective method to decrease the resistance of a-IGZO. However, hydrogen can rapidly diffuse out of the S/D region into the a-IGZO thin films at a temperature above 200 °C leading towards large series resistance in S/D regions of the device and poor device performance as shown in Figure 2.4. The oxygen vacancies in the S/D regions created by argon plasma treatment decrease after thermal annealing, which increase the sheet resistance of the S/D regions. Thus, thermal stability becomes the main concern for a-IGZO TFTs with S/D regions formed by argon or hydrogen plasma treatments [15].

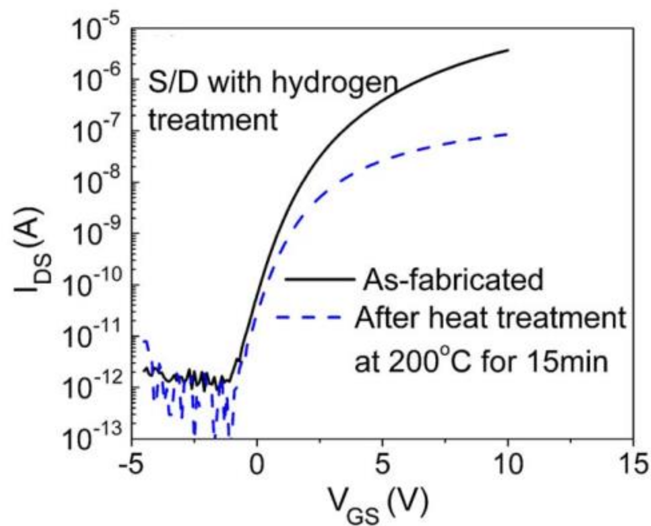
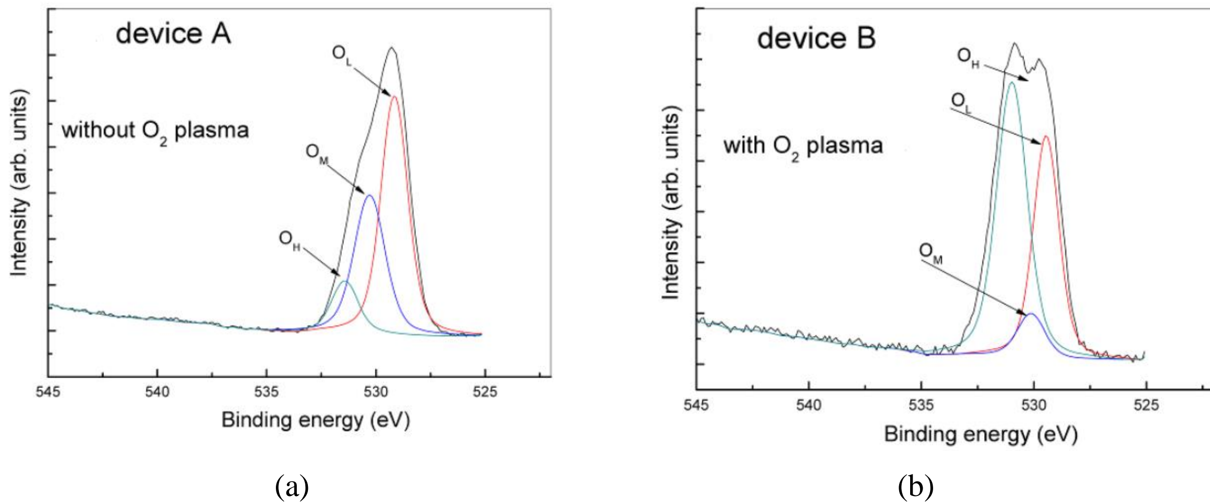


Figure 2.4: Transfer characteristics of the a-IGZO TFTs with S/D regions treated with hydrogen plasma under heat treatment at 200 °C. Adapted from [15].

2.2.2 *Oxygen Plasma*

In literature [14], O_2 plasma has been used for enhancing the performance of a-IGZO TFTs. The mobility of the plasma treated device increased by 38% compared to the non-treated device. It was suggested that the mobility enhancement was due to reduced oxygen vacancies, changed surface morphology and reduced trap density at the surface of the channel layer.



(a) (b)

Figure 2.5: XPS spectra of O1s (a) with (device A) and (b) without (device B) O_2 plasma treatment. Adapted from [14].

Peaks of O1s contain three different peaks including O_L, O_M and O_H corresponding to low, medium and higher binding energy as shown in Figure 2.5. The O_L component is attributed to the O^{2-} ions surrounded by Ga, In and Zn ions, the O_M peak corresponds to the deficiently bonded oxygen in the IGZO material and the O_H peak represents chemisorbed oxygen on the film surface [18]–[20]. It can be seen from the figure that both O_L and O_M decrease while O_H increases after the O_2 plasma treatment which indicates that deficiently bonded oxygen in the IGZO matrix decreases resulting into high field effect mobility.

2.2.3 Argon Plasma

In literature [21], it was found that energetic $^{40}Ar^{+}$ ion bombardment during plasma treatment induces the preferential sputtering of the relatively light atoms from the surfaces of II-VI or III-V group semiconductors as a result of the physical momentum transfer between the ions in the plasma and the atoms on the material surface. Therefore, the oxygen on the a-IGZO film surface is preferentially dissociated by the $^{40}Ar^{+}$ ion bombardment and increases the net electron concentration by the formation of an oxygen deficient surface layer as compared to the bulk IGZO film.

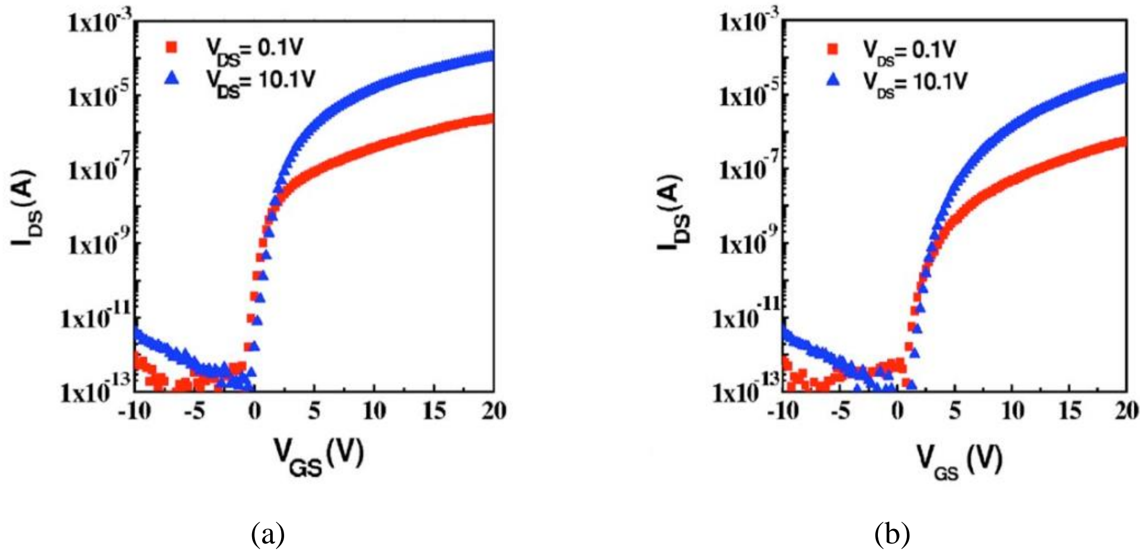


Figure 2.6: Transfer characteristics (W/L=50/4 μm) of a-IGZO TFTs (a) with and (b) without Ar plasma treatment on the contact regions before depositing the S/D electrode. Adapted from [21].

The transfer characteristics of a-IGZO TFT with and without $^{40}Ar^{+}$ plasma treatment is shown in Figure 2.6. An excellent SS of 0.19 V/decade, I_{on}/I_{off} ratio of 10^8 and μ_{FE} of 9.1 cm^2/Vs were achieved for the a-IGZO TFTs with $^{40}Ar^{+}$ plasma treatment. The improvements were attributed to

the reduction of the contact resistance between the source/drain electrodes and a-IGZO semiconductor.

2.3 ION IMPLANTATION

Ion implantation ($^{2}H^{+}$, $^{31}P^{+}$, $^{19}F^{+}$ etc) has also been used as an effective technique to decrease the resistance of a-IGZO film. S/D regions doped by hydrogen from silicon nitride by PECVD suffers from thermal stability issues caused by hydrogen diffusion in the a-IGZO thin films. The development of a SA IGZO TFT with good performance and high stability is necessary. Successful reports on SA IGZO TFTs with S/D regions doped by implanted arsenic or phosphorus have been found in literature which show good electrical performance and high thermal stability [15], [16].

2.3.1 Phosphorous Ion Implantation

In this report, the SA S/D regions were implanted with phosphorus at a dose of 5×10^{15} cm^{-2} and energy of 45 keV using the gate electrode Indium Tin Oxide (ITO) pattern as a mask as shown in Figure 2.7. The implanted phosphorus dopant was activated by annealing at 500 °C for 25 min in O_2 ambient. They exhibited good transfer TFT characteristics at a drain-to-source voltage (V_{ds}) of 0.2 V, such as μ_{FE} of 5 cm^2/Vs, V_T of 5.6 V, an SS of 0.5 V/dec, and an I_{ON}/I_{OFF} ratio of 6×10^7 [16].

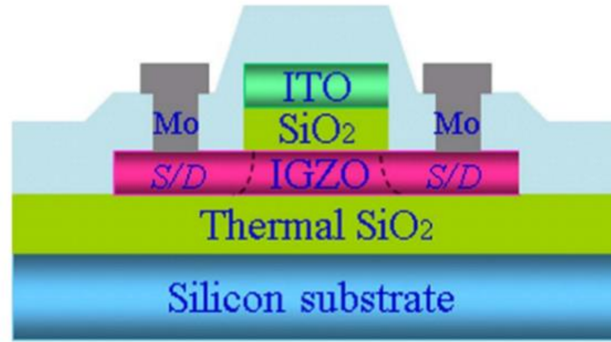


Figure 2.7: Cross-sectional schematic of the proposed a-IGZO TFT with SA-TG structure. Adapted from [16].

The proposed a-IGZO TFT shows much better thermal stability as shown in Figure 2.8 compared to the S/D regions formed by plasma treatment as shown in Figure 2.4.

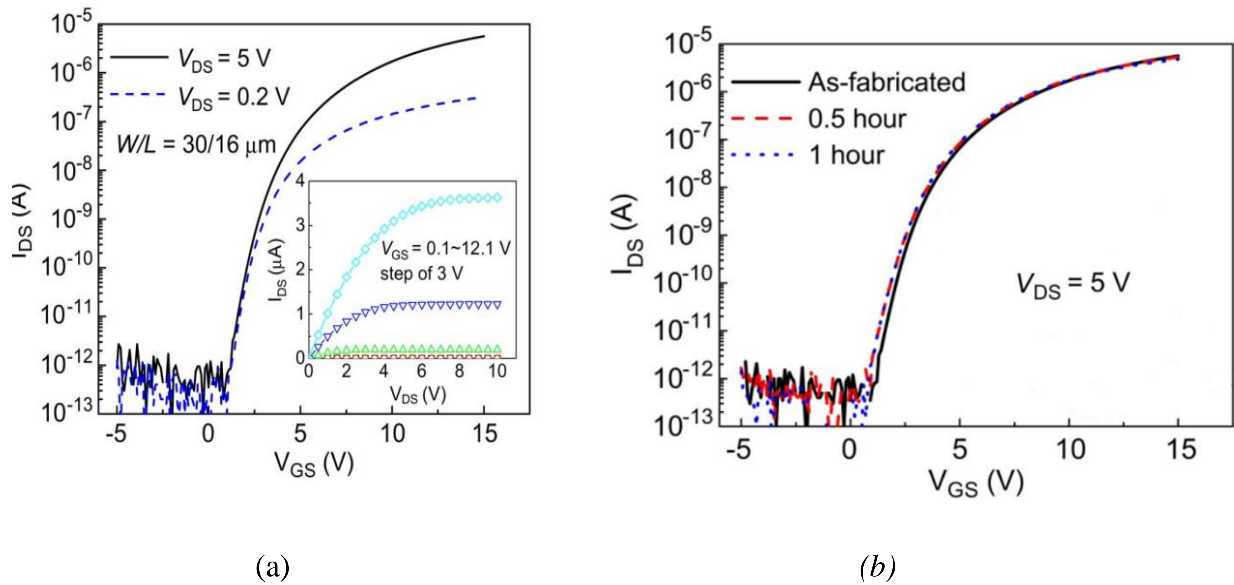
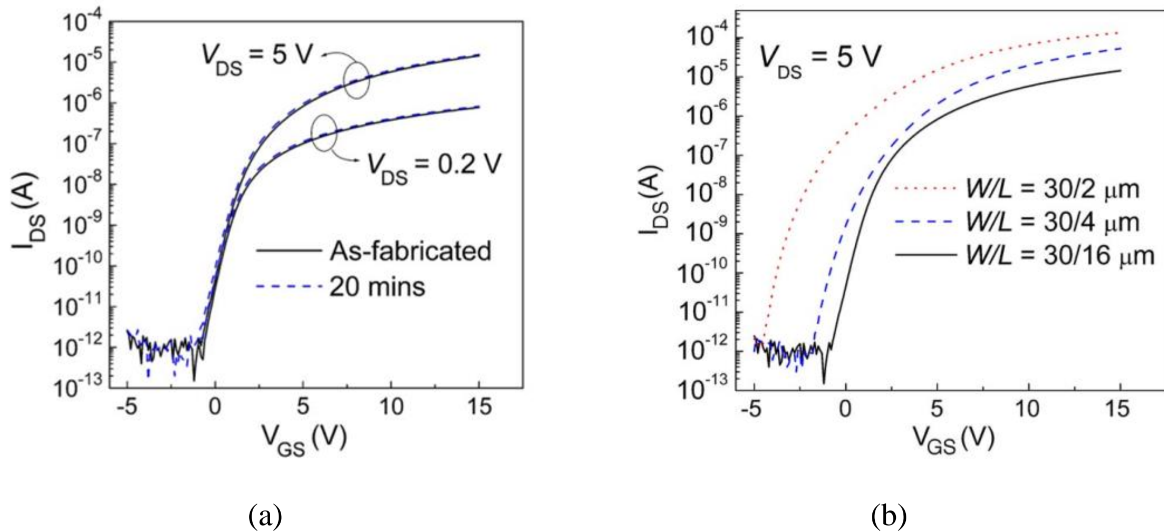


Figure 2.8: (a) Transfer and output characteristics (shown in the inset) of the SA-TG a-IGZO TFT with P doped S/D regions and (b) transfer characteristics under heat treatment at 200 °C. Adapted from [16].

2.3.2 Arsenic Ion Implantation

In this report, the SA S/D regions were masked using gate-electrode ITO pattern and implanted with arsenic at a dose of 5×10^{15} cm^{-2} and energy of 100 keV. To activate the implanted arsenic dopant, an annealing process at 525 °C for 30 min in O_2 ambient was performed. The proposed mechanism suggested arsenic substitution on the zinc site introducing a donor state. However, a potential alternative mechanism could be the defect associated with the presence of arsenic or displacements (i.e. oxygen vacancy). Also, oxygen vacancies in the S/D region decreased after the thermal annealing followed by the implant which increased the sheet resistance of the S/D region.



(a) (b)

Figure 2.9: (a) Transfer characteristics of the a-IGZO TFTs (a) with arsenic doped S/D regions under heat treatment at 200 °C (W/L=30/16) and (b) with the same channel width but different channel lengths. Adapted from [22].

The a-IGZO TFTs showed good transfer characteristics at V_{ds} of 0.2 V, such as μ_{FE} of 12 cm^2/Vs, V_T of 3.5 V, SS of 0.5 V/dec, and I_{ON}/I_{OFF} ratio of 9×10^7. The gate leakage current for the TFTs was ~10 pA. The devices were also thermally stable as seen from Figure 2.9a. However, channel length dependence was observed for the proposed a-IGZO TFTs. The TFTs

scaled down nicely to channel lengths of L ≥ 4 μm with a small change of the threshold voltage and little degradation of subthreshold swing as seen from Figure 2.9b. For 2 μm channel length devices, the threshold voltage shifted largely to the left which might be due to the lateral diffusion of the arsenic dopant into the channel region.

Chapter 3. SCALED IGZO TFT

An established process for the fabrication of IGZO TFTs exhibits excellent electrical characteristics in both BG and DG configurations [23]. The channel length is defined by the S/D metal liftoff process, with approximately zero process bias shown in Figure 3.1. This ensures a precise channel definition which is needed to approach the lithographic limit. However, limitations of the device electrostatics begin to give way to short channel behavior as the devices are scaled to channel lengths shorter than those shown in Figure 3.1. With the same IGZO and gate dielectric (SiO_2) thickness, the DG device shows superior current drive and subthreshold operation, with associated tradeoffs in process complexity.

To maintain long-channel operation on scaled devices, the dielectrics used for the gate and back-channel regions are typically adjusted to overcome short-channel effects as lateral dimensions are reduced. In addition, the IGZO thickness can also be reduced. TCAD simulation results listed in Table 3.1 shows how these parameters and gate electrode configuration influences drain-induced barrier lowering (DIBL), with the subthreshold voltage offset (ΔV) between low and high drain bias as a measure of short-channel behavior.

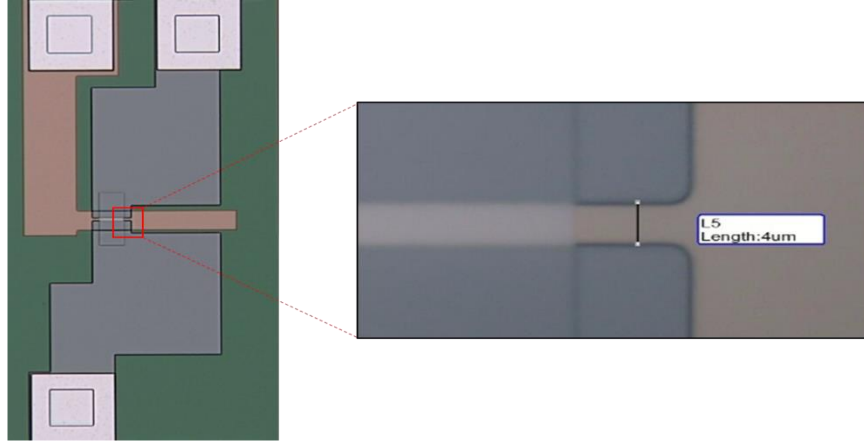


Figure 3.1: BG IGZO TFT with channel length L = 4 µm as defined by the S/D lift-off metallurgy using negative photoresist (Futurrex NR9g-1500PY) with almost negligible offset from the mask definition (i.e. ΔL ~ 0) [24].

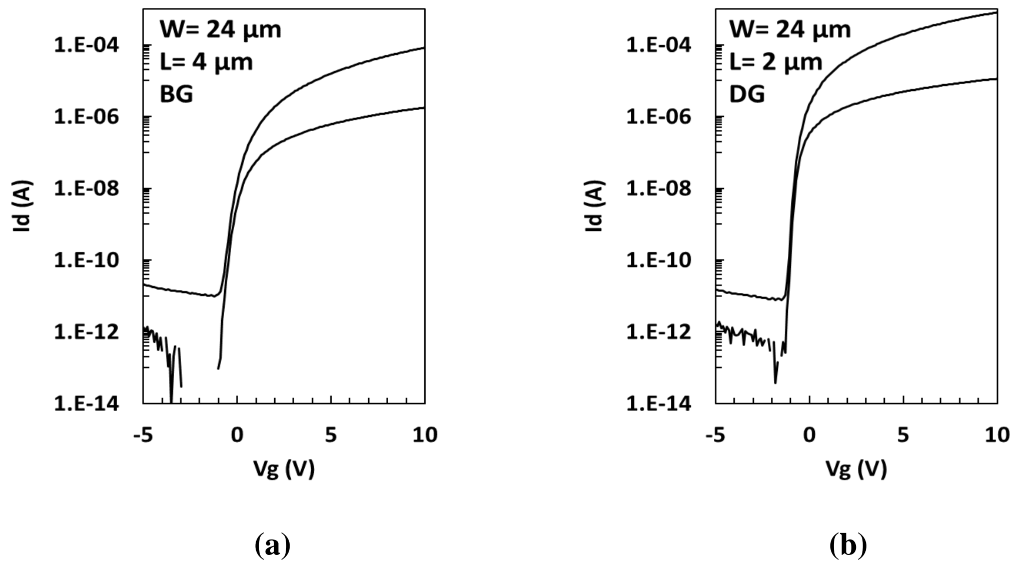


Figure 3.2: Transfer characteristics of IGZO TFTs with 100 nm SiO_2 gate/passivation dielectric. Drain bias conditions are 0.1 V and 10 V. (a) BG configuration with L = 4 µm and (b) DG configuration with L = 2 µm [24].

Table 3.1: TCAD simulation of short-channel response to TFT structure and film thicknesses [7].

	Thickness (nm)		Gate	Lin/Sat
L (µm)	IGZO	Gox	Electrode	ΔV
2.0	50	100	BG	0.02
1.0	50	100	BG	0.3
1.0	**50**	**50**	**BG**	**0.01**
0.5	50	50	BG	0.4
0.5	20	50	BG	0.2
0.5	50	50	DG	0.1

3.1 PRELIMINARY STUDY

The options for scaling are clear; thinner gate dielectric, thinner IGZO, and DG configuration. However, the choice among these options must consider process tolerances and interaction effects, and impact on device reliability. The BG device with the established process supports a 2 µm channel length with long-channel operation, however the gate dielectric (PECVD SiO_2) thickness must be reduced for a 1 µm channel length device. For an L = 0.5 µm device, the DG configuration suppresses short-channel behavior without the need to thin the gate dielectric or the IGZO below 50 nm. Thus, the initial focus was on the DG device configuration. Thinning the BG dielectric was considered straightforward, however thinning the top-gate oxide required adjustment of the O_2 passivation anneal used to establish the IGZO semiconductor properties. This modified process was verified on the BG device operation with electrical results shown in Figure 3.4, demonstrating consistency with Figure 3.2a.

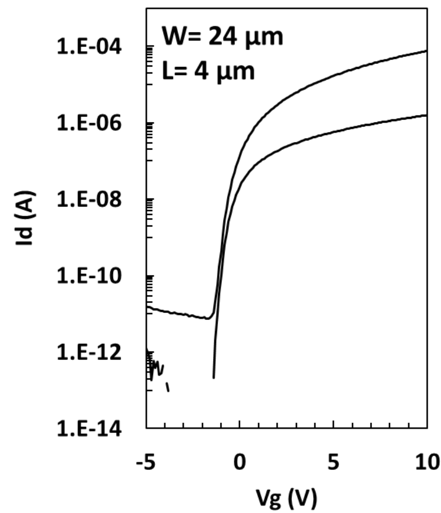


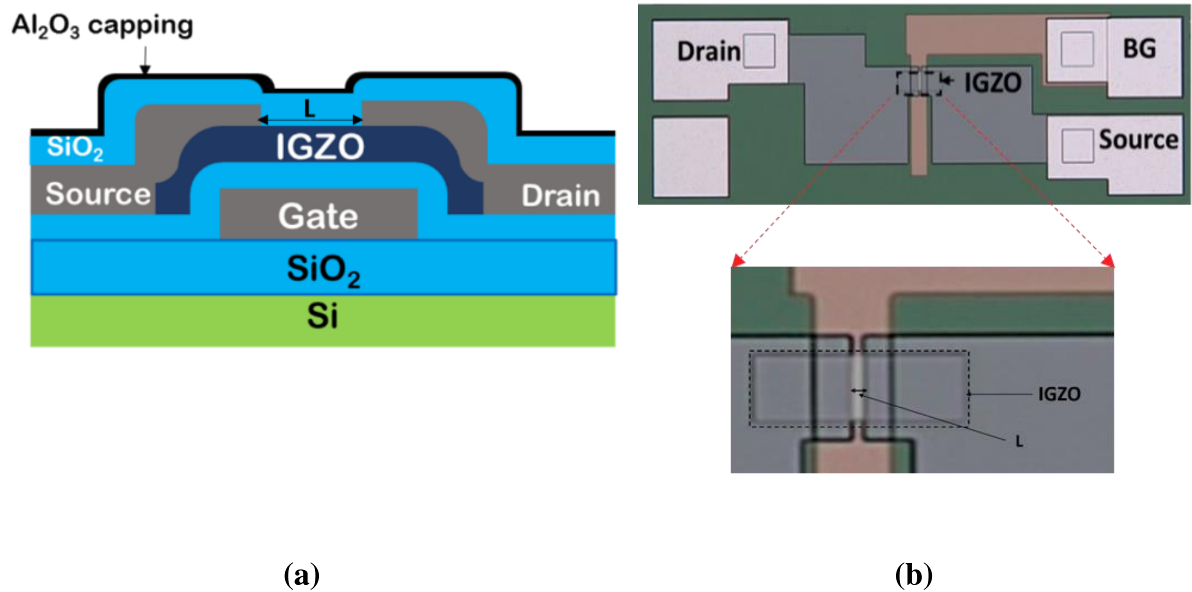
Figure 3.3: Transfer characteristics of an intermediate stage BG device with W = 24 µm and L = 4 µm. The gate oxide thickness remained at 100 nm and the passivation oxide thickness was reduced to 50 nm. Adjustments were made to the O_2 passivation anneal; process details provided in the experiment section [24].

At this intermediate stage, the device demonstrated characteristics that were consistent with the previously established process. Arriving at the optimal O_2 passivation anneal process recipe required a significant engineering effort yet appears deceptively trivial in hindsight. At this point, the focus shifted towards reducing the gate oxide thickness and evaluating the revised process flow on scaled BG devices. The exposure system used for the lithographic processes was limited to an image resolution of approximately 1 µm, and thus submicron DG devices were not realized. The outlined treatment listed in Table 3.1 indicates that the revised process flow with a BG device configuration should yield long-channel operation. The details of the revised process flow with select treatment comparisons are described in the following section.

3.2 Revised Process Conditions

IGZO TFTs were fabricated with BG staggered configuration on a thick isolation oxide (~650 nm SiO_2) thermally grown on silicon wafers. A 50 nm Mo gate electrode was sputtered and

patterned, followed by a 50 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified for 2 hours in N_2 at 600 °C in a furnace. A 50 nm IGZO layer was sputter deposited using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, followed by mesa pattern and etch using dilute HCl. The S/D contact metal (100 nm Mo-Al bilayer) was then sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. A second 50 nm PECVD SiO_2 layer was then deposited as the passivation material. A 3-hour O_2 passivation anneal at 400 °C with a 2-hour controlled ramp-down in O_2 ambient was performed, and immediately followed by an HMDS vapor treatment at 140 °C to avoid water adsorption. The devices were then capped with 10 nm Al_2O_3 film using atomic layer deposition (ALD) at 200 °C; alternative ALD deposition temperatures were also investigated. The gate and S/D contact windows were patterned and etched using 10:1 buffered HF solution. Figure 3.4 shows the cross-section schematic and top-down view of the BG staggered device.



(a) **(b)**

Figure 3.4: (a) Cross-section schematic of BG staggered TFT with ALD capping layer where L denotes the channel length. (b) Labeled top-down view of a fabricated BG TFT, with the IGZO channel outlined [24].

3.2.1 Scaled IGZO TFTs

BG devices using the revised process displayed excellent electrical performance, with representative transfer characteristics shown in Figure 3.5. The improvement over the characteristic shown in Figure 3.3 appears even more than what should be realized by the gate oxide thickness reduction alone. In addition to a steeper subthreshold region, there is a notable right-shift in the characteristic that supports enhancement-mode operation and suppresses off-state leakage. This behavior was demonstrated on device samples which had the ALD Al_2O_3 layer applied immediately after the HMDS vapor treatment, which immediately followed the 400 °C O_2 passivation anneal. The application of an ALD capping layer as a water barrier has been previously reported with associated benefits in thermal stability [25]. While all samples received the HMDS vapor treatment, the time delay before the ALD capping layer was applied typically varied from 0 to 2 hours.

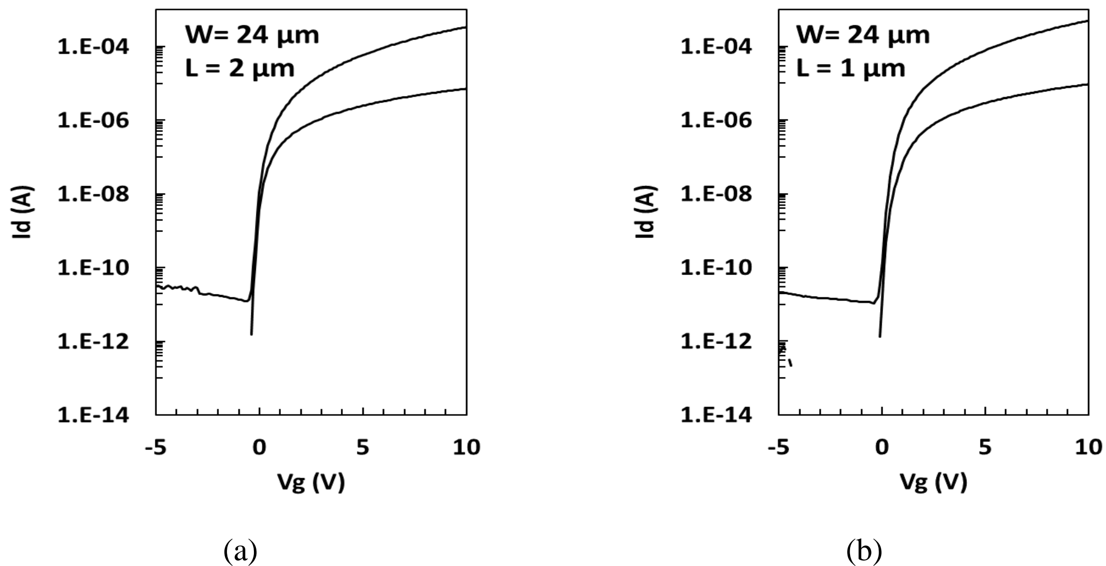


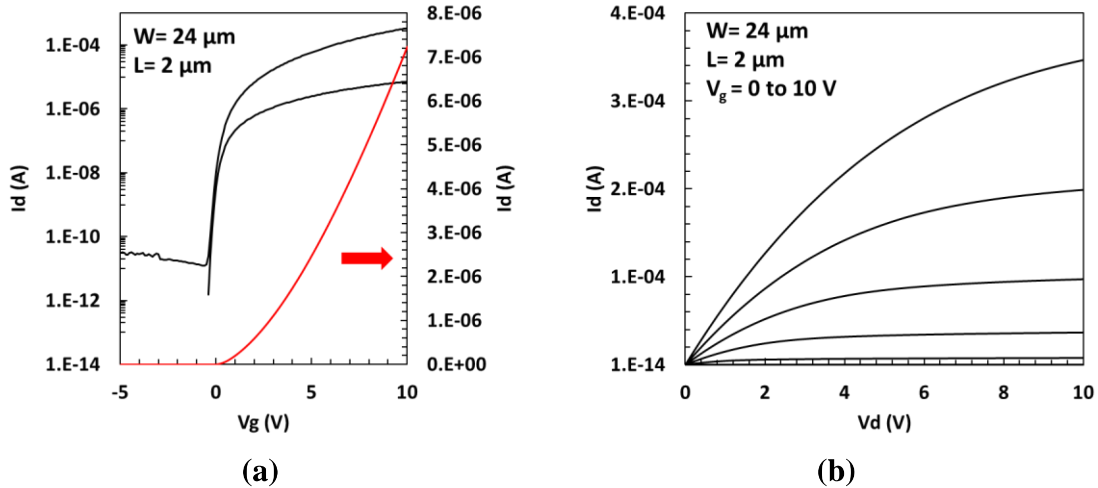
Figure 3.5: Transfer characteristics from BG devices fabricated with the revised process which included gate oxide thickness reduction to 50 nm. Excellent performance is demonstrated at

2 µm and 1 µm channel lengths, as suggested by Table 3.1[24].

This fortunate improvement in subthreshold and enhancement-mode operation seems to be associated with back-channel passivation that is absolutely free from adsorbed water molecules, indicating the difference is due to procedure rather than process definition.

3.2.2 Device Modeling of Scaled IGZO TFTs

The 2 µm channel length device transfer characteristics shown in Figure 3.5 are also shown in Figure 3.6 next to the I_d-V_{ds} output characteristics. The linear-scale transfer characteristic shown demonstrates the typical concave-up characteristic associated with band-tail states (BTS). The influence of BTS is dependent upon both the gate and drain bias conditions and renders traditional methods of parameters extraction not applicable. A new device model referred to as BTS2D has been recently developed that accounts for the bias-dependent level of trapped charge and free channel charge; complete details are described in [26].

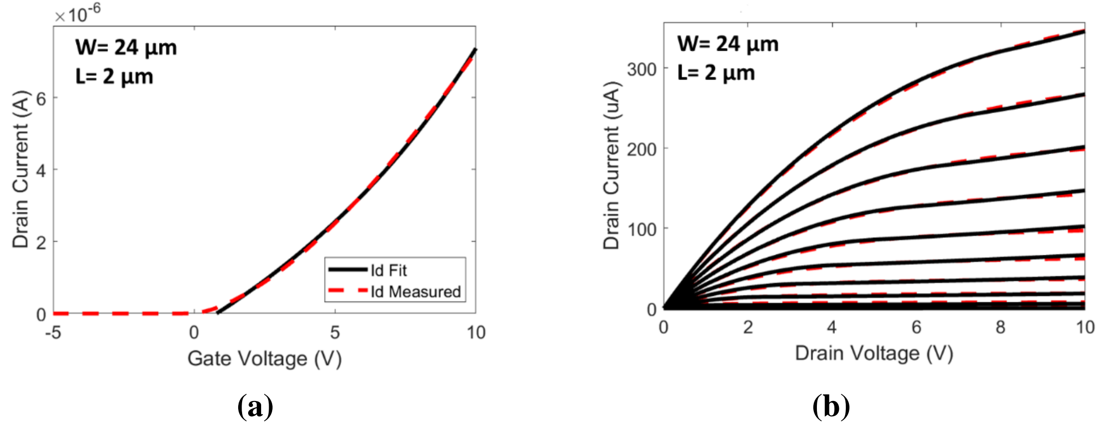


(a) **(b)**

Figure 3.6: (a) Transfer characteristics and (b) output characteristics of a representative BG device with 2 µm channel length. The Y2 axis in (a) shows the low-drain bias measurement on a linear-scale, demonstrating the influence of band-tail states on electrical behavior [24].

Extraction of the redefined V_T as well as other operational parameters that represent the on-state transfer and output characteristics, and account for BTS and short-channel effects (SCE), was

performed using nonlinear least-squares regression analysis in MathWorks® MATLAB®. The BTS2D model provides an excellent match to device measurements, as shown in Figure 3.7.



(a) **(b)**

Figure 3.7: BTS2D device model representing the on-state operation of a BG device with 2 µm channel length, showing an excellent fit to the linear-mode transfer characteristic (low drain bias) and output characteristic family of curves [24].

Table 3.2 shows the mean ± standard deviation of the SS and BTS2D model extracted V_T for 4 µm and 2 µm channel length devices with N = 10 sample size. The variation in V_T is relatively small and can be explained primarily by thickness variation in the PECVD SiO_2 gate dielectric. However, the same device die was measured for each device size, thus the difference in V_T cannot be attributed to differences in sampling or process non-uniformity, neither random nor systematic. This length-dependent characteristic shift is counter to short-channel behavior and, although subtle, appears to extend to the 1 µm channel length device seen in Figure 3.5.

Table 3.2: Extracted device parameters (N=10).

L **(µm)**	**V_T (V)**	**SS (mv/dec)**
4	0.79 ± 0.18	202.82 ± 31.23
2	1.07 ± 0.17	191.42 ± 27.78

3.2.3 *Thermal Stress Stability of Scaled IGZO TFTs*

As mentioned previously, the application of the ALD Al_2O_3 capping layer as a water barrier has been associated with good thermal stability, which is a standard requirement for product integration. Thermal degradation at temperatures T ≤ 200 °C typically cause a characteristic left shift, and is also reported to be a more pronounced issue on long channel devices [25]. The thermal stability of capped BG devices was found to depend upon the deposition temperature of the ALD process. Figure 3.8 shows a comparison of BG devices with ALD films deposited at 150 °C and 200 °C, with electrical characteristics measured following 1-hour thermal stress hotplate treatments performed sequentially at indicated temperatures.

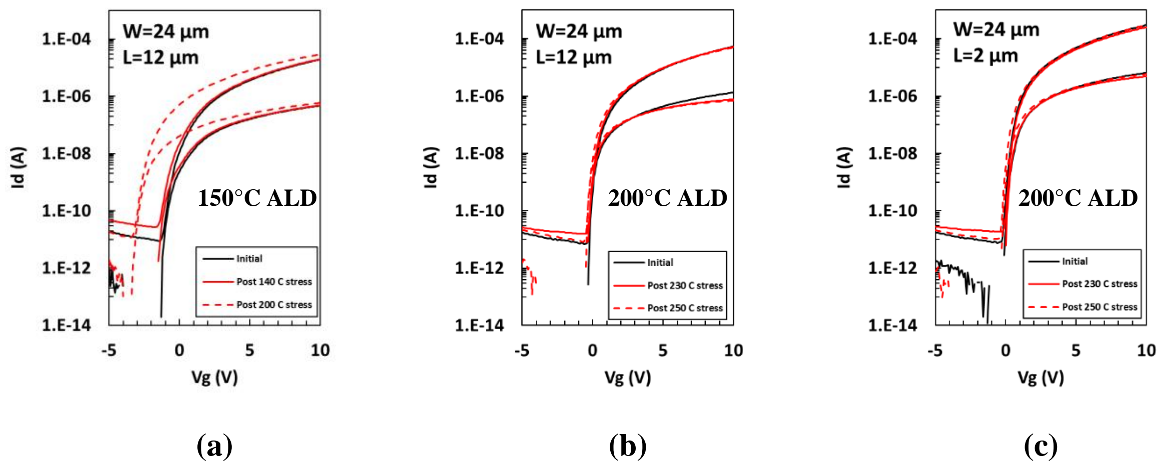


Figure 3.8: BG devices with ALD Al_2O_3 capping layer deposited at 150 °C (a) and 200 °C (b & c), with channel lengths and 1 hour sequential thermal stress treatment temperatures as indicated. The 200 °C ALD temperature maintains good thermal stability on both long and short devices at temperature up to 250 °C [24].

The lower ALD temperature was not adequate in supporting thermal stability on 12 µm channel length devices stressed at 200 °C. The same devices processed at higher ALD temperature maintained thermal stability up to 250 °C, as did 2 µm channel length device from the same sample. It is likely that H_2O molecules introduced as one of the Al_2O_3 precursors were allowed to

become absorbed into the passivation oxide during the 150 °C ALD process, but were successfully suppressed at 200 °C.

3.2.4 Bias Stress Stability of Scaled IGZO TFTs

The BG devices were also subjected to gate bias-stress conditions performed at room temperature to evaluate the resistance to the degradation of electrical characteristics. Positive bias-stress (PBS) and negative bias-stress (NBS) tests involved setting the gate voltage to ±10 V with S/D at reference ground. Devices used for bias-stress testing had a channel length of 4 µm, however the applied stress conditions did not present significant lateral electric fields, and thus the response would not have a strong dependence on channel length. Transfer characteristics were measured immediately following 1 hour applied stress, with results shown in Figure 3.9.

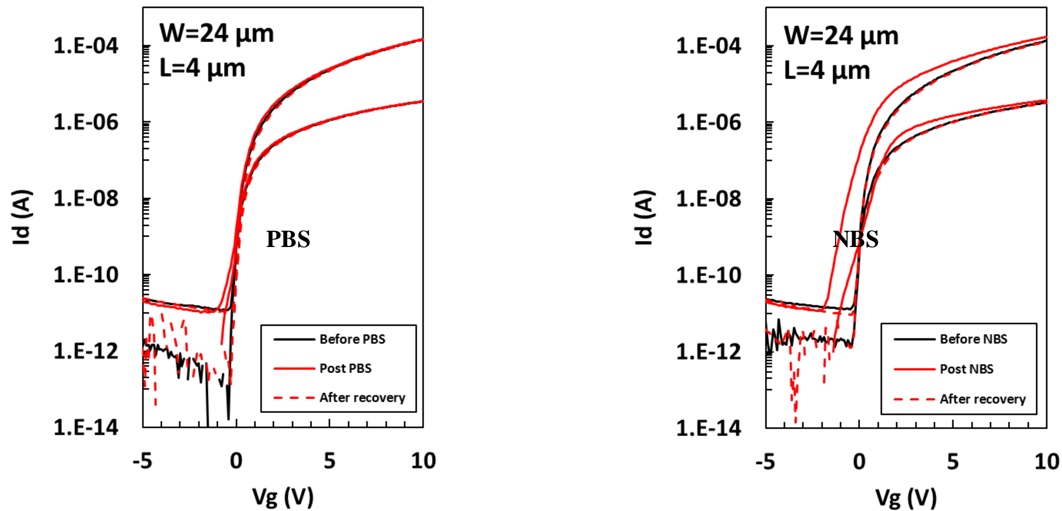
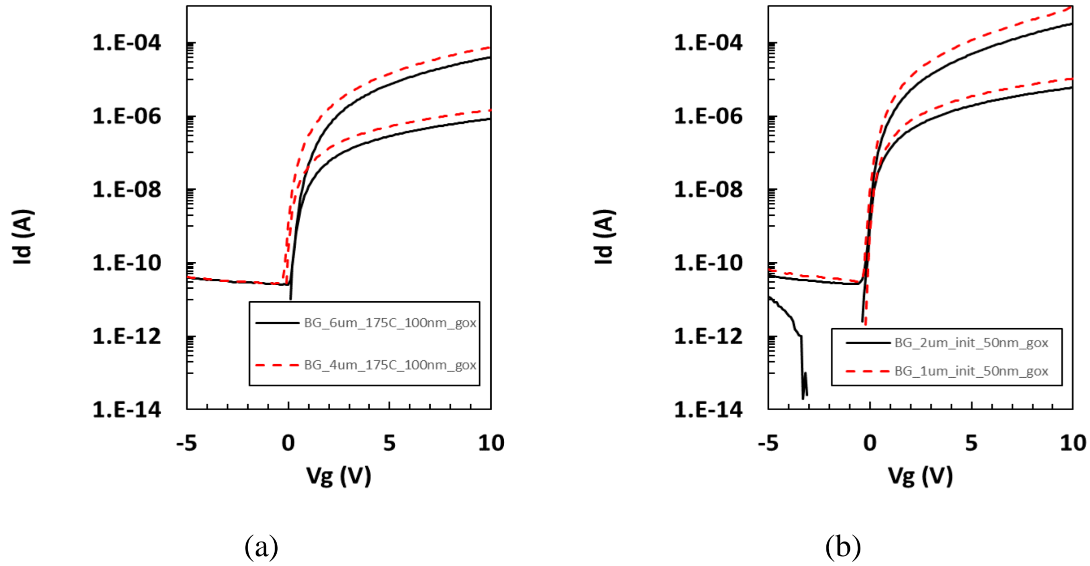


Figure 3.9: Two separate BG devices showing effects of PBS and NBS applied at V_G = ±10 V with S/D at reference ground. The post-stress measurements were taken immediately following 1 hour stress duration. The PBS effect is virtually negligible, whereas the NBS effect indicates the influence of carrier traps. Both PBS and NBS effects were completely reversible [24].

Both PBS and NBS induced an observable response that was completely reversible following 4 - 5 hours of relaxation time. The PBS response was very slight at pico ampere current levels; negligible by most standards. The NBS response demonstrated distortion and spreading which indicates an influence of carrier traps. The NBS depletion of channel electrons has the opportunity to interact with the entire IGZO layer and associated interface regions. A negligible effect of NBS in the absence of illumination has been claimed [27], [28], although the applied NBS E-field in this work (2 MV/cm) is higher than these reports. A model presented by Chowdhury, Migliorato and Jang [29] proposes a weak-bond neutral oxygen vacancy defect state that is susceptible to reconfiguration as a double-donor oxygen vacancy defect (V_O^{2+}) during NBS with above-bandgap illumination, or NBIS. This or a similar mechanism may be operative even without illumination due to the high E-field present. Note that in this work the degree of lateral left-shift is relatively small; the transfer characteristic separation is not due to SCE, but rather is attributed to the inhomogeneity of donor-like trap states [23].

3.3 IGZO TFTs on Glass Substrate

Most of the TFT applications will require fabrication on glass substrate. In our previous studies the devices were fabricated on thick oxide on Si wafer. To ensure the compatibility of our TFT process on glass substrates the scaled devices were fabricated on Corning NXT glass wafers. In this process the devices were fabricated with the revised process flow with both 100 nm and 50 nm gate oxide described in 3.2 except for the initial thermally grown oxide. As shown in Figure 3.10, the TFTs showed excellent transfer characteristics in long ($L \geq 4$ µm) and short channel devices. The short channel devices exhibited steeper subthreshold slope.



(a) (b)

Figure 3.10: Long (solid line) and short (dashed line) channel devices fabricated on Corning NXT glass substrate with (a) 100 nm and (b) 50 nm gate oxide respectively.

3.4 SUMMARY

Scaled BG devices with a reduction in gate oxide thickness to 50 nm demonstrated excellent electrical characteristics at channel lengths as small as L = 1 μm. Thickness adjustment of the PECVD SiO_2 passivation layer required re-engineering the O_2 passivation anneal. While this change at the back-channel was not needed for improved electrostatic control on the BG device, it presents an optimized process for a scaled top-gate dielectric on a DG device structure. The specific details of the ALD Al_2O_3 capping layer, both process and procedure, where shown to be important in supporting enhancement-mode BG device operation with steep subthreshold characteristics and excellent thermal stability up to 250 °C. An associated trend of increasing V_T at decreasing channel length is under further investigation. The scaled process also maintained good stability when subjected to PBS and NBS, with complete recovery to initial characteristics.

The scaled process is also fully compatible with glass substrate as excellent transfer characteristic has been observed for both long and short channel devices with steeper SS for shorter devices.

Both the BG dielectric and the IGZO thickness could be reduced further to enable shorter channel length, however the DG device structure presents a conservative approach towards submicron dimensions that supports low variation and reliability. Unfortunately, DG devices with channel length below 1 µm were not realized due to limitations in the S/D patterning and metal lift-off processes. While such techniques can be used for nanoscale devices, the lift-off defined channel region with lithographic alignment tolerances to ensure gate-S/D overlap presents significant scaling challenges. A self-aligned gate process scheme utilizing ion-implanted S/D regions would support scaling trends similar to silicon device technology. To achieve submicron devices, self-aligned strategy combined with high-k dielectric can be used.

Chapter 4. SELF ALIGNED IGZO TFT

Self-aligned channel regions in thin-film transistors have advantages in reduced parasitic capacitance and stage delay, and a reduction in overhead real estate. A common method used to fabricate self-aligned a-Si:H TFTs is to utilize a through-glass exposure of photoresist which is blocked by the opaque metal bottom-gate electrode [30], [31]. This process does not require an additional photomask or lithographic alignment, and thus supports low production cost. Sputtered IGZO has been introduced into flat panel display product manufacturing, exhibiting a channel mobility of approximately an order of magnitude higher than a-Si:H. The working source/drain (S/D) electrodes in IGZO TFTs can be direct metal contact regions to the IGZO, without the need for additional processes such as doping to render the IGZO conductive. Proper metallurgy and annealing processes can provide ohmic behavior with minimal series resistance [32], however this usually requires several microns of gate-to-S/D overlap in order to ensure such behavior. Various self-aligned channel strategies have been demonstrated that either utilize a TG structure [15], [33], or a through-glass exposure for BG configurations. The TG or associated BG feature must protect the channel region during S/D formation.

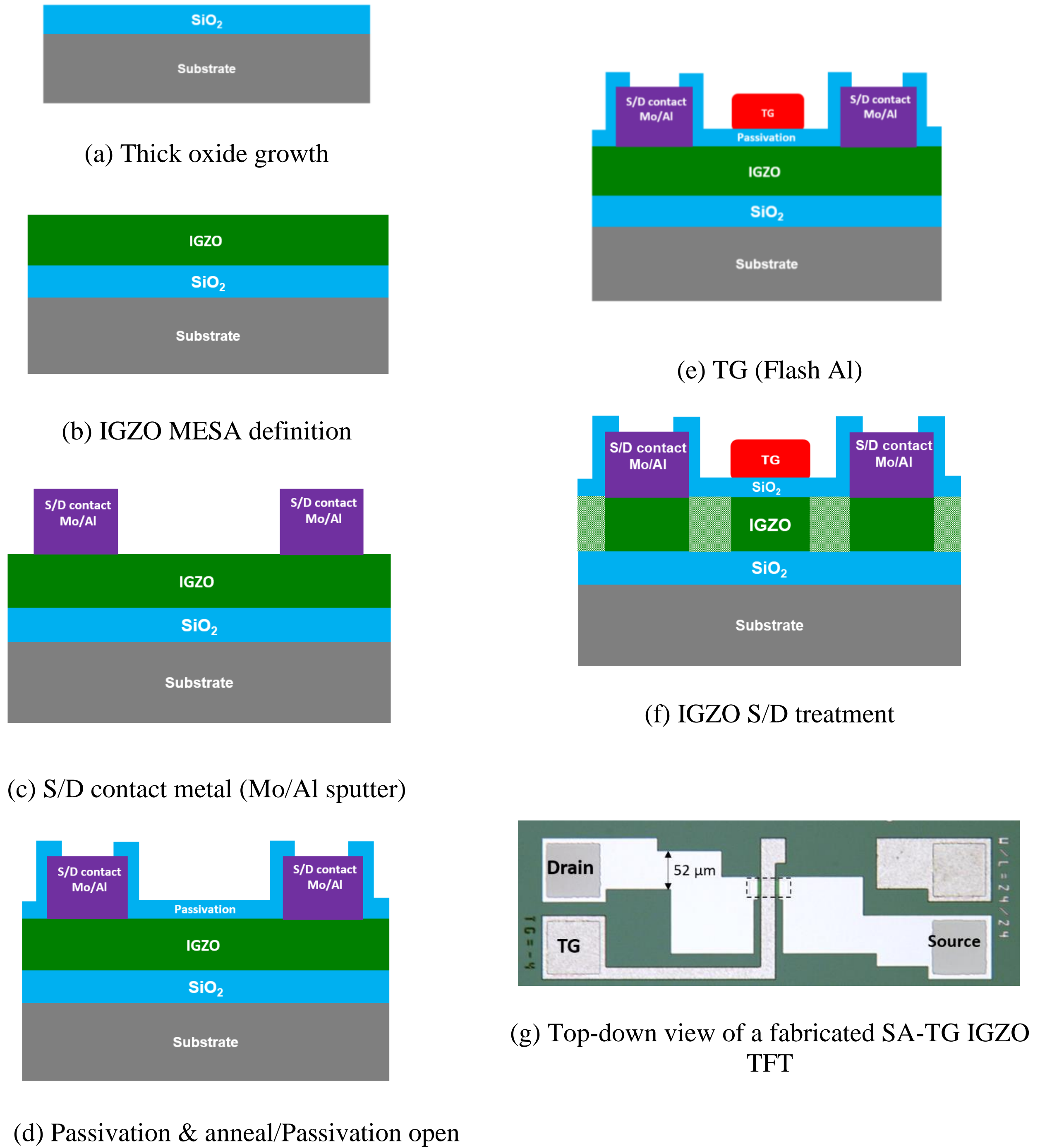
Techniques previously discussed in Chapter 2 that have been used to selectively form conductive IGZO regions include hydrogen diffusion [34], hydrogen plasma treatment [10]–[12], argon plasma treatment [13], [21] , and arsenic implantation [15]. In this work the activation of IGZO S/D regions by O_2 plasma and ion implantation using $^{31}P^{+}$, $^{19}F^{+}$, $^{40}Ar^{+}$, and $^{11}B^{+}$ has been investigated on SA-TG devices, designated Treatment Last (TL). Activation behavior due to $^{40}Ar^{+}$ implant would be associated with ionized defect states, such as oxygen vacancies [13], [21]

whereas activation behavior due to the other implanted ions would be associated with either ionized defect states and/or the implanted element serving as an electrically active species. Following the S/D activation treatment, annealing was done to explore the possibility of enhanced activation or thermal instability. However, due to metal electrode oxidation, no devices remained operational. Further investigation on integrating an activation enhancement anneal using an anneal-last strategy is in progress.

Boron and argon implanted devices resulted in ohmic contact behavior with TFT results showing DC operation comparable to metal-overlapped devices. SA-BG devices were also fabricated using backside flood exposure on glass substrate. In order to enable SA-BG staggered devices using top side flood exposure on Si substrate, a lithographic process is under development which utilizes the reflection from the underlying electrode, creating a mirror image of the gate electrode in positive photoresist above the IGZO channel region. This pattern definition, or extension thereof, can then be used to protect the channel region during subsequent S/D formation process. Experimental details and results for all these new techniques to realize SA device structures are described in this chapter.

4.1 SA-TG Co-Planar TFT

The SA-TG process shown in Figure 4.1 began with a thick isolation oxide (~500 nm SiO_2) thermally grown on a silicon wafer as the starting substrate. A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl. The S/D contact metal (100 nm Mo/Al bilayer) was sputtered and patterned using a lift-off process. A 50 nm PECVD SiO_2 layer was then deposited as the gate dielectric.



(a) Thick oxide growth

(b) IGZO MESA definition

(c) S/D contact metal (Mo/Al sputter)

(d) Passivation & anneal/Passivation open

(e) TG (Flash Al)

(f) IGZO S/D treatment

(g) Top-down view of a fabricated SA-TG IGZO TFT

Figure 4.1: (a-f) Step by step cross-sectional schematic of SA-TG (Type-TL (Treatment Last)) device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme (type-TL) the implant is blocked in both channel and S/D metal contact regions and (g) top-down view of a fabricated SA-TG IGZO TFT.

This was followed by 3 hr O_2 anneal at 400 °C with 2 hr controlled ramp-down in O_2 ambient. The devices were then capped with 10 nm Al_2O_3 film using ALD at 200 °C. The S/D contact regions were opened using 10:1 buffered HF. The TG electrode was then defined using evaporated Al with a lift-off process. Finally, the active S/D regions of the samples were then treated using ion-implantation or O_2 plasma. Figure 4.1g shows an image of a fabricated SA-TG device with S/D gaps of 4 μm visible over the outlined mesa region between the TG and the S/D metal contacts.

4.1.1 Oxygen Plasma Treatment

It is known that oxygen vacancies (V_o) act as donors in the IGZO film [5], thus it is crucial to optimize the channel region to achieve ideal characteristics. In this work, O_2 plasma was used to treat the underlapped IGZO regions in a similar fashion as previously investigated using argon plasma which attributed enhanced conductivity to the preferential dissociation of oxygen on the a-IGZO film surface by the $^{40}Ar^{+}$ ion bombardment due to its relatively high sputtering yield [21]. However, in this case, the IGZO is covered by protective passivation layers which prevent direct plasma exposure, thus a change in conductivity would likely be associated with induced dielectric charge or IGZO/passivation interface charge in the S/D gap regions.

The parameter settings of power and exposure time were 0.3 kW and 1, 2, and 5 minutes, respectively. The insight gained by showing the "non-activated" device operation is the lateral position of the characteristic in comparison to the "activated" device as shown in Figure 4.2a. The device characteristics are left shifted from standard TG device, with the amount of V_T shift (at $I_D = 10^{-10}$ A) and the low-drain current (taken @ $V_G = 10$ V) increasing with immersion time as shown in Figure 4.2b. The devices showed increased current with plasma immersion time which clearly indicates improvement in charge injection into the channel. Note that this is contrary to the

mechanism that is suggested in literature where it is described that O_2 plasma reduced oxygen vacancies, changing the surface morphology and reducing the trap density at the surface of the channel layer [14]. The associated shift in V_T progressively worsened with plasma immersion time. The V_T shift may be recoverable by O_2 anneal, although this would be counterproductive to maintaining a high carrier concentration. This technique is also not compatible with SA-BG devices since the O_2 plasma will etch the protective photoresist over the channel region. Plasma treated a-IGZO TFTs also suffer from thermal stability issues [34]. Hence, alternative strategy using ion implanted S/D activation is discussed in the following section.

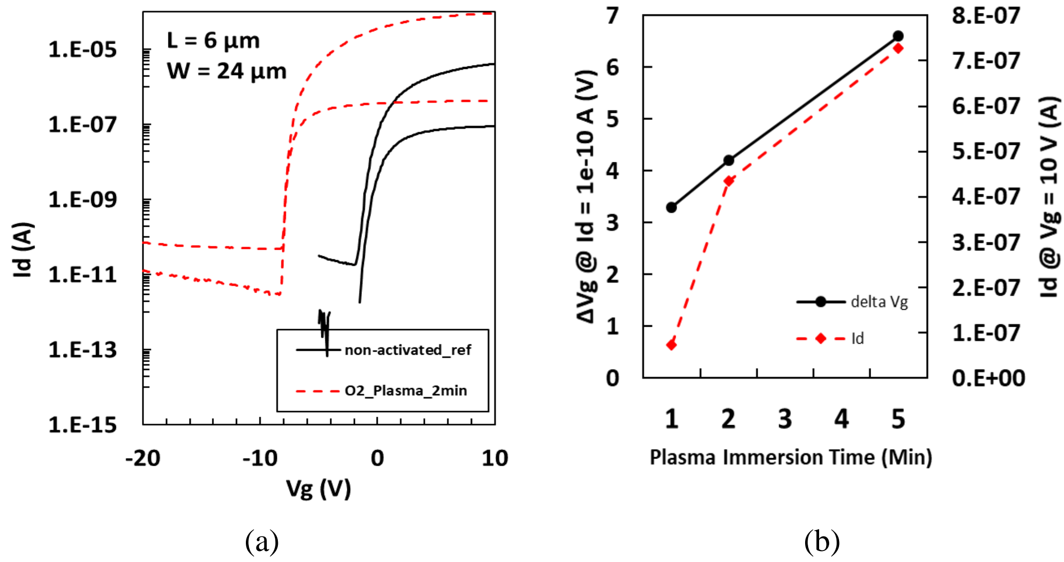


Figure 4.2: (a) O_2 plasma treated SA-TG device characteristics with L = 6 µm before (solid line) and after (dashed line) the treatment with t = 2 min and and 0.3 kW power and (b) the amount of shift in V_g at $I_d = 1\times10^{-10}$ A and the increase in I_d at $V_g = 10$ V and $V_{DS} = 0.1$ V observed based on the plasma immersion time. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between TG and S/D contact metal.

4.1.2 Ion Implantation

In this study, SA-TG and SA-BG co-planar TFTs has been fabricated using ion implantation technique to selectively form conductive IGZO regions, with the channel region masked by the gate electrode or associated pattern transfer. Several different species have been explored as shown in Table 4.1. Implant energies were chosen to ensure that a significant fraction of the dose resides in the IGZO film. The implant profiles were simulated using SRIM ion-matter interaction software [36], with a simulated distribution example shown in Figure 4.3. Only the implantation of boron and argon ions has been demonstrated to successfully "activate" IGZO.

Table 4.1: Design of experiments for ion-implantation treatment to realize SA-TG TFTs.

Species	**Energy (keV)**	**Dose (cm^{-2})**	**Beam Current (μA)**
$^{31}P^{+}$	80	4×10^{15}	100
$^{19}F^{+}$	60	2×10^{15}	30
$^{11}B^{+}$	35	4×10^{15}	50
$^{40}Ar^{+}$	80	2×10^{15} 4×10^{15}	80

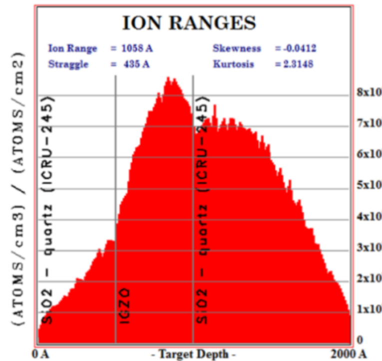


Figure 4.3: Representative SRIM analysis of $^{11}B^{+}$ implanted with energy E = 35 keV into IGZO beneath a 50 nm screen SiO_2 layer. The 50 nm screen oxide represents the gate dielectric above the IGZO. The IGZO material model was specified to have a compositional ratio of In:Ga:Zn:O = 1:1:1:4 and density of 6.1 g/cm^3 [37]. The simulation shows that approximately 40 percent of the implanted dose resides within the IGZO film, which translates to an average boron concentration of approximately 3.2×10^{20} cm^{-3} [35].

4.1.2.1 Phosphorus and Fluorine Implantation

SA-TG TFTs were implanted using $^{31}P^+$ and $^{19}F^+$ ions to activate the IGZO S/D regions. In both cases following the high-dose implants the device characteristics were shifted and distorted, with current levels below the initial non-implanted condition. The phosphorus implanted devices did not show any S/D activation and ~10 V left shifted transfer characteristics from standard TG devices was observed as shown in Figure 4.4a. It was initially hypothesized that this may be due to the devices being subjected to thermal stress during ion-implantation, however further results suggest a different origin that will be discussed.

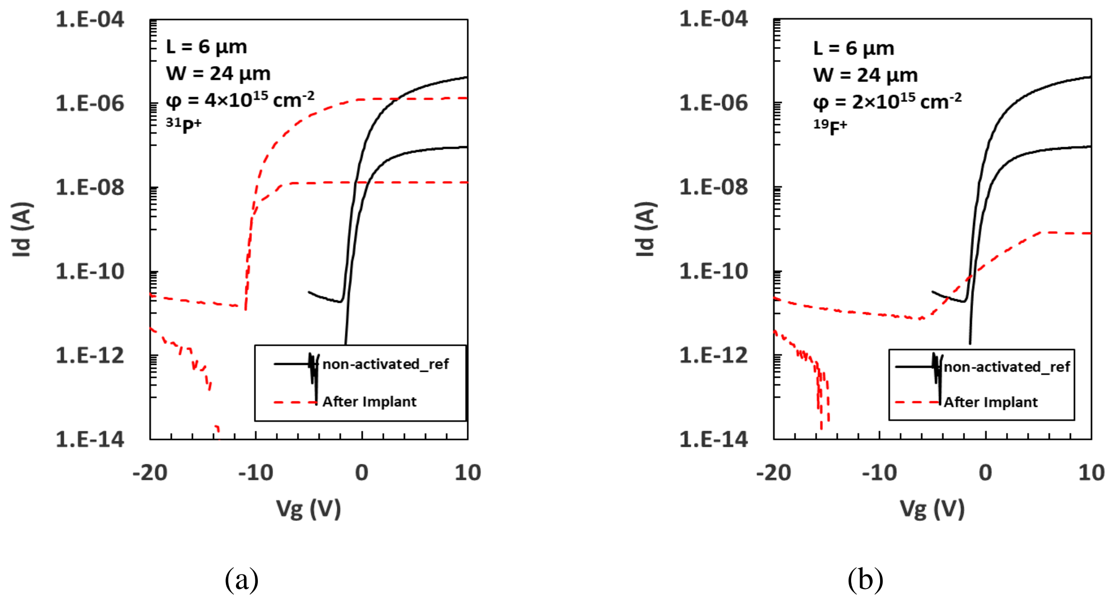


Figure 4.4: Comparison of SA-TG device characteristics for L = 6 µm with before (solid lines) and after (dashed lines) (a) $^{31}P^+$ implant with energy E = 80 keV and dose $\phi = 4\times10^{15}$ cm^{-2} and (b) $^{19}F^+$ implant with energy E = 60 keV and dose $\phi = 2\times10^{15}$ cm^{-2}. Here, the device width is 24 µm and the V_d is 0.1 V and 10 V respectively with 4 µm underlap between TG and S/D contact metal.

4.1.2.2 Argon Ion-Implantation

While argon plasma has been used to form selectively conductive IGZO regions, no work has been published with $^{40}Ar^+$ ion implantation into IGZO to make SA devices. In this work, $^{40}Ar^+$

ions have been implanted in the SA-TG devices at the very last step with two different doses. The activated S/D region became markedly conductive from the $\phi = 2\times10^{15}$ cm^{-2} implant, as shown in Figure 4.5a, albeit with a significant left shift. The electrical characteristic degradation at the higher dose ($\phi = 4\times10^{15}$ cm^{-2}) shown in Figure 4.5b happens to be more pronounced at the shorter channel length devices. A degradation in source injection results in current saturation and translates to poor current modulation in the transfer characteristics.

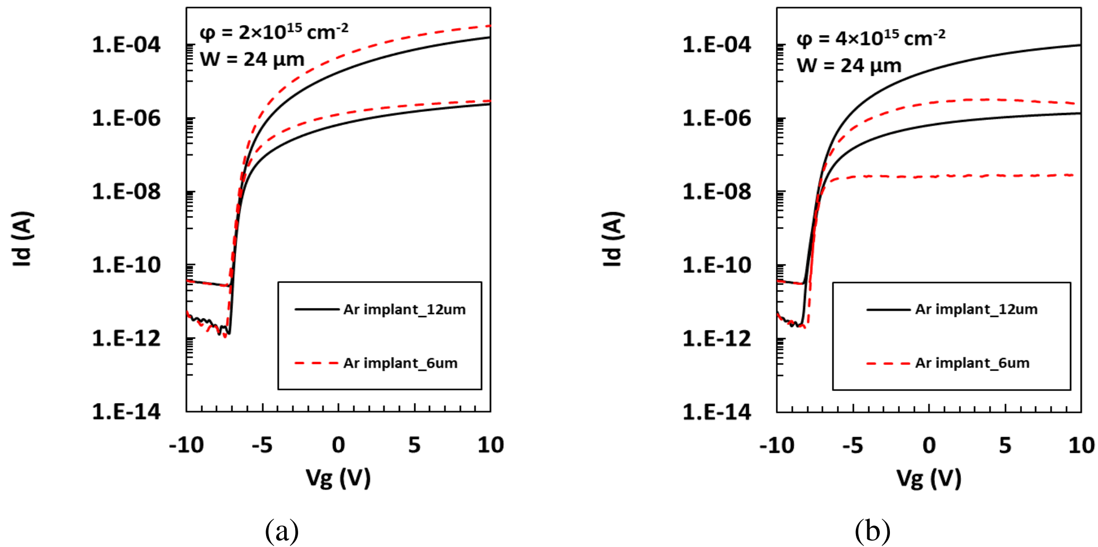


Figure 4.4: Comparison of $^{40}Ar^{+}$ implanted SA-TG device characteristics with L = 6 (red dashed line) and L = 12 µm (black solid line) with (a) $\phi = 2\times10^{15}$ cm^{-2} and (b) $\phi = 4\times10^{15}$ cm^{-2} and energy E = 80 keV. Here, the device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between TG and S/D contact metal.

Terada-Muta (T-M) analysis was done on $^{40}Ar^{+}$ implanted SA-TG devices with $\phi = 2\times10^{15}$ cm^{-2} [38], with the T-M plot shown in Figure 4.6. The common intersection of extrapolated characteristics occurs at $\Delta L \sim 1.67$ µm and a series resistance $R_{SD} \sim 0.68$ kΩ. The amount of series resistance equates to approximately one-fourth the measured sheet resistance of 2.75 kΩ/sq, which is close to the one-third estimation based on the device structure layout. The origin of free

electrons is not certain yet and there was no annealing following the implant process. Previous work in [21] suggests that the oxygen in the a-IGZO film surface is preferentially dissociated by the $^{40}Ar^{+}$ ion bombardment due to its relatively high sputtering yield. Hence, the carrier concentration increases most likely due to the formation of oxygen vacancies in a-IGZO film.

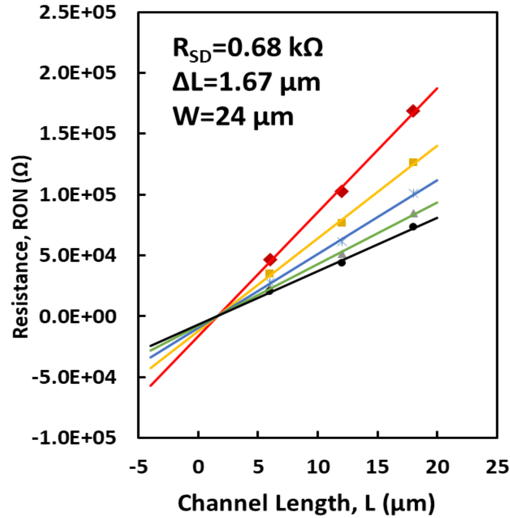


Figure 4.5: T-M analysis for $^{40}Ar^{+}$ implanted SA-TG devices using channel length of 6, 12, 18 µm devices. The resistance is calculated at Vg = 2, 4, 6, 8, 10 V with drain voltage at 0.1 V. The extracted parameters are ΔL = 1.67 µm and R_{SD} = 0.68 kΩ for 24 µm wide device.

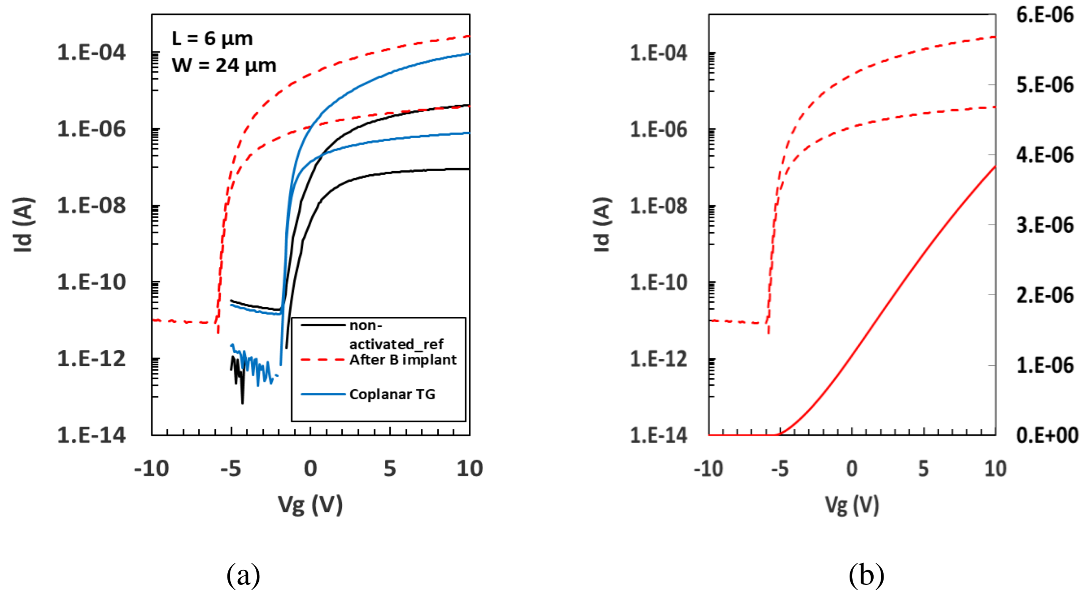
4.1.2.3 Boron Ion-Implantation

Boron-doped ZnO has been studied as a potential candidate in solar cell and solid state lighting [39]–[41] as a transparent conductive electrode. The ZnO:B film has low resistivity, high transparency and broad-band photoluminescence [39]. However, the doped regions were not formed selectively; no transistor characteristics were shown in these studies. Compared to polycrystalline ZnO, IGZO has better uniformity and stability due to its amorphous nature. This work is the first report of SA IGZO TFTs that have had selectively doped S/D regions formed via boron ion implantation [35]. The high-dose ($\phi = 4\times10^{15}$ cm^{-2}) $^{11}B^{+}$ implant was done at 35 keV

which is the lower energy limit of the ion implanter used. The boron implanted IGZO had a measured sheet resistance Rs ~ 9 kΩ/sq, which assuming an electron mobility $\mu_n = 10\ cm^2/(Vs)$ translates to an electron concentration of $n \sim 1.4\times10^{19}\ cm^{-3}$. This suggests an activation level of approximately 4% of the boron atoms present if in fact the mechanism involves boron behaving as an electrically active species, although the level of electrical activation is most likely higher considering mobility degradation due to implant damage and/or the presence of dopant ions. Note that there was no annealing following the implant process, and the relationship between boron and free electrons is not yet certain. However, results strongly suggest that boron is participating as an electrically active species, as will be discussed further in later portions of this chapter.

The I_d-V_{gs} transfer characteristics of the SA-TG TFT both before and after the boron implant are shown in Figure 4.7a, along with a comparison to a standard TG coplanar non-SA device. The SA-TG TFT prior to implant has significant series resistance which severely limits current flow. The boron implant increases the on-state current by more than two orders of magnitude and supports ohmic contact behavior and steep subthreshold operation.

The SA-TG characteristic exhibits a shift of approximately -4 V in comparison to the standard TG device with metal electrode overlaps, as shown in Figure 4.7a. The magnitude of shift is somewhat less in comparison to the results of other ion species; the origin of which remained uncertain. A similar left-shift was observed on implanted TG coplanar devices with metal blocking all IGZO regions, thus it is related to the implant process and not the presence of implanted boron atoms.



(a) (b)

Figure 4.6: (a) Comparison of device characteristics, SA-TG $^{11}B^+$ implanted ($\phi = 4\times10^{15}$ cm^{-2}) device with L = 6 µm (dashed lines) and standard co-planar TG device with L= 4 µm (blue solid line) and 4 µm underlap between TG and S/D contact metal. Here, the device width is 24 µm and V_d is 0.1 V and 10 V respectively. After $^{11}B^+$ implant, the I_d-V_{gs} curves are showing improved although left shifted characteristics. (b) SA-TG device characteristics with L= 6 µm after $^{11}B^+$ implant ($\phi = 4\times10^{15}$ cm^{-2}) in log scale (dashed line) and linear scale (solid line) [35].

To analyze the influence of generated heat during ion-implantation, $^{11}B^+$ was implanted using two different beam currents. From Figure 4.8a, it can be seen that the implant with relatively low beam current (20 µA) is left-shifted slightly less in comparison to the higher beam current (50 µA) implant; nonetheless the lower beam did not resolve the issue.

T-M analysis was done on SA-TG devices [38], with the T-M plot shown in Figure 4.8b. The common intersection of extrapolated characteristics occurs at ΔL ~2 µm and a series resistance R_{SD} ~ 8.5 kΩ. The lateral straggle from the boron implant has a negligible influence on the effective channel length, however the ΔL value incorporates process biases that are unique to the gate-defined channel length of the SA-TG device. The amount of series resistance equates to approximately "one square" of sheet resistance, which is higher than the device layout would

suggest. Regardless, the contact behavior is ohmic and has a minor influence on device behavior as shown in Figure 4.7b.

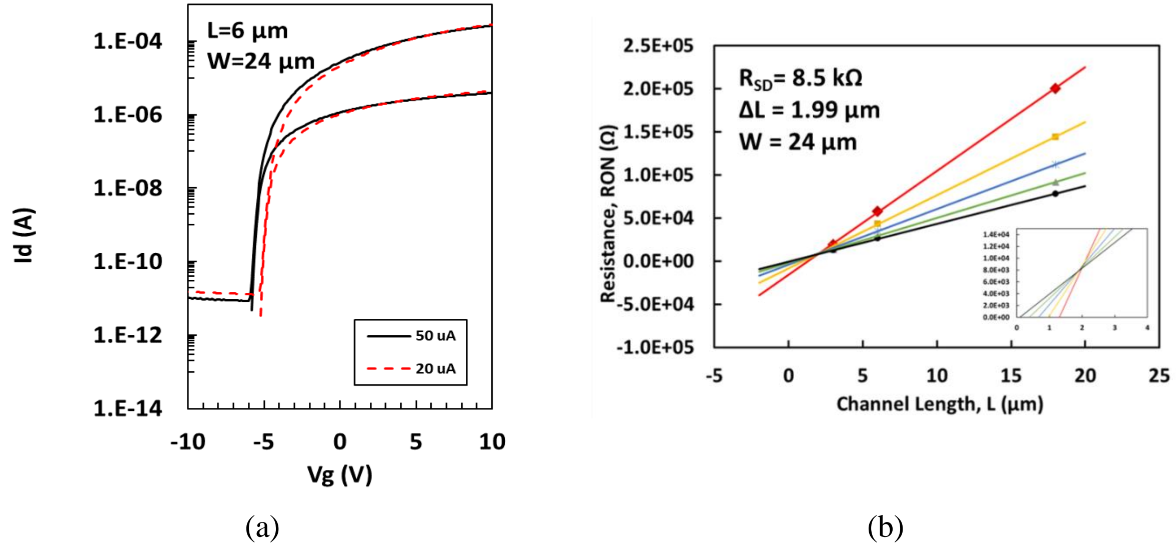


Figure 4.7: (a) Comparison of SA-TG device characteristics for L = 6 µm $^{11}B^{+}$ implanted ($\phi = 4\times10^{15}$ cm^{-2}) device with 20 µA (solid line) and 50 µA (dashed line) beam current. (b) T-M analysis for $^{11}B^{+}$ doped ($\phi = 4\times10^{15}$ cm^{-2}) SA-TG devices using channel length of 3, 6, 18 µm devices. For T-M analysis, the resistance is calculated at Vg = 2, 4, 6, 8, 10 V with drain voltage at 0.1 V [35]. The device width is 24 µm and the V_d is 0.1 V and 10 V respectively with 4 µm underlap between TG and S/D contact metal. The extracted parameters are ΔL = 1.99 µm and R_{SD} = 8.5 kΩ.

In addition to the SA-TG devices demonstrating left shifted characteristics, they also suffered from thermal instability during subsequent hotplate treatments, causing further shifting and distortion. This is presumably due to residual water reacting with the top metal gate during any successive high temperature steps [25]. These topics were further investigated on the BG self-aligned structure that does not include a top-gate metal feature that is likely operative in these noted issues.

4.2 SA-BG STAGGERED TFT

Traditional BG staggered TFT configuration has also been explored which utilizes back-side through-glass exposure. Several different ion species have been explored as well to make IGZO selectively conductive as shown in Table 4.2. Both $^{11}B^{+}$ and $^{40}Ar^{+}$ ion implantation has demonstrated good TFT transfer characteristics. Here, the dose values were chosen based on previous SA-TG device results including a higher dose value for $^{11}B^{+}$.

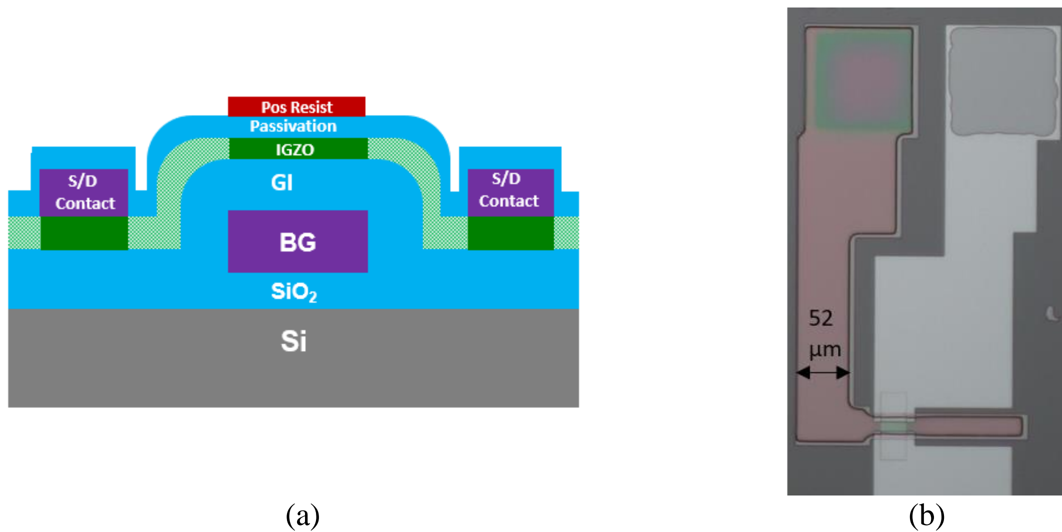
Table 4.2: Design of experiments for ion-implantation treatment to realize SA-BG TFTs.

Species	Energy (keV)	Dose (cm^{-2})	Beam Current (μA)
$^{11}B^{+}$	35	4×10^{15}	50
		8×10^{15}	85
$^{40}Ar^{+}$	80	2×10^{15}	100

4.2.1 Pseudo-SA BG Lithographic Process

The SA-BG process was investigated using a "pseudo" self-aligned process. It is not truly self-aligned; rather it mimics a self-aligned device concept where the channel was protected from ion implant by using a BG photoresist pattern with special attention to overlay. The process flow had several steps common to the standard staggered BG process, with top-side exposure using BG mask to protect the channel region from S/D activation techniques on silicon wafers. This is done to ensure that the SA-BG strategy will work with the implanted species. A 50 nm Mo gate electrode was sputtered and patterned on a thick isolation oxide (~650 nm SiO_2) thermally grown on silicon wafers, followed by a 50 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390 °C). The SiO_2 was densified for 2 hours in N_2 at 600 °C in a furnace. A 50 nm IGZO layer was sputter deposited using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, followed by mesa pattern and etch using dilute HCl. The S/D contact metal (100 nm Mo-Al bilayer) was then

sputtered and defined by lift-off technique using Futurrex NR9g-1500PY negative photoresist. A second 50 nm PECVD SiO_2 layer was then deposited as the passivation material. The wafer was coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C and over-exposed for 5 sec using BG mask which left resist on top of BG polygon with careful attention to overlay, thereby protecting the IGZO channel region. The alignment of the BG polygon is critical for the appropriate activation of the underlapped S/D region. Note that the overexposure ensures the resist polygon is inside the original gate definition. After exposure, the resist was developed for 45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 s at 140 °C. The wafer was then ion implanted for S/D activation and resist was removed after the ion implantation using lift-off technique.



(a) (b)

Figure 4.8: (a) Cross-sectional schematic and (b) top-down view of pseudo-SA BG device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme, the implant is blocked in the channel region only and the alignment of the BG pattern is critical.

A 3-hour O_2 passivation anneal at 400 °C with a 2-hour controlled ramp-down in O_2 ambient was performed, and immediately followed by an HMDS vapor treatment at 140 °C to avoid water adsorption. The devices were then immediately capped with 10 nm Al_2O_3 film using ALD at 200 °C after annealing to minimize exposure to air ambient. Finally, the gate and S/D contact windows were patterned and etched using 10:1 buffered HF solution. Figure 4.8 shows the cross-section schematic and top-down view of the pseudo SA-BG device. The device characteristics shown in Figure 4.9 represents a $^{11}B^+$ implanted pseudo-SA BG device with E = 35 keV and $\phi = 4\times10^{15}$ cm^{-2}. The characteristics do not experience the pronounced left-shift demonstrated by SA-TG devices. This implies that the origin of the left-shift was due to metal electrode charging during the implant, subjecting the gate dielectric to electrical stress and inducing positive bulk oxide charge. The pseudo-SA BG characteristics are left shifted compared to the standard non-SA BG device characteristics shown in chapter 3 (Figure 3.6a), however the shift is relatively minor ($\Delta V \sim 1$ V).

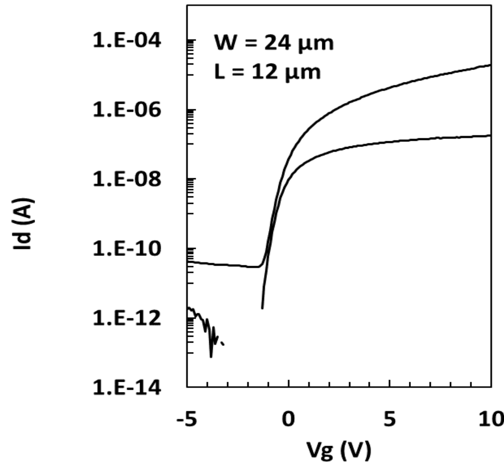


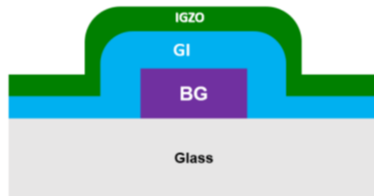
Figure 4.9: $^{11}B^+$ implanted ($\phi = 4\times10^{15}$ cm^{-2}) pseudo-SA BG device characteristics with L = 12 µm. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between BG and S/D contact metal.

4.2.2 SA-BG Lithographic Process Using Backside Flood Exposure

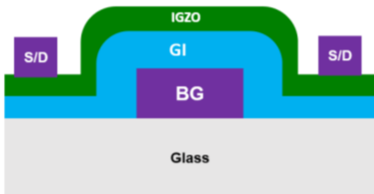
The SA-BG process investigated had several steps common to the SA-TG process flow, with back-side flood exposure through glass. Figure 4.10 shows cross-sectional schematics of the SA-BG lithographic process. Using a glass substrate, a 50 nm thick Mo gate electrode was sputtered and patterned, followed by a PECVD SiO_2 gate dielectric which was densified for 2 hours at 600 °C in N_2. A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl. The S/D contact metal (100 nm Mo/Al bilayer) was then sputtered and patterned using a lift-off process. A 50 nm PECVD SiO_2 passivation oxide was then deposited, followed by the O_2 anneal and Al_2O_3 capping layers described previously. The wafer was then coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C. Back-side illumination with broadband spectrum was done using Suss MA150 Contact Aligner and a black absorbing layer was used to avoid reflections. After exposure, the resist was developed for 45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 s at 140 °C. The samples were then ion implanted for S/D activation. Finally, the resist was removed, and the S/D contact regions were opened using 10:1 buffered HF.

(a) BG definition

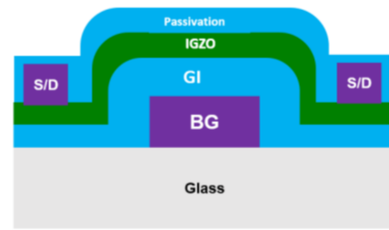
(b) BG dielectric (TEOS)



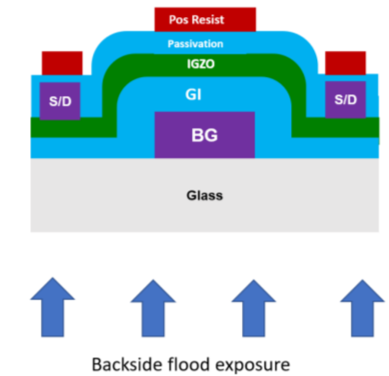
(c) IGZO MESA definition



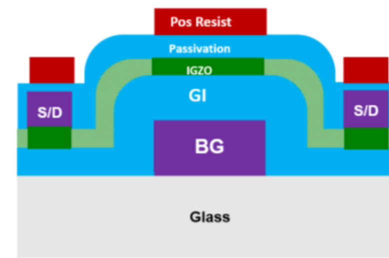
(d) S/D contact metal (Sputter Mo/Al)



(e) Passivation oxide/ Passivation anneal



(f) Positive resist & back side flood exposure

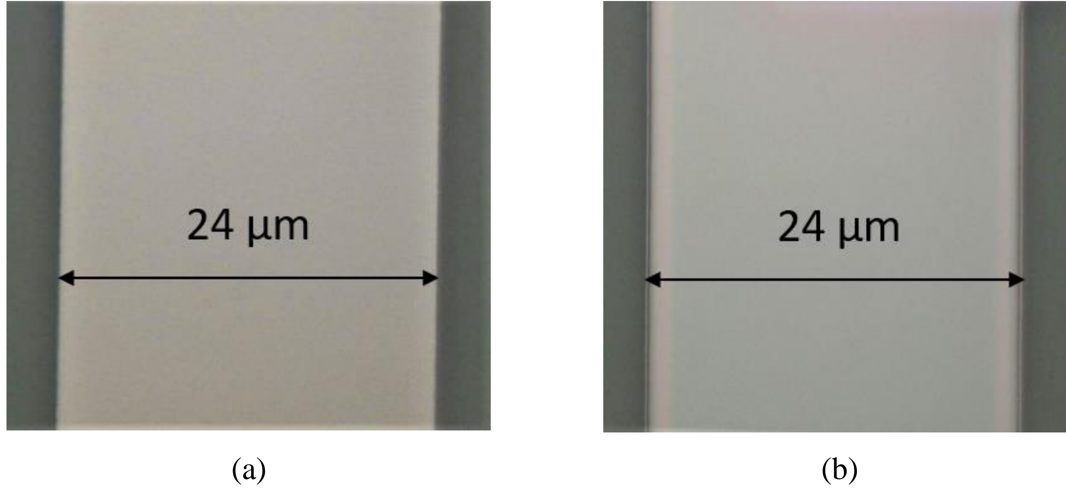


(g) S/D treatment on IGZO

(h) Resist removal/Passivation Open

Figure 4.10: Step by step cross-sectional schematic of SA-BG device, where the textured and non-textured IGZO represents implanted and non-implanted regions, respectively. Note that in this process scheme the implant is blocked in both channel and S/D metal contact regions.

Figure 4.11 shows the resist profile with and without backside flood exposure. Resist was remaining everywhere without the backside flood exposure whereas resist was only remaining on top of BG polygon with the backside flood exposure.



(a) (b)

Figure 4.11: BG pattern (a) without backside flood exposure and (b) with backside flood exposure. Note that, resist is remaining everywhere without the backside flood exposure whereas resist is only remaining on top of BG polygon with the backside flood exposure.

4.2.2.1 Boron Ion-Implantation

In this experiment, $^{11}B^{+}$ was implanted with 35 keV energy at two different doses (4×10^{15} cm^{-2} and 8×10^{15} cm^{-2}). The initial results were similar to the characteristics of pseudo-SA-BG devices. From the transfer characteristics for SA-BG $^{11}B^{+}$ implanted (4×10^{15} cm^{-2} dose) device shown in Figure 4.12a, it was observed that there is a left shift in the characteristics for 6 µm device compared to the 12 µm device. From the T-M analysis, R_{SD} is ~ 23 kΩ and ΔL is 3.6 µm as shown in Figure 4.12b. Thus, the effective channel length for a 6 µm device is only ~2.5 µm, however the origin of the left shift in the transfer characteristics is still in question and will be discussed further.

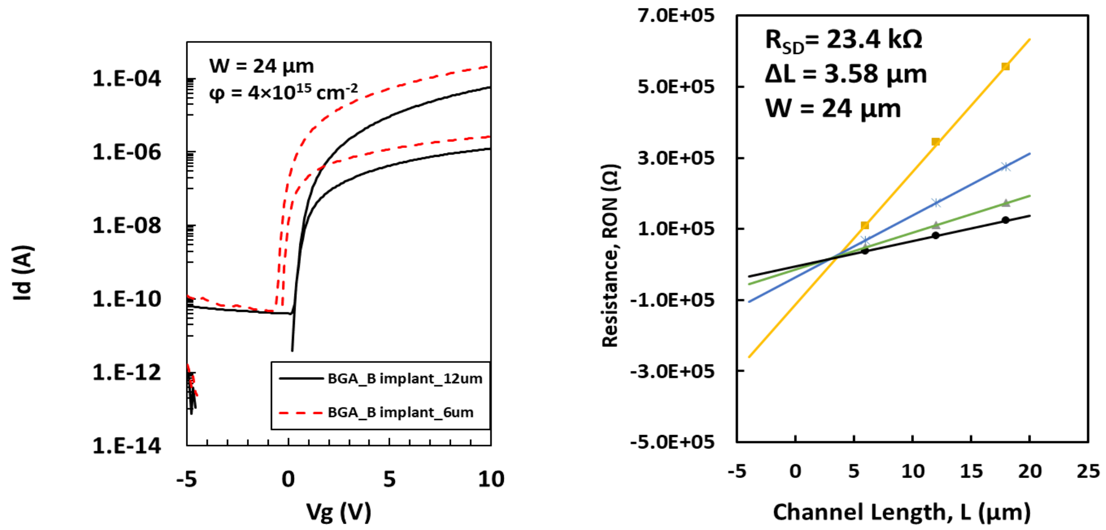


Figure 4.12: (a) Comparison of $^{11}B^{+}$ implanted SA-BG device characteristics with $L = 6$ µm (dashed line) and $L = 12$ µm (solid line) with $\phi = 4\times10^{15}$ cm^{-2} into 4 µm underlap regions between resist mask and source-drain metal. The device width is 24 µm and V_{ds} is 0.1 and 10 V and (b) T-M analysis for $^{11}B^{+}$ implanted SA-BG devices using channel lengths of 6, 12, 18 µm devices. The resistance is calculated at $V_g = 4, 6, 8, 10$ V with drain voltage at 0.1 V. The extracted parameters are $\Delta L = 3.58$ µm and $R_{SD} = 23.4$ kΩ.

The large ΔL is mainly due to the subtractive wet-etch for the bottom gate patterning. As seen from microscope images of the SA-BG devices in Figure 4.13a, the gate pattern has ~2 µm offset from the mask defined gate length.

(a) (b)

Figure 4.13: (a) SA-BG IGZO TFT with channel length $L = 6$ µm with effective channel length of $L = 4$ µm as defined by the subtractive wet etching using positive photoresist with 2 µm offset from the mask definition (i.e. $\Delta L \sim 2$ µm) and (b) SA-TG IGZO TFT with channel length $L = 6$ µm as defined by the S/D lift-off metallurgy using negative photoresist (Futurrex NR9g-1500PY) with almost negligible offset from the mask definition (i.e. $\Delta L \sim 0$).

The SA-TG devices as shown in Figure 4.13b do not have any offset since the TG is patterned by lift-off using NR9g-1500PY negative resist with almost no offset as shown previously in Figure 3.1.

After subjecting the devices to 175 °C hot-plate bake for an hour, there was a slight shift in the transfer characteristics of the 12 μm long device as shown in Figure 4.14a, which became significant as the cumulative time was increased to 2 hours and finally 4 hours. The standard non-SA devices did not exhibit any left shift upon thermal stress testing, which suggests this left shift in SA-BG devices is due to B entering the channel region and behaving as a donor species. Figure 4.14b is an adjusted overlay of the original and 4 hour hot-plate bake characteristics, and shows that the thermal stress response is only a shift, and is not a reduction in channel length. This suggests that the active boron species in the S/D regions remains stable, however inactive boron may be more mobile and provide a relatively low dose throughout the channel region.

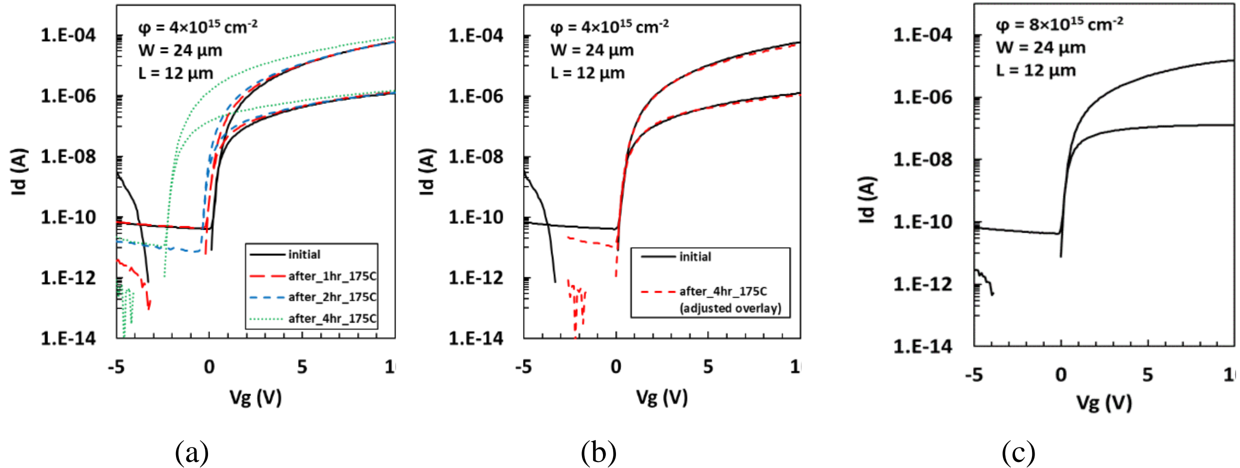
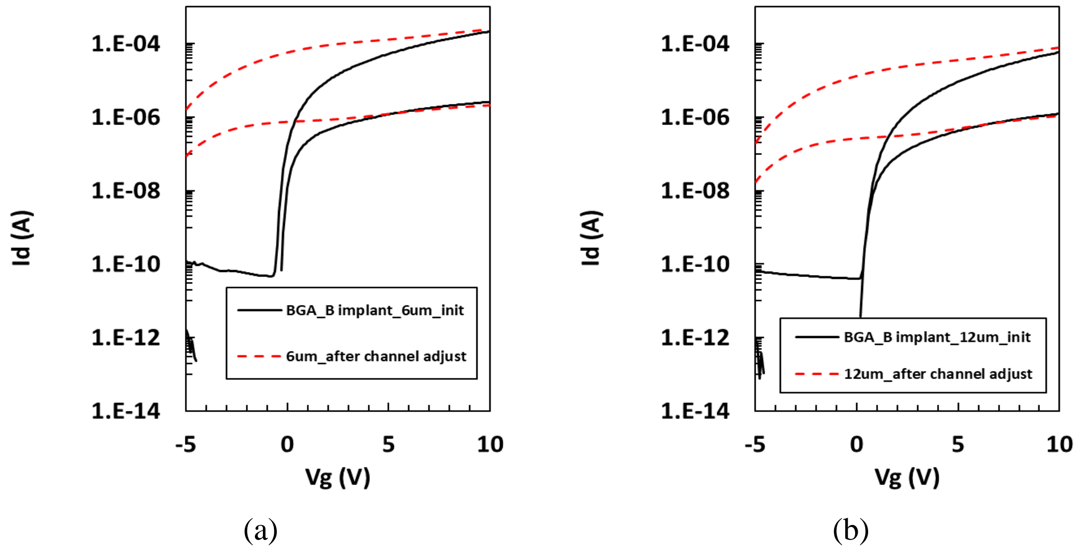


Figure 4.14: (a) Comparison of $^{11}B^{+}$ implanted SA-BG device characteristics with (a) L = 12 μm and ϕ = 4×10^{15} cm^{-2} before (solid line) and after (dashed lines) successive 175 °C bakes, (b) adjusted overlay of the original and 4 hour hot-plate bake characteristics and (c) L = 12 μm with ϕ = 8×10^{15} cm^{-2}. The device width is 24 μm and the V_d is 0.1 and 10 V respectively with 4 μm underlap between BG and S/D contact metal.

This may also be the origin of the left-shifted characteristics of the 6 µm device shown in Figure 4.14a, which has a much shorter effective channel length and could experience thermal diffusion during the implant due to heat generated. When the dose was doubled to 8×10^{15} cm^{-2}, the transfer characteristics degraded as shown in Figure 4.14c. This suggests that 4×10^{15} cm^{-2} dose was already at or above the limit of B solid solubility in IGZO and additional B doping (8×10^{15} cm^{-2}) created interstitial point defects in the underlapped region. The devices exhibited degradation in charge injection from source to the channel that is pronounced at low drain bias (0.1 V) as shown in Figure 4.14c. It should be reinforced that the channel was not implanted; this was only an effect of the additional implant in the S/D region.

4.2.2.2 V_T Adjust



(a) (b)

Figure 4.15: Comparison of low dose ($\phi = 2\times10^{12}$ cm^{-2}) $^{11}B^{+}$ implant on $\phi = 4\times10^{15}$ cm^{-2} $^{11}B^{+}$ implanted SA-BG device characteristics for V_T adjust with (a) L = 6 µm and (b) L = 12 µm. The device width is 24 µm and the V_d is 0.1 and 10 V respectively with 4 µm underlap between BG and S/D contact metal.

Here, the entire IGZO mesa (IGZO channel and conductive IGZO S/D with 4×10^{15} cm^{-2} dose) is subjected to a low dose (2×10^{12} cm^{-2}) ion implant at E = 35 keV in order to adjust the V_T. However, all the devices exhibited > 5V left shifted characteristics as shown in Figure 4.15.

4.2.2.3 Argon Ion-Implantation

Argon was implanted to realize SA-BG devices with 80 keV energy and 2×10^{15} cm^{-2} dose, with transfer characteristics shown in Figure 4.16. As in the case of boron-implanted SA-BG devices, the transfer characteristics do not show the left shift associated with SA-TG devices. The initial characteristics after implant exhibited a slight crossover effect, which is attributed to localized defects in the transition between the active S/D regions and the channel. This cross-over was not apparent on SA-TG devices due to the large amount of gate oxide induced charge which dominated the electrical behavior. It was also not present on boron implanted SA-BG devices.

After the 175 °C hot-plate bake for an hour, the characteristics degraded as shown in Figure 4.16. The current degradation suggests “deactivation” due to instability of the argon-induced activation mechanism. The Gate Induced Drain Leakage (GIDL) behavior is pronounced after thermal stress, suggesting the creation of secondary defects. There is no characteristic left-shift associated with the argon implanted SA-BG devices, which is consistent with a defect-induced activation mechanism rather than an electrically active argon species. These remaining defect effects would have to be eliminated for argon implant to be used in a self-aligned device strategy.

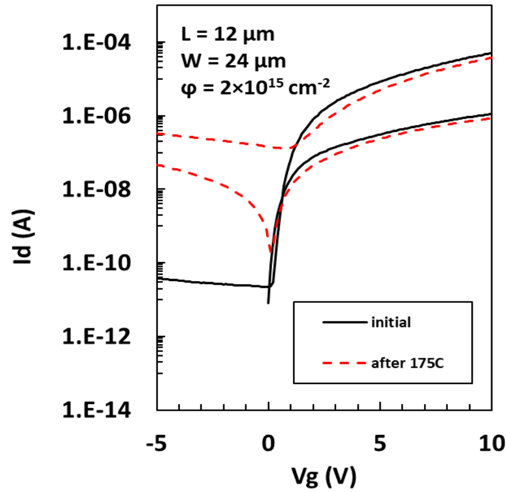


Figure 4.16: Comparison of $^{40}Ar^{+}$ implanted SA-BG device characteristics with $L = 12$ µm, $E = 80$ keV and $\phi = 2\times10^{15}$ cm^{-2} before (solid line) and after (dashed line) 175 °C bake for an hour.

4.2.3 SA-BG Lithographic Process Using Topside Flood Exposure

The SA-BG with topside flood exposure investigated had several steps common to the SA-BG with backside flood exposure process flow, with a top-side flood exposure and optical thin-film interference used to produce a "reflection gate" electrode to serve as an implant mask. Using the same oxidized silicon substrate described previously, a 50 nm thick Mo gate electrode was sputtered and patterned, followed by a PECVD SiO_2 gate dielectric which was densified for 2 hours at 600 °C in N_2. A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl. A 50 nm PECVD SiO_2 passivation oxide was then deposited, followed by the O_2 anneal and Al_2O_3 capping layers described previously. The wafer was then coated with AZ MIR 701 positive resist following an HMDS vapor prime at 140 °C. Top-side illumination at g-line ($\lambda = 436$ nm) with an irradiance of ~ 100 mW/cm^2 was done using an exposure array to determine the resulting contrast between photoresist lying above the field and gate regions. After exposure, the resist was developed for

45 sec in Microposit MF CD-26 developer solution and hotplate baked for 60 sec at 140 °C. Figure 4.17 shows cross-sectional schematics of the SA-BG lithographic process.

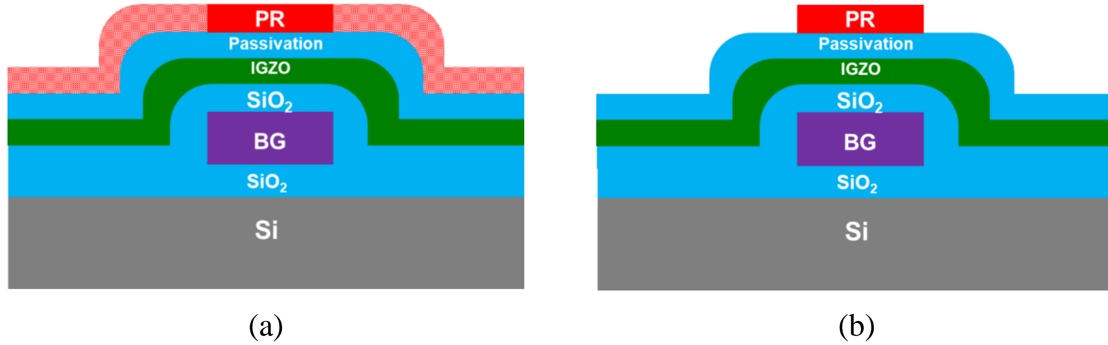


Figure 4.17: Cross-sectional schematic of a SA-BG lithographic process (a) after exposure and (b) after develop [35].

A preliminary indication of the feasibility of the "reflection gate" process was observed during the IGZO mesa lithographic process, which under standard exposure conditions resulted in underexposure over the BG electrode outside of the mesa region while the field area was completely cleared of photoresist. This was then recognized as a potential method for integration into a SA-BG process using a topside flood exposure under optimal exposure conditions. Because of the involvement of interface reflections and thin-film interference the process was found to be extremely sensitive to differences in film thickness and optical properties. For this process to work correctly, the photoresist must mirror the BG polygons with complete coverage.

An exposure array with short time increments ($\Delta t = 0.03$ s) was used for open field exposures on resist-coated BG structures in search of settings that would yield acceptable image contrast with minimal edge exclusion. Select results are shown in Figure 4.18, along with the exposure times used on the projection stepper system.

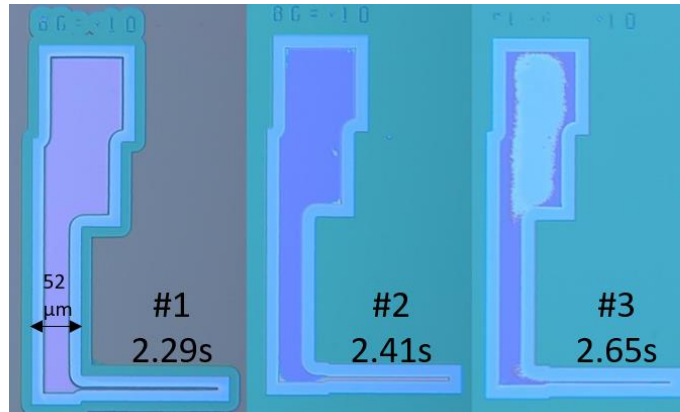


Figure 4.18. Photoresist-coated BG structures that were flood exposed for times indicated; all samples exhibit significant edge exclusion. The short exposure time of sample#1 did not clear the field region, whereas the long exposure time of sample#3 resulted in partial clearing of photoresist over the planar BG region [35].

The results shown in Figure 4.18 suggest that an exposure time of ~ 2.4 sec may clear the field of photoresist while maintaining the self-aligned BG image, shown by sample # 2. However, all samples exhibited an edge exclusion, which would result in a significant change in channel length dimension and large gate-S/D overlaps. In addition, the photoresist thickness loss in areas where it did remain may not provide an adequate implant masking layer. The BG image integrity over the mesa is the only region of importance for S/D implant blocking. Unfortunately, a suitable process window was not identified within the experimental conditions used. More experiments which investigate other parameters such as the develop process conditions (e.g. time, concentration) are required.

4.3 SUMMARY

Investigation on new techniques towards the realization of SA IGZO TFTs has been presented in this chapter. The non-traditional definition of the term "activation" has been used to indicate the

creation of ionized donors and associated free electrons from the applied process itself. Oxygen plasma has been demonstrated as an effective activation technique for SA-TG devices. Results suggested that the increase in O_2 plasma immersion time shifts the characteristics to the left compared to the non-treated one, as well as increases the current. This shift and rise indicates improvement in source charge injection; unfortunately the V_T shift ensures depletion-mode operation. These results guided efforts towards ion implantation as an alternative strategy for S/D regions formed selectively, with the channel region masked by the gate electrode (TG) or photoresist proxy (BG). Several different ion species were investigated including $^{40}Ar^{+}$, $^{11}B^{+}$, $^{31}P^{+}$ and $^{19}F^{+}$ as shown in Table 4.3. The damage level indicates the relative amount of displacements (i.e. vacancies) induced by the implant. While the resulting chemical bonding arrangement involving the ion species has not been determined, the interpretation of chemical involvement indicates the expected chemical role in promoting electrical activation.

Table 4.3: Interpretation of implanted species.

Implant Species	Damage Level	Chemical Involvement (Interpreted)
$^{40}Ar^{+}$	High	Null
$^{31}P^{+}$	High	Negative
$^{19}F^{+}$	Low	Negative
$^{11}B^{+}$	Low	Positive

Argon implanted activation appeared to be consistent with creation of donor-like defect states without chemical participation (e.g. oxygen vacancy defects). Phosphorus and fluorine treatments did not support free carriers. Boron implanted activation appeared to be consistent with boron participating as an electrically active species supporting free electrons. Both argon and boron resulted in a significant left-shift in SA-TG devices which was attributed to metal gate charging

during the ion implant process, which was not observed on SA-BG devices. Both species demonstrated degraded charge injection at higher level dose treatments which was attributed to high level defects and/or inactive species which degrades S/D activation behavior.

Boron implanted devices exhibited a characteristic left-shift via hotplate baking at 175 °C which was not observed on non-SA devices. The shift is apparent on short-channel devices without baking, presumably due to heat generation during ion implantation. It is attributed to some fraction of boron with high diffusivity spreading throughout the channel region and expressly not associated with a reduction in channel length or performance degradation. The shift due to low-dose boron V_T adjustment was much larger than expected (~ 3-4x), indicating that both defect and chemical roles may be operative.

Argon implanted SA-BG initial characteristics exhibited a slight crossover effect, which was attributed to localized defects in the transition between the active S/D regions and the channel. This cross-over was not apparent on SA-TG devices due to the large amount of gate oxide induced charge which dominated the electrical behavior. Argon implanted devices exhibited performance degradation via hotplate baking at 175 °C without any associated lateral shift, which is attributed to defect state reconfiguration. This current degradation indicates less donor states for charge injection and pronounced GIDL suggests creation of deep states that facilitate band-to-band tunneling.

Overall, boron implanted SA-BG devices demonstrated superior performance over SA-TG and argon implanted devices, with equivalent transfer characteristics as the standard (non-SA) BG staggered device. A novel lithographic technique has also been described with the potential of enabling SA-BG devices using topside exposure; process development is ongoing.

Chapter 5. CONCLUSION

This chapter provides a summary of the results and findings in the self-aligned TFT investigation, and how a self-aligned device structure will enable submicron scaling of IGZO TFTs. The main goal of this work was to fabricate SA-TG and SA-BG IGZO TFTs with different S/D activation techniques. While exposure to oxygen plasma demonstrated successful activation in a SA-TG device, a significant lateral left-shift was observed in the transfer characteristics due to induced dielectric charge and/or interface charge in the channel region. This strategy was not pursued for the BG structure since it involves a photoresist mask incompatible with the oxygen plasma process.

Implantation of select ion species was successful in demonstrating self-aligned IGZO TFTs. This is the first report of the use of either implanted boron or argon for selective activation of the source drain regions. Similarities and differences in the specific behavior of boron and argon activated SA devices were described in detail in Chapter 4. The interpretation of various electrical results is summarized by the following conclusions:

- SA-TG devices experienced a significant left-shift which was associated with charging of the metal gate electrode mask, thus subjecting the passivation dielectric to a higher electric field and the creation of bulk and/or interface charge. SA-BG devices did not experience this issue.
- Argon implant activation involves a defect-induced donor mechanism, likely involving oxygen vacancy defects and/or passivation with hydrogen. The resulting TFTs

demonstrate slight slow-trap behavior, with pronounced degradation following thermal stress treatments below 200 °C suggesting the formation of secondary defects.

- Boron implant activation involves formation of an electrically active donor species involving chemical bonding with a fraction of boron atoms present. These active regions remain fixed during thermal treatments, however unbound boron atoms may be mobile at thermal treatments below 200 °C and result in low active donor concentrations in the channel region, thus responsible for a left-shift in transfer characteristics.
- Both boron and argon species demonstrated pronounced degradation in charge injection at higher dose treatments. While the activation mechanisms are interpreted to be distinctly different, the additional defects associated with high-dose treatments result in similar degradation behavior.

Boron implanted SA-BG devices demonstrated superior performance over SA-TG and argon implanted devices, with equivalent transfer characteristics as the standard non-SA BG staggered device. The devices are subject to thermal V_T shift related to the presence of boron, however the mechanism is distinctly different than that attributed to the presence of water at the back-channel region [25]. Minimizing thermal exposure would limit the influence of this mechanism. Alternatively, this mechanism may be a method for the selective formation of depletion-mode NMOS devices for improved circuit performance. Refinements in this self-aligned device strategy will enable the ability to scale to smaller channel lengths without the associated limitations of a channel length defined by the S/D contact regions.

Further studies must be done to investigate alternative integration strategies, such as performing the boron S/D implant prior to the 400 °C O_2 furnace anneal. Material characterization

of the doping process must be done to establish the role that boron has in supporting free carriers in IGZO. X-ray Photoelectron Spectroscopy (XPS) for $[V_o]$ comparisons, and Secondary Ion Mass Spectroscopy (SIMS) for channel region analysis, are in progress. Additional techniques need to be identified to characterize bonding and ionization state; a significant challenge at species $< 1\%$ atomic concentration.

Advancements in self-aligned S/D activation techniques, in combination with the application of a high-κ gate dielectric for improved channel control, and process development for gate patterning and etch processes, will enable high-performance submicron IGZO TFTs with minimal parasitic resistance and capacitance.

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