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Semiconductor Nanofabrication via Metal-Assisted Chemical Etching: Ternary III-V Alloys and Alternative Catalysts

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Semiconductor Nanofabrication via Metal-Assisted Chemical Etching: Ternary III-V Alloys and Alternative Catalysts

by

Thomas S. Wilhelm

A dissertation submitted in partial fulfillment of the requirements

for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering

Kate Gleason College of Engineering

Rochester Institute of Technology

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Abstract

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The increasing demand for complex devices that utilize three-dimensional nanostructures has incentivized the development of adaptable and versatile semiconductor nanofabrication strategies. Without the introduction and refinement of methodologies to overcome traditional processing constraints, nanofabrication sequences risk becoming obstacles that impede device evolution. Crystallographic wet-chemical etching (e.g., Si in KOH) has historically been sufficient to produce textured Si surfaces with smooth sidewalls, though it lacks the ability to yield high aspect-ratio features. Physical and chemical plasma etching (e.g., reactive-ion etching) evolved to allow for the creation of vertical structures within integrated circuits; however, the high energy ion bombardment associated with dry etching can cause lattice and sidewall damage that is detrimental to device performance, particularly as structures progress within the micro- and nano-scale regimes.

Metal-assisted chemical etching (MacEtch) provides an alternative processing scheme that is both solution-based and highly anisotropic. This fabrication method relies on a suitable catalyst (e.g., Au, Ag, Pt, or Pd) to induce semiconductor etching in a solution containing an oxidant and an etchant. The etching would otherwise be

inert without the presence of the catalyst. The MacEtch process is modelled after a galvanic cell, with cathodic and anodic half reactions occurring at the solution/catalyst and catalyst/semiconductor interfaces, respectively. The metal catalyzes the reduction of oxidant species at the cathode, thereby generating charge carriers (i.e., holes) that are locally injected into the semiconductor at the anode. The solution interacts with the ionized substrate, which creates an oxide that is preferentially attacked by the etchant. Thus, MacEtch offers a nanofabrication alternative that combines the advantages of both wet- and dry-etching, while also overcoming many of their accompanying limitations. This provides a tunable semiconductor processing platform using controlled top-down catalytic etching, affording engineers greater processing control and versatility over conventional methodologies.

Here, Au-enhanced MacEtch of the ternary alloys InGaP and AlGaAs is demonstrated for the first time, and processes are detailed for the formation of suspended III-V nanofoils and ordered nanopillar arrays. Next, a lithography-free and entirely solution-based method is outlined for the fabrication of black GaAs with solar-weighted reflectance of $4\,\%$. Finally, a comparison between Au- and CNT-enhanced Si MacEtch is presented towards CMOS-compatibility using catalysts that do not introduce deep level traps. Sample preparation and etching conditions are shown to be adaptable to yield an a priori structural design, through a modification of injected hole distributions. Critical process parameters that guide the MacEtch mechanisms are considered at length, including heteroepitaxial effects, ternary material composition, etching temperature, and catalyst type, size, and deposition technique. This work extends the range of MacEtch materials and its fundamental mechanics for fabrication of micro- and nano-structures with applications in optoelectronics, photovoltaics, and nanoelectronics.

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Onward in the pursuit of discovery.

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Chapter 1

Introduction and Motivation

1.1 Motivation

Micro- and nano-structured semiconductor architectures have been an area of extensive study for years, and are being incorporated into a wide variety of electronic and photonic devices due to their unique properties compared to their bulk counterparts [1–4]. Traditional top-down nanostructure fabrication techniques include patterned wet-etching and reactive-ion etching (RIE), though these methods come with a variety of limitations and disadvantages [5, 6]. A major advantage of RIE is its directionality and ability to generate highly anisotropic geometries. However, it often requires processing at elevated temperatures with hazardous gases. Additionally, RIE causes sidewall damage and lattice defects, which are undesirable as devices continue to move toward smaller dimensions and higher aspect ratio features [7]. Likewise, patterned wet-etching is advantageous for being solution-based and having fabrication compatibility with conventional benchtop semiconductor processing methods. Although its simplicity and cost-efficiency is attractive, patterned wet-etching lacks the ability to generate high aspect ratio features because of its isotropic nature and/or crystallographic etching dependencies [8].

Metal-assisted chemical etching (MacEtch) techniques provide top-down, solution-based nanofabrication strategies that combine many of the advantages of other top-down techniques (e.g., low cost and simple processing, and ability to yield high aspect

ratio architectures), without many of the corresponding disadvantages (e.g., isotropic etching, processing requirements at high temperature with hazardous gases, and high vacuum instrumentation) [8, 9]. Forward-progression MacEtch behavior was reported by Dimova-Malinovska et al. in 1997 [10]. Inverse-progression MacEtch (I-MacEtch) behavior was first noted under UV-illumination by Asoh et al. in 2010 and termed metal-assisted photodissolution [11]. The MacEtch and I-MacEtch processes were detailed and formalized in 2000 [12] and 2015 [13], respectively. These techniques are powerful alternatives for the fabrication of micro- and nano-structures that have been utilized throughout many fields, such as energy storage [14], photonics [15, 16], nanoelectronics [17, 18], photovoltaics [19], optoelectronics [2, 20]. Although much of the research in this field has focused on Si [21–24], binary III-V materials, including GaN [25, 26], GaAs [20, 27–39], InP [11, 13, 17], and GaP [40], have been explored in recent years, as well as several ternary III-V alloys, including InGaAs [41], InGaP [42], and AlGaAs [43].

Fundamentally, MacEtch techniques rely on catalytic oxidation of a semiconductor directly beneath a metal catalyst layer (e.g., Au, Ag, Pt, or Pd), followed by dissolution of the selectively oxidized material [41]. Etching solutions consist of an oxidant, an acid, and often a surfactant or diluent. When a sample is submerged in a MacEtch solution, cathodic and anodic reactions occur at the solution/catalyst and catalyst/semiconductor interfaces, respectively [42]. The cathodic reaction includes oxidant reduction, and hole injection (i.e., charge carrier transport) into the semiconductor interfaced with the catalyst [23]. In the presence of a suitable catalyst, hole injection produces an oxidized state of the semiconductor material that is soluble in the MacEtch solution. The anodic reaction consists of solution access to, and dissolution of, the selectively oxidized regions (i.e., mass transport) [42]. That is, MacEtch techniques induce or enhance an etch rate through the iterative and continuous selective oxidation and preferential dissolution cycle of a semiconductor in the

presence of an appropriate catalyst and etchant [8, 9]. For inverse-progression MacEtch specifically, the oxidized material directly beneath the metal layer is not immediately dissolved, allowing the injected holes to diffuse from underneath the catalyst and form hemispherical hole distributions about their injection sites [42]. The extent of the hole distributions is a function of a variety of material- and reaction-related properties (e.g., magnitude of the redox potential relative to the ionization potential of the semiconductor, carrier mobility and diffusion length, solution temperature, etc.) [42]. Therefore, the semiconductor areas not interfaced with metal (i.e., the off-metal regions) are the first to be dissolved, once those regions become oxidized to a state that is soluble in the I-MacEtch solution. Subsequently, the oxidized regions below the catalyst are dissolved as they become exposed by the dissolution of the non-interfaced areas between the metal-coated regions. The vertical and lateral etch rates (VER and LER, respectively) are functions of the relative strength of the cathodic and anodic reactions, which are tunable with the composition and temperature of the I-MacEtch solution, and with the size, pitch, thickness, and type of catalyst [23]. Given that development of MacEtch conditions for III-V alloys is relatively new, the utilization of these techniques has not become commonplace as of yet, in part due to the limited exploration for many semiconductors, such as AlGaAs.

The versatility of MacEtch is exhibited in Figure 1.1, which demonstrates forward-progression Si MacEtch to yield an RIT logo and nanowires with an aspect-ratio

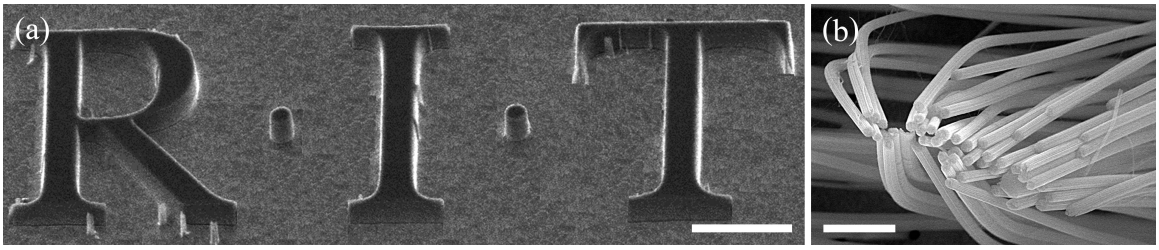

Figure 1.1: Tilted-view SEM images demonstrating Au-catalyzed Si MacEtch of (a) an RIT logo, and (b) nanowires with an aspect-ratio of approximately 100. Scale bars in (a) and (b) represent 30 μm and 2 μm, respectively.

of ∼100. While acclaimed as powerful processing alternatives to other top-down methodologies, its fundamental research is still in its infancy. A growing number of researchers have been utilizing MacEtch to produce semiconductor architectures for a wide variety of applications[13, 20], whereas others have primarily focused on expanding our understanding of the underlying dynamics [21, 23].

This work aims to expand the library of known materials available to be MacEtched, as well as the current understanding of its fundamental mechanisms. Au-enhanced MacEtch of the ternary alloys InGaP and AlGaAs is demonstrated for the first time, and processes are detailed for the formation of suspended III-V nanofoils and ordered nanopillar arrays. Next, a lithography-free and entirely solution-based method is outlined for the fabrication of black GaAs with solar-weighted reflectance of 4 %. Finally, a comparison between Au- and CNT-enhanced Si MacEtch is presented towards CMOS-compatibility using catalysts that do not introduce deep level traps. Sample preparation and etching conditions are shown to be adaptable to yield an a priori structural design, through a modification of injected hole distributions. Critical process parameters that guide the MacEtch mechanisms are considered at length, including heteroepitaxial effects, ternary material composition, etching temperature, and catalyst type, size, and deposition technique. This work extends the range of MacEtch materials and its fundamental mechanics for fabrication of micro- and nanostructures with applications in optoelectronics, photovoltaics, and nanoelectronics.

1.2 Organization of Dissertation

This dissertation is organized into ten chapters.

Chapter 1 motivates and summarizes the work that is covered in the remaining chapters. This body of work focuses on developing semiconductor nanofabrication methodologies to provide engineers alternative approaches that overcome consequential processing constraints.

Chapter 2 presents requisite background information related to metal-assisted chemical etching (MacEtch). This includes an exploration of the fundamental mechanisms that govern the technique itself, as well as critical process parameters that affect its mechanisms.

Chapter 3 contains background information regarding semiconductor physics and photovoltaics. This chapter covers essential concepts within semiconductor physics, before providing a more complete description of how and why photovoltaic devices function.

Chapter 4 details various experimental methodologies and techniques that were utilized throughout this work. Specific experimental details can be found within each chapter.

Chapter 5 presents the first demonstration of Au-catalyzed InGaP MacEtch, and provides a practical route towards formation of suspended nanofoils using heteroepitaxial systems. The observed etching behavior is modeled by considering an overlap of injected hole distributions.

Chapter 6 introduces the first demonstration of AlGaAs MacEtch, which uses Au-catalysts to form ordered nanopillar arrays. The etching behavior can be tuned through a modification of injected hole distributions, which is shown to be controlled with Al fraction and temperature of the etching solution.

Chapter 7 expands on a recent push towards producing CMOS compatible MacEtch, by utilizing carbon nanotubes to catalyze Si etching. Here, process simplification and feasibility is explored for devices that benefit from low reflectance surfaces and/or embedded contacts.

Chapter 8 combines GaAs MacEtch and electrodeposition of Au-catalysts for fabrication of black GaAs. This work establishes a simple and cost-effective route towards low reflectance GaAs that utilizes room-temperature and entirely solution-based processing.

Chapter 9 summarizes the work detailed in Chapters 5 - 8, and outlines my research contributions to the metal-assisted chemical etching community.

Chapter 10 discusses future works that stem from this body of research. Emphasis is placed on several projects, including the first demonstration of GaSb MacEtch, a simple process to generate black AlGaAs, and the development of a process whereby carrier-selective asymmetric heterojunction GaAs photovoltaics are fabricated.

Chapter 2

Background of Metal-Assisted Chemical Etching

The basis for metal-assisted chemical etching (MacEtch) is the promotion or enhancement of semiconductor etching in the presence of an appropriate catalyst. More accurately stated, a thin metallic catalyst - in direct contact with a semiconductor - catalyzes the reduction of oxidant species with the etching solution, thereby generating charge carriers that are locally injected into the substrate along the catalyst/semiconductor interface. That is, only specific regions of the semiconductor become ionized, which are defined by the catalyst coverage. Then, the solution interacts with the selectively ionized regions, which generates an oxide that is preferentially attacked by the etchant within the solution. Therefore, the presence of an appropriate catalyst locally forms an oxide that is soluble in the MacEtch solution, while the remaining semiconductor regions remain undisturbed.

MacEtch techniques are anisotropic, solution-based alternatives to conventional top-down fabrication methods. These relatively simple and cost-effective techniques combine many of the advantages of traditional top-down processes, while neglecting many of the corresponding disadvantages [8]. Sample fabrication for use with MacEtch processing can be performed in conventional semiconductor facilities, and consists of depositing a metal catalyst layer (e.g., Au, Ag, Pt, or Pd) onto a semiconductor substrate. The metal layer has two important regions, namely where the metal is, and is not interfaced with the semiconductor (i.e., the "interfacial" and "off-metal" regions, respectively). The techniques themselves can be performed in standard

semiconductor wet benches, and are the consequence of localized cathodic and anodic reactions resulting from a specific set of MacEtch solution, metal catalyst layer, and the substrate to be etched [42, 43]. This section will provide the necessary details for a fundamental understanding of MacEtch processing.

2.1 History

Metal-assisted chemical etching (MacEtch, or "forward-progression" MacEtch) behavior was reported by Dimova-Malinovska et al. in 1997 [10], and the technique was outlined and formalized independently by two separate groups in 2000, Xia et al. [44] and Li and Bohn [12]. Inverse metal-assisted chemical etching (I-MacEtch, or "inverse-progression" MacEtch) behavior was first noted under UV-illumination by Asoh et al. in 2010 [11], and termed "metal-assisted photodissolution." DeJarld et al. also observed inverse-progression MacEtch behavior in 2011 [31] while producing GaAs zig-zag structures. In 2015, Kim et al. formalized the I-MacEtch process through an examination of soluble and insoluble oxide formation in the off-metal and interfacial regions, respectively, using X-ray photoelectron spectroscopy [13].

Although research in this field has predominantly focused on Si [12, 21, 23, 24, 44–46], binary III-V materials, including GaAs [20, 29, 31], InP [13], GaP [40], and GaN [25, 26] have been explored in recent years. Additionally, ternary III-V alloys, including InGaAs [41], InGaP [42], and AlGaAs [43] have been reported in the past year.

2.2 Introduction

One of the remarkable advantages of metal-assisted chemical etching is its simplicity, both in preparation and execution. Generic process flows delineating forward- and inverse-progression MacEtch are illustrated in Figures 2.1 and 2.2, respectively. Both consist of patterning a catalyst layer interfaced with a semiconductor, subjecting the

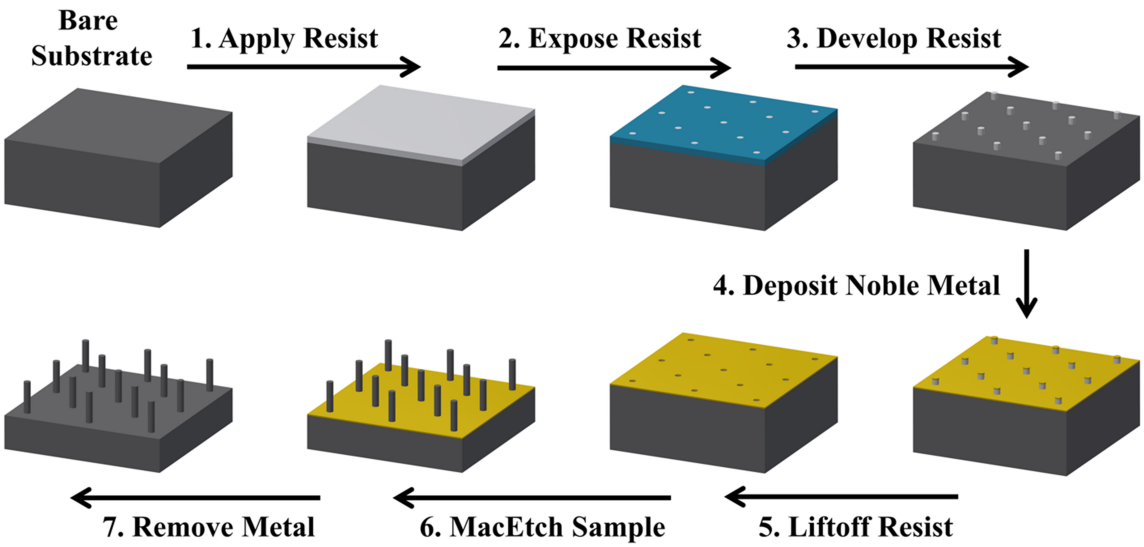

Figure 2.1: Models illustrating a forward-progression MacEtch process flow. A patterned metal catalyst layer sinks into the semiconductor with which it is interfaced. The resulting vertical structures take on the shape of the patterned voids in the metallic layer. This process flow assumes the use of positive photoresist.

sample to an appropriate MacEtch solution, and removing the metal from the substrate for subsequent processing. It should be noted that both process flows assume the use of positive photoresist. Admittedly, these depictions do not exhaust the fabrication options (e.g., nanosphere lithography), and not every procedural nuance is portrayed within each step; however, these top-level models are sufficient representations for further discussion. Their paramount facets include the introduction of a metal catalyst layer to a semiconductor, and determining the appropriate chemical constituents and their relative concentrations within the etching solution [9]. Etching behaviors (e.g., etch rate) have been described for various material systems in the literature, though this information often details very specific etching conditions. While the extrapolation of these values for similar systems is useful as first-order approximation, they should be treated as such for initial experimentation.

Catalyst geometry is often a pivotal consideration if a specific feature architecture is targeted, though this becomes a secondary concern for globally disordered structures (e.g., random porosity for reduced surface reflectance) [9]. Various lithog-

raphy techniques are routinely employed to achieve a desired catalyst pattern, such as photolithography, e-beam lithography, soft lithography, nanosphere lithography, nanoimprint lithography, etc. Likewise, thoughtful design of the etching solution is also of considerable consequence. Common etching solutions for a growing library of material systems can typically be found in the literature; however, discerning the relative concentrations of each constituent can become a formidable task if tight tolerances are placed on the final structure dimensions (e.g., nanowire height).

Forward-progression MacEtch has been heralded as a highly anisotropic processing technique [8]. An important detail of the etch progression often omitted in the literature is the distinction between the local and global etching behavior illustrated in Figure 2.3. The substrate is oxidized at the catalyst/semiconductor interface [8, 9]. The local etching behavior of the oxidized material is isotropic, resembling that of conventional wet-etching. The globally anisotropic nature of MacEtch is a result of the metal catalyst layer sinking - vertically - into the substrate as the oxidized

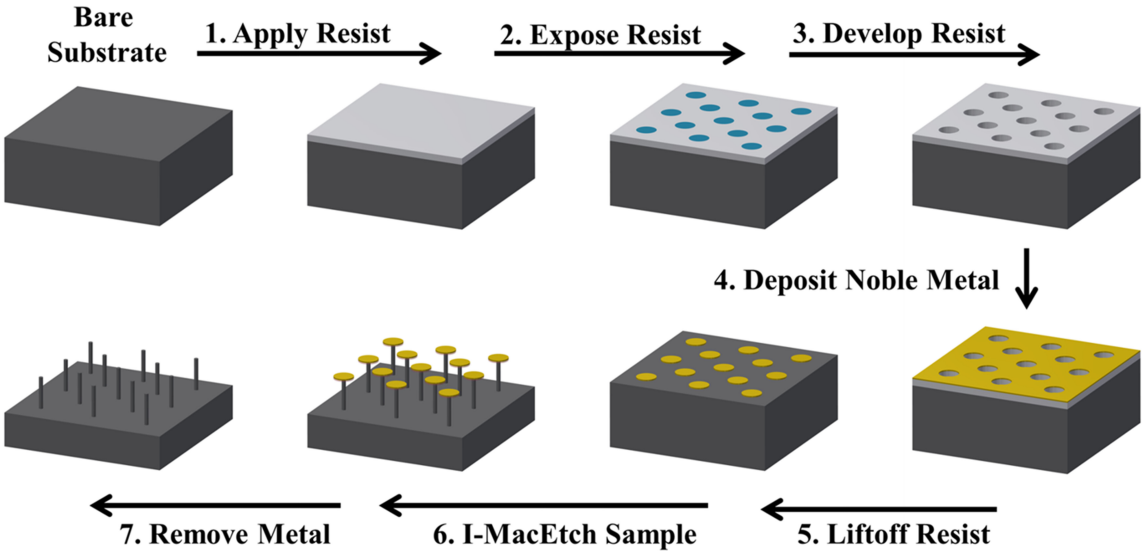

Figure 2.2: Models illustrating an inverse-progression MacEtch process flow. Conversely, the patterned metal catalyst layer does *not* sink into the semiconductor with which it is interfaced. Instead, the exposed semiconductor between the patterned metallic layer dissolves first, followed by the oxidized regions beneath the catalyst as they become exposed. This process flow assumes the use of positive photoresist.

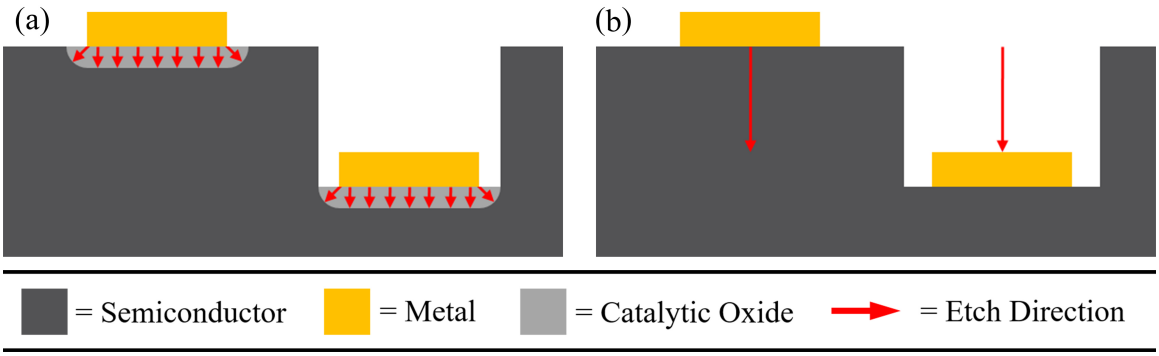

Figure 2.3: Schematics depicting the (a) continuous isotropic etching localized about the metal catalyst layer that leads to the (b) globally anisotropic nature of forward-progression MacEtch.

semiconductor underneath is dissolved. A major strength of MacEtch comes from these seemingly contradictory behaviors being married through the continuous isotropic etching localized about the metal catalyst layer. That is, the localization of isotropic etching to the catalyst/semiconductor interface results in the globally anisotropic process.

2.3 Catalytic Etching Mechanisms

Fundamentally, MacEtch techniques rely on catalytic oxidation of a semiconductor directly beneath a metal catalyst layer (e.g., Au, Ag, Pt, or Pd), followed by dissolution of the selectively oxidized material [9]. Consistent with the model of a galvanic cell, the essential kinetics include cathodic and anodic reactions. These are promoted by an etching solution containing an oxidant such as hydrogen peroxide (H_2O_2) or potassium permanganate ($KMnO_4$), an acid such as hydrofluoric acid (HF) or sulfuric acid (H_2SO_4), and often a diluent or surfactant such as deionized water (DI-H_2O) [42]. While the chemical reactions describing the mechanics of Si MacEtch have been postulated and accepted by the MacEtch community [9], it is important to note these conclusions are based on abductive inference due to the lack of in situ measurement capabilities.

2.3.1 Galvanic Oxidation-Reduction Reactions

MacEtch reaction kinetics follow the model of a galvanic cell, with the net result being the extraction of holes from the semiconductor to accommodate oxidant reduction. Introducing a catalyst-patterned semiconductor to an appropriate MacEtch solution results in cathodic and anodic half reactions at the solution/catalyst and catalyst/semiconductor interfaces, respectively [43]. The semiconductor undergoes localized oxidation at the anodic sites, followed by dissolution of the oxidized species via the etchant. For the sake of discussion, the specific case of Au-patterned Si MacEtch in an electrolyte solution of hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF) will be considered at times to avoid ambiguity, as depicted in Figure 2.4.

Cathodic Half Reaction

The cathodic half reaction occurs at the solution/catalyst interface, and is the reduction reaction of H_2O_2. This is referred to as charge carrier generation. The oxidant reduction transfers free electrons from the metal catalyst to the oxidant [42]. That is, the Au

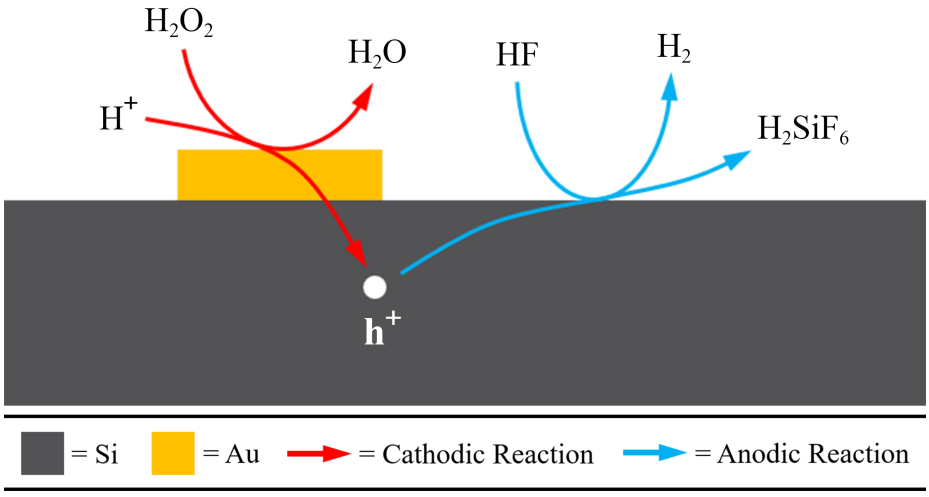

Figure 2.4: Schematic representation of the cathodic (red arrows) and anodic (blue arrows) reactions. The cathodic reaction includes oxidant reduction and hole injection (i.e., charge carrier transport) into the underlying semiconductor, and the anodic reaction consists of solution access to - and dissolution of (i.e., mass transport) - the catalytically oxidized material formed by the cathodic reaction.

catalyzes the reduction of H_2O_2 at the solution/metal interface, and holes (h^+) are generated according to the following reaction [8, 9]:

$$H_2O_2 + 2\,H^+ \xrightarrow{Au} 2\,H_2O + 2\,h^+ \tag{2.1}$$

Proposed cathodic half reactions for solutions utilizing potassium permanganate include [31]:

$$MnO_4^- + 8\,H^+ + 5\,e^- \xrightarrow{Au} Mn^{2+} + 4\,H_2O \tag{2.2}$$

$$MnO_4^- + 4\,H^+ + 3\,e^- \xrightarrow{Au} MnO_2 + 2\,H_2O \tag{2.3}$$

Anodic Half Reaction

The anodic half reaction completes the galvanic cell model, whereby the generated holes are injected into the semiconductor at the catalyst/semiconductor interface. This is referred to as charge carrier transport. Electrons are transferred from the semiconductor to the metal, resulting in no net consumption of the catalyst [43].

While Equation 2.1 is well accepted as the cathodic half reaction describing the reduction of H_2O_2, several models for the anodic half reaction have been proposed [9]. The main distinction in the models is in the composition of the catalytic oxide, which arises due to the lack of *in situ* measurements and the uncertainty in post-MacEtch *ex situ* characterization (e.g., native oxide growth). The ultimate result is that the injection of holes in the semiconductor forms an ionic or oxidized state, silicon hexafluoride, that is soluble in the MacEtch solution.

Upon hole injection, the semiconductor becomes oxidized according to the following

reaction [8, 9]:

$$\mathrm{Si} + 6\,\mathrm{HF} + 4\,\mathrm{h}^{+} \longrightarrow \mathrm{SiF}_6^{2-} + 6\,\mathrm{H}^{+} \tag{2.4}$$

Similarly, proposed anodic half reactions for GaAs MacEtch using solutions containing potassium permanganate include [31]:

$$\mathrm{Ga} \longrightarrow \mathrm{Ga}^{3+} + 3\,\mathrm{e}^{-} \tag{2.5}$$

$$2\,\mathrm{As} + 3\,\mathrm{H_2O} \longrightarrow \mathrm{As_2O_3} + 6\,\mathrm{H}^{+} + 6\,\mathrm{e}^{-} \tag{2.6}$$

$$\mathrm{As} + 2\,\mathrm{H_2O} \longrightarrow \mathrm{HAsO_2} + 3\,\mathrm{H}^{+} + 3\,\mathrm{e}^{-} \tag{2.7}$$

Dissolution of Catalytically Oxidized Material

Etching of the catalytically oxidized semiconductor occurs via its reaction with the etchant within the MacEtch solution. For the specific case of Si MacEtch noted above and illustrated in 2.4, the formation of soluble silicon hexafluoride is the result of HF reacting with the catalytically oxidized Si [9]. The solution access to, and dissolution of, catalytically oxidized semiconductor material is referred to as mass transport. While both the cathodic and anodic half reactions influence the etch rate, the accessibility of the etchant to oxidized material also plays a role. That is, limited mass transport pathways will impede the dissolution of oxidized material [42].

2.3.2 Role of the Catalyst

As mentioned previously, the metal catalyst often plays the most pivotal role during MacEtch. Although a slew of catalyst parameters could be discussed at length without exhausting the ways in which the process is influenced, only a select few will be

detailed here. Namely, the consequence of catalyst continuity, a requisite condition for a metal to promote the cathodic reaction, and its affect on the catalytic mechanism. The role of the oxidant will also be considered where appropriate, as its consequences are often complementary with those of the catalyst.

Catalyst Thickness and Continuity

The continuity of the metal catalyst layer is of considerable consequence for the anodic reaction, and a secondary concern for the cathodic reaction. A universal method for ensuring a continuous metallic layer is through a slow deposition of a relatively thick film. An as-deposited catalyst thickness of approximately 30 nm - 50 nm is generally sufficient to provide a continuous layer [42, 43]. While metal thicknesses of less than 30 nm often lead to discontinuous films comprised of isolated nanoparticles, its deposition rate will influence coverage as well. Additionally, excessive stress at grain boundaries can be generated via rapid deposition rates, and may cause weakened locations susceptible to cracking during MacEtch.

The anodic reaction is highly dependent on the continuity of the catalyst layer. Figure 2.5 compares solution access to (red arrows), and mass transport of (blue arrows), oxidized material for continuous and discontinuous metallic films in panels a and b, respectively. Solution access and material dissolution is only supported around the periphery of a discrete catalyst, whereas a porous film provides additional solution and mass transport pathways. Moreover, these supplemental avenues shorten the distance dissolved materials must travel, which results in a more rapid etch rate. However, porous layers will also result in residual vertical whiskers of unetched substrate at the voids in the catalyst.

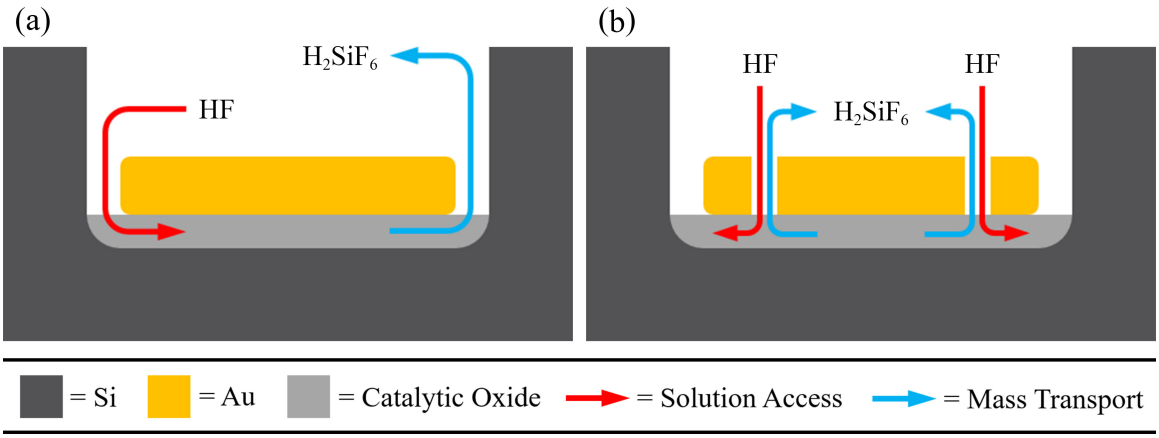

Figure 2.5: Models showing modes of solution access to, and mass transport of, oxidized material for (a) continuous, and (b) discontinuous metal catalyst layers.

Promotion of the Cathodic Reaction

An examination of several parameters that have been proposed to govern charge transport across the metal/semiconductor interface is necessary. Work function would seem to be the most obvious, as the type of contact (i.e., Schottky or Ohmic) between the catalyst and semiconductor defines the barrier that charge carriers must overcome. Catalyst reduction potential, and semiconductor electron affinity (i.e., conduction band minimum) and ionization potential (i.e., valence band maximum) are other values of note. Au, Ag, and Pt are known to promote Si MacEtch, while Cr has been shown to prohibit the process. The work function and reduction potential of these metals, along with the corresponding values for p-type Si, can be found in Table 2.1.

Work function is a surface characteristic rather than a property of the bulk material, and materials have distinct work function values. Conceptually, it refers to the energy difference between the Fermi energy level (E_{F}) of a solid, and the vacuum energy level (E_{VAC}) or the energy level at which an electron is free of the material. In metals, electrons fill every available energy state up to the Fermi level, therefore metals do not have a band gap. Hence, the work function of metals defines the boundary between occupied and unoccupied states, and the minimum energy required to liberate an

electron from the lattice. In particular, the Fermi level, work function, electron affinity (i.e., conduction band), and ionization potential (i.e., valence band) all reside at the same energy level in metals. Work function defines the energy required to remove an electron from the Fermi level to the vacuum level for semiconductors as well; however, the model is more complex since the aforementioned states do not necessarily have the same energy.

Considering the values in Table 2.1, Au has a larger work function than p-type Si and therefore creates an Ohmic contact. Likewise, Cr has a smaller work function than p-Si and should form a Schottky barrier. This is consistent with experimental data; Au promotes Si MacEtch, whereas Cr inhibits it [42, 43]. Pt is in agreement with the assertion that the relative work functions govern charge carrier transport (i.e., hole injection) across the metal/semiconductor interface; however, Ag is known to promote catalytic oxidation although it has a similar work function to Cr. Likewise, Au and Cr result in the inverse contacts with n-type Si. That is, Au and n-Si yield a Schottky barrier, whereas Cr should form an Ohmic contact [21]. The consequences of this should be that Au promotes p-type Si MacEtch and blocks the requisite charge carrier

Table 2.1: Work function and reduction potential, relative to the standard hydrogen electrode (SHE), of Si and metals commonly incorporated with MacEtch experimentation. The Si work function is calculated from p-Si with resistivity in the range of 0.1 - 1 Ω∗cm.

Material	Work Function (eV)	Reduction Potential (V/SHE)	Promotes Si MacEtch?
Au	5.10	$Au^{3+} + 3e^- \rightarrow Au$ (1.50 V)	Yes
Ag	4.26	$Ag^+ + e^- \rightarrow Ag$ (0.80 V)	Yes
Pt	5.63	$Pt^{2+} + 2e^- \rightarrow Pt$ (1.18 V)	Yes
Ni	5.15	$Ni^{2+} + 2e^- \rightarrow Ni$ (−0.26 V)	No
Cr	4.44	$Cr^{3+} + 3e^- \rightarrow Cr$ (−0.74 V)	No
Si	4.75	Electron affinity (−0.46 V) Ionization potential (0.67 V)	N/A

transport for n-type Si, while Cr should impede p-type Si MacEtch and support hole injection for n-type Si. However, experimental results debunk the claim that relative work functions dominate the charge carrier transport process [21].

Nevertheless, the ease at which charge carriers may be transported across the catalyst/semiconductor interface should not be neglected. While the relative work functions of the metal and semiconductor do not govern whether hole injection may occur, it absolutely plays a role in the depth to which holes may be injected. An unavoidable cause of reducing the extent of hole injection is native oxide growth prior to catalyst deposition, which is less conductive than an ideal catalyst/semiconductor interface.

Next, the reduction-oxidation or redox parameter will be considered. Redox reactions involves the transfer of electrons by means of two complimentary half-reactions; reduction at the cathode where electrons are gained, and oxidation at the anode where electrons are lost. Table 2.1 shows the reduction or redox potential of several metals known to promote, and prohibit, Si MacEtch. Reduction potential is the tendency of a material to be reduced through acquiring electrons. Every material has an intrinsic redox potential, and its tendency to collect electrons increases with a more positive potential. Figure 2.6 compares the redox potentials of the metals (panel a) from Table 2.1, and common oxidants (panel b) utilized in Si MacEtch. The electron affinity and ionization potential for Si are provided as well.

As redox reactions are charge transfer processes, their interaction with occupied energy states should be considered. This becomes particularly relevant as Si oxidation involves the liberation of bound electrons within the Si lattice. To that end, some reports suggest a comparison of redox potential and electron affinity as the dictating mode of carrier transport during MacEtch [21]. At first glance, this is a plausible evaluation, as the reduction potential many known catalysts are more positive than the conduction band and should promote hole injection. However, Cr and Ni straddle

the electron affinity of Si, yet both are known to prohibit hole injection.

Instead, the ionization potential appears to be the governing parameter for charge transport. The position of the metallic reduction potential and the semiconductor valence band edge is the relation of consequence. The metals known to promote hole injection are at higher (i.e., more positive) potentials than the ionization potential, while those known to prohibit carrier transport reside closer to the vacuum level and have insufficient reduction potential to support the cathodic reaction [43].

Therefore, a necessary condition for the metal to serve as a catalyst in the redox reaction between the oxidant and the semiconductor is that the reduction-oxidation potential of the metal must lie lower than the ionization potential (i.e., valence band edge) of the semiconductor. That is, the ionization potential of the semiconductor must reside closer to the vacuum level than the redox potential of the catalyst for the promotion of catalytic oxidation [42]. Otherwise stated, in order to facilitate the requisite cathodic reaction, the reduction potential (E^0) of the metal must be offset

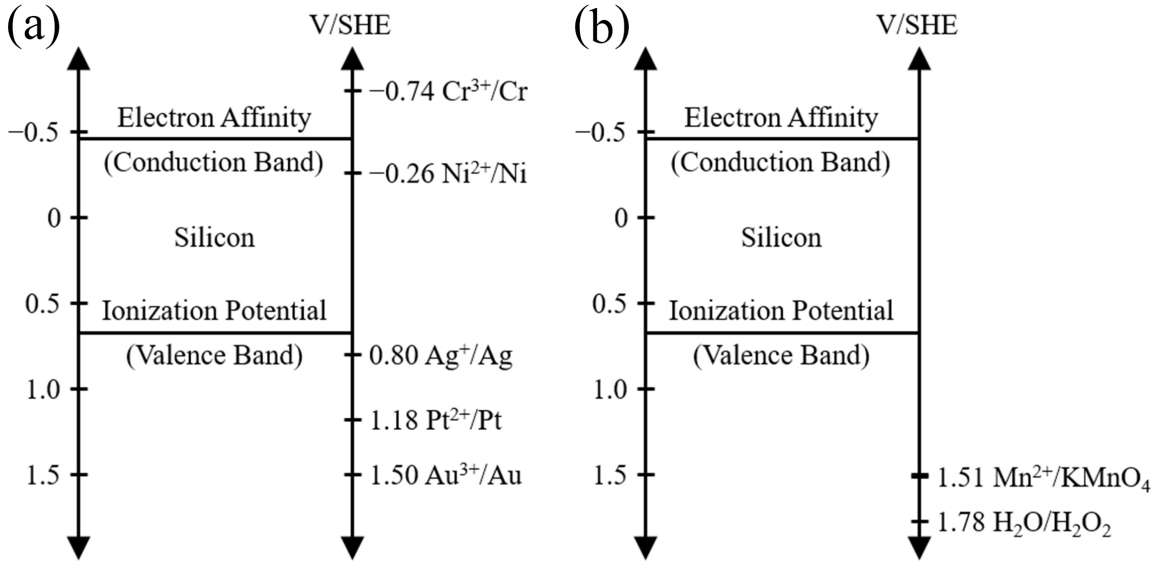

Figure 2.6: Diagrams showing reduction potentials of (a) common metals known to promote and inhibit catalytic injection into Si, and (b) common oxidants utilized in Si MacEtch. Reduction potentials are shown in relation to the electron affinity (i.e., valence band) and ionization potential (i.e., conduction band) of Si, referenced to the standard hydrogen electrode (SHE).

relative to the more negative semiconductor ionization potential, when referenced to a standard electrode [e.g., the standard hydrogen electrode (SHE)]. On this basis, while Au (E^0 = +1.50 V/SHE) is commonly used as a catalyst in standard Si MacEtch experiments, Cr (E^0 = -0.74 V/SHE) is known to prohibit catalytic etching [21].

Influences on the Cathodic Reaction

Based on the galvanic cell model, the catalytically generated holes must be transported from the cathode to the catalyst/semiconductor interface. The electrical conductivity of common catalysts (e.g., Au and Ag) is quite high and not considered to be the limiting factor for hole injection. Instead, attenuation of carrier transport across the catalyst/semiconductor interface is often the culprit of reduced hole injection. The most common cause of a transport barrier is due to the formation of a low-quality interface during sample preparation, such as the presence of a native oxide.

Another important consideration is the level of disparity between the catalyst reduction potential and the semiconductor ionization potential. With all other parameters held constant, a larger potential difference results the extraction of electrons from deeper within the valence band [21]. For example, Figure 2.6 indicates the redox potential of Au will inject holes deeper into the valence band than Ag. Since hole injection is the cause of catalytic oxidation, the extent to which holes are injected increases with the level of potential disparity [42]. This is particularly important for inverse-progression MacEtch. In contrast to forward-progression MacEtch, the catalyst or plane of hole injection does not sink during I-MacEtch processing [43]. In such a scenario, and due to the finite extent of oxidized material under the catalyst, a corresponding limit to catalytic etching will arise and lead to etch rate saturation, as reported in the case of InP I-MacEtch [13].

Studies evaluating the etch rate of III-V MacEtch as a function of doping type are very limited, particularly in the inverse-progression MacEtch regime. Several

comparisons of vertical etch rates between intrinsic or nominally undoped (which will be referred to as i-type for simplicity), n-type, and p-type have been reported for forward-progression MacEtch. Although Si [23] and GaAs [20] have been shown to have dissimilar vertical etch rates based on doping type, this can be attributed to the formation of a Schottky barrier at the metal/semiconductor interface (*vide infra*). A 2018 study on InGaP is the only current comparison of vertical etch rate (VER) as a function of doping for I-MacEtch [42]. For InGaP, no apparent trend was shown favoring an enhanced VER for one doping type over another, as i-, p-, and n-type samples all exhibited comparable etch rates. Therefore, the VER of Au-patterned InGaP in the inverse-progression MacEtch regime is independent of differences in Fermi energy and work function. This is consistent with the model for metal-catalyzed etching whereby the offset between metal reduction potential and semiconductor ionization potential is more critical than the availability and type of free carriers [42].

Schottky Junction Formation

In the previous section, the vertical etch rate of InGaP in the inverse-progression MacEtch regime was shown to be indifferent to doping type, work function, and the type and concentration of free carriers. While the consequences of this analysis on hole injection play an active role in all MacEtch experiments, they must be weighed against other mechanisms that are influential to injected holes. Although other fundamental etching kinetics are present when catalytic etching is independent of Fermi energy, their effects are often overshadowed in the I-MacEtch process. Conversely, the Schottky junction formed via the availability and type of semiconductor free carriers is prominent in forward-progression MacEtch [23].

In addition to catalyzing the reduction of oxidant species within the MacEtch solution, the metal creates a Schottky junction with the semiconductor as depicted in Figure 2.7 [23]. The junction influences the spatial localization of injected holes,

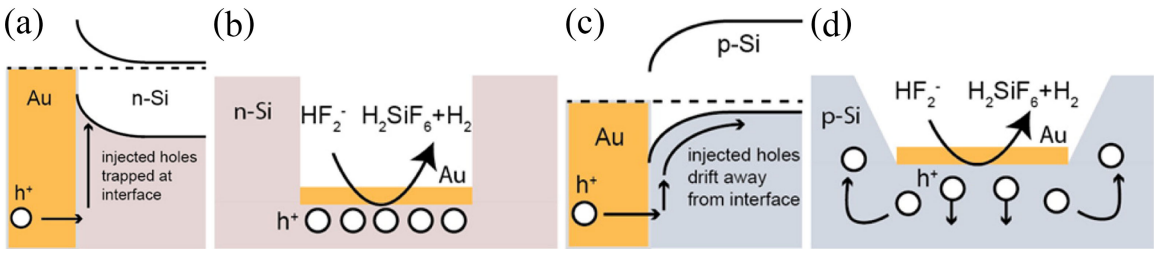

Figure 2.7: Schematics showing the Schottky barrier formed by (a) and (b) Au/n-Si that confines injected holes near the metal, and (c) and (d) Au/p-Si that sweeps injected holes away from the catalyst [23].

and is a function of the type and concentration of dopants within the semiconductor. The band bending for n-type Si forms a Schottky barrier that serves to trap the injected holes at the catalyst/semiconductor interface [23]. This focuses the oxidation at the catalyst, leading to more rapid and anisotropic etching. The Schottky junction band bending as a result of p-type Si encourages injected holes to drift from the catalyst/semiconductor interface. This expands the spatial distribution of injected holes beyond the immediate vicinity or interface of the catalyst, which decreases the etch anisotropy and promotes etching in the off-metal regions.

Expanding the volume of hole distribution without also increasing the flux of holes into the semiconductor will slow the evolution of oxidation to a state sufficiently ionized to be soluble in the MacEtch solution. That is, band bending that encourages holes to drift away from the catalyst will increase the regions susceptible to MacEtch, though it will decrease the overall etch rate. This can be seen in Figure 2.8, which illustrates Au-patterned n- and p-type silicon samples subjected to identical MacEtch conditions. Due to the influence of a Schottky junction, n-Si has an increased VER over p-Si, whereas the lateral etch rate is higher for samples doped with acceptors.

As described previously, etch rate is a highly dependent symptom of the catalyst capacity for oxidant reduction. It is worth considering hole injection into various crystallographic planes as a source of etch rate disparity. As the surface energy varies for the distinct Si facets, particularly the {100} and {111} families compared to {110}

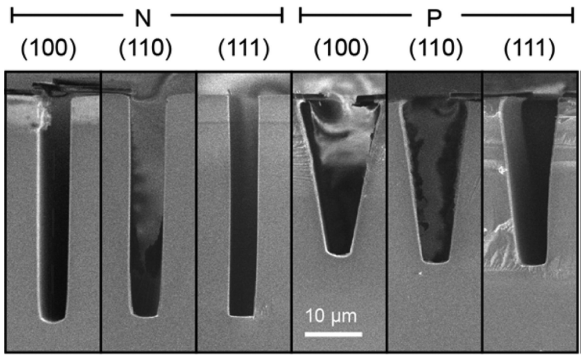

Figure 2.8: Cross-sectional SEM images showing vertical etching of n-Si due to a Schottky junction confining injected holes near the catalyst, and additional lateral etching for p-Si due to a Schottky junction sweeping injected holes away from the metal [23].

[47], the etch rates would intuitively be expected to scale accordingly. However, Figure 2.8 indicates a relatively small difference in etch rate as a function of crystal axis. This can be attributed to common metallic catalysts having very similar Schottky barrier heights which have a small dependence on their interfacial facet [48].

2.3.3 Hole Distributions

The spatial dimensions of catalytically injected hole distributions is a vital aspect of MacEtch processes, as they define the volume of ionized material available for preferential dissolution [42, 43]. The previous several sections have discussed some of the major dependencies of hole distributions, including the catalyst reduction potential and the formation of a Schottky junction. Recall that the magnitude of disparity between the catalyst reduction potential and semiconductor ionization potential affects how deep holes are injected into the valence band [21], and the type and concentration of substrate dopants impacts the ease to which injected holes may drift from the anode [23]. The extent of hole distributions is a function of a multitude of other material- and reaction-related attributes, such as temperature, diffusion, and the type and concentration of oxidant species within the MacEtch solution.

Role of the Oxidant

The type and concentration of oxidant species work in conjunction with the metal catalyst to generate holes. The metal catalyzes oxidant reduction and facilitates hole injection into the underlying semiconductor based on the reduction potential of the catalyst. The reduction half reaction potential of the oxidant must be considered as well, because it also dictates the depth to which holes can be injected into the valence band. An oxidant possessing a reduction potential that straddles that of the catalyst and the ionization potential of the semiconductor will result in relatively shallower hole injection. In this scenario, the catalyst capacity for oxidant reduction is not fully exploited. Fortunately, common oxidants, such as hydrogen peroxide (H_2O_2) and potassium permanganate ($KMnO_4$), have reduction potentials more positive than that of common catalysts, as seen in Figure 2.6b [9].

Role of Temperature and Diffusion

The size of hole distributions increases with temperature for several reasons. The cathodic half reaction is enhanced, and a larger number of holes are generated through thermally activated catalytic decomposition of oxidant species [49]. The anodic half reaction follows suit with the amplification of carrier transport through the catalyst and across the metal/semiconductor interface [50]. Moreover, injected holes diffuse from the anode at a higher rate with increasing temperature, and the size of hole distributions expand accordingly [51]. That is, increasing temperature promotes a more rapid decomposition of the oxidant species, faster carrier transport through the catalyst and across the barrier into the semiconductor, and the hole diffusion rate from their injection sites. In short, the size of hole distributions and the catalytically-enhanced etch rates increase with temperature [43].

2.4 Forward- and Inverse-Progression MacEtch

While "highly anisotropic" has been a common descriptor for MacEtch because the etch front continuously sinks into the substrate, the nomenclature must evolve for the sake of accuracy once inverse-progression MacEtch is considered as well. Both scenarios involve catalytic oxidation at the metal/semiconductor interface, followed by preferential dissolution of the selectively oxidized material. During inverse-progression MacEtch, however, the catalyst or plane of hole injection remains stationary and does not sink into the substrate. In I-MacEtch, the off-metal regions (i.e., exposed areas with no interfacial metal) are the first to be etched, followed by the regions underneath the catalyst as they become exposed.

2.4.1 Forward-Progression MacEtch

Forward-progression MacEtch consists of continuous catalytic oxidation and preferential dissolution causing the metal to sink into the substrate, such that the off-metal regions remain intact. That is, voids in the catalyst define the vertical structures that will be remaining after etching [9]. Ordered patterning of a large area catalyst will result in an array of vertical structures, such as wires, pillars, or cones. These are referred to as "positive" structures, as seen in Figure 2.9a. Likewise, discrete catalysts

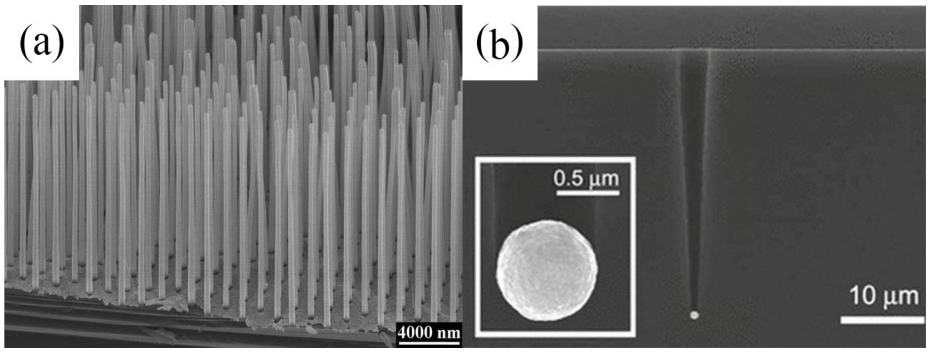

Figure 2.9: SEM images showing Ag-enhanced forward-progression MacEtch of Si generating (a) nanowires [9], and (b) pits [46].

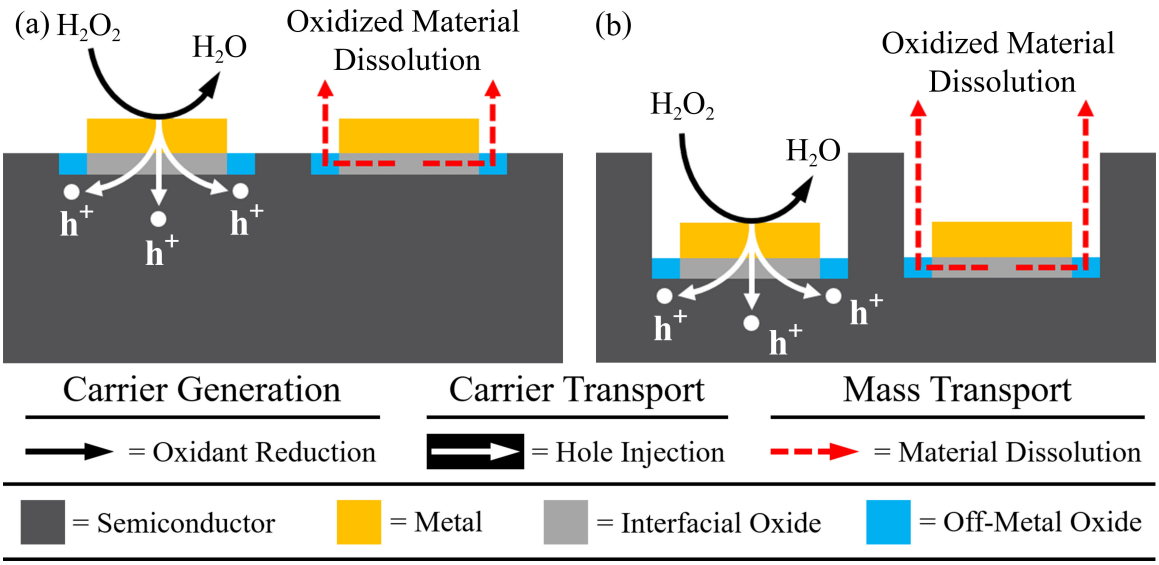

Figure 2.10: Models showing the mechanisms of forward-progression MacEtch (a) at the onset of etching, and (b) during the generation of structures.

- either ordered or disordered - will generate pits or trenches in the semiconductor, leaving behind the vast majority of substrate material. These are characterized as "negative" structures, and are depicted in Figure 2.9b.

Figure 2.10 shows a basic overview of forward-progression MacEtch mechanisms, including those at the onset of etching (panel a) and during the generation of structures (panel b). As described previously, the formation of a Schottky junction at the catalyst/semiconductor interface is a major factor in the geometry and morphology of the final structures [23]. As such, Figure 2.10 depicts a qualitative representation of the injected holes remaining relatively close to the anode. This minimizes the spatial dimensions of hole distributions, and focuses the etching to the substrate regions interfaced with the catalyst.

It should be noted that these models include a region of off-metal oxide (highlighted in blue) immediately outside the metal periphery. If the catalyst is sufficiently thick to be continuous, mass transport (i.e., solution access to, and dissolution of, oxidized material) pathways will be limited to beyond the interfacial regions [9]. Additionally, if the rate of charge transport (i.e., hole injection into the substrate) is greater than

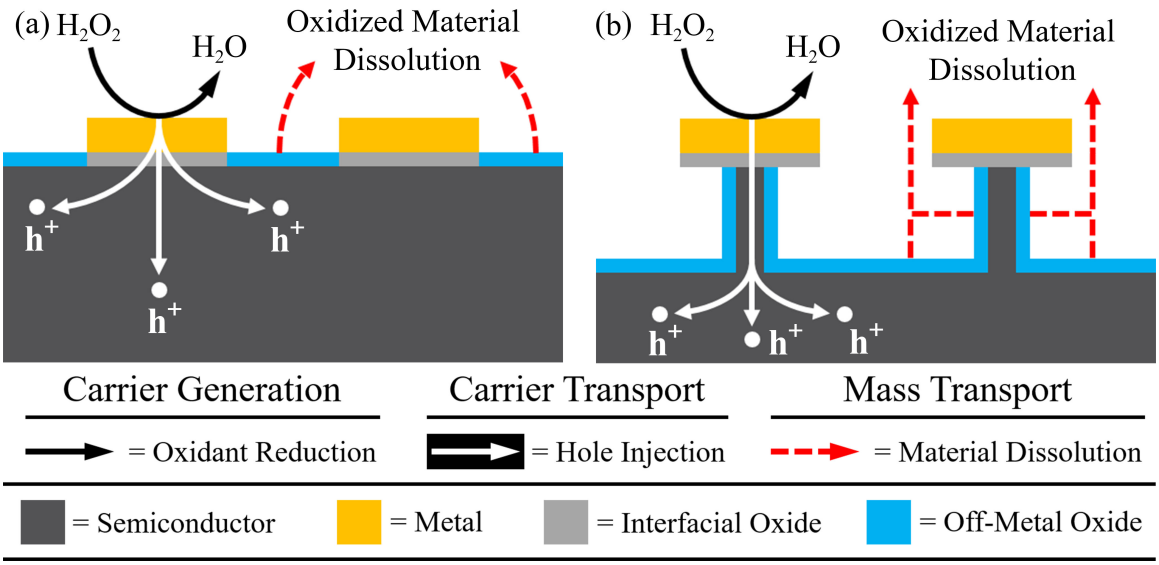

Figure 2.11: Models illustrating the mechanisms of inverse-progression MacEtch (a) at the onset of etching, and (b) during the generation of structures.

that of mass transport, holes will diffuse from underneath the catalyst and promote sidewall etching. This is the "mass transport limited" scenario, and can be seen in Figure 2.9b as continued lateral etching while the Ag nanoparticle sinks into the substrate.

2.4.2 Inverse-Progression MacEtch

The inverse-progression MacEtch process relies on many of the mechanisms described in the forward-progression scenario (e.g., catalytic oxidation and preferential dissolution of selective regions). However, several mechanisms are fundamentally different. Most notably, the metal does not sink into the substrate as observed in MacEtch; instead, the metal acts as a patterned mask as well as a catalyst, and generates inverse structures through preferential dissolution of off-metal regions [13, 42, 43]. An overview of the I-MacEtch mechanisms and the etching progression is illustrated in Figure 2.11.

A 2015 study on the inverse-progression MacEtch behavior of Au- and Pt-patterned InP proposed its mechanism to be based on the formation of distinct oxides at the metal/semiconductor interface and in the off-metal regions [13]. Figure 2.12 shows

XPS spectra for the P 2p bonding states for the Au-covered (red curve) and off-metal (black curve) regions [13]. Notice that both the Au-interfaced and off-metal regions exhibit the In-P bonding at 131 eV; however, the P-O bonding states present in $InPO_4$, $In(PO_3)_3$, and $In(PO_3)_4$ materials is much more pronounced in the regions covered by Au (i.e., the interfacial regions). These interfacial and non-interfacial oxides are non-soluble and soluble in the I-MacEtch solution, respectively. The non-soluble oxide layer generated at the metal-interfaced regions does not prevent the anodic half reaction (i.e., hole injection); however, it acts as a dissolution barrier and prevents solution access to the underlying material. This allows the hole distributions to spatially expand, and for the injected holes to diffuse into the off-metal regions.

Another possible explanation for I-MacEtch behavior could be related to the quality of the catalyst/semiconductor interface, and the spatial hole distributions generated about the metal. Holes are injected along the anode; however the metal/substrate interface is sufficiently thick (i.e., continuous and containing no voids) and wide such that it does not allow solution access to the oxidized material covered by the catalyst [42]. This prevents material dissolution underneath the metal, and allows the injected holes to diffuse from the anode to form extended hole distributions. Neighboring hole distributions may even overlap and increase the rate of oxide formation in these areas.

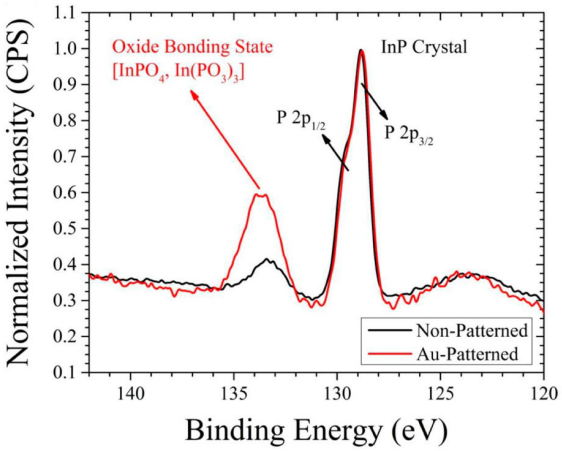

Figure 2.12: High-resolution XPS spectra for the P 2p bonding states for the (red curve) Au-covered and (black curve) off-metal regions [13].

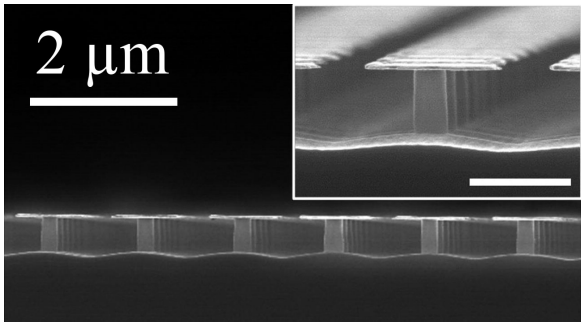

Figure 2.13: Cross-sectional SEM images of Pt-enhanced I-MacEtch of InP. Inset scale bar represents 1 μm [13].

This would subsequently increase the dissolution rate in the overlapped regions as well [42].

As illustrated in Figure 2.11, the result of inverse-progression MacEtch is the preferential dissolution of off-metal regions, followed by etching of the oxidized regions underneath the metal as those regions become exposed [43]. An example of post-I-MacEtch structures can be seen in Figure 2.13. An important limitation of this process is one of its defining characteristics; that is, the depth to which holes are injected into the substrate is finite for a particular set of system parameters (e.g., oxidant type and concentration, catalyst type and thickness, carrier mobility and diffusion length of the semiconductor, etc.) [13]. This is contrary to forward-progression MacEtch, where the catalyst will continue to sink into the substrate indefinitely, assuming the oxidant and etchant species are not exhausted within the solution. Instead, the vertical etching

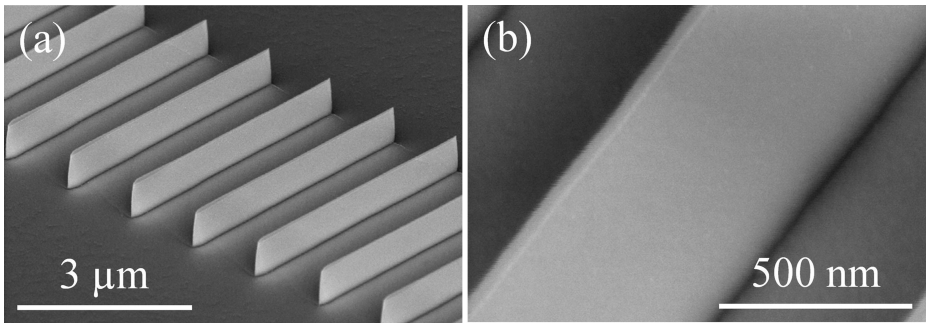

Figure 2.14: Cross-sectional SEM images of Pt-enhanced I-MacEtch of InP. Inset scale bar represents 1 μm [13].

for I-MacEtch will eventually saturate, whereas the lateral etching will not. This can be exploited to generate structures of extremely small lateral dimensions without the need to pattern the catalyst to similar sizes. A perfect example of this can be seen in Figure 2.14, where InP nanofin structures 20 nm wide and 700 nm tall were fabricated via I-MacEtch using Au catalyst strips 500 nm wide [13].

Chapter 3

Background of Photovoltaics

This chapter provides a detailed description of photovoltaics. While the focus of this dissertation is ultimately not on device performance, MacEtch is applied to GaAs substrates in Chapter 10 towards creating a viable process flow towards carrier-selective asymmetric heterojunction GaAs photovoltaics. To that end, device physics is described here, including those following conventional p-n junction and carrier-selective architectures.

The essence of a photovoltaic solar cell is a device that generates power in the presence of light (i.e., photons). Fundamentally, a solar cell converts light energy into electrical energy by means of the photovoltaic effect. Conceptually, the most basic and idealistic explanation of solar cell functionality consists of carrier generation (i.e., electrons and holes), carrier separation and transport, and carrier collection. A more complete and realistic illustration of solar cell operation requires the addition of practical limitations to the ideal situation. An overview of semiconductor physics will be given, and then the fundamentals of photovoltaics will follow. Lastly, an introduction into transparent conductive oxides (TCOs), transition metal oxides (TMOs), and carrier-selective photovoltaics will be provided.

3.1 Physics of Photovoltaics

Some foundational concepts in semiconductor physics must be outlined before a more complete description of how and why photovoltaic devices function. Mathematical

derivations will be avoided unless necessary for discussion, however approximations, models, theorems, etc. will be noted if the reader would like to explore the evolution of concepts beyond the scope of this work.

3.1.1 Energy Band Structure

Conceptualizing an electron within a semiconductor material is analogous to the quantum mechanical approach to a particle in a box. The time-independent Schrödinger equation describes the motion of an electron based on its wave function and defines the band structure of materials. That is, it defines the allowable energy quanta and the energy-momentum relationship for a given material. Fortunately, the Drude-Sommerfeld model (or free electron model), in conjunction with Blochs theorem, describes the quantum mechanical behavior (e.g., Fermi-Dirac statistics, Pauli exclusion principle, etc.) of particles within a crystal lattice using a classical approach. A classical model for a subatomic particle in a periodic lattice was found to be sufficient if the particles mass, m, is replaced by its effective mass, m^*,

$$m^* \equiv \left(\frac{\mathrm{d}^2 E}{\mathrm{d}p^2}\right)^{-1} = \left(\frac{1}{\hbar^2}\frac{\mathrm{d}^2 E}{\mathrm{d}\mathbf{k}^2}\right)^{-1} \tag{3.1}$$

where $\mathbf{k}$ is a wave vector and proportional to momentum, p, by $p = \hbar\mathbf{k}$.

Figure 3.1 is an example of a semiconductors band structure, albeit a simplified representation. It should be noted that the valence and conduction bands in semiconductors are separated by an energy gap or band gap energy (E_g) larger than $k_\mathrm{B}T$ (i.e., $\sim$0.0259 eV at room temperature), where k_B and T represent the Boltzmann constant and temperature, respectively. The valence band represents more tightly bound valence electrons, while conduction band electrons have had their bonds broken and are free to move about the lattice. Conduction band electrons are aptly named, as they may flow or transport (i.e., conduct) current under conditions that will be

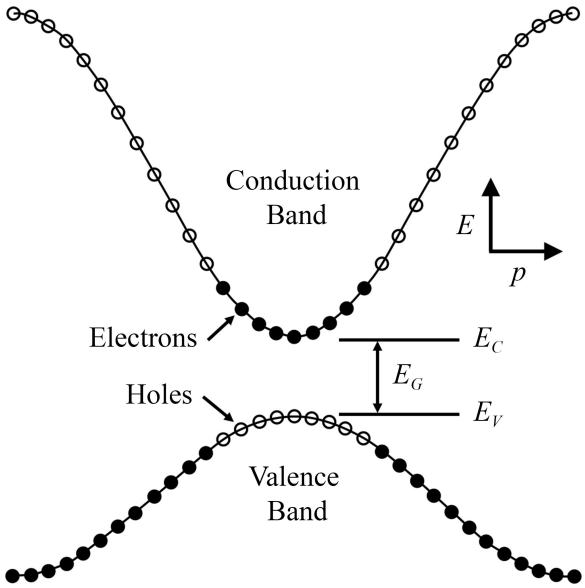

Figure 3.1: Illustration of the valence and conduction band density of states for a direct band gap semiconductor. The filled circles in the conduction band represent electrons that have been excited from the valence band, and the empty circles in the valence band represent the holes created by the excitation of valence electrons.

discussed below.

The allowed energy quanta that satisfy the Schrödinger equation are highlighted as distinct rows of filled and unfilled circles in Figure 3.1. Electrons fill these available energy states from bottom to top, and there exists a probability for loosely bound valence electrons (i.e., those at the top of the valence band) to be thermally excited to the conduction band at temperatures above 0 K. Excited electrons leave behind a vacant electron position or hole in the lattice. Although a hole physically represents a "lack of an electron" and is therefore a quasiparticle, band structure calculations are simplified by considering them particles with mass and of positive charge. Furthermore, Equation 3.1 indicates the effective mass of both electrons and holes vary with their energy (i.e., which energy quantum they happen to reside in).

As mentioned previously, distinct energy quanta make up the allowable levels of occupation for electrons and holes. The Pauli exclusion principle states that each energy quantum may contain a maximum of two electrons, however the distribution or density of these states can vary wildly. The valence band and conduction band

effective density of states (N_{V} and N_{C}, respectively) are needed to determine the carrier concentration and distribution within each band. Calculating the effective density of states (DOS) requires solving the time-independent Schrödinger equation for a wave vector of a particle in a box again, however this is simplified due to the effective mass formulation. The effective DOS for the valence and conduction bands, with units of cm^{-3}, are

$$N_{\mathrm{V}} = 2\left(\frac{2\pi m_p^* k_{\mathrm{B}} T}{h^2}\right)^{3/2} \tag{3.2a}$$

$$N_{\mathrm{C}} = 2\left(\frac{2\pi m_n^* k_{\mathrm{B}} T}{h^2}\right)^{3/2} \tag{3.2b}$$

An important consequence of Figure 3.1 is that electrons near the bottom of the conduction band (represented by stars) are considered to have a constant effective mass, as is the case for holes near the top of the valence band (indicated by circles). Electrons are particles with half-integer spin (i.e., fermions), and therefore obey Fermi-Dirac statistics and the Pauli exclusion principle. For a semiconductor under thermal equilibrium, the Fermi-Dirac distribution provides the probability of a particular energy quantum being occupied by a fermion, and is given by

$$f(E) = \frac{1}{1 + \mathrm{e}^{(E - E_{\mathrm{F}})/k_{\mathrm{B}}T}} \tag{3.3}$$

where E_{F} is the Fermi energy, k_{B} is the Boltzmann constant, and T is temperature. The Fermi energy, by definition, is the energy level at which the probability of occupation by an electron is 1/2, which can be seen by setting $E = E_{\mathrm{F}}$.

$$f(E_{\mathrm{F}}) = \frac{1}{1 + \mathrm{e}^{(E_{\mathrm{F}} - E_{\mathrm{F}})/k_{\mathrm{B}}T}} = \frac{1}{1+1} = \frac{1}{2} \tag{3.4}$$

The concentration of electrons in the conduction band, n_0, and holes in the valence band, p_0, can be found, to a good approximation, by combining the effective DOS

Equations 3.2a and 3.2b with the Fermi-Dirac distribution, Equation 3.3.

$$n_0 = N_{\mathrm{C}} \mathrm{e}^{(E_{\mathrm{F}} - E_{\mathrm{C}})/k_{\mathrm{B}}T} \tag{3.5a}$$

$$p_0 = N_{\mathrm{V}} \mathrm{e}^{(E_{\mathrm{V}} - E_{\mathrm{F}})/k_{\mathrm{B}}T} \tag{3.5b}$$

Equations 3.5a and 3.5b express the concentration of electrons and holes based on the Fermi energy. A commonly used alternative for these is an approximation whereby the Fermi energy of intrinsic semiconductors (i.e., no impurities or dopants) is close to midgap. In this scenario, the concentrations of holes and electrons are each equal to the intrinsic carrier concentration. That is, $n = p = n_{\mathrm{i}}$ and $E_{\mathrm{F}} = E_{\mathrm{i}}$, which provides the following equations describing carrier concentration based on known intrinsic values

$$n_0 = n_i \mathrm{e}^{(E_{\mathrm{F}} - E_{\mathrm{i}})/k_{\mathrm{B}}T} \tag{3.6a}$$

$$p_0 = n_i \mathrm{e}^{(E_{\mathrm{i}} - E_{\mathrm{F}})/k_{\mathrm{B}}T} \tag{3.6b}$$

3.1.2 Carrier Generation

Generation (i.e., "carrier generation" or "charge generation") of electron-hole pairs (EHPs) is the excitation of valence electrons to the conduction band, thereby leaving a vacant electron location (i.e., a hole) in the valence band. That is, electrons are liberated from the tightly bound valence band and excited to the loosely bound conduction band, and holes are created by the electron excitation. Carrier generation under equilibrium conditions (e.g., constant temperature, no illumination or photogeneration, no applied fields, etc.) consists of thermal excitation and relaxation, which occurs continuously in semiconductors not at 0 K. While band-to-band recombination and generation (R-G) is typically the most intuitive process, indirect thermal R-G within

the semiconductor must be taken into account. Particular impurities (e.g., Au, Cu, and Fe in Si) or lattice defects create allowed energy levels (E_{T}) within the band gap, which are referred to as traps because they serve to catch and hold carries. The carrier may be annihilated (i.e., recombined with the opposite carrier) if it is trapped for too long, in which case the trap is then referred to as a recombination center. The recombination process will be discussed in later sections.

As an example, a valence electron can be excited to a midgap energy level or trap center (E_{T}) when the semiconductor absorbs thermal energy. The electron excitation creates a holes in the valence band, and the thermal EHP generation process is complete once the electron is excited to the conduction band by absorbing additional thermal energy. Under equilibrium conditions, carriers are generated and recombined at the same rate (i.e., no net carrier concentration is created). However, if carriers the carrier concentration is altered by some external process (e.g., photogeneration via illumination), the thermal generation or recombination rates automatically adjust in an attempt to bring the system back to equilibrium.

Photogeneration will be the main source of external carrier generation discussed here, and is the result of absorbing incident photons with energies at, or above the band gap energy (E_{g}) of the semiconductor. The photogeneration rate (G_{L}), or the number of excess carriers created by illumination, is expressed in Equation 3.7, where τ is the minority carrier lifetime and represents the average time a minority carrier exists before it recombines with a majority carrier. The photogeneration rate is also influenced by the depth to which photons penetrate into the semiconductor.

$$G_{\mathrm{L}} = \frac{\delta n}{\tau_{\mathrm{n}}} = \frac{\delta p}{\tau_{\mathrm{p}}} \tag{3.7}$$

Some portion of light incident on an absorbing material will be reflected off its outer surface, while the remaining light is attenuated by absorption as it passes through

the material. Refractive index describes how light propagates through a material, and mathematically it has real and imaginary contributions. The real portion is the absorption coefficient, α, and the imaginary part is the extinction coefficient, κ. The intensity of the light will decrease exponentially through the material. Assuming the incident light is normal to the material surface and a uniform absorption coefficient, the Beer-Lambert law describes the intensity at any given depth, x, within the material

$$I(x) = I_0 \exp(-\alpha x) = I_0 \exp\left(\frac{-4\pi\kappa x}{\lambda}\right) \tag{3.8}$$

where I_0 is the intensity, and λ is the wavelength, of the light that enters the material. Similarly, the total carrier generation rate can be expressed by

$$G(x) = (1-s)\int_{\lambda} F(\lambda)\left[1 - R(\lambda)\right]\alpha(\lambda)\, e^{-\alpha(\lambda)x} d\lambda \tag{3.9}$$

where s is the covered device area (i.e., shadowing factor), F is the incident photon flux, and R is the reflection coefficient.

Photovoltaic devices convert light energy into electrical energy, and the most abundant source of light energy on Earth comes from the Sun. The Suns emission

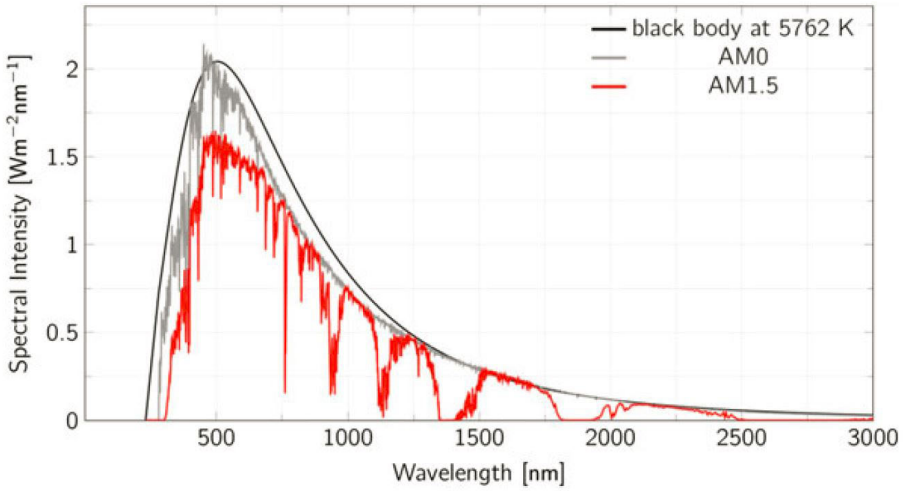

Figure 3.2: Spectral intensity for an ideal 5762 K blackbody (black curve), AM0 (grey curve), and AM1.5 (red curve) [52].

spectrum resembles that of a blackbody, which means it emits a radiation distribution of quantized energy based on its surface temperature, ∼5800 K. Due to the makeup of Earth's atmosphere, the solar spectrum passing through it changes in shape and undergoes attenuation, resulting in a reduction in spectral irradiance observed on Earths surface. The air mass (AM) coefficient defines the spectral irradiance based on attenuation from traversing a particular number of Earth atmospheres of standard thickness and composition. For example, AM0 represents the solar spectrum prior to entering the atmosphere, and therefore is the appropriate consideration for extraterrestrial applications. However, the convention in the field of terrestrial photovoltaics is to use the AM1.5 spectrum for calculations. Figure 3.2 compares the theoretical emission spectrum of a blackbody at 5762 K (black line) with the spectral intensity of AM0 (grey curve) and AM1.5 (red curve). Unless otherwise specified, the remainder of this work will consider the AM1.5 global (AM1.5g) spectrum, which takes into account contributions from both direct and diffuse radiation. The AM1.5 spectrum provides approximately 1000 W/m^2, though this value varies based on factors such as altitude, cloud cover, the position of the sun in the sky, etc.

Absorption of incident photons is a requisite process for photovoltaic energy conversion. Additionally, separate energy states within the semiconductor are required, with an energy gap or band gap energy (E_g) larger than $k_\mathrm{B}T$ (i.e., ∼0.0259 eV at room temperature), where k_B and T represent the Boltzmann constant and temperature, respectively. Photon absorption promotes an electron from a particular energy state to one of higher energy. For now, electron promotion from the valence to conduction band will be considered, though intra-band excitation and relaxation occur as well. Photons with energy $h\nu < E_\mathrm{g}$ will not be absorbed, but instead will pass through the semiconducting material as seen in Figure 3.3a. Incident photons with energy equal to or greater than the band gap energy (i.e., $h\nu \geq E_\mathrm{g}$, where h and ν represent the Planck constant and frequency, respectively) will excite a conduction band electron to

the valence band, leaving behind a vacant electron position or hole in the lattice (Figure 3.3b). Although a hole is a 'lack of an electron and therefore a quasiparticle, band structure calculations are simplified by considering them particles with mass and of positive charge (*vide supra*).

Intrinsic semiconductors are often implanted with particular dopants in order to tune its electrical properties. Specifically, these impurity atoms, referred to as "donors" or "acceptors", are used to module electron or hole concentration within the semiconductor. The total number of donors (N_{D}) and acceptors (N_{A}) are generally known values, as they determined and controlled experimentally. Donors are group V elements with five valence electrons. When introduced to a group IV element (e.g., Si), an extra and unbounded valence electron is added to the lattice (hence, donor). The surplus of electrons creates a net negative charge, and the semiconductor is accordingly called n-type. Similarly, acceptors are group III elements with three valence electrons; that is, the missing fourth valence electron creates a broken bond, or hole, within the lattice. With fewer electrons, these impurities result in the semiconductor having a net positive, or p-type, charge.

3.1.3 Carrier Separation and Transport

The fundamentals of carrier separation and transport will be discussed here, including such topics as drift and diffusion currents, and electrostatics and electrodynamics of the P-N junction.

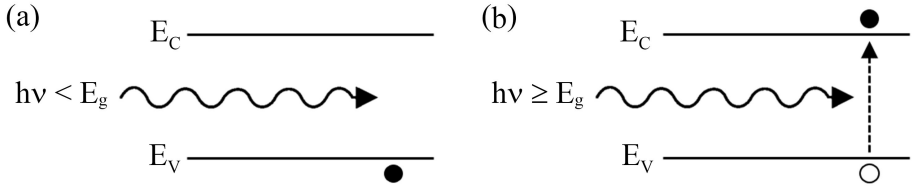

Figure 3.3: Schematics illustrating photons with (a) less energy than the band gap energy (E_{g}) which pass through the semiconductor, and (b) higher energy than E_{g} which excites a valence electron to the conduction band and leaves behind a hole.

Drift Current

Carrier motion or current conduction is governed by two fundamental concepts, drift and diffusion. Drift is an electromotive force that causes motion of charged particles in the presence of an electric field, and therefore obeys Ohm's law. Holes or positively charged carriers ($+q$) move in the direction of the electric field, whereas electrons or negatively charged carriers ($-q$) drift in the opposite direction. A microscopic inspection of these carriers would resemble Brownian motion due to frequent collisions and scattering with other particles within the lattice. However, they move in a single direction on a macroscopic scale over time, which is referred to as drift velocity (v_{d}). It should be noted that thermal motion also influences these particles, though it averages to no net movement over time (i.e., completely random) and therefore does not contribute to the directional flow discussed here.

Carrier mobility is the ease with which carriers can move with a lattice. As this describes the net movement in a particular direction, increasing the number of collision events over a given amount of time decreases the mobility of a carrier. Therefore, mobility is a proportional relation between the electric field and drift velocity. With that, the drift current density can be described as

$$J_{n\text{-drift}}(x) = q\mu_n n(x)E(x) \tag{3.10a}$$

$$J_{p\text{-drift}}(x) = q\mu_p p(x)E(x) \tag{3.10b}$$

where q is the elementary charge, n and p are the carrier concentration for electrons and holes, μ is the carrier mobility, and E is the electric field.

Diffusion Current

Diffusion is the process by which particles spread out due to a concentration gradient, and as such are governed by Fick's laws. In semiconductors, diffusion requires a nonzero spatial concentration gradient of holes or electrons (i.e., $\nabla p \neq 0$ and $\nabla n \neq 0$), and the flux of carriers scales with the concentration gradient. As electrons and holes are charged particles, current is generated in the direction of their motion based on Fick's first law

$$J_{n\text{-diff}}(x) = qD_n \frac{dn(x)}{dx} \tag{3.11a}$$

$$J_{p\text{-diff}}(x) = -qD_p \frac{dp(x)}{dx} \tag{3.11b}$$

Combining the carrier drift Equations 3.10a and 3.10b and the time-independent diffusion Equations 3.11a and 3.11b gives the total current density for electrons and holes

$$J_n(x) = q\mu_n n(x)E(x) + qD_n \frac{dn(x)}{dx} \tag{3.12a}$$

$$J_p(x) = q\mu_p p(x)E(x) - qD_p \frac{dp(x)}{dx} \tag{3.12b}$$

where J is the total current density, and D is the diffusion coefficient. Diffusivity or the diffusion coefficient can be determined experimentally using the Haynes-Schockley experiment, or it can be calculated if the carrier mobility is known (or vice versa) using the Einstein relation in Equation 3.13.

$$\frac{D}{\mu} = \frac{k_\mathrm{B}T}{q} \tag{3.13}$$

Transport Equations

Next, the change in carrier concentration through an infinitely thin volume over time will be considered. This is simply the concentration of carriers exiting the volume compared to the number that entered; however, carrier recombination and generation within the volume will also be included. The total increase in carriers includes the sum of the drift and diffusion currents, and the carrier generation rate. Likewise, a reduction in carrier concentration is the result of recombination. The equations outlining the difference in these values are called the continuity equations, and are

$$\frac{\partial \Delta n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} - \frac{\delta n}{\tau_n} + G_n \tag{3.14a}$$

$$\frac{\partial \Delta p}{\partial t} = \frac{1}{q}\frac{\partial J_p}{\partial x} - \frac{\delta p}{\tau_p} + G_p \tag{3.14b}$$

where G represents the generation rate. Equations 3.14a and 3.14b consist of three components: diffusive, recombination, and generation terms. It should be noted that the recombination term is of the same form as the photogeneration expressions in Equation 3.7. This is due to the photogeneration and recombination rates being equal (though opposite) under steady state conditions. Otherwise stated, the generation and recombination rates for a semiconductor under steady state conditions will naturally adjust in order for the two processes to balance each other out and result in no net generation or recombination. If drift current is assumed to be negligible, then the diffusion current density Equations 3.11a and 3.11b can be substituted into Equations 3.14a and 3.14b, which gives the diffusion equations and take the form of Fick's second law

$$\frac{\partial \Delta n}{\partial t} = D_n \frac{\partial^2 \delta n}{\partial x^2} - \frac{\delta n}{\tau_n} + G_n \tag{3.15a}$$

$$\frac{\partial \Delta p}{\partial t} = D_p \frac{\partial^2 \delta p}{\partial x^2} - \frac{\delta p}{\tau_p} + G_p \tag{3.15b}$$

In the case of steady state conditions, the time-dependence in Equations 3.15a and 3.15b are zero, and the recombination and generation components cancel each other out. Rearranging the reduced equations as noted above leaves a relationship defined as the diffusion length (L) given by

$$L_n \equiv [D_n \tau_n]^{1/2} \tag{3.16a}$$

$$L_p \equiv [D_p \tau_p]^{1/2} \tag{3.16b}$$

P-N Junction Electrostatics

P-N junctions are one of the hallmarks of conventional photovoltaic devices, as they are the most commonly utilized method by which carriers are separated. For the sake of discussion, an unrealistic thought experiment will be explored; namely, creating a P-N junction by joining two slabs of similar material doped p- and n-type, respectively. Prior to coupling the pieces, the p-type material has a large concentration of holes (and relatively few electrons), and the n-type has an abundance of electrons (and relatively few holes). Bringing the two pieces together creates a carrier gradient at the junction, which causes the migration of both holes and electrons to establish an electrostatic equilibrium. "Equilibrium" represents the scenario in which no external potential, or magnetic or electric field is applied, the material is not illuminated, and it is at a uniform temperature.

A larger concentration of holes are present on the p-side (p_p) of the junction than on the n-side (p_n), as seen in Figure 3.4, and conversely for electrons. This creates a concentration gradient for both carriers at the interface, and they will diffuse from

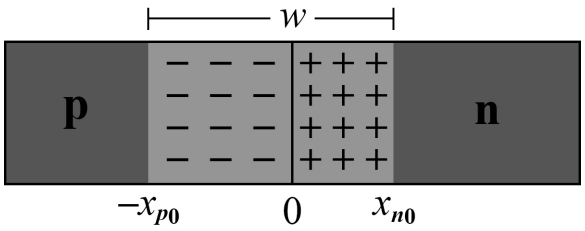

Figure 3.4: Schematic showing carrier inversion about a P-N junction with $N_{\mathrm{D}} > N_{\mathrm{A}}$.

one side to the other while attempting to bring the material back to equilibrium (i.e., homogeneous distribution). Instead, the carrier diffusion is halted as the charge balance on each side of the junction is disrupted. Holes diffuse from the p-side and leave negative acceptor ions, and electrons migrate from the n-side while leaving positive donor ions behind. This is a result of the donors and acceptors being fixed in the lattice while the holes and electrons are mobile.

Negative charges accumulate on the p-side of the junction, and positive charges line the opposite side. Thus, an electric field is induced in the direction of the negative charge (opposite to that of the diffusion current), which creates a drift current in the same direction. Recall that no net current is present in equilibrium, therefore the electric field continues to increase until the drift and diffusion currents exactly cancel one another (i.e., steady state conditions). The electric field is formed in a localized region about the junction, called the transition region (W), while the material is in equilibrium (i.e., no electric field and constant potential) further away. The separate regions of equilibrium are at different electrostatic potentials (i.e., no externally applied potential). This potential difference between the two equilibrium regions is called the contact or built-in potential (V_0), and physically represents the potential barrier across the transition region.

$$V_0 = \frac{k_{\mathrm{B}}T}{q} \ln\left(\frac{N_{\mathrm{D}}N_{\mathrm{A}}}{n_{\mathrm{i}}^2}\right) \tag{3.17}$$

The built-in electric field sweeps carriers out of the transition region, which leaves only

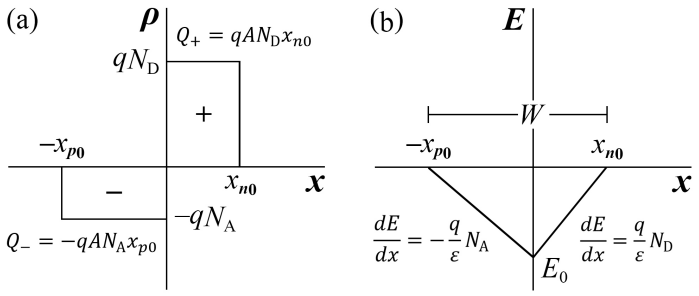

Figure 3.5: Plots showing the (a) charge density and (b) electric field within the depletion region (w) in Figure 3.4 for a P-N junction with $N_D > N_A$.

uncompensated donor and acceptor ions that create the space charge region within *W*. For this reason, the transition region is also referred to as the "space charge" and "depletion" regions. The depletion approximation states that $N_A \gg n_p$ or p_p, $N_D \gg n_n$ or p_n, and that the charge density (ρ) is zero outside the depletion region. More elegantly stated, the depletion approximation assumes charge neutrality outside the depletion region (i.e., equilibrium), and that no carriers are within *W*.

With the electric field increasing until the drift and diffusion components of current balance out, the magnitude of charge on each side of the junction must be equal. Since the initial doping concentration of each side is unlikely to be the same, the spatial width to which the depletion region extends into the p- and n-sides will be different to ensure steady state conditions. For example, if the n-side is doped higher than the p-side (i.e., N_D ¿ N_A), the depletion region will penetrate deeper into the p-side (-x_{p0}) than the n-side (x_{n0}) of the metallurgical junction ($x = 0$).

This concept can be visualized graphically (Figure 3.5a) by considering the penetration depth and charge density on each side of the junction, which will have an equal cross-sectional area. The total charge on each side of the junction can then be expressed as

$$qx_{p0}N_A = qx_{n0}N_D \tag{3.18}$$

$$\frac{dE(x)}{dx} = \frac{q}{\varepsilon}(p - n + N_D - N_A) \tag{3.19}$$

Then, utilizing Poisson's equation (Equation 3.19) and assuming the carrier contributions (p and n) are zero in the depletion region, the space charge on each side of the junction is found to be constant (Figure 3.5b) as follows

$$\frac{dE}{dx} = \frac{q}{\varepsilon} N_{\mathrm{D}} \quad \text{for} \quad 0 < x < x_{n0} \tag{3.20a}$$

$$\frac{dE}{dx} = -\frac{q}{\varepsilon} N_{\mathrm{A}} \quad \text{for} \quad -x_{p0} < x < 0 \tag{3.20b}$$

Integrating Equations 3.20a and 3.20b gives the maximum electric field strength, located at $x = 0$, which can then be integrating to find the contact potential (V_0) across the depletion region. Essentially, this relates the built-in potential with the depletion region width (W), giving

$$W = \left[\frac{2\varepsilon V_0}{q} \left(\frac{N_{\mathrm{A}} + N_{\mathrm{D}}}{N_{\mathrm{A}} N_{\mathrm{D}}} \right) \right]^{1/2} \tag{3.21}$$

Applying Potential Bias

Non-equilibrium conditions will now be considered; namely, applying an external potential bias across the terminals. A P-N junction more easily flows current from

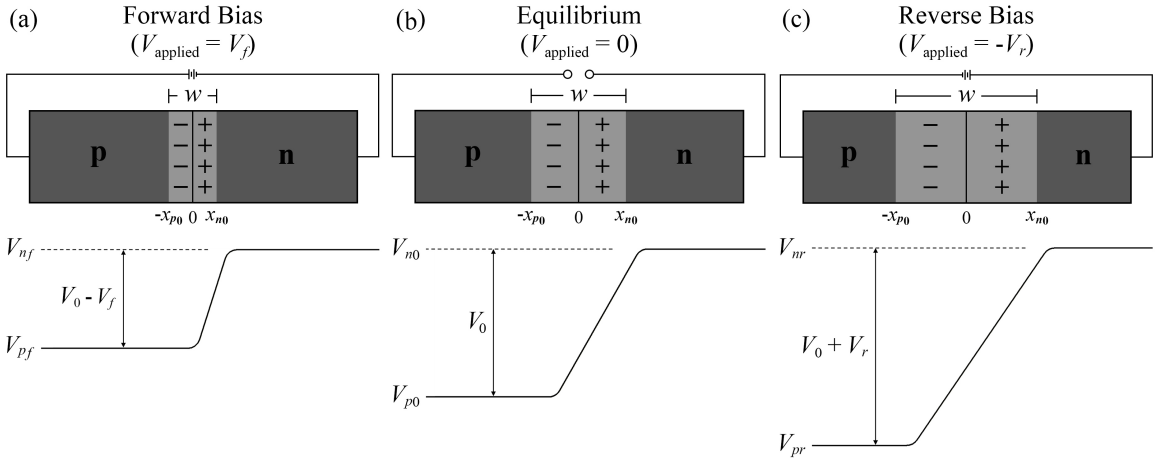

Figure 3.6: Schematics showing the depletion width and contact potential for a P-N junction with $N_{\mathrm{D}} > N_{\mathrm{A}}$ under (a) forward bias, (b) equilibrium, and (c) reverse bias.

the p- to n-side when the p-side has an increased potential relative to that of the n-side (Figure 3.6a). That is, current flows more easily under forward bias and forward current conditions than when in equilibrium (Figure 3.6b). This is a result of a reduction in the electrostatic contact potential (V_0) barrier due to the forward bias raising the p-side potential to be closer to that of the n-side potential. Moreover, the reduced disparity in contact potentials decreases the build-in electric field and the depletion region width, allowing carriers to cross more easily.

Conversely, very little current flows when the opposite conditions are applied (i.e., reverse bias and reverse current). In this scenario, V_0 is increased relative to equilibrium conditions (Figure 3.6c). The p-side potential is pushed further from that of the n-side potential, creating a larger potential barrier. Similarly, the larger contact potential increases the build-in electric field and widens the depletion region width to accommodate the additional donor and acceptor ions.

Recall, the total current crossing the depletion region is the sum of the drift and diffusion components. Under equilibrium conditions, the drift and diffusion currents cancel each other out, and the net current flowing across the junction is zero. Reverse bias generates a negligible diffusion current due to the heightened potential barrier; however, under forward bias the currents start behaving nicely. As expected, very little current flows at negative potential, which is the result of carriers generated (I_{gen}) within the depletion region or diffusive carriers (I_{diff}) that are collected. At $V = 0$, I_{gen} and I_{diff} cancel each other out, resulting in no current.

In forward bias, the diffusion current is found by multiplying the equilibrium diffusion current by the exponential, $\exp(qV/k_{\text{B}}T)$. The equilibrium diffusion current is equivalent to the generation current (I_{gen}), therefore the diffusive current is $[(I_{\text{gen}})]\,[\exp(qV/k_{\text{B}}T)]$ when bias is applied. The difference in these (i.e., the diffusion

and generation currents) gives the total current

$$I = I_0 \left(e^{qV/k_B T} - 1 \right) \tag{3.22}$$

which is also referred to as the Shockley or ideal diode equation. From Equation 3.22 and as seen in Figure 3.7, current increases exponentially in the forward direction, and very little current flows in the reverse direction. The latter current, I_0, is called the reverse saturation current (hence, the current saturates in the reverse direction). It should be noted, however, that Equation 3.22 can be used to describe the total current through a diode operated in forward or reverse bias.

$$I_0 = qA \left(\frac{D_n n_i^2}{L_n N_A} + \frac{D_p n_i^2}{L_p N_D} \right) \tag{3.23}$$

where A is the area of the active device. Discussing the current (I) output of a solar cell can be useful at times; however, it is more common to refer to its current density (J). While the total current output of a device is an important parameter, it provides no information on the physical size necessary to provide that current. Instead, current density will now be the emphasis, as its value scales with size.

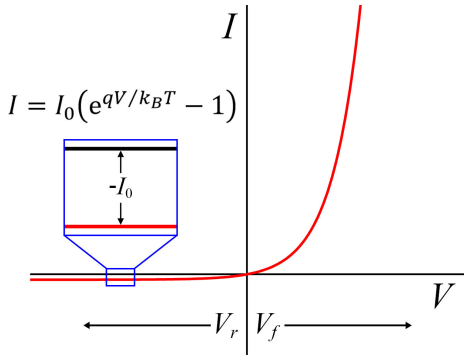

Figure 3.7: I-V characteristic of a P-N junction or ideal diode.

3.1.4 Loss Mechanisms

Recombination Mechanisms

Carrier recombination is the process by which holes and electrons reunite before they reach their respective contacts. This is detrimental to device performance because it reduces the number of charge carriers available for current generation outside the device (i.e., electricity). Recall, thermal recombination within semiconductors in equilibrium was discussed previously. Here, the three main recombination mechanisms that will be discussed include: radiative or band-to-band, Shockley-Read-Hall or trap-assisted, and Auger recombination.

Radiative or band-to-band recombination takes the form of spontaneous emission, whereby excited electrons in the conduction band emit energy (i.e., a photon of similar energy to the band gap energy). This is essentially the inverse of carrier generation via illumination, and is the fundamental mechanism for light-emitting devices (e.g., lasers and LEDs). As the electron losses energy, it relax down to the valence band and recombines with a hole, as seen in Figure 3.8. This process is most influential for direct band gap semiconductors due to indirect band gap materials requiring additional

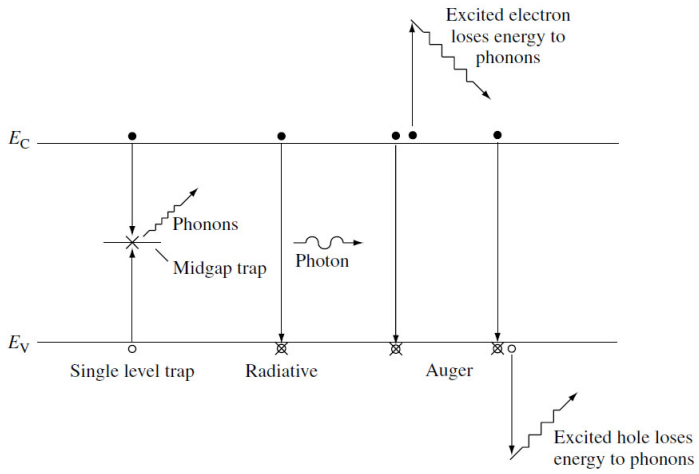

Figure 3.8: Illustration of various recombination phenomena, including Shockley-Read-Hall or trap-assisted, band-to-band or radiative, and Auger recombination [53].

momentum loss (given off in the form of a phonon) prior to relaxation. The net radiative recombination rate (R_{rad}) under state-state conditions is given by Equation 3.24, which is also useful relative to the effective carrier lifetime (τ; Equation 3.25).

$$R_{\mathrm{rad}} = B_{\mathrm{rad}} \left(np - n_i^2 \right) \tag{3.24}$$

$$\tau_{\mathrm{rad}} = \left[B_{\mathrm{rad}} \left(n_0 + p_0 + \Delta n \right) \right]^{-1} \tag{3.25}$$

Where B_{rad} is the radiative capture probability.

Shockley-Read-Hall (SRH) or trap-assisted recombination is the result of impurity dopants that create trap centers within the band gap. Carriers become trapped at these locations until they gain sufficient energy to escape. The amount of energy required to release a trapped carrier depends on how "deep" the trap state is within the band gap. For example, trap centers near a band edge require relatively little energy to escape compared to trap centers near mid-gap. The time a carrier remains trapped is directly related to the amount of energy required to release it, and therefore on how deep the trap resides within the forbidden region. If, for example, a hole reaches a trapped electron before it is thermally re-emitted to the conduction band, the EHP recombine and the trap is then referred to as a recombination center. This recombination releases energy to the lattice in the form of phonons, as seen in Figure 3.8. The SRH recombination rate (R_{SRH}) and carrier lifetime (τ_{SRH}) can be expressed by Equation 3.26 and 3.27, respectively

$$R_{\mathrm{SRH}} = \frac{pn - n_i^2}{\tau_{\mathrm{SRH},n} \left[p + n_i \mathrm{e}^{(E_{\mathrm{i}} - E_{\mathrm{T}})/k_{\mathrm{B}}T} \right] + \tau_{\mathrm{SRH},p} \left[n + n_i \mathrm{e}^{(E_{\mathrm{T}} - E_{\mathrm{i}})/k_{\mathrm{B}}T} \right]} \tag{3.26}$$

$$\tau_{\mathrm{SRH}} = \left[\sigma v_{\mathrm{th}} N_{\mathrm{T}} \right]^{-1} \tag{3.27}$$

where σ is the capture cross-sectional area, v_{th} is the carrier thermal velocity, E_{T} is the trap energy, and N_{T} is the trap density.

Auger recombination is a several step process and involves three carriers. First, an EHP recombine and give off energy that excites a carrier within the conduction band. The excited third carrier will tend to relax back to the lowest available conduction band energy state by releasing its excess energy to the lattice in the form of thermal vibrations (i.e., phonons). This process can be seen in Figure 3.8. Auger recombination is particularly prevalent in highly doped semiconductors or under high injection conditions (i.e., concentrated illumination). In these scenarios, the Auger recombination rate (R_{Auger}) and carrier lifetime (τ_{Auger}) are inversely related to the doping level and number of majority carriers. R_{Auger} and τ_{Auger} can be expressed by Equations 3.28 and 3.29, respectively.

$$R_{\text{Auger}} = (C_{n\text{n}} + C_{p\text{p}}) \left(pn - n_i^2\right) \tag{3.28}$$

$$\tau_{\text{Auger}} = \left[n^2 C_n + 2n_{\text{i}}^2 (C_n + C_p) + p^2 C_p\right] \tag{3.29}$$

Where C_n and C_p are the Auger capture probabilities.

Parasitic Resistance Losses

Resistive effects will now be considered, which are referred to as parasitic resistance losses due to their detrimental influence on device performance. Series (R_{S}) and shunt (R_{SH}) resistances are the most common, and both reduce the output of photovoltaic cells. Additionally, two crucial concepts must be briefly provided, both of which will be explained in detail in the following sections; that is, short-circuit current density (J_{SC}) and open-circuit voltage (V_{OC}). J_{SC} is the maximum current density obtainable by a particular device, and it occurs at zero voltage (hence "short-circuit"). Likewise, V_{OC} is the most voltage a solar cell can output, and it occurs at zero current (hence "open-circuit").

R_{S} is attributed to carrier resistance through the semiconductor layers towards

their respective contacts, and contact resistance formed by barriers abrupt metal-semiconductor interfaces (this will be discussed in detail below). Series resistance is often an indicator of either low quality material or poor device design. V_{OC} is not affected by series resistance because no current flows through the device under short-circuit conditions. However, R_{S} can have a dramatic effect on the illuminated J-V, or light J-V, curve. Ultimately, minimal series resistance is desired for well performing solar cells.

Shunt or parallel resistance is the process by which alternative pathways (i.e., shunts) are provided for current, and is often the result of poor device fabrication. Low shunt resistance (i.e., low resistance to shunting) limits the amount of current that flows through the device and reduces its voltage output. As shunt resistance is also considered parallel resistance (discussed below), it becomes particularly detrimental at low voltages and under low injection (i.e., minimal photogeneration) conditions.

Figure 3.9 shows a set of light J-V curves. Figure 3.9a shows an ideal curve with $R_{\mathrm{S}} = 0$ and $R_{\mathrm{SH}} = \infty$ (black), a curve affected by high series and shunt resistance (blue), and a curve exhibiting low R_{S} and R_{SH} (red). Both parasitic resistance losses can be determined numerically (Equations 3.30 and 3.31) or by inspection of the light J-V curves (Equations 3.32 and 3.33).

$$J = \frac{V}{R_{\mathrm{SH}}} \tag{3.30}$$

$$V = JR_{\mathrm{S}} \tag{3.31}$$

$$R_{\mathrm{S}} = -\frac{\Delta V_{\mathrm{OC}}}{\Delta J_{\mathrm{OC}}} \tag{3.32}$$

$$R_{\mathrm{SH}} = -\frac{\Delta V_{\mathrm{SC}}}{\Delta J_{\mathrm{SC}}} \tag{3.33}$$

Short-circuit current density (J_{SC}) and open-circuit voltage (V_{OC}) are the maximum values a particular photovoltaic cell can have; however, the maximum power output

("maximum power point" or P_{M}) of the device does not occur at the product of J_{SC} and V_{OC} as one might expect, because no power is generated at either of these points. This can be seen in Figure 3.9b, with an ideal light J-V curve highlighted in red. Instead, the maximum power output (blue curve) is the product of the maximum current density (J_{M}) and voltage (V_{M}) points, which can be generalized as such

$$P = JV = V\left[J_{\mathrm{SC}} - J_0\left(\exp\left[\frac{qV}{nk_{\mathrm{B}}T}\right] - 1\right)\right] \tag{3.34}$$

$$P_{\mathrm{M}} = J_{\mathrm{M}}V_{\mathrm{M}} \tag{3.35}$$

$$J_{\mathrm{M}} = J_{\mathrm{SC}} - J_0\left[\exp\left(\frac{qV_{\mathrm{M}}}{nk_{\mathrm{B}}T}\right) - 1\right] \tag{3.36}$$

$$V_{\mathrm{M}} = V_{\mathrm{OC}} - \frac{nk_{\mathrm{B}}T}{q}\ln\left(1 + \frac{qV_{\mathrm{OC}}}{nk_{\mathrm{B}}T}\right) \tag{3.37}$$

Another important parameter used to determine the quality of a solar cell is its fill factor (FF), which is a ratio of the maximum output power and the product of J_{SC} and V_{OC}. This can be seen graphically in Figure 3.9b, where the fill factor represents the quotient of Area 1 (light grey region, defined by J_{M} and V_{M}) and Area 2 (dark

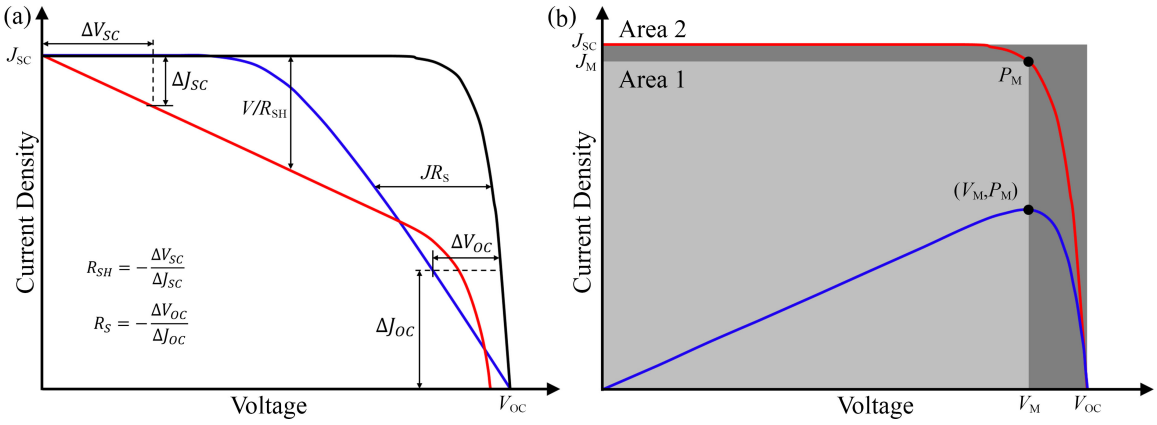

Figure 3.9: Light J-V curves illustrating (a) the influence of series (blue curve) and shunt (red curve) resistance on an ideal device (black curve), and (b) showing the current density output (red curve), power output (blue curve), and fill factor (relative area of light grey rectangle compared to that of the dark grey rectangle). Adapted from [54].

grey region, defined by J_{SC} and V_{OC}). By definition, fill factor cannot be 1 (or 100%) because no power is generated at either J_{SC} and V_{OC}. FF is a parameter that can be used to quickly determine the quality of a device and its fabrication process. Fill factor can be calculated using one of several methods

$$FF = \frac{J_{\mathrm{M}} V_{\mathrm{M}}}{J_{\mathrm{SC}} V_{\mathrm{OC}}} \tag{3.38}$$

$$FF = \frac{v_{oc} - \ln\left(v_{oc} + 0.72\right)}{v_{oc} + 1} \tag{3.39}$$

$$v_{oc} = V_{\mathrm{OC}} \frac{q}{n k_{\mathrm{B}} T} \tag{3.40}$$

where v_{oc} is referred to as normalized V_{OC}.

Power conversion efficiency (PCE; η), or "efficiency" for short, is the ratio of output power from the cell and the input or incident power from the sun. PCE is one of the main characteristics used for device comparison, and is calculated using

$$\eta = \frac{V_{\mathrm{OC}} I_{\mathrm{SC}} FF}{A P_{\mathrm{in}}} = \frac{V_{\mathrm{OC}} J_{\mathrm{SC}} FF}{P_{\mathrm{in}}} \tag{3.41}$$

where A is the illuminated area of the solar cell, and 1000 W/m^2 or 0.1 W/cm^2 is typically used as the input power, P_{in}, under standard testing conditions.

3.1.5 Equivalent Circuit Models

The behavior of a photovoltaic cell can be modeled using electrical circuit diagrams. In its most basic form, a solar cell has an equivalent circuit to that of a current source in parallel with a diode (i.e., an asymmetric and nonlinear resistive element). The cell produces a photocurrent density (J_{L}) that is proportional to the intensity of incident light and the area under illumination, which is divided between the diode and output (i.e., the terminals, or load). Here, the diode serves as a rectifier to impede the flow of current by providing a more resistive path, which drives the photocurrent through the

terminals with negligible resistance.

Several crucial equations become conceptually evident from considering representative circuit diagrams for photovoltaic cells. The short-circuit current density (J_{SC}) is the output current density when the terminals are connected (Figure 3.10a), and represents the maximum current density the cell can generate. That is, when the load resistance is negligible (or removed) and the voltage across the terminals is zero. The open-circuit voltage (V_{OC}) is the voltage across the terminals are disconnected or isolated from the circuit (Figure 3.10b), and corresponds to the maximum voltage that can be generated by the cell. That is, when an infinite load resistance is attached and no current flows between the terminals.

$$V_{\mathrm{OC}} = \frac{k_{\mathrm{B}}T}{q}\ln\left(\frac{J_{\mathrm{SC}}}{J_0}+1\right) \tag{3.42}$$

A current density is created from a potential difference between the terminals (i.e., in the presence of a load) that is in the opposite direction of the photocurrent. Photovoltaic cells generally behave as a diode in the dark, such that current flow is enhanced in forward bias and reduced in reverse bias. As discussed previously, this rectifying behavior is an important property of solar cells because carrier separation is a consequence of an asymmetric junction.

$$J_{\mathrm{dark}} = J_0\left(\mathrm{e}^{qV/k_{\mathrm{B}}T}-1\right) \tag{3.43}$$

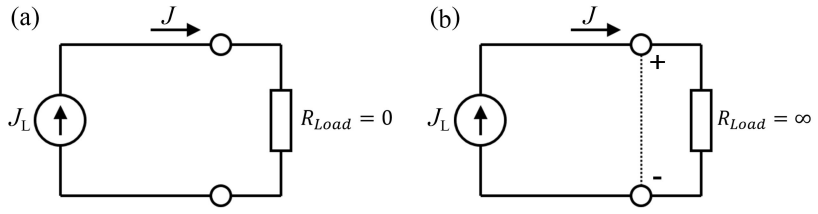

Figure 3.10: Equivalent circuits illustrating (a) J_{SC} with connected terminals, and (b) V_{OC} with isolated terminals or an infinite load connecting them.

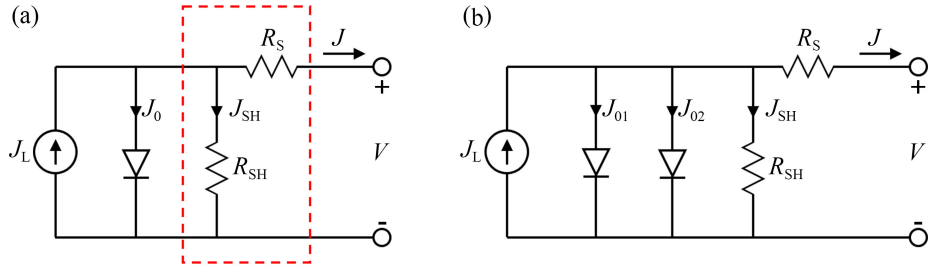

Figure 3.11: Equivalent circuits illustrating (a) the single diode model, and ideal diode equation with the red dashed rectangle removed (i.e., parasitic resistance losses), and (b) the complete two diode model.

Figure 3.11 shows circuit diagrams that are equivalent to photovoltaic devices, and will serve as a visualization for the following discussion. Essentially, the total current density output (J) is the difference between Equation 3.22 and the photocurrent density generated under illumination (J_{SC}). The ideal diode equation is adjusted slightly to more accurately include the ideality factor (n), which is set to 1 in the "ideal diode case. This can be seen in the illuminated single-diode Equation 3.44, and is a representative circuit diagram can be seen in Figure 3.11a (excluding the features highlighted by a red dashed rectangle). Ideality factor ranges from $1 \leq n \leq 2$, and describes how closely a cell behaves like a perfect diode. A cell matching the predicted behavior of an ideal diode (i.e., $n = 1$) will exhibit no carrier recombination within the depletion region, whereas an ideality factor of $n = 2$ often describes a device with recombination occurring within the space charge region. Most solar cells feature both regimes, which is referred to as the two-diode or double-diode Equation 3.45. The two diode case seen in Figure 3.11b is necessary for scenarios in which recombination occurs within the depletion region. For example, amorphous and polycrystalline Si-based cells, and those with high impurity concentrations, are high ideality devices. That is, the device exhibits non-ideal (i.e., $n>1$) regimes in which a second diode is needed to account for the depletion region recombination that otherwise does not occur in an ideal scenario.

$$J = J_{\mathrm{SC}} - J_0 \left(\mathrm{e}^{qV/nk_{\mathrm{B}}T} - 1\right) \tag{3.44}$$

$$J = J_{\mathrm{SC}} - J_{01} \left(\mathrm{e}^{qV/k_{\mathrm{B}}T} - 1\right) - J_{02} \left(\mathrm{e}^{qV/2k_{\mathrm{B}}T} - 1\right) \tag{3.45}$$

Components that reduce the output of solar cells must now be added for the sake of accuracy, including series ($\mathrm{R_S}$) and shunt ($\mathrm{R_{SH}}$; or "parallel) resistance components which are set in series and parallel with the photocurrent, respectively. Equivalent circuit diagrams that include these resistance losses can be seen in Figure 3.11 (panel a for the single diode case, and panel b for the two diode scenario). These are referred to as parasitic resistance losses, and as such, high $\mathrm{R_{SH}}$ and low $\mathrm{R_{SH}}$ values serve to abate device performance. In the ideal situation discussed above, $\mathrm{R_{SH}} = \infty$ and $\mathrm{R_S} = 0$. That is, the parallel shunt resistance stops current from flowing down an alternate path, and the series resistance does not attenuate the photocurrent enroute to the terminals. Mathematically, these parasitic resistance losses transform Equation 3.45 into

$$J = J_{\mathrm{SC}} - J_{01} \left[\mathrm{e}^{q(V+JR_{\mathrm{S}})/k_{\mathrm{B}}T} - 1\right] - J_{02} \left[\mathrm{e}^{q(V+JR_{\mathrm{S}})/2k_{\mathrm{B}}T} - 1\right] - \frac{(V + JR_{\mathrm{S}})}{R_{\mathrm{SH}}} \tag{3.46}$$

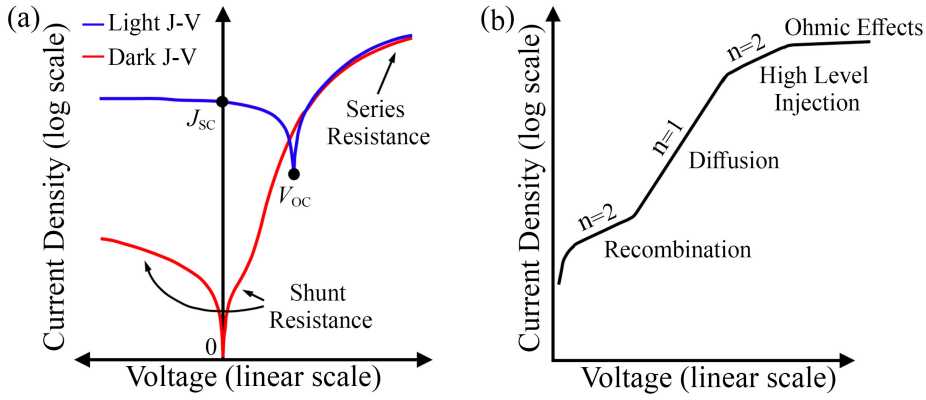

Figure 3.12: Semi-log axis plots showing (a) light (blue curve) and dark (red curve) J-V curves [55], and (b) a detailed dark J-V curve highlighting different regimes in forward bias [56].

Figure 3.12 shows examples of dark J-V curves on plots with semi-log axes; that is, a linear horizontal axis for voltage, and a logarithmic vertical axis to account for the exponential dependence of current density. Dark J-V is a useful characterization because it illustrates how a device behaves without illumination (hence "dark" J-V). Instead, a controlled flux of carriers are electrically injected into the device via the contacts. Figure 3.12a shows an overlay of both light J-V (blue curve) and dark J-V (red curve) on the same plot, and J_{SC} and V_{OC} are highlighted as well. Notice the dark J-V curve in reverse bias does not appear as ideal as that seen in Figure 3.7, which is the result of non-infinite shunt resistance allowing current leakage. Figure 3.12b is a representation of an ideal diode under forward bias, as evident by the straight lines and abrupt changes in slope (loss mechanisms discussed above would - at the very least - produce curvature instead of sharp slope changes). At low currents, carrier recombination within the junction dominates, and shunt resistance is prevalent in this regime. This results in a high ideality factor (n = 2), and the J_{02} component of the saturation current can be extracted. Moderate currents exhibit low level carrier injection and current limited by diffusion, which is susceptible to series resistance losses. This leads to ideal diode behavior (n = 1), and the J_{01} component of the saturation current can be extracted from this regime. High level injection (resulting in n = 2 behavior) and ohmic losses dominate high currents, which is often the result of devices under concentrated illumination.

3.1.6 Spectral Response and Quantum Efficiency

Figure 3.13 shows spectral response (SR; panel a) and external quantum efficiency (EQE; panel b) curves for ideal and realistic solar cells. Spectral response is the photocurrent generated by a photovoltaic cell relative to its incident power. Figure 3.13a shows the SR for an ideal cell (red curve) exhibits a linear increase in responsivity until a sharp drop at the wavelength corresponding to the band gap energy. The

blue curve is an example of a more practical measurement. The short-wavelength response is reduced due to this particular device being covered in glass, which absorbs the high energy photons. The mid-wavelength response appears to be nearly ideal; however, the performance near the band gap energy (i.e., relatively long-wavelength) demonstrates non-ideal behavior. The example device is Si-based, which is an indirect band gap semiconductor. This explains the long-wavelength response beyond the band gap energy instead of a more abrupt cutoff. External and internal spectral response can be calculated using Equation 3.47 and 3.48, respectively.

$$SR_{\text{ext}}(\lambda) = \left[\frac{q\lambda}{hc}\right] \frac{J_{\text{SC}}(\lambda)}{F(\lambda)} \tag{3.47}$$

$$SR_{\text{int}}(\lambda) = \left[\frac{q\lambda}{hc}\right] \frac{J_{\text{SC}}(\lambda)}{(1-s)\left[1-R(\lambda)\right]F(\lambda)} \tag{3.48}$$

Where s is the covered device area (i.e., shadowing factor), F is the incident photon flux, R is the reflection coefficient, h is the Planck constant, and c is the speed of light.

External quantum efficiency (EQE) is the number of carriers collected relative to the number of photons incident on a photovoltaic device of sufficient energy for photogeneration. This includes the effects of incident photons that are reflected or

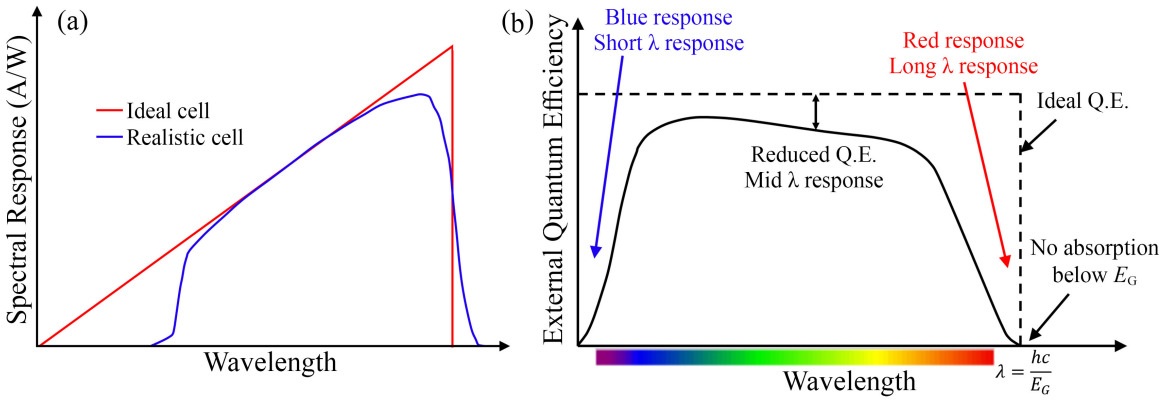

Figure 3.13: Graphs showing (a) ideal (red curve) and practical (blue curve) spectral response, and (b) external quantum efficiency [54].

transmitted, and that do not contribute to carrier generation. Internal quantum efficiency (IQE) is the ratio of carriers collected to the number of incident photons that participate in the generation of charge carriers. Otherwise stated, IQE is a measure of how efficiently a solar cell collects carriers that have been generated, whereas EQE indicates the efficiency with which the device collects charge carriers relative to the number of carriers that could possibly be generated and collected from the incident photons. Therefore, by definition EQE cannot be larger than the corresponding IQE.

It should be noted that internal quantum efficiency cannot be measured; rather, IQE must be calculated from external quantum efficiency measurements. Poor EQE can be indicative of a highly reflective device, and low IQE means the device is not utilizing the sufficiently energetic photons well. Figure 3.13b is an example of an external quantum efficiency measurement. The black dashed rectangle indicates the shape of an ideal - though unrealistic - quantum efficiency measurement. As longer-wavelength photons penetrate deeper into a semiconductor than those of higher energy, the spectral response of a QE measurement provides information regarding various depths within a device. Short-wavelength (i.e., high energy photons on the blue end of the visible spectrum) response describe the efficiency of the top-most layers of a device, and a poor response in this regime could indicate high recombination at the front surface. This could be a sign the front surface requires better passivation to minimize surface recombination. The mid-wavelength response is influenced by the bulk of the device, and a low carrier diffusion length could lead to reduced QE response. Long-wavelength (i.e., low energy photons on the red end of the visible spectrum) response provides information about the rear surface of the solar cell. Low QE values in this regime could indicate low carrier diffusion lengths as well as back surface recombination. This could be mitigated by improving the back surface field (BSF) to improve passivation and reduce surface recombination. Finally, the quantum efficiency drops to zero for long photon wavelengths corresponding to energies below

the band gap energy and insufficient to promote photogeneration. EQE and IQE can be calculated using Equations 3.49 and 3.50, respectively, and an expression relating the two is also provided.

$$EQE\left(\lambda\right) = \frac{J_{\mathrm{SC}}\left(\lambda\right)}{qF\left(\lambda\right)} = \left(\frac{hc}{q\lambda}\right) SR_{\mathrm{ext}}\left(\lambda\right) \tag{3.49}$$

$$IQE\left(\lambda\right) = \frac{J_{\mathrm{SC}}\left(\lambda\right)}{q\left(1-s\right)\left[1-R\left(\lambda\right)\right]F\left(\lambda\right)} = \left(\frac{hc}{q\lambda}\right) SR_{\mathrm{int}}\left(\lambda\right) \tag{3.50}$$

$$IQE\left(\lambda\right) = \frac{EQE\left(\lambda\right)}{1-\mathrm{Reflection}\left(\lambda\right)}$$

3.1.7 Ohmic and Rectifying Contacts

Ohmic contacts are metal-semiconductor junctions that allow current to flow equally in both directions, and their current-voltage (I-V) relationship is similar that of a resistor (i.e., they follow Ohms law, hence the name 'ohmic). Rectifying contacts allows current to flow in only one direction, and their I-V curves resemble that of a diode. Rectification can be the result of a variety of device aspects, such as a Schottky barrier, a p-n junction (i.e., homojunction), or a heterojunction. Both ohmic and rectifying contacts are dependent on the Schottky barrier height, which acts as an interface threshold that must be overcome for electrons to flow.

Anderson's Rule

Andersons rule is utilized to describe energy band diagrams of two dissimilar semiconductor materials (i.e., a semiconductor-semiconductor heterojunction). Here, the construction of heterojunction energy band diagrams relies on aligning the vacuum levels of both materials to the same energy. Once aligned, the electron affinity (χ) and the band gap energy (E_{G}) can be used to determine the locations of the conduction and valence bands for the corresponding materials. Their bands, along with their representative work functions (Φ), are then aligned to create a continuous Fermi level,

and Poissons equation can be used to determine the shape of the band bending at the interface. An important limitation of Andersons rule is that it neglects practical chemical bonding effects at the interface, such as surface and interface states, defect states, and dislocations.

Schottky-Mott Rule

The Schottky-Mott rule is very similar to Andersons rule, except the former is used to describe energy band diagrams of metal-semiconductor heterojunctions. The work function of each material (relative to the same vacuum level) is drawn first, followed by either the electron affinity (i.e., conduction band) or ionization potential (i.e., valence band) of the semiconductor (relative to the same vacuum level). The band diagrams for the separate materials are complete, and their Fermi levels are aligned. As the materials are brought together, the Schottky-Mott model accurately predicts the presence of band bending at the interface; however, it inaccurately illustrates the Schottky barrier height with varying amounts of disparity for various material systems. Like Andersons rule, the Schottky-Mott rule fails to account for surface and metal-induced gap states (i.e., Fermi level pinning), which will be discussed below.

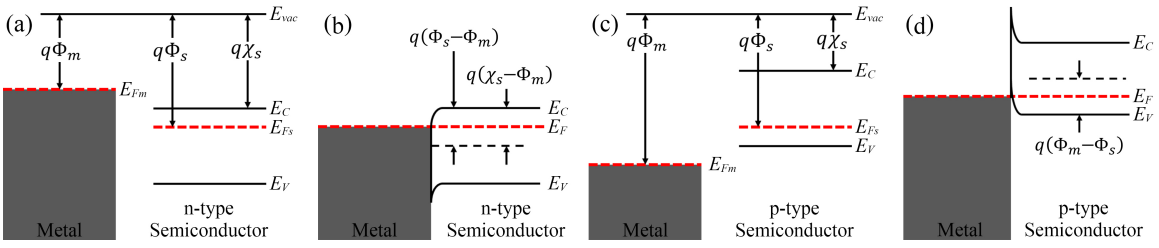

Figure 3.14: Models illustrating metal-semiconductor ohmic contacts for an n-type semiconductor (a) before and (b) after being interfaced, and for a p-type semiconductor (c) before and (d) after being interfaced.

Ohmic Contacts

Ohmic contacts are metal-semiconductor heterojunctions whose I-V curves resemble that of a resistor with a negligible voltage drop; that is, the contact exhibits linear current-voltage behavior under both forward- and reserve-bias. The resistance of the metal-semiconductor junction (i.e., contact resistance, or R_{C}) should be insignificant compared to the total resistance of the device, and is defined at zero bias to be

$$R_{\mathrm{C}} \equiv \left(\frac{\mathrm{d}J}{\mathrm{d}V} \right)^{-1}_{V_{\mathrm{applied}}=0} \tag{3.51}$$

Contact resistance decreases with the Schottky barrier height at the junction, which can be seen in the following proportionality

$$R_{\mathrm{C}} \propto \exp\left(\frac{q\Phi_{\mathrm{B}}}{k_{\mathrm{B}}T} \right) \tag{3.52}$$

where Φ_{B} is the barrier height. Depictions of ideal ohmic contact scenarios can be seen in Figure 3.14. Panels a and b illustrate creating an ohmic contact between a metal and n-type semiconductor, which results in the unencumbered transport of electrons from the semiconductor to the metallic contact. The work function of the function of the n-type semiconductor is greater than that of the metal (i.e., χ_{s} ¿ χ_{m}), therefore the Fermi level of the semiconductor is raised to align that of the metal. Electrons flow from the metal into the semiconductor to bring the junction back to equilibrium conditions, which lowers the electrostatic potential barrier ($q\,V_0$). Likewise, Figure 3.14c,d shows an example of an ohmic contact being made wherein χ_{m} ¿ χ_{s} (i.e., metal and p-type semiconductor). Here, the Fermi level of the semiconductor is lowered and holes may pass freely from semiconductor to the contact.

Rectifying Contacts

Rectifying contacts only allow current to flow in one direction, and therefore their I-V characteristics resemble diode-like behavior. While rectification is not isolated to contacts (e.g., p-n junctions and heterojunctions), this section will deal with the rectifying behavior at metal-semiconductor junctions due to the formation of barriers referred to as Schottky barrier diodes (i.e., Schottky barriers). At first, ideal forms of these barriers can be modeled using the Schottky-Mott rule, and are therefore proportional to the relative difference in the metal work function and the semiconductor conduction band (each relative to the same vacuum level). Particularly important aspects of these barriers are: (1) their height (Φ_B), and (2) the width of the depletion region (W) they create at the metal-semiconductor interface. That is, the potential barrier is sufficiently high that the flow of carriers across the metallurgical junction is impeded, and can even serve to repel carriers intended for transport to the contact. Under equilibrium conditions and low voltage biases, these barriers give rise to high resistances and the formation of a depletion region inside the semiconductor and along the metal interface. The built-in potential of the depletion region sweeps away, or repels, those carriers enroute to the contact in order to create electrical current outside the device. It should be noted that the barrier height and width is reduced in forward bias and carriers may overcome the barrier via diffusion; likewise, the barrier height and width is increased under reverse bias conditions, and carrier transport across the

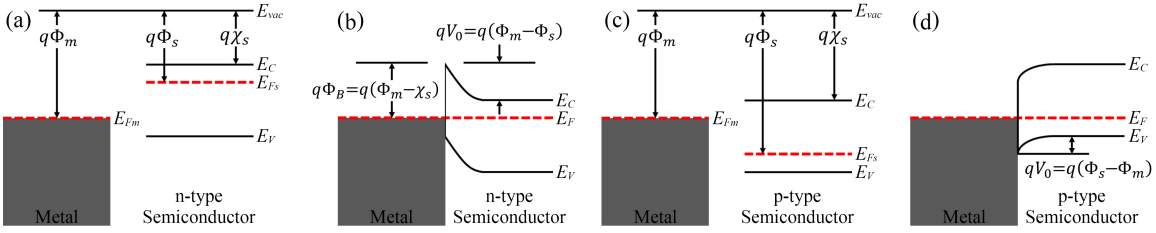

Figure 3.15: Models illustrating metal-semiconductor rectifying contacts for an n-type semiconductor (a) before and (b) after being interfaced, and for a p-type semiconductor (c) before and (d) after being interfaced.

barrier is negligible.

Figure 3.15 illustrates ideal scenarios of contacts exhibiting rectifying behavior due to the formation of Schottky barriers at the metal-semiconductor interface. As with the case for ohmic contacts, charge transfer between the metal and semiconductor occurs due to their disparate work functions (relative to the same vacuum level), which results in band bending (i.e., a junction) to reestablish equilibrium conditions. That is, positively charged donor ions accumulate on the semiconductor side of the metallurgical junction to compensate for the buildup of negative charges at the metal surface. Figure 3.15a,b is an example of rectifying contact being formed between a metal and n-type semiconductor (i.e., $\Phi_{\mathrm{m}} > \Phi_{\mathrm{s}}$). At the interface, the electron energy is reduced and the electrostatic barrier potential is increased on the semiconductor side of the junction. The potential barrier height ($q\Phi_{\mathrm{B}}$) represents the potential conduction electrons must overcome to reach the contact. Similarly, Figure 3.15c,d highlights the potential barrier height that holes must overcome to reach their corresponding contact. This barrier tends to effectively repel holes away from the contact. Here, the p-type semiconductor has a larger work function than the metal ($\Phi_{\mathrm{s}} > \Phi_{\mathrm{m}}$), and the electron energy within the semiconductor must be raised to align the Fermi levels on each side of the junction. In a similar fashion as for n-type semiconductors, a depletion region is formed to sweep holes away from the contact. In this scenario, negatively charged acceptor ions accumulate within the p-type semiconductor to compensate for the electrons that left the metal during the formation of the junction.

Fermi Level Pinning and Surface States

The past several sections have been dedicated to outlining ideal metal-semiconductor contacts; however, joining two dissimilar materials creates an abrupt termination at the interface. Practical complications will now be considered, which have the potential to drastically alter the shape and magnitude of Schottky barriers. While atoms within

the bulk semiconductor share electrons with neighboring atoms in all directions in order to fill or stabilize their orbitals, atoms along the surface do not have neighbors in one direction to facilitate electron sharing (i.e., incomplete covalent bonds). The periodicity or uniformity of the bulk material can be represented as Bloch waves and their motion described via solutions to the single electron Schrödinger equation. Bloch waves are no longer appropriate to describe the energy eigenstates at surfaces due to the termination of the lattice periodicity; however, the Bloch waves from within the lattice extend beyond the surface, where their tails decay exponentially. This perturbation creates surface states at the abrupt interface, which lead to a phenomenon called "Fermi level pinning.

Simply put, surface states are forbidden electronic states created at interfaces due to the abrupt termination of a lattice. These electronic states are only found at the atomic layers immediately adjacent to the interface, and they have a reduced potential relative to those found within the bulk material. Although surface states are often categorized as either Shockley or Tamm surface states, they ultimately describe the same phenomena with differing mathematical approaches. Shockley states are derived from the nearly-free electron model, and are useful for describing metals and small band gap semiconductors. Tamm states arise from the tight-binding model, and are more appropriate for large band gap materials (e.g., semiconductors and transition metals).

Along with the incorporating the influence of surface states into energy band diagrams, an interfacial layer must also be included for a more realistic model. Avoiding the presence of this interfacial layer is incredibly difficult during the deposition of metal onto a semiconductor. This layer is atomically-thin (i.e., on the order of angstroms) and does not prohibit carrier transport, but a potential difference exists across the layer. Figure 3.16 illustrates similar to the scenario described in Figure 3.15b (i.e., metal on n-type semiconductor), but depicts a more detailed and realistic contact

exhibiting rectifying behavior. Figure 3.16 will be used as a visual representation for the following discussion. Here, E_{G} represents the band gap energy, and qV_0 is the built-in potential created when the conduction and valence bands are bent to accommodate the semiconductor Fermi level being pinned to the same level as the metal Fermi level. Electrons must overcome the metal-semiconductor barrier height, Φ_B, to flow from the semiconductor to the metallic contact. That is, Φ_B serves to repel the flow of electrons towards the contact. D_{IS} is the density of surface states along the interface. This value is constant for interfacial surface states below the Fermi level, because this example depicts an n-type semiconductor. As such, the Fermi level is above the neutral interfacial states (Φ_0), and D_{IS} is not constant above E_{F} as these traps consist of surface acceptor sites within the depletion region. The width of the interfacial layer is δ, the potential difference across it is Δ, and the permittivities within the interfacial layer (defined to be vacuum) and the semiconductor are ε_i and ε_s, respectively. The charge density along the interfacial sites (Q_{IL}) and within the depletion region (Q_{DR}) are expressed in Equations 3.53 and 3.54, respectively. An equal magnitude, but opposite in charge or sign, charge density forms along the metal surface (Q_m; Equation 3.55) as well, and is equal to the opposite (i.e., opposite sign

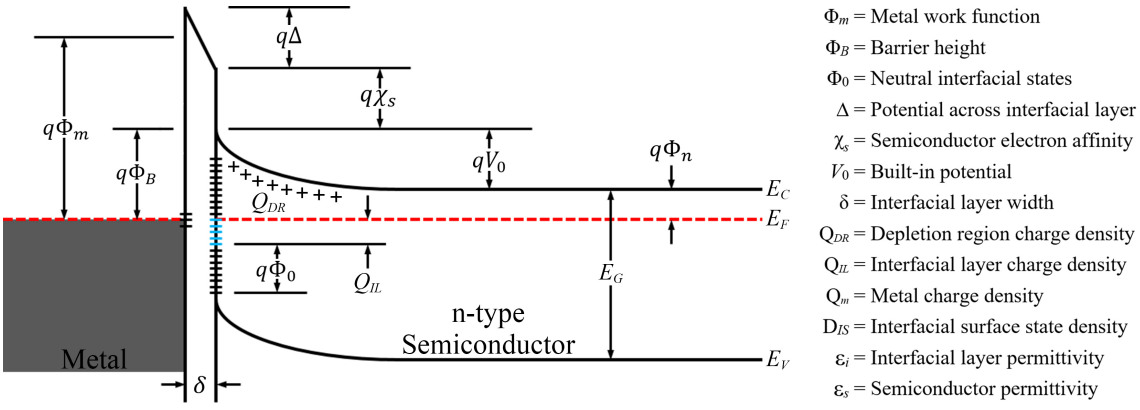

Figure 3.16: Model detailing a rectifying contact with surface states and Fermi level pinning.

or charge) of the sum of the semiconductor interfacial charge densities.

$$Q_{IL} = -qD_{IS}\left(E_{\mathrm{G}} - q\Phi_0 - q\Phi_B\right) \tag{3.53}$$

$$Q_{DR} = \left[2q\varepsilon_s N_{\mathrm{D}}\left(\Phi_B - \Phi_n - \frac{k_{\mathrm{B}}T}{q}\right)\right]^{1/2} \tag{3.54}$$

$$Q_m = -\left(Q_{IL} + Q_{DR}\right) \tag{3.55}$$

The potential across the interfacial layer can be found either numerically by applying Gauss law to Equation 3.55, or analytically by interpreting values Figure 3.16. The two approaches provide the following solutions, respectively

$$\Delta = -\frac{\delta Q_m}{\varepsilon_i} \tag{3.56}$$

$$\Delta = \Phi_m - \left(\chi_s + \Phi_B\right) \tag{3.57}$$

Equating Equations 3.56 and 3.57, and substituting Equations 3.53 and 3.54 for Q_m provides a long and convoluted expression that can be simplified by defining constants c_1, c_2, and c_3. Doing so also provides numerical solutions for the neutral interfacial states (Φ_0) and the density of surface states along the interface-semiconductor boundary

(D_{IS}).

$$c_1 \equiv \frac{2q\varepsilon_s N\delta^2}{\varepsilon_i^2} \tag{3.58}$$

$$c_1 \equiv \frac{\varepsilon_i}{\varepsilon_i + q^2\delta D_{IS}} \tag{3.59}$$

$$\Phi_B = c_2\left(\Phi_m - \chi_s\right) + \left(1 - c_2\right)\left(\frac{E_G}{q} - \Phi_0\right) \equiv c_2\Phi_m + c_3 \tag{3.60}$$

$$\Phi_0 = \frac{E_G}{q} - \frac{c_2\chi_s + c_3}{1 - c_2} \tag{3.61}$$

$$D_{IS} = \frac{\left(1 - c_2\right)\varepsilon_i}{c_2\delta q^2} \tag{3.62}$$

where the constants c_1, c_2, and c_3 contain interfacial properties. c_2 approaches 0 as D_{IS} approaches ∞, which results in fermi-level pinning and is independent of the metal work function. c_2 approaches 1 as D_{IS} approaches 0, which results in an ideal metal-semiconductor contact. Modern substrate cleaning processes produce an interfacial layer thickness (δ) of 4-5 Å, which reduces its permittivity (ε_i) and can be approximated by the permittivity of free space (ε_0). By inspection of Equations 3.60, 3.61, and 3.62, two scenarios emerge for the barrier height.

First, as $D_{IS} \to \infty$, $c_2 \to 0$, which gives

$$q\Phi_B = E_G - q\Phi_0 \tag{3.63}$$

Here, the density of interfacial surface states approaches infinity, and the surface states above the valence band (i.e., the neutral interfacial states, Φ_0) pin the Fermi level at the interface. As seen in Equation 3.63, the barrier height is independent of the metal work function. Instead, it is purely the result of the semiconductor and its surface characteristics. This is an expression for the refined barrier height that represents a more realistic representation than the ideal case discussed previously.

Second, as $D_{IS} \rightarrow 0$, $c_2 \rightarrow 1$, which yields

$$q\Phi_B = q\left(\Phi_m - \chi_s\right) \tag{3.64}$$

In this situation, the density of interfacial surface states approaches zero, and the barrier height becomes a function of the metal work function and the semiconductor electron affinity. Notably, this is the same equation for the ideal scenario described previously in Figure 3.15b.

3.1.8 Heterojunctions

The majority of discussion has been on p-n junctions formed by similar materials with varying doping levels (i.e., homojunctions). Although metal-semiconductor heterojunctions have been described, semiconductor-semiconductor heterojunctions will now be the primary focus. These junctions are the joining of two semiconductor materials with distinct band gap energies. Along with disparate band gaps, the materials will also have different work functions, electron affinities, and ionization potentials. Therefore, band bending brought about from aligning these materials for a continuous Fermi level will create discontinuities in both the valence and conduction bands. It is important to highlight a useful consequence of these discontinuities; namely,

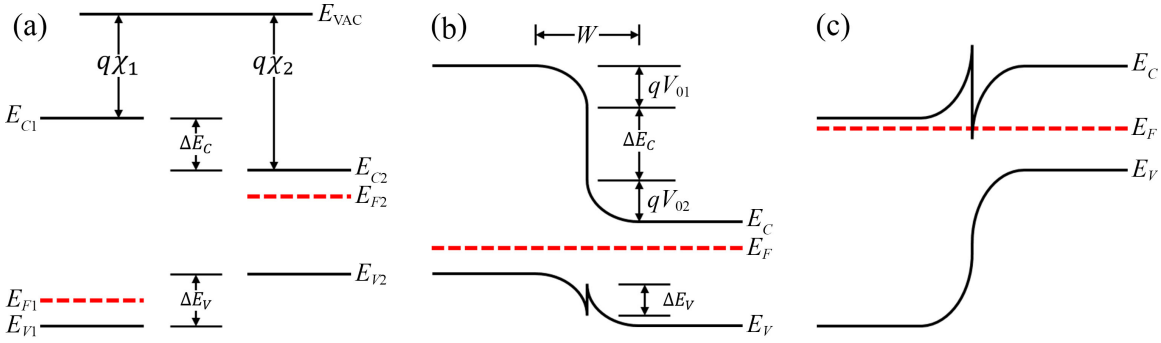

Figure 3.17: Models depicting an ideal heterojunction between wide band gap p-type and narrow band gap n-type semiconductors (a) before and (b) after being interfaced, and (c) an example of a heterojunction between wide band gap and heavily doped n-type (n^+) and lightly doped p-type semiconductors.

the barrier that carriers must overcome to travel in one direction can be engineered to be drastically different than the barrier for the corresponding carriers flowing in the opposite direction. Figure 3.17 illustrates an example of a heterojunction formed by a large band gap p-type semiconductor and a small band gap n-type material.

Ideally, the change in valence band energy levels from one material to the other is the difference of their conduction band energies subtracted from the difference in their band gap energies (i.e., $\Delta E_{\mathrm{V}} = \Delta E_{\mathrm{G}} - \Delta E_{\mathrm{C}}$). Likewise, the difference in conduction band energies can be determined by their respective electron affinities (i.e., $\Delta E_{\mathrm{C}} = q\left(\chi_2 - \chi_1\right)$). The built-in potential is comprised of components from each material as such, $qV_0 = q\left(V_{01} - V_{02}\right)$. The extent of penetration of the depletion region into each material, and the potential at each side of the junction (which sums to the contact potential, V_0) is determined by Poisson's equation (Equation 3.19) by applying the depletion approximation.

Another important point to highlight is hinted at in Figure 3.17c. The discontinuity in the conduction band allows electrons from the large band gap material to become trapped in the potential well, which results in an accumulation of conduction electrons on the opposite side of the junction (i.e., within the smaller band gap semiconductor). The increased conduction band electron concentration raises the Fermi level, potentially to an energy level above the discontinuity. This effect can be seen in Figure 3.17c. These electrons will have heightened mobility because their presence is a result of transfer from the opposing material rather than doping. Increased conduction electron concentration without the associated dopants leads to minimal impurity scattering. Instead, their mobility tends to be dictated by lattice or vibrational scattering (i.e., phonons).

3.2 Carrier-Selective Photovoltaics

Solar cells based on carrier-selective asymmetric heterojunction (CSAH) architectures rely on wide band gap transition metal oxides (TMOs) to produce carrier inversion and selectivity. That is, the emitter in a conventional P-N junction device is replaced with a TMO such that one minority carrier is permitted to transport across the TMO/absorber junction, while the other minority carrier is repelled towards the opposite contact (i.e., rectifying behavior). TMOs must be carefully matched with absorbers in order to create a junction whereby the barrier imposed on the carrier intended to traverse the layer is minimized, while the barrier for the opposite carrier is sufficient (i.e., in height and width) to force them in the opposite direction. The sections below will detail the materials commonly incorporated into CSAH-based devices, and will highlight the implications of various material and fabrication parameters. Namely, transparent conductive oxides (TCOs) and TMOs (serving as contact and emitter layers, respectively) will be outlined, leading to a more specific and in-depth description of the physics governing CSAH photovoltaics.

3.2.1 Transparent Conductive Oxides

Transparent conductive oxides (TCOs) are heavily doped metal oxides with large band gap energies ($E_g \gtrsim 3.4$ eV), causing them to be transparent in the visible regime (300 nm $\lesssim \lambda \lesssim$ 800 nm). These are often degenerately-doped (e.g., $n \geq 10^{20}$ cm^{-3}) with carrier concentrations as high as 10 at% (which far exceeds typical levels for common substrates such as Si and GaAs), and have high concentrations of free electrons in their conduction bands [57]. This, of course, refers to n-type TCOs, which will be the focus of discussion here; however, a brief description of p-type TCOs will also be provided below.

Indium oxide-based (In_2O_3) materials dominate TCO utilization, with indium tin

oxide (ITO) overwhelmingly being the most common. Some others include indium zinc oxide (IZO), indium gallium oxide (IGO), and indium gallium zinc oxide (IGZO). Much of this section will deal with ITO, as it is the favored TCO because it combines the lowest film resistivity with the highest transmission in the visible spectrum. ITO is is a highly degenerate ($n \geq 10^{21}$ cm^{-3}) semiconductor with low resistivity ($\rho \lesssim 1 \times 10^{-4}$ Ω·cm) due to its excess in free conduction band electrons [57]. Free carriers are introduced to In_2O_3 through donor impurities; namely, four-valent substitutional Sn atoms, and oxygen vacancies. Its resistivity is inversely proportional to the product of the carrier density (n) and mobility (μ_n). However, the transmission window is narrowed on the long wavelength tail with excessive conduction band electrons, which leads to an important trade-off between conductivity and long wavelength transparency [57].

A range of alternatives to indium-based TCOs are available, which predominantly focus on zinc oxide-based (ZnO) materials such as aluminum zinc oxide (AZO) and zinc tin oxide (ZTO). Some others include fluorine tin oxide (FTO) and antimony tin oxide (ATO) to name a few. It should be noted that the performance of ZnO is more heavily influenced by oxygen impurities than ITO, making ZnO processing more stringent. Regardless, the attention of researchers and industry alike is drawn primarily to ITO due to the lack of a reliable alternative with comparable performance, despite the rarity of elemental indium [57].

The development of a reliable p-type TCO with comparable performance to that of ITO is an area of extensive research. A 1996 study of $CuAlO_2$ delafossite energized the search for an acceptable n-type counterpart [58]; however, the relatively low carrier concentration and mobility ($p \leq 10^{18}$ cm^{-3} and $\mu < 1$ cm^2/V·s, respectively) has plagued Cu-based solutions. An emphasis on generating p-type ZnO has been prevalent for nearly two decades, as some of its properties would be similar to those of GaAs [57]. Moreover, Mg and Cd dopants can be used to broaden or narrow its band

gap energy, respectively, though none of the p-TCOs have been shown to be reliable or reproducible yet [57]. Fundamentally, the main challenge in creating a comparable high mobility p-type TCO comes back to the presence of oxygen impurities, which often results in a relatively flat valence band density of states and a large effective mass (m_p^*) [57].

The popularity of incorporating TCOs into photovoltaic devices relies on three of their basic attributes; their (1) electrical conductivity, (2) optical transmittance in the visible and near infrared (NIR) regimes, and (3) the cost-efficiency and relative ease with which high-quality films can be repeatedly produced. For the sake of discussion, tin-doped In_2O_3 (i.e., ITO) will be compared with undoped and aluminum-doped ZnO (i.e., AZO).

Electrical Conductivity

Although the level to which a TCO film is structurally ordered (i.e., its crystallinity) can intuitively be mistaken as the limiting factor for carrier mobility, grain boundaries have not been found to be a notable hindrance for electron transport through common TCOs [59]. This can be explained by considering their typical carrier concentration (n), carrier mobility as a function of doping [$\mu(n)$], density of grain boundary traps (N_t), and their Seebeck coefficient (S).

First, some background into the nature and mechanics of grain boundaries within TCO films must be provided. Impurity acceptor atoms coalesce at lattice defects along grain boundaries, which subsequently leads to localized electron trapping. The increase in carrier concentration in these regions reduces the number of electrons within the grain and decreases intra-grain conductivity [57]. Additionally, the accumulation of acceptor states create potential barriers that require electrons to either tunnel through, or be thermionically emitted over, to promote inter-grain transport. The extent to which these barriers are detrimental to long-range conductivity depends on

their height (eV) and width (nm) [57].

Typical carrier concentrations for ITO are $n \geq 5 \times 10^{20}$ cm^{-3} (or even several orders of magnitude higher) and result in resistivities $\rho \leq 5 \times 10^{-4}$ Ω·cm [60]. The degeneracy of these films makes them metal-like, with their Fermi level residing within the conduction band and their carrier concentration being independent of temperature (i.e., thermal generation is reduced, or even negligible). Undoped ZnO is non-degenerate and has carrier concentrations on the order of $\sim 10^{16}$ cm^{-3}, whereas doped zinc oxide (e.g., AZO and ZTO) can reach degenerate levels comparable with ITO [57]. It should be noted that degenerately doped and highly conductive ZnO films have been produced at the laboratory level [61]; however, deposition processes that yield stable and reproducible films have yet to be developed with sufficient throughput for manufacturing feasibility [57].

At such elevated doping levels (e.g., $n \gtrsim 10^{20}$ cm^{-3}), the carrier mobility for TCOs is similar to that for monocrystalline semiconductors [59]. As such, these degenerately doped films promote relatively unimpeded electron tunneling across sufficiently narrow grain barriers found to be less than 1 nm in width. Conversely, decreasing carrier concentration correlates with grain barrier broadening and reduced carrier mobility [59]. The important distinction arises from the disparate carrier concentration values that activate grain barrier scattering for ITO and AZO [62]. Carrier mobility within ITO

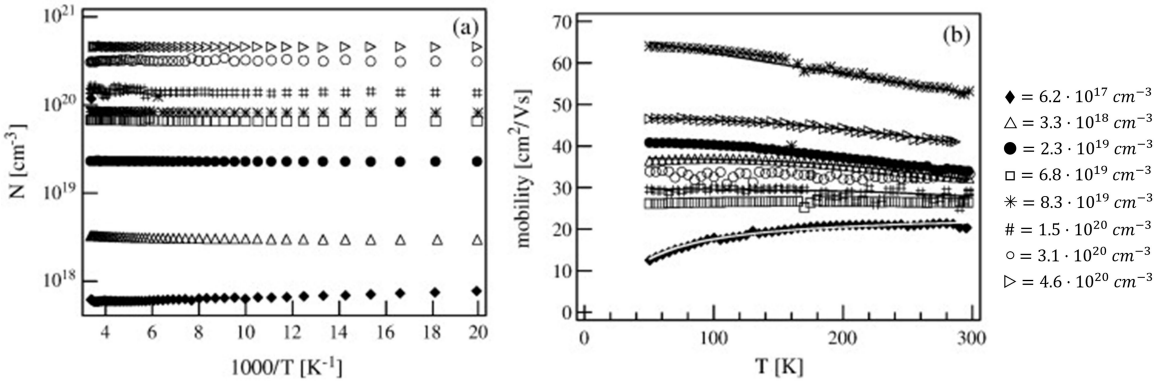

Figure 3.18: Plots showing (a) carrier concentration and (b) mobility of ITO films deposited via sputtering, as a function of temperature [59].

films remains high at doping levels which are several decades below the concentration values at which the electron mobility of AZO begins to diminish. That is, carrier mobility of ITO deposited at room temperature has been shown to be relatively constant down to $n \approx 10^{18}$ cm^{-3}; however, AZO exhibits a substantial decline in mobility at doping levels below $\sim 10^{20}$ cm^{-3} [59]. This is attributed to their notably dissimilar grain boundary trap densities (N_t), which directly influence carrier mobility [62]. Common grain boundary trap density values for ITO are $\sim 1.5 \times 10^{12}$ cm^{-2}, whereas N_t for ZnO and AZO films typically range from 5×10^{12} cm^{-2} and 3×10^{13} cm^{-2} depending on their deposition method (which will be discussed later).

Figure 3.18 shows the carrier concentration and mobility of ITO films deposited via sputtering, as a function of temperature [59]. Recall, the Fermi level of degenerate semiconductors lies within the conduction band, resulting in their carrier concentrations being independent of temperature, as seen in Figure 3.18a . However, carrier mobility as a function of doping [$\mu(n)$] demonstrates a varying effect due to temperature (Figure 3.18b). Interestingly, Figure 3.18b shows that the carrier mobility of ITO with $n \approx 7 \times 10^{19}$ cm^{-3} (i.e., open square symbols) is independent of temperature. That is, the carrier mobility for that particular doping level exhibits no fluctuation as a function of temperature (i.e., a regression of the measurements at that doping level would be a flat, horizontal line). However, carrier mobilities for doping levels above and below $n \approx 7 \times 10^{19}$ cm^{-3} appear to be dependent on temperature. That is, a regression for measured carrier mobilities at doping levels above and below $n \approx 7 \times 10^{19}$ cm^{-3} have nonzero derivatives as a function of temperature [59]. Otherwise stated, distinct regimes for $\mu(T)$ exist at carrier concentrations above and below $n \approx 7 \times 10^{19}$ cm^{-3}. At higher doping levels, $\mu(T)$ decreases more rapidly as carrier concentrations increase, exhibiting metal-like behavior. Conversely, at lower doping levels, $\mu(T)$ increases more rapidly as carrier concentrations decrease (i.e., thermally activated), indicating transport behavior limited by grain barriers [59]. The limitation

on grain boundary scattering for non-degenerate materials follows Maxwell-Boltzmann statistics [57] and is described by

$$\mu_{\text{eff}} = Lq\left(\frac{1}{2\pi m_{\text{n}}^{*} k_{\text{B}} T}\right)^{1/2} \exp\left(\frac{-E_{\text{B}}}{k_{\text{B}} T}\right) \tag{3.65}$$

Similarly, degenerate TCOs obey Fermi-Dirac statistics and can be described by

$$\mu_{\text{eff}} = BT^{\text{-1}} \exp\left(\frac{-E_{\text{a}}}{k_{\text{B}} T}\right) \tag{3.66}$$

where L is the size of the grain, q is electric charge, m_n^* is effective mass, k_{B} is the Boltzmann constant, T is temperature, E_{B} is the potential height of the grain barrier, B is a constant, and E_{a} is the activation energy required to overcome the grain potential barrier. The grain boundary potential height for both scenarios is less than $k_{\text{B}}\,T$, based on plotting $\ln\left(\mu T^{1/2}\right)$ and $\ln\left(\mu T\right)$ versus $\left(k_{\text{B}} T\right)^{-1}$ for non-degenerate and degenerate TCOs, respectively [57].

Carrier mobility in the temperature independent regime varies from approximately 30 - 70 $\text{cm}^2/\text{V}\cdot\text{s}$, and from 24 - 117 $\text{cm}^2/\text{V}\cdot\text{s}$ at carrier concentrations whereby mobility is a function of temperature. Moreover, the grain potential height is $\sim$3 meV, and is therefore unlikely to infringe on inter-grain transport. AZO demonstrates similar trends as ITO, though less pronounced [59].

Optical Transmittance

Figure 3.19a shows transmission (T) and reflection (R) spectra for ITO deposited on a glass substrates with film thicknesses of 40, 110, and 300 nm [63]. The critical values (e.g., short and long wavelength cutoffs, relative reflection and transmission percentages, etc.) will vary based on the TCO and its composition, as well as processing conditions such as deposition technique, temperature, and annealing. However, the general shape of the optical spectra in Figure 3.19a is representative of most TCOs,

and will serve to provide a visualization throughout discussion. Here, Figure 3.19a will be decomposed; important material attributes will be highlighted, along with their symbiotic relationship will electrical properties discussed above.

TCO materials are highly transparent in the visible spectrum due to their large band gap. Figure 3.19b shows the optical band gap for 40, 110, and 300 nm-thick ITO films to be 3.99, 4.09, and 4.18 eV, respectively [63]. ITO exhibits approximately 80% optical transmission between 400-700 nm [57]. Oscillations in the transmission and reflection spectra are interference effects due to the nature of thin films. Photons are absorbed by the semiconductor at high energies (i.e., short wavelengths) above the band gap energy between 3-4 eV (i.e., approximately 300-400 nm), resulting in electron excitation from the valence band to conduction band. The transmission begins to decrease around 1,000 nm, and the reflection begins to increase at ∼1,500 nm. The reduced optical performance at long wavelengths is a result of oscillations within the conduction band [57]. That is, the excitation of plasma oscillations or plasmon quasi-particles. The wavelength at which plasmon absorption is maximum (λ_P) is proportional to the electron concentration within the conduction band (i.e., $\lambda_P \propto n^{-1/2}$) [57]. Therefore, the plasma oscillation wavelength is reduced and optical absorption is increased at high doping levels.

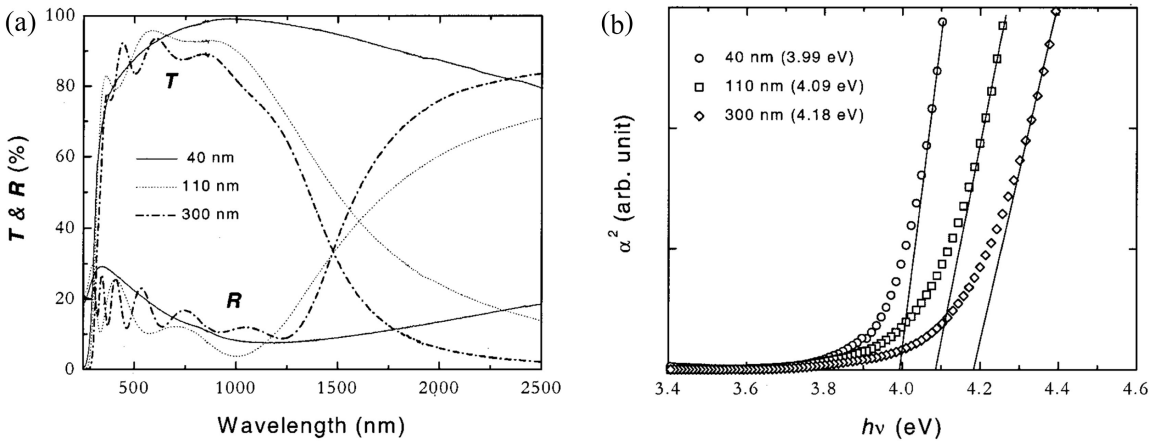

Figure 3.19: Plots showing (a) transmission and reflection spectra, and (b) optical band gap for ITO films with thicknesses of 40, 110, and 300 nm [63].

Film Deposition and Fabrication

In 1966, ITO was realized as an excellent transparent conductor with low resistivity [64], leading to many research groups and corporations worldwide to focus on its development. A list of ITO deposition techniques and their resistivities include: spray pyrolysis (2×10^{-4} Ω·cm) in 1968 [65], direct current (DC) diode sputtering with sintered oxide target (1.77×10^{-4} Ω·cm) in 1972 [66], chemical vapor deposition (CVD; 2.2×10^{-4} Ω·cm) in 1975 [67], and thermal evaporation (2×10^{-4} Ω·cm) in 1975 [68]. The rapid development of manufacturing-level deposition processes for all mainstream methodologies in less than a decade demonstrates the overwhelming demand for such a material. Today, the highest quality ITO films are deposited via the physical vapor deposition (PVD) techniques e-beam evaporation or magnetron sputtering, both of which can produce films with resistivity ρ = 1-2 $\times$ 10^{-4} Ω·cm [57].

Reactive sputtering can be used to lower the carrier concentration by incorporating low levels of reactive oxygen species (e.g., 1-4 sccm) to the inert sputtering gas (Ar). While the carrier mobility for ITO has been shown to be relatively resilient to this effect down to $n \approx 10^{18}$ cm^{-3}, AZO exhibits a significant reduction in mobility if carrier concentrations drop below 10^{20} cm^{-3} [59]. For most sputtering techniques (e.g., magnetron or diode, DC or RF, and for frequencies at both 13.56 and 27.12 MHz), trap densities (N_t) increase with the plasma discharge voltage (V_{DC}), and by extension carrier mobility is therefore inversely related to V_{DC}. Moreover, the reactive oxygen species become highly energetic based on the potential difference between the target and sample [59]. To that end, thermalization due to the reduced cross-sectional collision area for highly energetic ions should be considered at processing pressures over approximately 35 mT (i.e., ∼5 Pa).

As already stated, the as-deposited film stoichiometry can be tuned via the inclusion of oxygen during the sputtering process. Interestingly, low oxygen partial pressures (F_{O_2}) result in opaque ITO films that are metal-rich, and exhibit almost paradoxically

low carrier mobilities less than 5 $cm^2/V{\cdot}s$ with relatively high doping levels [59]. While the layer remains opaque, increasing F_{O_2} serves to raise n without improving carrier mobility. The ITO becomes transparent as the oxygen partial pressure increases to the level such that the carrier concentration is $\sim 5 \times 10^{20}$ cm^{-3}, at which point the mobility increases significantly to approximately 40 $cm^2/V{\cdot}s$ [59].

Deposition and annealing temperatures play an un-intuitive role in the resulting ITO film, particularly considering the material starts showing crystallinity at a relatively low temperature ($T \gtrsim 150$ °C) [69]. That is, ITO films deposited at elevated temperatures have drastically disparate morphologies than those that were deposited at room temperature and then annealed at the deposition temperature of

Table 3.1: Table showing deposition parameters, post-deposition parameters, sheet properties, and surface roughness for amorphous ITO (a-ITO), amorphous ITO with small amounts of crystalline sites (a+p-ITO), randomly oriented polycrystalline ITO (p-ITO), polycrystalline ITO with grains oriented along the <111> direction (p'-ITO), and polycrystalline ITO with grains oriented along <100> direction (p"-ITO) [69].

	a-ITO	**a+p-ITO**	**p-ITO**	**p'-ITO**	**p''-ITO**
Deposition parameters					
Substrate temperature [°C]	Ambient	Ambient	Ambient	200	200
Working pressure [Pa]	0.3	0.3	0.3	0.6	0.3
Reactive gas [%]	H_2 (3.9)	-	H_2 (3.9)	O_2 (2.0)	O_2 (0.8)
Post-deposition parameters					
Annealing temperature [°C]	-	-	200	-	-
Atmosphere, duration	-	-	air, 1 hr	-	-
Sheet properties					
ρ_{spec} [μΩ·cm]	1460	540	220	200	150
T_{film} [%] @ 550 nm	84	89	92	93	92
$\delta\varepsilon$ / δt [nm/min]	598	100	38	25	26
σ [Mpa]	-220	a	+280	-350	-310
Surface roughness					
RMS [nm]	~1.2	a	~1.1	~3	< 2.6
R_{max} [nm]	~5.6	a	~5.3	~13	~11

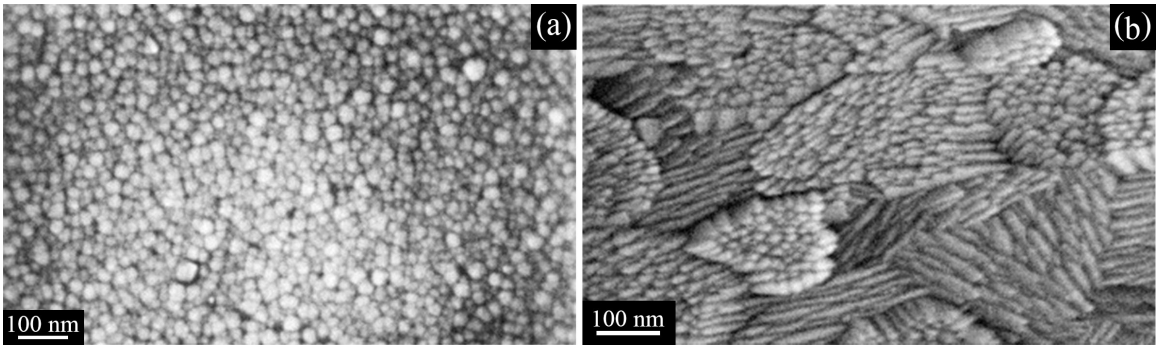

Figure 3.20: Top-view SEM images of ITO deposited (a) at ambient temperature followed by a 1 hour annealing step at 200 °C, and (b) at 200 °C with no subsequent annealing step [69].

the first sample. For example, Table 3.1 provides extensive material and experimental information for a temperature-dependent ITO study [69]. Films were deposited at room temperature and 200 °C, and comparisons were made with post-deposition anneals ranging in temperature from 150 °C to 250 °C. ITO layers are defined as such: a-ITO represents amorphous, a+p-ITO represents amorphous with small amounts of crystalline appearance, p-ITO represents randomly oriented polycrystalline, and p'-ITO and p"-ITO represent polycrystalline films with grains oriented in the <111> and <100> directions, respectively.

Figure 3.20 shows top-view SEM images of two separate ITO films deposited under similar conditions (e.g., substrate, sputter gas flows, and both used DC magnetron sputtering), except temperature [69]. ITO was deposited in at room temperature and subsequently annealed at 200 °C for 1 hour in air (p-ITO; panel a), and a similar layer was deposited at 200 °C with the grains preferentially oriented in the <111> directions (p"-ITO; panel b).

Figure 3.21 shows a set of AFM scans demonstrating ITO films deposited at room temperature (a-ITO; panel a) and subsequently annealed at 200 °C for 1 hour (p-ITO; panel b), and layers deposited at 200 °C with grains oriented along <111> and <100> directions (p'-ITO and p"-ITO; panels c and d, respectively) [69]. Scans were performed in tapping mode, and cover an area of 1 × 1 μm^2. Figure 3.21b

indicates an increase in the cluster packing density with an anneal step; that is, annealing the amorphous film smoothed the as-deposited clusters into randomly oriented grains. Panels c and d highlight the formation of distinct bimodal clusters when ITO is deposited along particular crystallographic directions and above the crystalline activation temperature.

Figure 3.22a shows a set of glancing incident X-ray diffraction (GIXRD) spectra for the different ITO film, and Figure 3.22b tracks the evolution of material resistivity as amorphous layers are subjected to elevated annealing temperatures for extended periods [69]. For all three annealing temperatures (i.e., 150, 200, and 250 °C), the resistivity was dramatically reduced within the first five minutes. Notice the resistivity for 150 °C anneals remains well above the others over the course of two hours. The crystalline activation temperature for amorphous ITO is approximately 150 °C, therefore some contribution from both amorphous and crystalline ITO should be expected. However, at annealing temperatures of 200 and 250 °C, the layers should become more crystalline and do so more rapidly [69]. The low resistivity (hence, high conductivity and mobility) for crystalline ITO supports the model that grain boundaries do not impinge on carrier mobility due to the potential barriers having minimal width and especially height (*vide supra*).

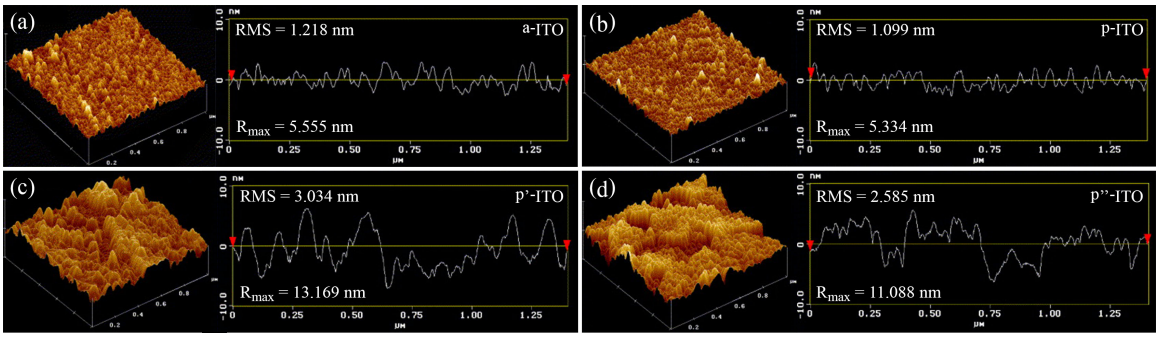

Figure 3.21: AFM scans showing (a) a-ITO deposited at ambient temperature, (b) p-ITO formed after annealing a-ITO for 1 hour at 200 °C, (c) p'-ITO deposited at 200 °C, and (d) p"-ITO deposited at 200 °C [69].

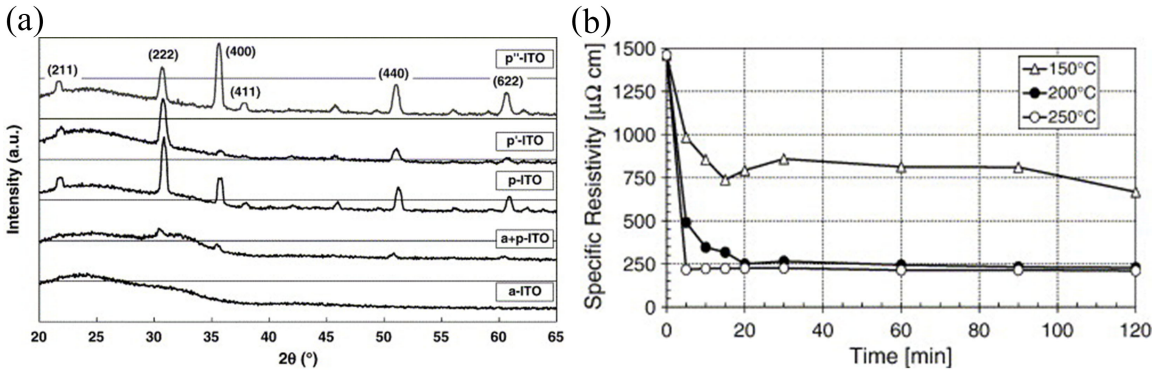

Figure 3.22: (a) glancing angle XRD spectra showing the crystalline structure for polycrystalline ITO formed by annealing amorphous ITO for 1 hour at 200 °C and by depositing ITO at 200 °C, and (b) film resistivity of amorphous ITO annealed at various temperatures [69].

3.2.2 Transition Metal Oxides

Oxides that form on transition metals are referred to as transition metal oxides, or TMOs. These are large band gap semiconductors ($E_G \geq 3$ eV) with high carrier concentrations (e.g., $n \geq 10^{18}$ cm^{-3}) [70]. While this definition may seem straightforward and obvious, the physics behind TMOs is unexpectedly complex and research in this field dates back almost a century. Transition metals are typically considered to be d-block elements, or those with incomplete d-orbitals (i.e., elements exhibiting properties transitioning from s to p orbitals) [71]. With several minor exceptions based on which definition of "transition metal is used, most elements within Group 4 through 11 (not to be confused with the semiconductor physics nomenclature for groups) qualify as transition metals. Titanium dioxide (TiO_2) and copper oxide (Cu_2O) are the extremes of the 3d TMOs, and are well known as n-type and p-type materials, respectively [72].

Titanium dioxide will be considered in detail, including its optical and electrical properties. The anatase, rutile, and brookite phases of TiO_2 are typically the main considerations due to their crystallinity (as seen in Figure 3.24); however, the amorphous and anatase phases will be the primary focus here due to the relatively

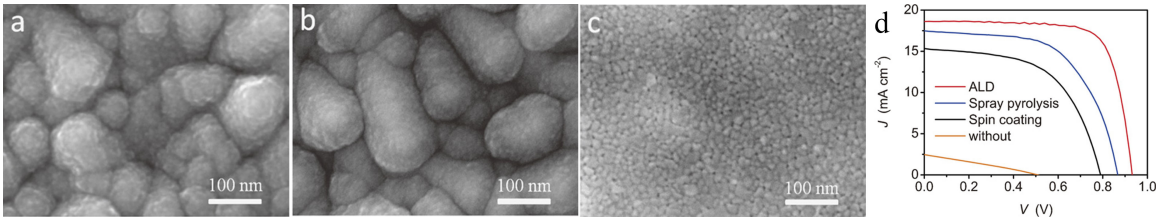

Figure 3.23: Top-view SEM images of 50 nm-thick TiO_2 deposited by (a) ALD, (b) spray pyrolysis, and (c) spin coating, and (d) J-V curves for perovskite solar cells with TiO_2 deposited by various techniques [73].

low thermal budget for deposition [72, 75]. It is difficult to find comprehensive data for a particular TiO_2 film, because a wide variety of deposition and post-deposition processes can drastically alter its properties [73, 76–80]. This is due to the very nature of the oxide, which is highly dependent on chemical bonding and oxygen vacancies [70]. For example, sputtering and atomic layer deposition (ALD) at a constant temperature will yield distinct films, and even utilizing various ALD precursors [e.g., H_2O and $TiCl_4$ [78], titanium isopropoxide (TTIP) [77, 80], wet or H_2O-based tetrakis-dimethylamido titanium (TDMAT) [73, 76, 79], and dry or O_3-based TDMAT [75]] results in varied deposition rates and TiO_2 layers with disparate optical and electrical characteristics. For example, Figure 3.23 shows an example of depositing TiO_2 using various deposition techniques [73]. The average thickness of each film is approximately 50 nm,

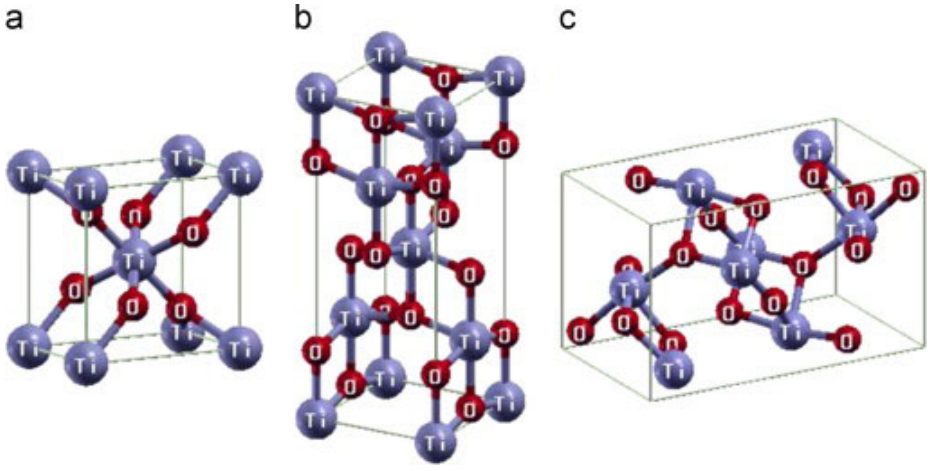

Figure 3.24: Models depicting the crystal structure of the (a) rutile, (b) anatase, and (c) brookite TiO_2 phases [74].

which was deposited via ALD, spray pyrolysis, and spin coating in panels a, b, and c, respectively. Figure 3.23d demonstrates the influence these techniques can have on the J-V characteristics of a solar cell.

Optical Properties

Figure 3.25 shows absorbance and transmittance spectra for various titanium dioxide films. Figure 3.25a represents absorbance spectra of TiO_2 layers deposited via ALD (H_2O and TDMAT precursors) at 75 °C with thickness ranging from 2 - 10 nm [76]. The stack of Al_2O_3 and FTO underneath the TiO_2 were held constant to determine the affect of varying the TiO_2 thickness. The maximum absorbance (A_{max}) increases from film thicknesses of 2 nm to 5 nm, and the wavelength at which A_{max} occurs (λ_{max}) dramatically blue-shifts from 481 to 451 nm for the 2 and 5 nm thick layers, respectively. The shift in λ_{max} is much less pronounced (7 nm) for thicknesses between 5 and 10 nm; however, A_{max} steadily decreases over that same range.

Figure 3.25b shows the transmittance spectra for TiO_2 layers deposited by ALD (H_2O and TTIP precursors) onto FTO at 150 °C with thicknesses of ranging from 68 - 368 nm, and the pure FTO spectrum is provided as well [80]. The transmittance of pure FTO is over 98% between in the visible regime (i.e., ≈450-900 nm), and the TiO_2

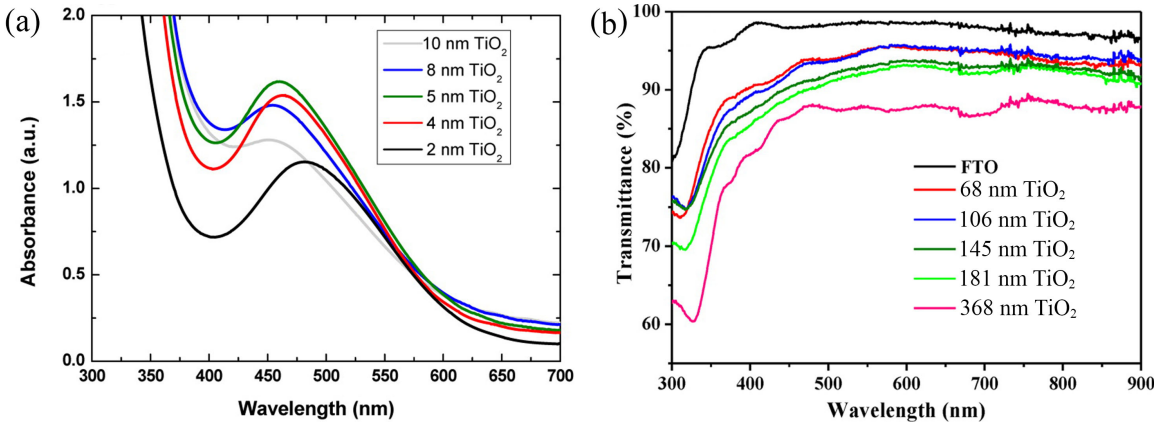

Figure 3.25: (a) absorbance spectra for thin TiO_2 films deposited via ALD onto AL_2O_3 [76], and (b) transmittance spectra for TiO_2 deposited onto FTO/glass via ALD [80].

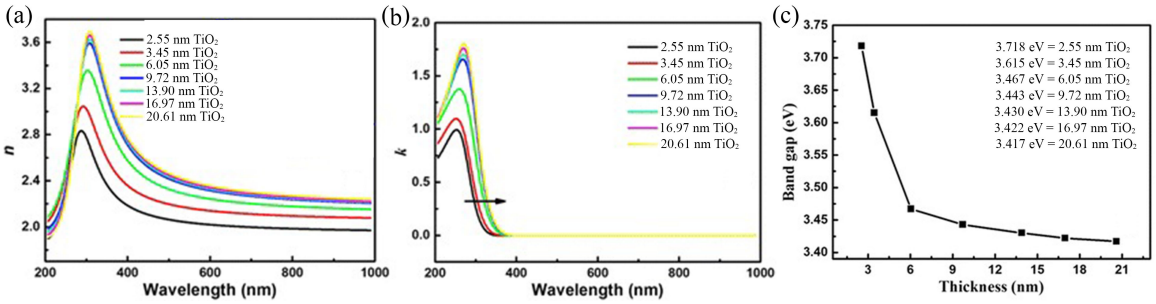

Figure 3.26: (a) refractive index and (b) extinction coefficient spectra for TiO_2 deposited onto Si via ALD, and (c) the band gap energy of the various TiO_2 films [77].

spectra would intuitively be expected to plummet due to such thick layers. While the transmittance indeed reduces with TiO_2 thickness, the value does not dramatically decrease until after a thickness of 181 nm.

Figure 3.26 shows refractive index (n) and extinction coefficient (k) spectra for TiO_2 films deposited via ALD (H_2O and TTIP precursors) onto Si(100) wafers at 80 °C with thicknesses ranging from 2.55 to 20.61 nm [77]. Figure 3.26a shows that n increases with TiO_2 thickness, and the peaks also shift to longer wavelengths (i.e., red-shift) as the TMO thickness increases. Similarly, panel b indicates a similar peak intensity increase as well as red-shift, which indicates that the optical band gap decreases as the TiO_2 becomes thicker, as seen in Figure 3.26c.

Film Morphology

Figure 3.27 shows a set of AFM micrographs (produced in tapping mode) detailing a scanning area of 5×5 μm^2 for TiO_2 layers deposited via ALD (H_2O and TTIP precursors) onto Si(100) wafers at 80 °C with thicknesses ranging from 2.55 to 20.61 nm [77]. The RMS surface roughness varies from 0.03 nm to 1.23 nm for TMO thicknesses of 2.55 nm and 20.61 nm, respectively, as seen in Figure 3.27h. At a deposition temperature of 80 °C, all of these layers should be purely amorphous and exhibit no crystallinity. That is, TiO_2 films deposited via ALD have been shown to exhibit no signs of crystallinity below a deposition temperature of 150 °C [78, 81–83].

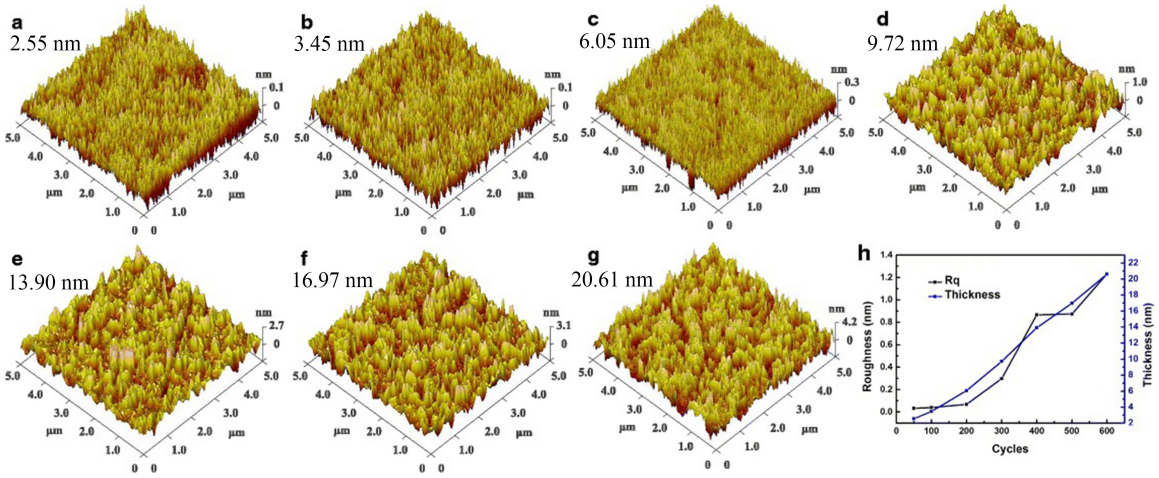

Figure 3.27: AFM scans showing qualitative surface roughness for TiO_2 films deposited onto Si via ALD with thicknesses of (a) 2.55 nm, (b) 3.45 nm, (c) 6.05 nm, (d) 9.72 nm, (e) 13.90 nm, (f) 16.97 nm, and (g) 20.61 nm, and (h) a plot illustrating a trend of increased surface roughness with film thickness [77].

Figure 3.28 shows a set of XRD patterns for various TiO_2 films. Panel a represents TiO_2 layers deposited by ALD (H_2O and $TiCl_4$ precursors) onto Si(100) wafers at 38, 50, 75, 100, 125, and 150 °C [78]. The TiO_2 begins to show crystalline behavior at a deposition temperature around 150 °C as the anatase (101) peak becomes discernible. However, the spectra for the deposition temperatures below 150 °C indicate the films are purely amorphous, as expected. This highlights another advantage of utilizing ALD, which is that other low temperature deposition techniques require a post-deposition annealing step up to 300 - 500 °C to yield crystalline behavior [84].

Figure 3.28b shows a set of XRD spectra for TiO_2 films deposited via ALD (H_2O and TTIP precursors) onto Si(100) substrates at 190 °C [79]. The as-deposited films are amorphous, and were subjected to 400 and 600 °C post-deposition anneals. Upon annealing, the TMO layers begin to show signs of crystallinity, as evident by the appearance of the anatase (101) peak. Several values for a critical thickness whereby TiO_2 will remain amorphous even at elevated deposition temperatures have been proposed. Thicknesses of 5 to 15 nm have been reported to show no sign of crystallinity at deposition temperatures upwards of 300 °C [78, 85].

3.2.3 Physics of CSAH Devices

The path to our modern concept of carrier-selective asymmetric heterojunction (CSAH) photovoltaics began in 1974 with the presentation of a-Si:H/c-Si (i.e., hydrogenated amorphous silicon/crystalline silicon) heterostructures [86]. The first silicon heterojunction (SHJ) solar cell, known as the "Honeymoon" cell, was reported in 1983 [87], which consisted of tandem device with an a-Si:H/poly-Si bottom cell that yielded 12.37% power conversion efficiency (PCE; η). Progressive improvements were made towards more efficient SHJ cells, and in 1992 a modified SHJ device was reported with a thin and undoped a-Si:H buffer layer sandwiched between the doped a-Si emitter and c-Si absorber layers [88]. This device, known as the heterojunction with intrinsic thin-layer (HIT), provided 14.5% PCE, and regular advancements on the SHJ architecture continue to this day.

Improving todays silicon photovoltaics comes down to considering a dollars-per-watt (DPW; \$/W) metric. While marginal increases in PCE continue to be reported due to innovative device designs, the primary focus is now on reducing the fabrication costs without sacrificing PCE or reliability. Initially, cost-reduction was promoted by decreasing solar cell thickness [90], thereby reducing the cost of material. However,

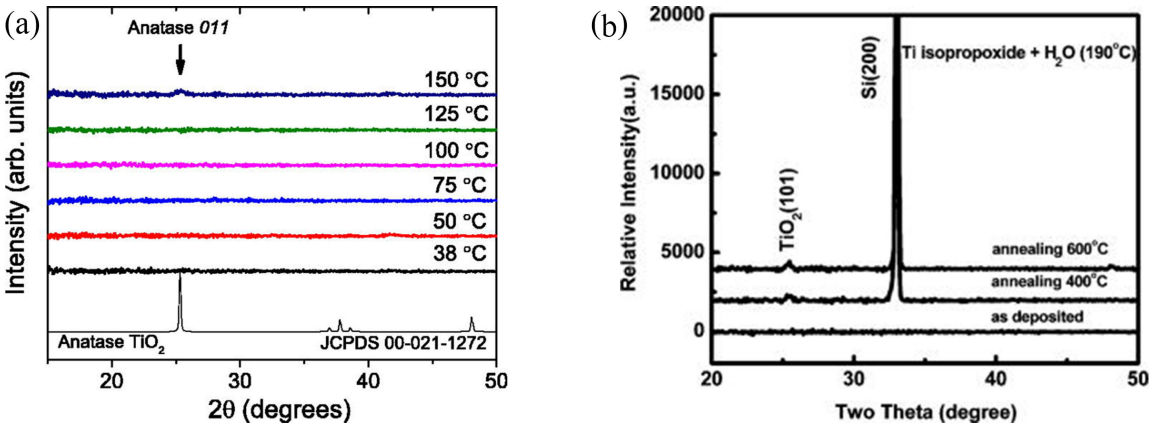

Figure 3.28: (a) gracing incidence XRD spectra for TiO_2 deposited via ALD at various temperatures [78], and (b) XRD spectra for TiO_2 films deposited via ALD at 190 °C with subsequent anneals at various temperatures [79].

conventional device processing requires a relatively high thermal budget, which became a limiting factor for device thinning due to wafer bending and lattice strain at elevated temperatures [91]. In the past several decades, silicon photovoltaics have shifted from traditional p-n junctions towards SHJ designs, as the latter allows for processing temperatures less than 200 °C [92, 93] and wafer thinning below 100 μm [91]. The highest Si-based PCE (not under concentrated illumination) was reported in 2017, which utilized a SHJ-based device with an interdigitated back contact (IBC) and provided 26.3 ± 0.5% PCE [89]. A cross-sectional schematic, light I-V curve, and QE spectra for this silicon HJ-IBC device can be seen in Figure 3.29.

As some researchers continue to find small though nevertheless groundbreaking PCE improvements via clever design modifications [e.g., passivated emitter and rear

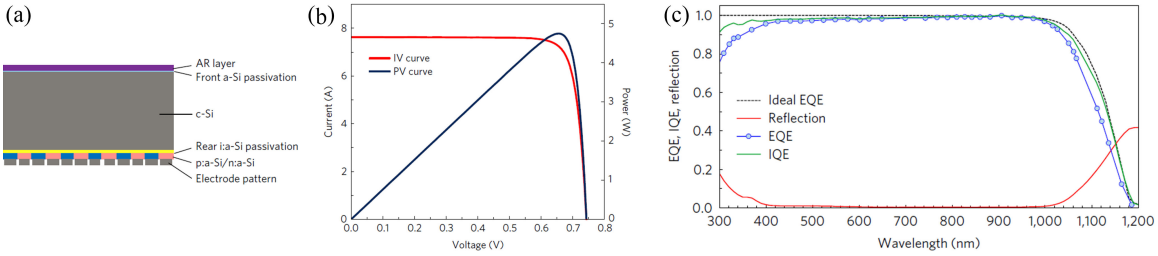

Figure 3.29: (a) cross-sectional schematic of the silicon heterojunction (SHJ) with interdigitated back contact (IBC), and (b) current-voltage (I-V; red curve) and power-voltage (P-V; blue curve), and (c) quantum efficiency and reflection spectra for the SHJ-IBC device [89].

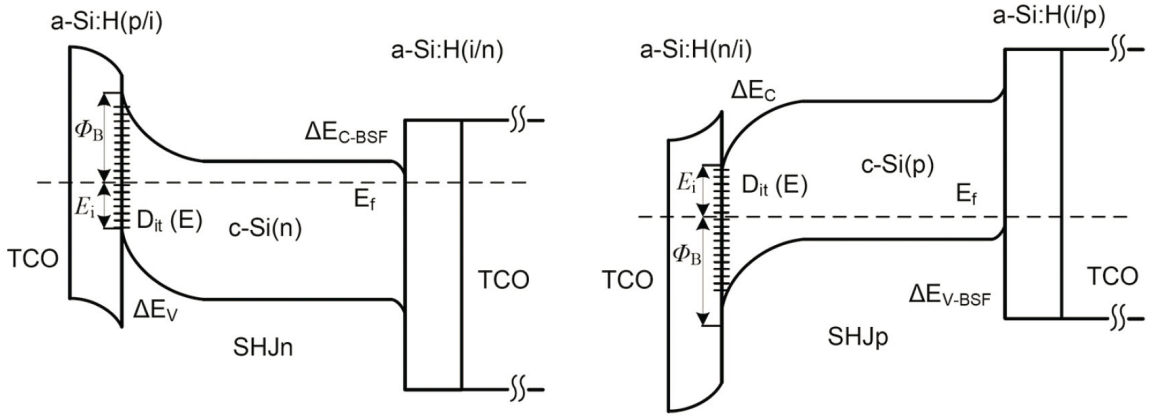

Figure 3.30: Band diagrams for (left) n-SHJ and (right) p-SHJ structures with rectifying junctions [91].

cell (PERC) [94], passivated emitter with rear locally diffused (PERL) [95], and HJ-ICB], others are exploring alternative device structures that allow for cheaper and simplified fabrication processes. Notably, replacement of the standard a-Si:H emitter by transition metal oxides (TMOs) has become an increasingly popular approach for improving the \$/W metric [96]. TMOs are advantageous in that they have large band gaps which reduces parasitic absorption in the emitter, and they have been shown to have simple and low temperature deposition capabilities allowing for a reduced thermal budget [91, 96]. Such design alternatives will be the focus of discussion in upcoming sections; for now, a detailed overview of the fundamental physics behind SHJ mechanics will be provided, which will later be extended to non-SHJ-based architectures. It should be noted that the majority of remaining discussion in this section will be based on simulated results to provide ideal visualizations of parameter dependences that would otherwise be impractical to demonstrate (e.g., precisely varying only the density of surface defect states along an interface). Moreover, an emphasis will be given on various SHJ attributes, and the influence they posses on V_{OC} (and - ultimately - η) per the following equations

$$V_{\mathrm{OC}} = \frac{\Phi_{\mathrm{B}}}{q} - \frac{nk_{\mathrm{B}}T}{q}\ln\left(\frac{qN_{\mathrm{V}}S_p}{J_{\mathrm{SC}}}\right) \tag{3.67}$$

$$V_{\mathrm{OC}} = \frac{\Phi_{\mathrm{B}}}{q} - \frac{nk_{\mathrm{B}}T}{q}\ln\left(\frac{qN_{\mathrm{C}}S_n}{J_{\mathrm{SC}}}\right) \tag{3.68}$$

where Φ_{B} is the barrier height, n is ideality, and S is the interface recombination velocity [91].

Figure 3.30 shows band diagrams for n-SHJ and p-SHJ, where D_{it} is the interface defect density [91]. As seen previously, an interfacial inversion layer is formed at the a-Si:H(i)/c-Si heterojunction, and the band bending can be expressed as $E_{\mathrm{i}} = E_{\mathrm{C}} - E_{\mathrm{F}}$. The front a-Si:H/c-Si interface plays a crucial role in the performance of SHJ devices, as the relative band gap energies, electron affinities, etc., create defect states and form

valence and conduction band discontinuities that affect carrier transport across the interface [91, 97]. A variety of parameters will now be examined that influence these band diagrams and, therefore, device performance, including: defect states at the front a-Si:H/c-Si interface, band bending at the front a-Si:H/c-Si interface, an a-Si:H(i) passivation layer at the front a-Si:H/c-Si interface, alternative materials to create carrier inversion, and detrimental Schottky barrier formation at the front TCO/a-Si:H interface.

Defect States at the Front a-Si:H/c-Si Interface

The influence of the interface defect or surface state density (D_{it}) on the inversion layer and the interface or surface recombination will be considered first. Figure 3.31a shows the dependence of V_{OC}, and therefore η, on D_{it} for n-SHJ (curves with closed squares) and p-SHJ (curves with open circles) [91]. Device performance is inversely related to the density of interface defects, and the band diagrams in Figure 3.31b for p-SHJ will help explain the relationship between carrier recombination and defect states. Extreme values for D_{it} were chosen for comparison. The red curve represents the lower limit at $D_{\mathrm{it}} = 10^9$ cm^{-2}, which exhibits rectifying behavior due to the accumulation of

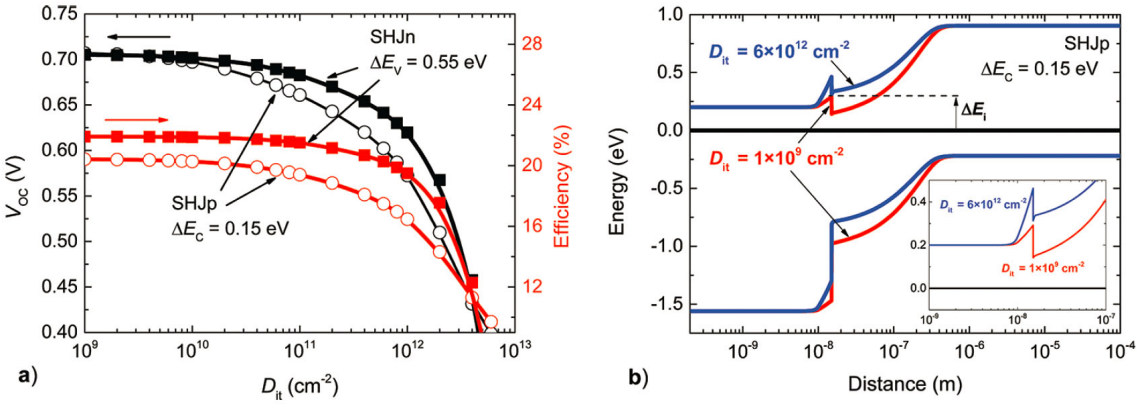

Figure 3.31: (a) V_{OC} and efficiency (η) dependence on the interface defect density (D_{it}), and (b) band diagrams for two disparate D_{it} values. The inset shows the influence on carrier inversion (i.e., the distance change between the conduction band and Fermi level at the heterointerface) [91].

positively charged donor ions and negatively charged acceptor ions on the a-Si:H and c-Si sides of the interface, respectively [98]. The distinct semiconductor materials that make up SHJs have highly disparate doping levels, leading to the depletion region extending further into the c-Si (and a greater diffusion voltage, V_{diff}) than in the a-Si:H. Energy band discontinuities are formed based on the dissimilar materials, and an inversion layer is created due to minority electrons accumulating on the c-Si side of the junction [97]. For high carrier inversion, as seen in the red curves, the concentration of minority electrons is much higher than that for majority holes within the c-Si. The electrons have a high probability of either being thermally emitted over the barrier, Φ_{B}, or tunneling through it. This, along with the highly disparate concentration of carriers, promotes conduction electrons to flow freely towards the front contact with little recombination occurring at the interface [99].

For systems with a much higher D_{it} (blue curves), the interface defects serve as trap states for minority electrons and impede the inversion process. That is, the relatively high concentration of trapped electrons attenuates the exchange of carriers and reduces the depletion width into the c-Si. Otherwise stated, the effects noted for the low D_{it} scenario are dampened, and the built-in separation of minority electrons and majority holes is less pronounced [91]. Furthermore, this leads to a reduced electric field and barrier height, which increases the probability of majority hole diffusion and recombination along the interface [99].

Band Bending at the Front a-Si:H/c-Si Interface

As discussed above, the nature of SHJs (i.e., a junction of dissimilar materials) creates an energy band discontinuity and forms a carrier inversion layer that results in an accumulation of minority carriers on the c-Si side of the metallurgical junction (e.g., minority electrons for p-SHJ). Figure 3.32a shows the V_{OC} dependence on the conduction band offset (ΔE_{C}), for p-SHJ, by varying the density interface states (i.e.,

D_{it} values of 10^{10}, 5×10^{10}, 10^{11}, and 5×10^{11} cm^{-2}) [91]. V_{OC} tends to increase with ΔE_{C}, which would seem intuitive because band bending was a symptom of the formation of a carrier inversion layer. The density of surface states can have a dramatic effect on this dependence. The conduction band offset varies little for the lowest concentration of interface defects (black curve; $D_{\mathrm{it}} = 10^{10}$ cm^{-2}), while the opposite extreme (purple curve; $D_{\mathrm{it}} = 5{\times}10^{11}$ cm^{-2}) has a much more pronounced influence.

Since the conduction band offset, and therefore the V_{OC}, varies the most for higher D_{it}, the highest density will be used for a band diagram analysis in Figure 3.32b. Two disparate ΔE_{C} values were chosen for comparison, 0.10 eV (blue curve) and 0.30 eV (red curve). Band bending on the c-Si side of the junction increases with the conduction band offset due to higher carrier inversion. Similar to the dependence purely on D_{it}, larger ΔE_{C} causes an accumulation of positively charged donor ions and negatively charged acceptor ions on the a-Si:H and c-Si sides of the interface, respectively [98]. The depletion width into the c-Si is extended, and the electric field and barrier height becomes more pronounced. High concentrations of minority electrons can pass the barrier and reach the front contact with a relatively low probability of recombining with a majority hole due to their low concentration [91]. While the V_{OC} dependence on ΔE_{C} is informative, aiming to tune the performance of a device in this fashion would be impractical. The band alignment can be adjusted by varying the hydrogen within the a-Si:H film [100]; however, the relative conduction band alignment can be offset for a-Si:H(n)/c-Si(p) heterojunctions by less than 0.30 eV. Therefore, a more feasible approach to maximize the V_{OC} for SHJ devices is by minimizing the surface state density along the interface.

a-Si:H(i) Passivation Layer at the Front a-Si:H/c-Si Interface

It has been established that the most feasible method for improving carrier inversion is by reducing the concentration of surface states along the interface. The a-Si:H emitter layer is plagued by an abundance of dangling bonds and lattice defects [101], which serve to increase D_{it}. This can be remedied with the introduction of a passivation layer between the doped a-Si:H and c-Si; namely, a thin a-Si:H(i) layer with a significantly

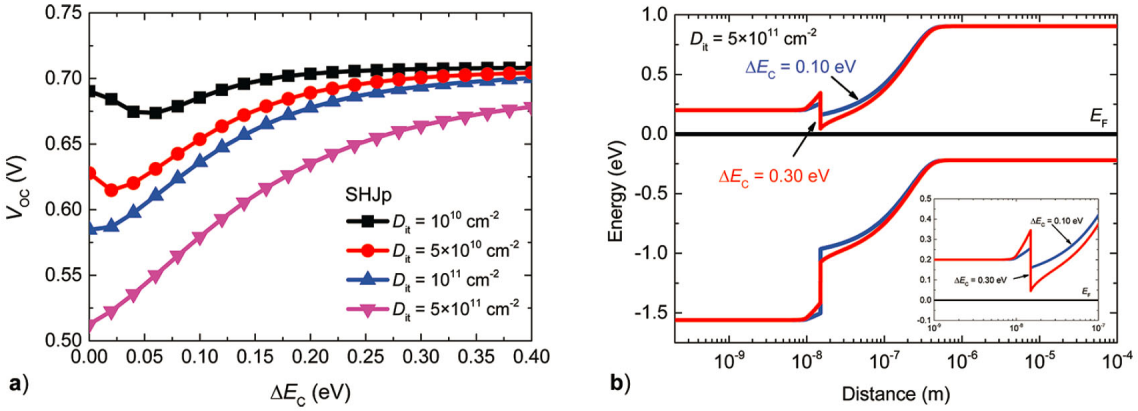

Figure 3.32: (a) V_{OC} as a function of the change in conduction band energy (ΔE_{C}) by varying the interface defect density (D_{it}), and (b) band diagrams for two disparate ΔE_{C} values where $D_{\mathrm{it}} = 5 \times 10^{11}$ cm^{-2}. The inset shows the influence on carrier inversion (i.e., the distance change between the conduction band and Fermi level at the heterointerface) [91].

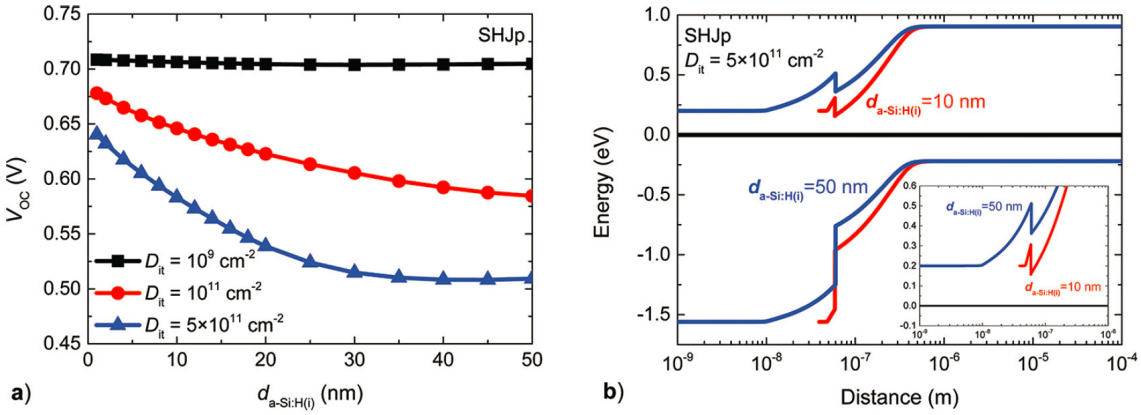

Figure 3.33: (a) V_{OC} as a function of the passivation layer [a-Si:H(i)] thickness for various interface defect densities (D_{it}), and (b) band diagrams for two disparate passivation layer thicknesses and D_{it}=5 $\times$ 10^{11} cm^{-2}. The inset shows the influence on carrier inversion (i.e., the distance change between the conduction band and Fermi level at the heterointerface) [91].

lower defect density (approximately 4×10^{21} m^{-3}) [102]. A careful trade-off must be considered regarding the a-Si:H(i) thickness ($d_{\text{a-Si:H(i)}}$). Passivation increases with $d_{\text{a-Si:H(i)}}$ and improves device performance; however, parasitic resistance losses also increase with the passivation layer thickness, which results is detrimental to fill factor and PCE [103].

Figure 3.33a shows the influence $d_{\text{a-Si:H(i)}}$ has on the V_{OC} of p-SHJs, with three interface defect densities chosen for demonstration (i.e., D_{it} values of 10^9, 10^{11}, and 5×10^{11} cm^{-2}) [91]. The dependence on the passivation layer thickness varies heavily on the concentration of interface states. V_{OC} for the lowest D_{it} value (black curve) appears to be practically independent of the passivation layer thickness, or even if a passivation layer is present. As the purpose of a passivation layer is to decrease surface states, it is reasonable that a doped a-Si:H layer with a low concentration of interface states would benefit less from passivation. Almost paradoxically, V_{OC} decreases with passivation for the higher D_{it} values (red and blue curves).

The intermediate value of D_{it} (10^9 cm^{-2}) is utilized for band diagram analysis in Figure 3.33b, and two extreme passivation layer thicknesses are chosen for comparison (i.e., 10 and 50 nm represented by the red and blue curves, respectively). It should be noted that the band discontinuities are aligned for comparison. Band bending, and therefore carrier inversion at the interface, is reduced as $d_{\text{a-Si:H(i)}}$ increases. The intrinsic passivation layer has relatively few free carriers compared to the adjacent materials [101, 102]. This results in a reduction in the potential difference across the junction, as well as a lower electric field within the depletion region. Otherwise stated, less charge density is required to accumulate on each side of the metallurgical junction to regain equilibrium across the system [97]. This effect is pronounced for thicker passivation layers [103], which exhibit reduced band bending and carrier inversion.

Recall, carrier inversion is inversely related to the concentration of interface defects. For a relatively low surface state density (e.g., $D_{\text{it}} = 10^9 cm^{-2}$), carrier inversion and

V_{OC} is increased [91]. Thus, the potential difference due to the high concentration of minority electrons accumulated on the c-Si side of the heterojunction counters the potential drop resulting from the intrinsic layer. Likewise, the opposite effect occurs for higher D_{it} values (e.g., 5×10^{11} cm^{-2}). Here, surface states trap ionized dopants on each side of the junction; positively charged donor ions and negatively charged acceptor ions accumulate on the a-Si:H and c-Si sides of the interface, respectively [98]. This hinders carrier inversion, and leads to a reduction in the depletion width extending into the c-Si, band bending, and the electric field. In this scenario, relatively fewer minority carriers accumulate on each side of the junction, which makes the potential drop across the intrinsic layer more influential. Moreover, carrier inversion decreases and the depletion region width is extended as the influence of the potential difference increases with thicker passivation layers [102].

V_{OC} is reduced as carrier inversion becomes weaker [91]. Limited carrier inversion is the result of less band bending along the c-Si side, and more band bending on the a-Si:H side, of the heterojunction. This effect is pronounced for thicker intrinsic passivation layers [103], which explains the tendency for V_{OC} to lower with increased $d_{\text{a-Si:H(i)}}$. Careful consideration must be placed on device design due to the trade-off between improved V_{OC} with passivation effects, yet reduced performance with passivation layer thickness.

Schottky Barrier Formation at the Front TCO/a-Si:H Interface

Until now, discussion has focused on device performance based on various parameters influencing the quality of the emitter/absorber heterointerface. The top-most TCO/emitter interface will now be considered. For SHJ photovoltaics, transparent conductive oxides serve as an intermediary between the metal contact and emitter; however, devices are also being explored whereby the metal contact is eliminated and direct contact is made to the TCO [104]. Regardless, the influence of the TCO

cannot go overlooked. Recall, transparent conductive oxides are large band gap and highly doped semiconductors, which are practically all n-type and considered to be degenerate [57].

An important consideration is the possibility of forming a parasitic rectifying barrier at the TCO/a-Si:H heterointerface. The presence of a Schottky barrier is often the result of poorly chosen TCO that is incompatible or at least nonoptimal with the device structure [105]. TCOs should either be chosen or engineered such that their work function does not create a detrimental barrier. It has been shown that a parasitic Schottky barrier height (Φ_B) of 0.35 eV at the TCO/emitter interface can decrease the PCE of SHJ devices by 40% [106]. Carrier transport across these barriers often depends on its height. For relatively low Φ_B, carrier transport is dominated by thermionic emission over the barrier, while high Φ_B includes carrier tunneling through the barrier (assuming the doping is sufficiently high on both sides of the heterojunction) [107].

Figure 3.34a highlights the affect of parasitic Schottky barriers on the V_{OC} of p-SHJs [91]. Additionally, the influence TCOs may impose on carrier inversion at the

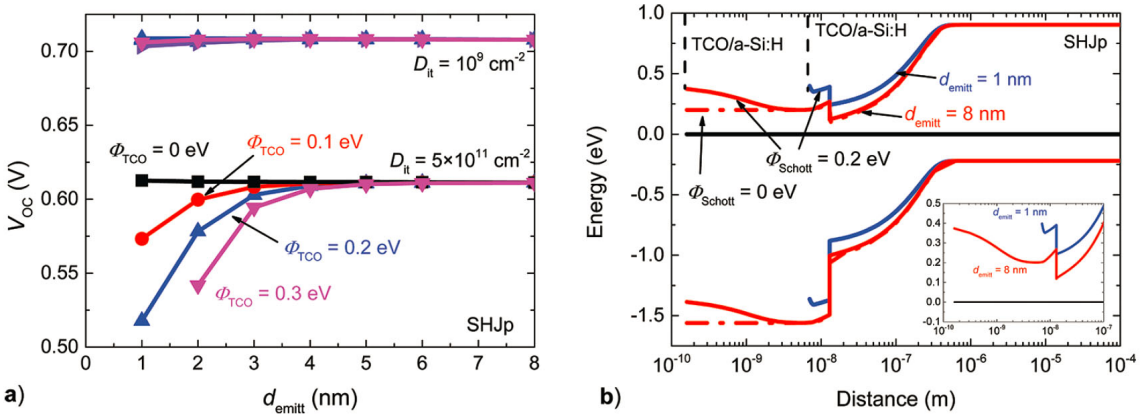

Figure 3.34: (a) V_{OC} as a function of emitter thickness for various TCO/emitter barrier heights and two interface defect densities (D_{it}), and (b) band diagrams for two disparate emitter thicknesses and a barrier height of 0.2 eV. The inset shows the influence on carrier inversion (i.e., the distance change between the conduction band and Fermi level at the heterointerface) [91].

a-Si:H/c-Si interface will also be discussed. Figure 3.34a shows the V_{OC} dependence on the thickness of the emitter layer, and on Φ_B. Two extreme values for the interface defect density are considered as well, including D_{it} values at 10^9 and 5×10^{11} cm^{-2}, which will serve as a comparison between high and low interface qualities, respectively. Negligible fluctuations in V_{OC} appear for high quality interfaces, indicating device performance is impervious to the presence of a barrier or its height for interfaces with a low concentration of defects (i.e., $D_{it} = 10^9$ cm^{-2}). However, low quality interfaces with a high density of surface defects (i.e., $D_{it} = 5{\times}10^{11}$ cm^{-2}) exhibit a strong dependence on the barrier height. For either case, Φ_B becomes less influential on V_{OC} as the emitter becomes thicker.

Figure 3.34b shows representative band diagrams illustrating the dependence on several parameters, all of which are taken from the $D_{it} = 5{\times}10^{11}$ cm^{-2} (i.e., low quality interface) curves from Figure 3.34a [91]. Two extreme emitter thicknesses (d_{emitt}) are compared, including 1 nm (blue curve) and 8 nm (red curve). A Schottky barrier height of 0.2 eV is shown for both emitter thicknesses (solid curves), and a the red-dashed curve signifies no barrier is present. It should be noted that the band discontinuities for both emitter thicknesses are aligned for comparison.

For $d_{emitt} = 8$ nm, barrier heights of both 0 and 0.2 eV exhibit the same carrier inversion on the emitter side of the a-Si:H/c-Si heterojunction; however, carrier inversion decreases as the emitter thickness drops to 1 nm. The parasitic Schottky barrier for $d_{emitt} = 1$ nm forms a depletion region at the TCO/a-Si:H heterointerface, which results in an electric field directly opposing the flow of minority electrons towards the front contact [91]. The carrier inversion is significantly decreased at the emitter/absorber interface due to the high concentration of interface states trapping positively charged donor ions and negatively charged acceptor ions accumulate on the a-Si:H and c-Si sides of the interface, respectively [98]. That is, for the barrier height plays a larger role for interfaces with high defect densities, as Figure 3.34a

shows low D_{it} exhibits a negligible reaction to Φ_{B}. In the $d_{\text{emitt}} = 8$ nm scenario, the high concentration of free electrons in the emitter compensates for or mitigates the influence of the barrier height and electric field due to the TCO, resulting in negligible deterioration of carrier inversion at the a-Si:H/c-Si interface [91]. For the low emitter thickness case, the depletion region created by the Schottky barrier due to the TCO can extend into the device and lower the diffusion current through the a-Si:H/c-Si heterojunction. Thus, the parasitic Schottky barrier formed at the TCO/a-Si:H interface will attract holes from the c-Si [97]. This leads to a reduction in carrier inversion and increased recombination, and ultimately a lowered V_{OC} and overall device performance [99].

Alternative Materials to Create Carrier Inversion

The previous sections highlighted the crucial need for high carrier inversion at the heterojunction in order to yield high V_{OC} for SHJ photovoltaics. As noted, increasing band bending or decreasing the interface defect density should be targeted results for optimal device performance; however, precisely tuning these parameters is not a feasible task during fabrication. Instead, these important fundamentals should be considered requisite effects of realistically tunable processing conditions. Specifically, fabrication techniques and material variables for emitter optimization that minimizes interface defects and maximizes carrier inversion is the key to improving device performance. Alternative materials that serve as both emitter and passivation layer will now be considered; namely, transition metal oxides.

Transition metal oxides are large band gap semiconductors with high work functions, and are leading contenders as a replacement for the a-Si:H emitter [108]. TMOs can provide high carrier inversion and tunable electrical properties [109], along with a variety of material compositions to choose from. Although TMOs act as n-type semiconductors due to their inherent oxygen vacancies, their large work functions

allow them to serve as n- or p-contacts due to band alignment with the c-Si [110]. These layers are referred to as carrier selective layers, or electron selective (ESLs) and hole selective layers (HSLs). That is, ESLs promote electron transport across the interface while repelling holes, and likewise HSLs allow holes to pass while rejecting electrons. For example, MoO_x, V_2O_5, and WO_3 are common HSLs, and TiO_2, LiF_x, KF_x, and CsF_x can serve as ESLs. Similar to utilizing a-Si:H, carrier inversion at the TMO/c-Si heterointerface is highly dependent on surface states [111]. Thus, passivation with a-Si:H(i) layers remains a necessity for optimal SHJ device performance. While the use of intrinsic a-Si:H has been explored for c-Si passivation since 1979 [112], research into its replacement by TMOs is still in its infancy. As will be discussed below, regular advancements are being made in the field of photovoltaics utilizing TMOs serving as carrier selective layers. However, transport and collection mechanisms for photogenerated carriers is not net fully understood, and remains an ongoing area of research [91]. Regardless of the rectifying behavior of TMO/c-Si heterojunctions, reports indicate that the conventional depletion approximation can be used to describe the junction [109]. Moreover, a two-diode model may also be used to describe recombination limiting current within the depletion region, and diffusion limited current under low injection conditions and at low potentials [109].

3.2.4 State of the Art CSAH Devices

Si PV with Asymmetric Heterocontacts

In 2016, a n-SHJ device was demonstrated that utilized front and back carrier-selective heterocontacts; namely, MoO_x and LiF_x as the hole-selective and electron-selective contacts, respectively [110]. The device (referred to as a solar cell with dopant-free asymmetric heterocontacts, or a "DASH cell) exhibited a power conversion efficiency of 19.42% under AM1.5g conditions, and required no fabrication processing over 200 °C. The structure of the device can be seen in Figure 3.35.

First, double-sided textured c-Si(n) ($N_D \sim 1 \times 10^{15}$ cm^{-3}) had ∼6 nm of intrinsic a-Si:H(i) deposited at 200 °C by PECVD on both sides for passivation. Approximately 10 nm of MoO_x was deposited on the front surface via thermal evaporation, followed by ∼55 nm of hydrogenated indium oxide (IO:H) and ∼10 nm of ITO was sputtered. The front grid consisted of screen-printed Ag covering ∼5% of the device. Then, an ∼1 nm LiF_x and ∼100 nm Al stack was evaporated onto the back surface. Cross-sectional SEM images and false-colored expanded views, of the textured front and back surfaces can be seen in Figure 3.36.

Intrinsic passivation layers [i.e., a-Si:H(i)] are incorporated on both surfaces to minimize recombination, and are kept sufficiently thin to avoid excessive parasitic resistance and absorption losses [113]. Conventionally, SHJ devices use doped a-Si:H layers to form heterojunctions and create carrier selectivity; however, the device reported here uses transition metal oxides with large work functions to selectively transport and repel holes and electrons towards their appropriate contacts. The X-ray photoelectron spectroscopy secondary electron cutoff was used to extract work function, with LiF_x/Al and MoO_x measuring ∼2.86 and ∼5.7 eV, respectively. Light J-V and QE measurements can be seen in Figure 3.37 [110].

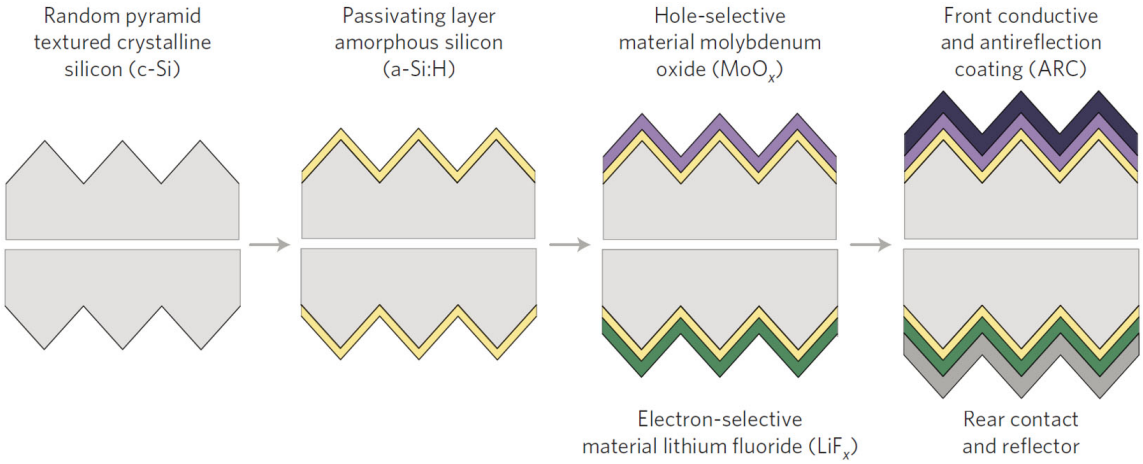

Figure 3.35: Cross-sectional schematics showing the fabrication process flow [110].

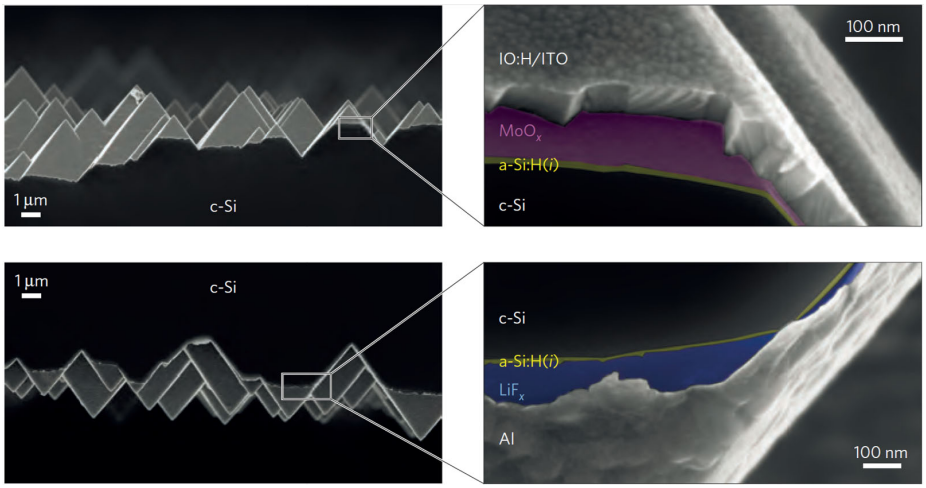

Figure 3.36: Cross-sectional SEM images of the (top) front and (bottom) back surfaces, both with false-colored expanded views to highlight the various layers [110].

InP PV with Electron-Selective Contact

Conventional III-V photovoltaics use doping to obtain carrier selectivity, while SHJ and organic solar cells commonly use transition metal oxides instead. TiO_2 and MoO_x are commonly utilized as electron- and hole-selective contacts, respectively [110]. In 2014, titanium dioxide was applied to InP to create a III-V carrier-selective photovoltaic device [114]. The cell provided 19.2% PCE, with a fill factor, V_{OC} and J_{CS} of 80.1%, 785 mV, and 30.5 mA/cm^2, respectively. As seen in Table 3.2,

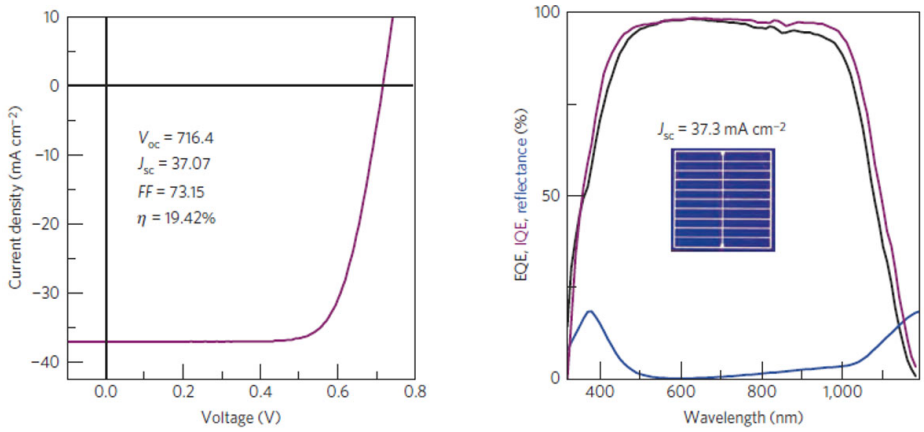

Figure 3.37: Plots showing (left) a light J-V and (right) quantum efficiency and reflection spectra for the dopant-free asymmetric heterocontacts (DASH) cell [110].

Table 3.2: Table showing device performance comparisons of a InP carrier-selective solar cell with InP cells fabricated using other techniques and using various device structures [114].

device type	description	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	eff [%]
MOCVD	homojunction	878	29.5	85.4	22.1
TiO_2/InP	heterojunction	785	30.5	80.1	19.2
ITO/InP	buried homojunction	813	28.0 (28.2[a])	82.9	18.9
CdS/InP	heterojunction	750	32.3 (28.6[b])	72.0	17.4

these values are comparable with other single-junction InP devices, including those fabricated via a much more expensive technique (i.e., MOCVD).

Figure 3.38a,b shows the device structure and a basic overview of the fabrication process flow [114]. Zn-doped p-InP(100) ($p = 2\times10^{17}$ cm^{-3}) wafers were used. The backside p-contact (20 nm Zn/100 nm Au) was deposited via sputtering, followed by an annealing step (420 °C for 40 minutes in a N_2 environment) to drive-in the metal and form an ohmic contact. TiO_2 was then deposited on the front surface by ALD (120 °C deposition temperature, and H_2O and TTIP as precursors), followed by ITO (In_2O_3:SnO = 90%:10%) deposition by sputtering at room temperature at a pressure of 6-7 mT. Finally, the front Ag contact was deposited by e-beam evaporation. A light J-V curve for the optimized device can be seen in Figure 3.38c.

A constant net ITO/TiO_2 thickness of ~70 nm was maintained in order to keep the reflectance minimum around 600 nm [114]. The TiO_2 film thickness and deposition temperature was optimized to obtain the highest V_{OC} value, using thicknesses and temperatures from 0-30 nm and 120-300 °C, respectively. Figure 3.39 shows light

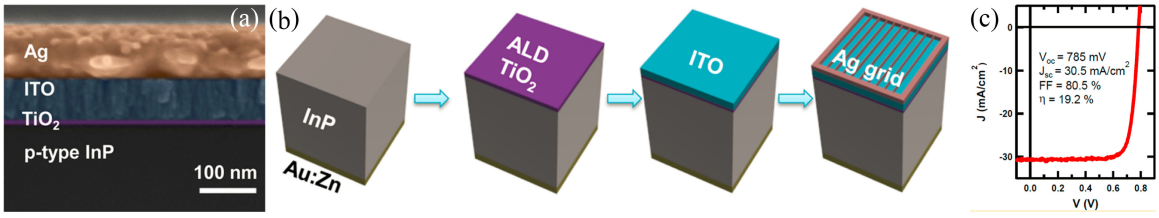

Figure 3.38: (a) false-colored and cross-sectional SEM image showing the InP carrier-selective device structure, (b) schematics showing the fabrication process flow for the InP device, and (c) a light J-V curve showing cell performance [114].

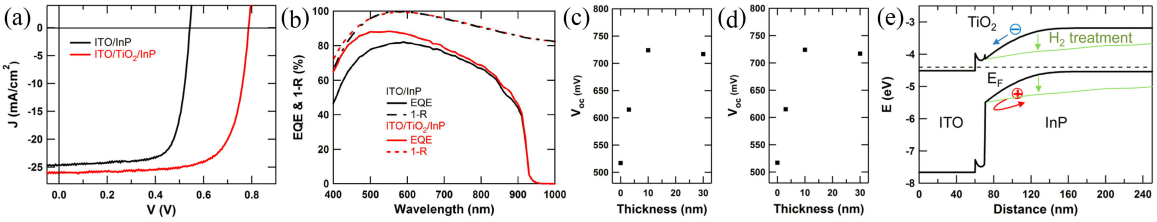

Figure 3.39: Plots showing (a) light J-V curves and (b) quantum efficiency and reflectance spectra for InP solar cells with and without the TiO_2 carrier-selective layer, the V_{OC} dependence on the TiO_2 layer (c) thickness, and (d) deposition temperature, and (e) band diagram schematic illustrating the carrier-selective InP device [114].

J-V curves and QE spectra for devices with and without the TiO_2 electron-selective layer, the V_{OC} dependence on TiO_2 thickness (deposited at a contact temperature of 250 °C), and the influence of deposition temperature on V_{OC} for TiO_2 films of a constant 10 nm thickness in panels a, b, and c, respectively. Figure 3.39e shows a band diagram of the final device, which demonstrates the purpose of the TiO_2 layer. Minority electrons flow towards the front contact, while majority holes are repelled by the Schottky barrier. This promotes carrier separation and reduces the probability of recombination [114].

Comparing the devices with and without TiO_2 reveals a 240 mV improvement in V_{OC} (i.e., 545 and 785 mV with and without TiO_2, respectively), a 1.2 mA/cm^2 improvement in J_{SC} (i.e., 24.6 and 25.8 mA/cm^2 with and without TiO_2, respectively), and a 5.5% improvement in PCE (i.e., 9.9 and 15.4% with and without TiO_2). The

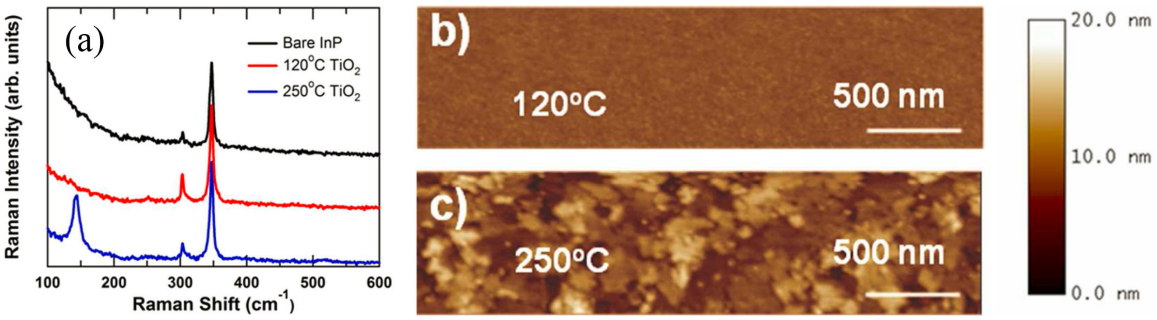

Figure 3.40: (a) Raman scattering spectra for bare InP and TiO_2/InP with disparate TiO_2 deposition temperatures, and AFM scans of 30 nm-thick TiO_2 films deposited onto InP at (b) 120 °C and (c) 250 °C [114].

increased J_{SC} is attributed to the TiO_2 reducing recombination on the front surface (Figure 3.39b), and the dramatic jump in V_{OC} is attributed to the optimization of the TiO_2 film [114]. Figure 3.39c,d show the TiO_2 thickness and deposition temperature optimization, respectively. V_{OC} rapidly increases with the film thickness until it plateaus at 10 nm, and device performance gradually decreases as temperature is increased.

Figure 3.40 shows a comparison of the TiO_2 surface morphology at deposition temperatures of 120 and 250 °C using AFM and Raman spectroscopy [114]. Titanium dioxide is known to begin exhibiting crystallinity between 150 and 200 °C [78, 81–83]. The layer deposited at 120 °C appears to be a smooth (RMS roughness of 0.3 nm) and purely amorphous film, with no Raman peak around 140 cm^{-1}. On the other hand, the layer deposited at 250 °C reveals the formation of a roughened (RMS roughness of 1.2 nm) film exhibiting some crystalline anatase phase, as seen by the corresponding Raman peak at 140 cm^{-1}.

Chapter 4

Methodologies

4.1 Fabrication

4.1.1 Atomic Layer Deposition

Atomic layer deposition (ALD) is a thin-film chemical vapor deposition (CVD) technique that relies on gas precursors reacting with the surface of a sample to incrementally deposit monolayers at a time. Repeatedly alternating between precursors [e.g., H_2O and and tetrakis-dimethylamido titanium (TDMAT) for TiO_2] allows for thin films to be slowly deposited. The first precursor (precursor A) is pulsed, which introduces the gas to the chamber and reacts with the functionalized sample surface. Inert gas is then pulsed into the chamber to purge any reaction by-products and leftover precursor A species. The second precursor (precursor B) is then pulsed, which introduces the gas to the chamber and reacts with surface. Then, inert gas is again pulsed to purge the chamber of any reaction by-products and leftover species of precursor B. This process deposits single atomic layers at a time, and is repeated for a determined number of cycles to achieve a target film thickness.

4.1.2 Sputtering

The planar magnetron sputtering was invented (i.e., patented) in 1974, and quickly became the worlds leading method for ITO deposition. Sputtering is a form of physical vapor deposition (PVD), and a variety of modes are available. Direct current

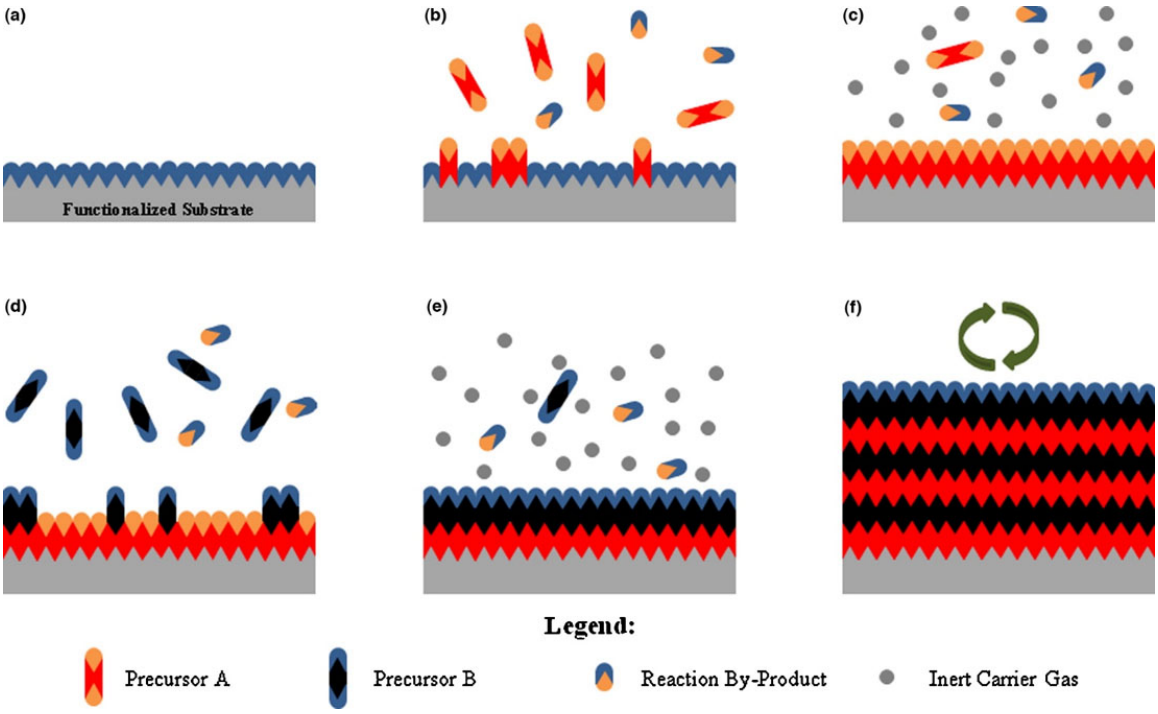

Figure 4.1: Models illustrating the atomic layer deposition (ALD) process. (a) a functionalized surface has (b) a precursor (precursor A) introduced to the deposition chamber where precursor A reacts with the surface. (c) inert gas purges the chamber of any reaction by-products and left-over precursor A species, followed by the introduction of (d) a precursor (precursor B) to the deposition chamber that also reacts with the surface. (e) inert gas purges the chamber again to remove any reaction by-products and remaining precursor B species. (f) steps (b)-(e) are repeated, which deposit atomic layers at a time, for a number of cycles until a determined film thickness is met. Adapted from [115].

sputtering is the simplest, cheapest, and most commonly used method that supplies a constant bias across the target (i.e., cathode) and sample (i.e., anode). This ionizes the sputtering or working gas (e.g., argon) and accelerates it towards the target, which ejects or sputters atoms off the target to be deposited onto the sample. Positive ions will accumulate on the target in DC mode if it is not sufficiently conductive. Radio frequency (RF) sputtering also applies a bias across the target and sample; however, an alternating current (AC) power source is applied to the target and sample at 13.56 MHz. The applied potential results in high energy ions bombarding the target, leading to an accumulation of positive ions near the target surface. As the current alternates, the ejected ions accelerate towards the sample to be deposited. Pulsed DC or pulsed

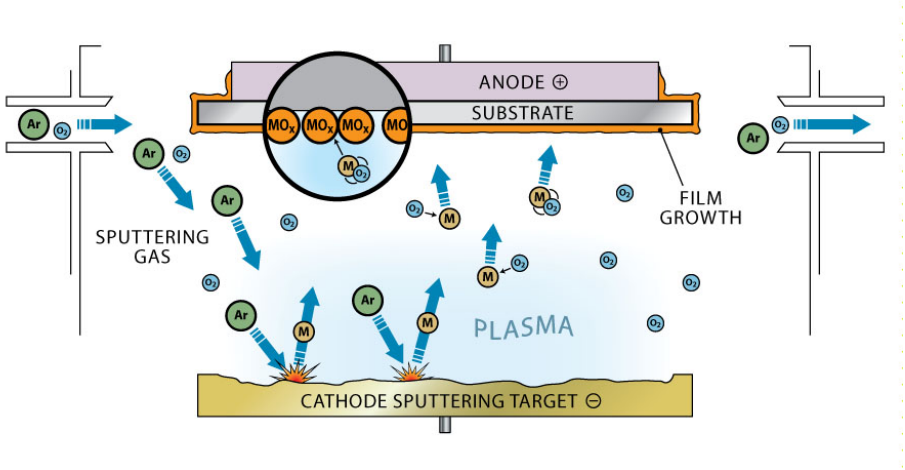

Figure 4.2: Illustration showing the deposition process within a sputter tool chamber. Highly energetic plasma gas (often Ar) collide with the cathode or target, ejecting target atoms that are accelerated towards the anode or sample for deposition. Adapted from [116].

magnetron sputtering is another alternative to standard DC sputtering, whereby the applied potential is modulated at the target between negative and positive (or reverse) bias. This technique is useful for limiting or eliminating plasma arcing by continuously removing the accumulation of charge on the target. Pulsed DC power is particularly important during reactive sputtering, which introduces a reactive gas (e.g., oxygen or nitrogen) to the inert species. The reactive gas interacts with the plasma created by the inert gas, resulting in a chemical reaction at the target. In this case, the deposited film is different from the target material, and its stoichiometry can be tuned by controlling the flow of reactive and inert gases.

4.2 Characterization

4.2.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) uses a focused beam of high energy electrons to generate an image of a sample. A comparison of functionality between light and scanning electron microscopes is depicted in Figure 4.3. The wavelength of incident particles dictates the resolution capability of a microscope. As such, the resolving

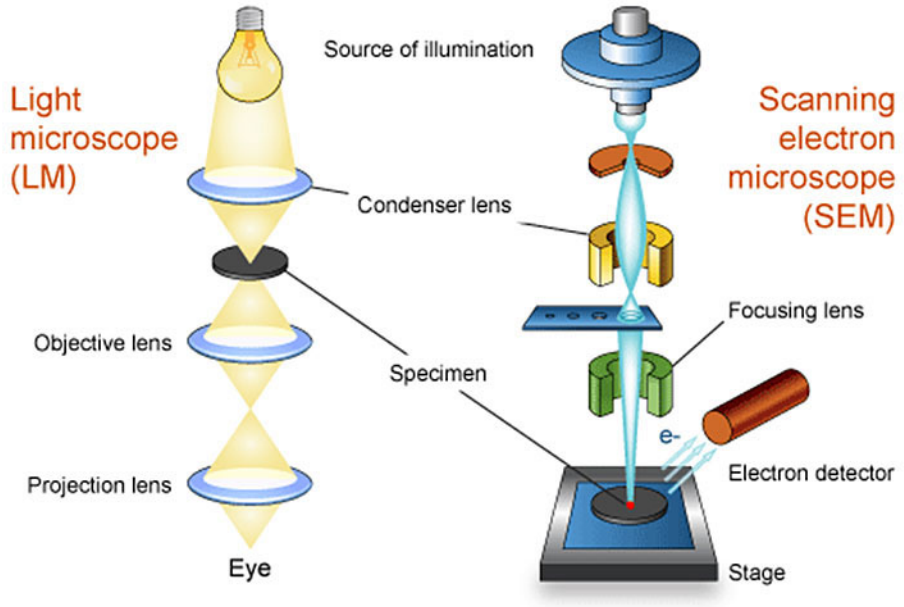

Figure 4.3: Schematics comparing (left) optical and (right) scanning electron microscopy. Adapted from [117].

capability of optical microscopes is limited by the wavelength of visible light. On the other hand, SEM accelerates electrons to a set energy and wavelength, which greatly increases the resolution (to ∼1 - 10 nm) over optical microscopy. Moreover, instead of using optical lenses to focus a beam of photons as is the case with conventional microscopes, SEMs use electromagnetic lenses to center and focus the beam of electrons.

Primary electrons (i.e., incident electrons) can interact with the bulk material and be reflected or scattered backwards. These are referred to as backscattered electrons (BSE). Alternatively, primary electrons may collide with an electron bound to the sample, thereby ejecting an electron from the specimen. These are referred to as secondary electrons (SE).

4.2.2 Energy Dispersive X-ray Spectroscopy

Energy dispersive X-ray spectroscopy (EDXS) is a chemical characterization technique that can be performed using scanning or transmission electron microscopes, and is illustrated in Figure 4.4. A focused beam of high energy electrons interacts with

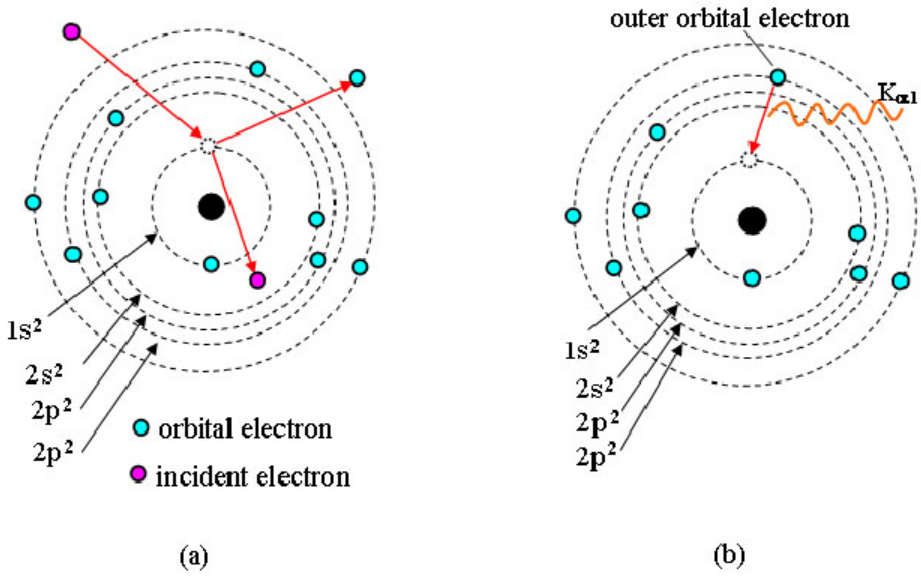

Figure 4.4: Illustrations depicting (left) primary electrons ejecting an inner shell electron from a sample and (right) outer shell electrons relaxing to the vacant inner shell position and releasing characteristic X-rays. Adapted from [118].

a sample, and ejects an inner-shell from its unexcited state. Then, an outer shell electron relaxes into the vacant electron position of lower energy, which can result in characteristic X-ray emission of energy dependent on the particular element and which orbital the electron relaxes from. Each element has a unique atomic structure that have distinct emission spectra. That is, X-rays with energy corresponding to elements within the sample will be collected to form EDX spectra. Known emission values allows for elemental analysis of collected EDX spectra.

4.2.3 Photoluminescence

Photoluminescence (PL) is a non-destructive technique which is often used to characterize the electronic structure of materials. A schematic representation of the technique is depicted in Figure 4.5. PL can be used to detect and identify impurities, and characterize the radiative and non-radiative carrier recombination rates. This technique is heavily utilized with III-V alloys due to their high internal quantum efficiency (IQE). That is, the measure of photogenerated electron-hole pairs (EHPs)

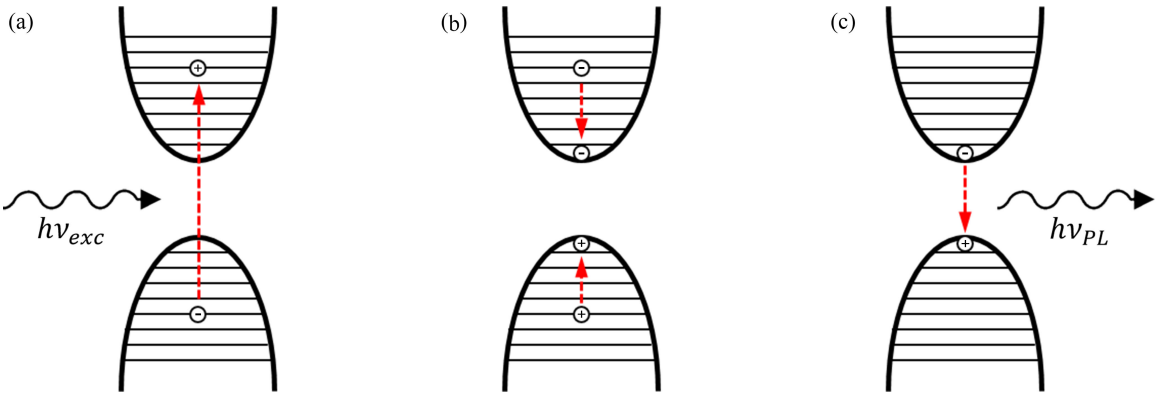

Figure 4.5: Schematic showing (a) an incident photon that excites a valence electron to the conduction band, (b) the valence hole and conduction electron relaxing to the valence and conduction band edges, respectively, via lattice vibrations and (c) the conduction electron relaxing back to the valence band and emitting a photon.

that undergo radiative recombination and emit light.

Careful attention should be given while mounting samples for measurement, as any induced strain will affect the emitted light. Photogeneration of EHPs is done via a laser of energy larger than the band gap energy (i.e., $h\nu > E_{\mathrm{G}}$). The penetration depth of the incident light (typically on the order of microns) and the minority carrier diffusion lengths define the characterization volume. Using UV wavelengths is a method for analyzing a very thin surface layer.

Low temperature measurements (referred to as cryo-PL) are preferred, as line broadening is minimized and band-to-band recombination is rarely observed at low temperatures. The thermal distribution of carriers that are excited into a particular energy band make up a width of approximately $k_{\mathrm{B}}T/2$ of the emission line from that band. For example, the line broadening due to thermal activation at $T = 4.2$ K is only 1.8 meV.

4.2.4 Raman Spectroscopy

Raman spectroscopy (RS) is a non-destructive technique that measures the energy shift between emitted photons that have undergone elastic (Raleigh) and inelastic scattering. The mechanisms for this technique are depicted in Figure 4.6a. Very few

scattered photons exhibit a change in energy (i.e., inelastic) after they interact with the sample (approximately 1 in 10 million), therefore an intense monochromatic light source (i.e., a laser) is used for excitation. Inelastically scattered photons lose or gain energy via interaction with phonons (among other things).

The processes by which photons interact with optical and acoustic phonons are called Raman and Brillouin scattering, respectively. For either process, photons can either lose energy to the sample (i.e., Stokes scattering), or gain energy from it (i.e., anti-Stokes scattering). Stokes scattering is typically the mode for analysis, as anti-Stokes scattering occurs far less often and its signal is therefore much lower. Figure 4.6b shows an comparison of relative intensities for Rayleigh scattering and inelastic Raman scattering (i.e., Stokes and anti-Stokes).

RS is capable of determining sample composition and crystallinity, and it is sensitive to stress, strain, crystal orientation, and lattice damage or structural imperfections.

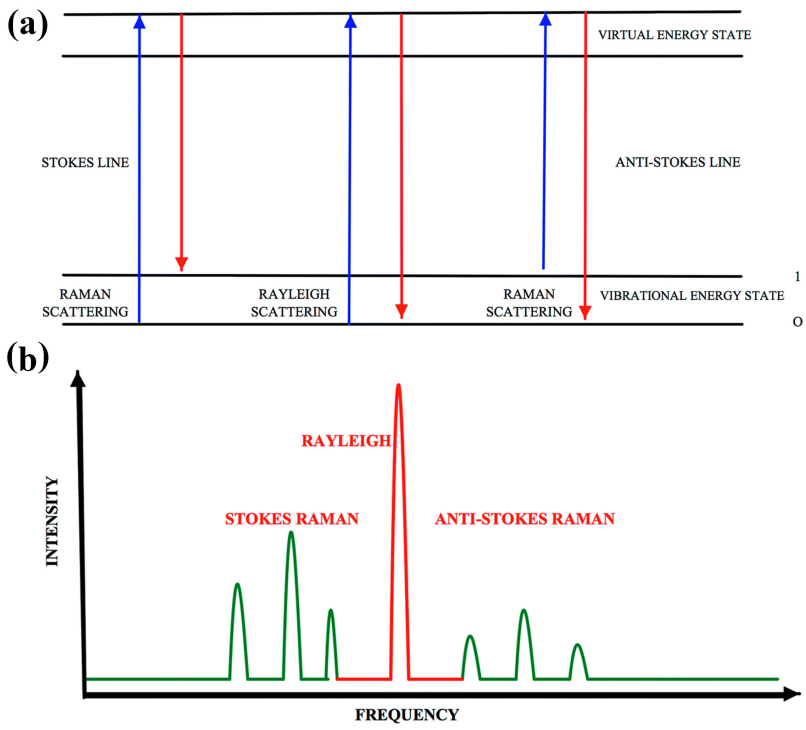

Figure 4.6: Plots showing the (a) mechanisms and (b) relative intensities for elastic Rayleigh scattering and inelastic Raman scattering (Stokes and anti-Stokes). Adapted from [119].

Peaks will shift and broaden as a material becomes less crystalline, and different crystal facets will have distinct Raman shifts. Additionally, various phonon modes (determined by selection rules) can provide complimentary information on different aspects of a sample, such as the bulk transverse optical (TO) and interfacial surface optical (SO) modes.

Chapter 5

Au-Catalyzed InGaP MacEtch for Suspended III-V Nanofoils

5.1 Summary

Metal-assisted chemical etching (MacEtch) has been established as a low-cost, benchtop, and versatile method for large-scale fabrication of semiconductor nanostructures, and has been heralded as an alternative to conventional top-down approaches such as reactive-ion etching. Application of the MacEtch technique to various binary III-V compound semiconductor materials has recently proven the utility of the method for beyond-Si technologies. However, extension of this technique to ternary compound alloys and heteroepitaxial systems has remained relatively unexplored. Here, Au-assisted and inverse-progression MacEtch (I-MacEtch) of the heteroepitaxial $In_{0.49}Ga_{0.51}P$/GaAs material system is demonstrated, along with a method for fabricating suspended InGaP nanofoils of tunable thickness in solutions of hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). A comparison between Au- and Cr-patterned samples is used to demonstrate the catalytic role of Au in the observed etching behavior. Vertical etch rates for nominally undoped, p-type, and n-type InGaP are determined to be ∼9.7 nm/min, ∼8.7 nm/min, and ∼8.8 nm/min, respectively. The evolution of I-MacEtch in the InGaP/GaAs system is tracked, leading to the formation of nanocavities located at the center of off-metal windows in the InGaP epilayer. Upon nanocavity formation, additional localized mass-transport pathways to the underlying GaAs substrate permit its rapid dissolution. Differential etch rates

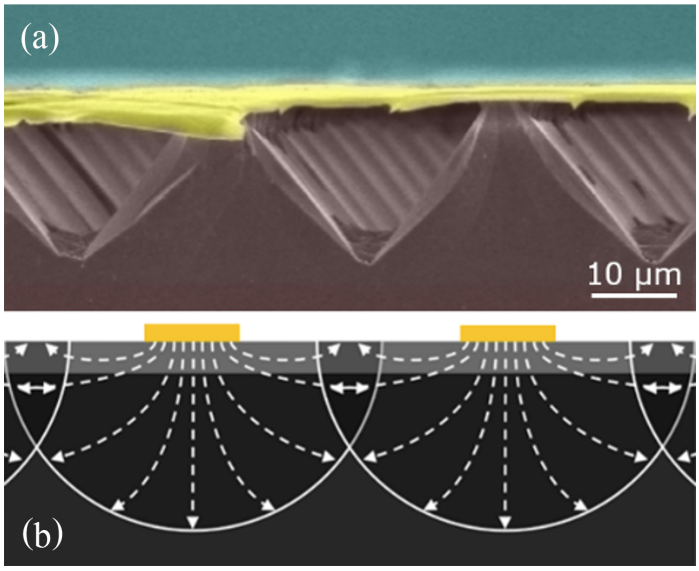

Figure 5.1: (a) False-colored cross-sectional SEM image showing Au-enhanced I-MacEtch of InGaP/GaAs leading to suspended InGaP nanofoils over GaAs micro-trenches, and (b) a model for the process based on an overlap of neighboring hole distributions.

between the epilayer and substrate are exploited in the fabrication of InGaP nanofoils that are suspended over micro-trenches formed in the GaAs substrate (Figure 5.1a). A model is provided for the observed I-MacEtch mechanism, based on an overlap of neighboring injected hole distribution profiles (Figure 5.1b). The nanofabrication methodology shown here can be applied to various heteroepitaxial III-V systems and can directly impact the conventional processing of device applications in photonics, optoelectronics, photovoltaics, and nanoelectronics.

5.2 Motivation

Micro- and nano-structured semiconductor architectures have been an area of extensive study for years, and are being incorporated into a wide variety of electronic and photonic devices due to their unique properties compared to their bulk counterparts [1**?** –3]. Conventional top-down micro-/nano-fabrication techniques include patterned wet-etching and reactive-ion etching (RIE); however, these methods can present challenges as desired features continue to move towards higher aspect-ratio geometries that are

free of crystallographic defects [7]. Patterned wet-etching is more cost-effective in that it is solution-based and can be performed in conventional semiconductor wet benches, although it lacks the ability to yield high aspect-ratio structures due to it being isotropic or having crystallographic dependences [8]. In contrast, RIE is a dry-etching technique that can generate high aspect-ratio geometries at the expense of exposing the target material to high energy ion bombardment, which causes sidewall damage and detrimental lattice defects in addition to the intended material removal [5, 6]. Moreover, RIE uses hazardous gases and is performed under high vacuum conditions at elevated process temperatures, making it less ideal for process simplification and cost reduction [8].

Ternary InGaP has important device applications in high electron mobility transistors (HEMTs) [120, 121] due to its deep donor levels, high power density, and linearity, and it is a prominent III-V alloy in many tandem solar cell designs [122, 123] due to its large bandgap energy and ability to be grown in a lattice-matched configuration with GaAs (i.e., $In_{0.49}Ga_{0.51}P$). Although catalytic etching of the binary components of InGaP (i.e., GaP and InP) have been reported [13, 40], MacEtch investigations involving the ternary phase have not been presented in the current literature. InP has been shown to exhibit I-MacEtch behavior [13], while GaP has been reported to demonstrate both MacEtch and I-MatEtch tendencies based on the dimensions of the metal catalyst [40]. Given that InGaP, when lattice-matched to GaAs, has a ternary composition consisting of nearly equivalent In- and Ga-content, and since the individual binary constituents InP and GaP exhibit tendencies toward dissimilar metal-catalyzed etching modes, the dominant catalytic etching mechanism for InGaP in not immediately known (i.e., MacEtch or I-MacEtch).

5.3 Introduction

The I-MacEtch process was formalized in 2015 and relies on many of the mechanisms described for the conventional MacEtch process (e.g., catalytic oxidation and preferential dissolution of selective regions) [13]. However, several mechanisms are fundamentally different. Most notably, the metal does not sink into the substrate as observed in MacEtch; instead, the metal acts as a patterned mask as well as a catalyst, and generates inverse structures through preferential dissolution of off-metal regions [13, 40]. As with forward MacEtch, a cathodic reaction occurs at the solution/metal interface, including oxidant reduction and hole injection through the metal and into the underlying semiconductor. However, as previously shown in the case of InP, distinct types of oxides are formed at the metal/semiconductor interface and in the off-metal regions [13]. These interfacial and non-interfacial oxides are non-soluble and soluble in the I-MacEtch solution, respectively. The non-soluble oxide layer generated at the metal-interfaced regions does not prevent the cathodic reaction (i.e., oxidant reduction and hole injection into the interfaced semiconductor). However, it acts as a dissolution barrier by preventing the anodic reaction from occurring in these regions [13]. Without the anodic reaction and dissolution of the oxidized material occurring beneath the metal, the injected holes diffuse from the interfacial regions and oxidize the off-metal regions as well. With the off-metal regions oxidized to a state that is soluble in the I-MacEtch solution, mass transport or material dissolution occurs in regions where the semiconductor is not directly interfaced with metal. Therefore, submerging a metal-patterned sample in an I-MacEtch solution results in preferential etching of the off-metal regions, followed by etching of the oxidized regions underneath the metal as those regions become exposed [13, 40]. The lateral and vertical etch rates (LER and VER, respectively) and maximum etch depth are tunable with the I-MacEtch solution, and with the size, pitch, thickness, and type of metal catalyst [13].

However, the main obstacle for routine use of these metal-assisted catalytic etching techniques is the limited fundamental research into the various etching conditions (e.g., metal catalyst type, solution components, and the relative concentrations of each) for various semiconductor materials, particularly for ternary III-V semiconductors such as InGaP.

The metal-catalyzed etching behavior of lattice-matched heteroepitaxial $In_{0.49}Ga_{0.51}P$ films on GaAs (100) substrates is reported. A strong inverse-mode etching tendency is identified for InGaP and the metal-catalyzed nature of the etching mechanism is revealed through a comparison of metallic masks with largely variant redox potentials. The vertical etch rate of nominally undoped, p-type, and n-type InGaP are quantified under well-controlled and fixed I-MacEtch conditions. The progression of the etch-front over time is tracked, leading to localized etching of the InGaP epilayer and subsequent rapid dissolution of the underlying GaAs substrate. Differential epilayers and substrate etch rates are exploited in the fabrication of suspended InGaP nanofoils of tunable thickness. Finally, a model is proposed for the InGaP/GaAs heterostructure I-MacEtch mechanism.

5.4 Experimental Details

All InGaP samples were grown on GaAs (100) substrates (WaferTech) using a 3 × 2" Aixtron close-couple showerhead metal-organic chemical vapor deposition (MOCVD) reactor. Prior to growth, oxide desorption was performed at 835 °C under arsine (AsH_3) over a period of 10 minutes, after which temperature was lowered to a growth set point temperature of 773 °C (equivalent surface temperature of 650 °C, based on LayTec EpiTT emissivity corrected pyrometry measurements). Growth of $In_{0.49}Ga_{0.51}P$ with thickness of 500 nm was carried out at a reactor pressure of 100 mBar. A cross-sectional schematic of the epistructure can be found in Figure 5.2a. Trimethylindium [TMIn, $In(CH_3)_3$], trimethylgallium [TMGa, $Ga(CH_3)_3$], and phosphine (PH_3) were

used as precursors for the supply of In, Ga, and P growth species, respectively. Doping was accomplished using disilane (Si_2H_6) for supply of Si dopants in n-type InGaP, and diethylzinc [DEZn, $(C_2H_5)_2Zn$] was used for supply of Zn dopants in p-InGaP samples. Dopant concentrations were determined as $n = 2 \times 10^{17}$ cm^{-3} for InGaP:Si and $p = 5 \times 10^{16}$ cm^{-3} for InGaP:Zn, based on post-growth Hall effect measurements (Nanometrics HL5500). For simplicity, nominally undoped (i.e., unintentionally doped) InGaP sample will henceforth be referred to as i-InGaP.

After crystal growth, all wafers were submerged in diluted HF for native oxide removal, followed by degrease with standard solvents. Photolithography was used to pattern the samples; an adhesion promoter, hexamethyldisilazane (HMDS; Micro-Chemicals), and a positive g-line photoresist (Fujifilm HPR 504) were spin-coated, followed by a 100 °C soft-bake. Exposure and development were performed using a g-line stepper (GCA 6300) and CD-26 (Microposit), respectively. A 35 nm-thick Au film was deposited by thermal evaporation (Lesker PVD75 Thermal Evaporator) at a rate of ∼1 Å/s, and liftoff was performed in an acetone bath with sonication. The size of each metal-patterned array was ∼2.5 × 2.5 mm^2, and consisted of a mesh-shaped Au grid of ∼20 μm width separated by ∼10 × 10 μm^2 windows (henceforth, referred to as the "off-metal" regions). A top-view schematic of the patterning can be found

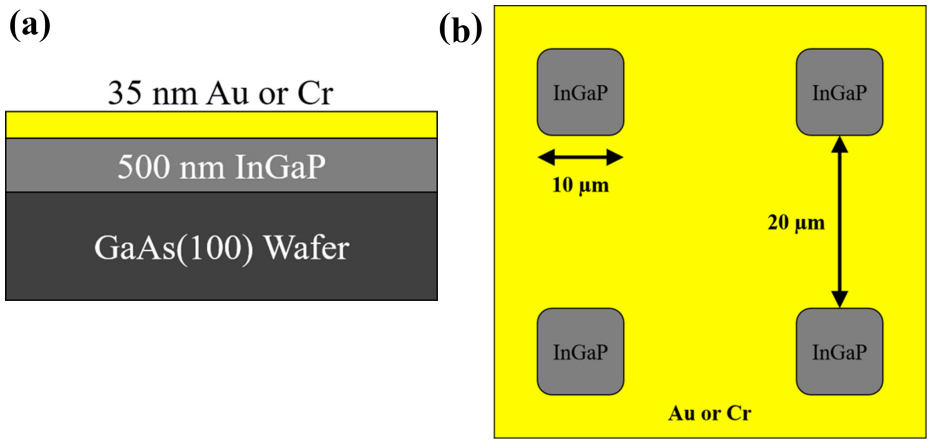

Figure 5.2: Schematics showing (a) cross-sectional view of the epistructure, and (b) top-view of the sample patterning.

in Figure 5.2b. For consistency, only this pattern dimension is considered at length to establish the current I-MacEtch behavior of InGaP. Additionally, Cr-patterned samples were fabricated for comparison with Au-patterned samples. The Cr-deposited samples were patterned using the same photolithography process described above, and a Cr film with a thickness of 35 nm was deposited via thermal evaporation at a rate of ∼1 Å/s to achieve an identical pattern thickness, geometry, and dimensions as that described for Au.

All I-MacEtch experiments presented here were performed at room-temperature using a common solution of H_2O_2 with molar concentration of 6.4 mol/L (to support the cathodic reaction and hole injection) and HF with molar concentration of 14.1 mol/L (to facilitate the anodic reaction and material dissolution). All etching times are reported in figure captions. Sample imaging was performed by scanning electron microscopy (SEM; Hitachi S-4000), and compositional mapping was carried out by energy dispersive X-ray spectroscopy (EDXS; TESCAN MIRA3 SEM).

5.5 Results and Discussion

5.5.1 Observable Inverse-Progression

The set of tilted SEM images in Figure 5.3 illustrate the etch progression for Au-patterned i-InGaP samples etched for increasing lengths of time. Panels e-h (right-hand side) show higher magnification views corresponding to the image from the same row in panels a-d, while the etch time increases from the top to bottom in both columns. As observed, both the vertical etch depth and lateral etch width increase with time in off-metal regions. The same etching behavior has been observed in the case of InGaP samples patterned with Au mesh features of differing micron-scale dimensions (*vide infra*). Regardless of whether the off-metal windows are small or large relative to the Au width shown Figure 5.3, similar inverse etching behavior is found in the

current micron-scale regime. Notably, Figure 5.3e-h show that the Au/InGaP interface remains intact with increasing etch time. As indicated by the white arrow in Figure 5.3h, prolonged etching periods results in the formation of a submicron or nanocavity (henceforth, referred to as a cavity) in the center of the off-metal region, indicating that the InGaP film is locally etched completely through.

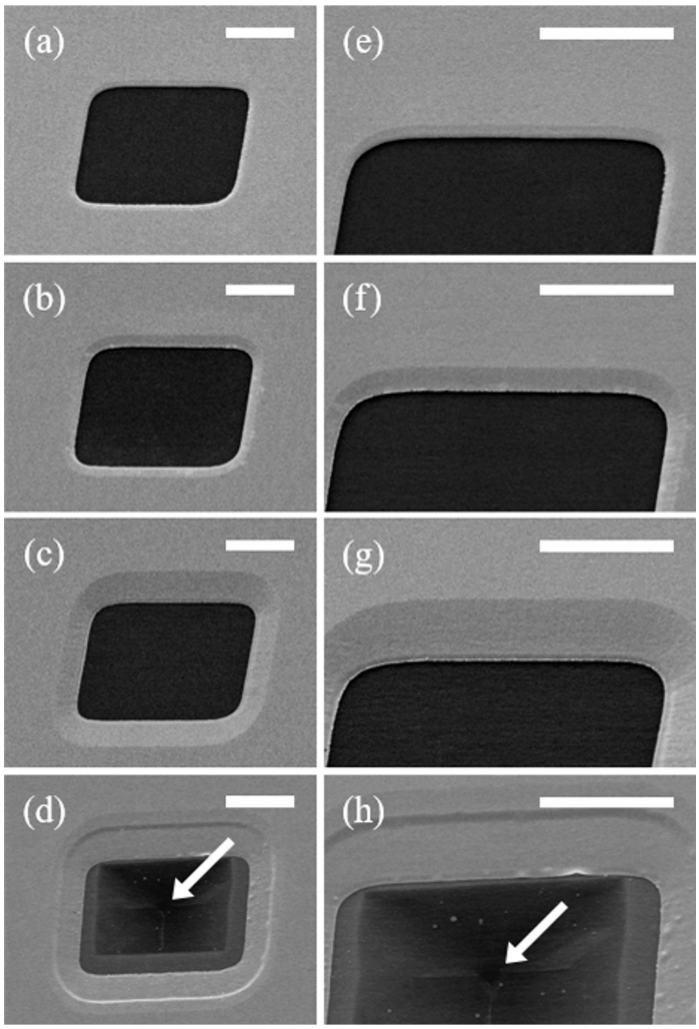

Figure 5.3: SEM images showing the etch progression of Au-patterned i-InGaP (initial thickness = 500 nm) with increasing time from the top to bottom columns. (a, e) shows a sample shortly after etching began after an etch time of 5 minute, (b, f) shows the i-InGaP layer approximately half-way etched through after an etch time of 20 minutes, (c, g) shows a sample shortly before the i-InGaP layer has been etched through after an etch time of 40 minutes, and (d, h) shows a sample immediately after the i-InGaP layer has been completely etched at the center of the off-metal window after an etch time of 50 minutes. The white arrows point to the location of the cavity. A suspended InGaP nanofoil has been formed in the regions surronding the central cavity. All scale bars represent 4 μm.

Figure 5.3 indicates that InGaP exhibits an I-MacEtch behavior under the etching conditions employed here, causing preferential dissolution of the off-metal regions. Several possible explanations for the mechanism are proposed. As described above, the oxidant is reduced at the solution/Au interface and holes are injected along locations where InGaP is interfaced with Au. Similar to what has been reported by Kim et al. for I-MacEtch of InP [13], the etching mechanism of InGaP observed here could imply the formation of distinct oxide layers in the Au-covered and off-metal InGaP regions that are non-soluble and soluble in the I-MacEtch solution, respectively. In the case of InP I-MacEtch, the P-based interfacial oxide layer [i.e., $InPO_4$, $In(PO_3)_3$] remained insoluble in the etchant bath consisting of H_2SO_4 and H_2O_2, but was dissolved in HF after removal of the catalyst layer. Since the current work only employs HF, which has been shown to permit dissolution of the P-based oxides [13, 17], it is likely that the observed I-MacEtch mechanism for InGaP differs from that of InP.

Another possible explanation for the I-MacEtch behavior observed here could be related to the quality of the Au/InGaP interface and the hole distributions generated in the semiconductor from the cathodic reaction. In this case, holes are injected everywhere InGaP is interfaced with Au, but the Au/InGaP interface is sufficiently thick (i.e., the 35 nm Au film is continuous and contains no voids) and wide (i.e., 20 μm Au grid width) such that it does not allow HF to access the oxidized InGaP regions covered by Au. Without solution access to the underlying InGaP regions, the anodic reaction is inhibited by the Au layer and material dissolution in metal-coated regions is prevented. As the cathodic reaction continues to inject holes that are free to diffuse from directly underneath the Au, extended hole distributions can form under the metal with profiles that are dependent on a variety of reaction- and material-specific properties (e.g., magnitude of the reduction-oxidation potential relative to the ionization potential of the semiconductor, carrier mobility and diffusion length, temperature, etc.) [9, 21, 23]. Under such conditions, the hole distributions from

neighboring Au-coated regions may overlap and generate a higher hole concentration in these overlapped regions, leading to locally enhanced oxidation rates in the off-metal regions [124]. Thus, material dissolution of the exposed InGaP (i.e., oxidized off-metal regions) occurs first, and is followed by etching of the Au-covered InGaP adjacent to the off-metal regions as it becomes exposed. This explanation may be supported by the observation that etched cavity is formed in the center of the off-metal window.

5.5.2 Varying the Catalyst Geometry

A series of I-MacEtch experiments with systematic variation of pattern size was also performed, as seen in the top- (left-side) and tilted-view (right-side) SEM images in Figure 5.4. In addition to the mesh structures with $\sim$10 $\times$ 10 μm^2 windows separated by 20 μm Au widths (panels a and b), considered here are $\sim$10 $\times$ 10 μm^2 windows separated by $\sim$2 μm Au widths (i.e., ratio of 5:1; panels c and d), $\sim$20 $\times$ 20 μm^2 windows separated by $\sim$5 μm Au widths (i.e., ratio of 4:1; panels e and f), $\sim$5 $\times$ 5 μm^2 windows separated by $\sim$25 μm Au widths (i.e., ratio of 1:1; panels g and h), and $\sim$5 $\times$ 5 μm^2 windows separated by $\sim$20 μm Au widths (i.e., ratio of 1:4; panels i and j). These samples validate the I-MacEtch behavior of micron-scale patterns with feature dimension ratios above and below that which were demonstrated in Figure 5.3. Importantly, all samples were prepared under identical conditions (i.e., Au thickness of 35 nm, same photolithographic process) and I-MacEtch was also conducted under the exact same conditions (i.e., in solutions of 6.4 mol/L H_2O_2 and 14.1 mol/L HF for 20 mins at room-temperature). As seen in Figure 5.4, samples with different Au pattern feature sizes all demonstrated the same I-MacEtch behavior, regardless of the window size and Au mesh width. Thus, when the window is very large with respect to catalyst mesh [i.e., $\sim$10 $\times$ 10 μm^2 windows separated by 2 μm widths (i.e., ratio of 5:1), shown in Figure 5.4(c,d) and $\sim$20 $\times$ 20 μm^2 windows separated by 5 m widths (i.e., ratio of 4:1), shown in Figure 5.4(e,f)], a persistent inverse etching progression

is observed. Moreover, increasing the relative area of the exposed off-metal region versus the width of the Au-coated strips leads to a corresponding increase in lateral I-MacEtch rate, which scales with vertical etch rate. In the regime of overlapping hole profiles, this is simply understood in terms of enhanced solution access to the exposed windows, which have been catalytically oxidized. Additionally, the greater the width of the Au catalyst, the higher the oxidation rate in all regions including off-metal areas. Considering Figure 5.4, in panel (a) where the window size is $\sim$10 $\times$ 10 μm^2 and the Au-coated strips have a width of $\sim$20 μm, an undercut etch width of $\sim$585 nm is observed. Keeping the same window size, but reducing the Au strip width to $\sim$2 μm (i.e., Figure 5.4c) results in a reduction of the lateral etch width to $\sim$245 nm. Keeping the strip width the same as Figure 5.4a, but reducing the window size to $\sim$5 $\times$ 5 μm^2 (i.e., Figure 5.4i) results in a slight reduction of the lateral etch extent to $\sim$470 nm. Thus, a larger window-to-strip ratio enhances etching for the micron-scale pattern sizes investigated in this work.

It should also be noted that nanometer-scale Au lines separated by micrometer-scale windows may not permit extensive overlap of hole distribution profiles and, therefore, may not be as conducive to inverse etching. This highlights an important dimensional-dependence of the I-MacEtch mechanism. It is anticipated that in the regime where nano-scale catalyst features are separated by larger off-metal areas, additional or different etching phenomena may occur. This will likely have to account for not only the effective hole diffusion length, but also solution access to oxidized regions below the metal-coated surface, as well as dramatic differences in the hole concentration gradients that generate overlapped oxidized profiles in micron-scales. In the nano-scale regime, an absence of oxidized material profile overlap and additional enhanced solution access to oxidized volumes may lead to a reduction of the inverse etching behavior and may lead to a tendency toward forward MacEtch as was observed by Cheung et al. in their study tilted, Mechanistic Characteristics of Metal-Assisted

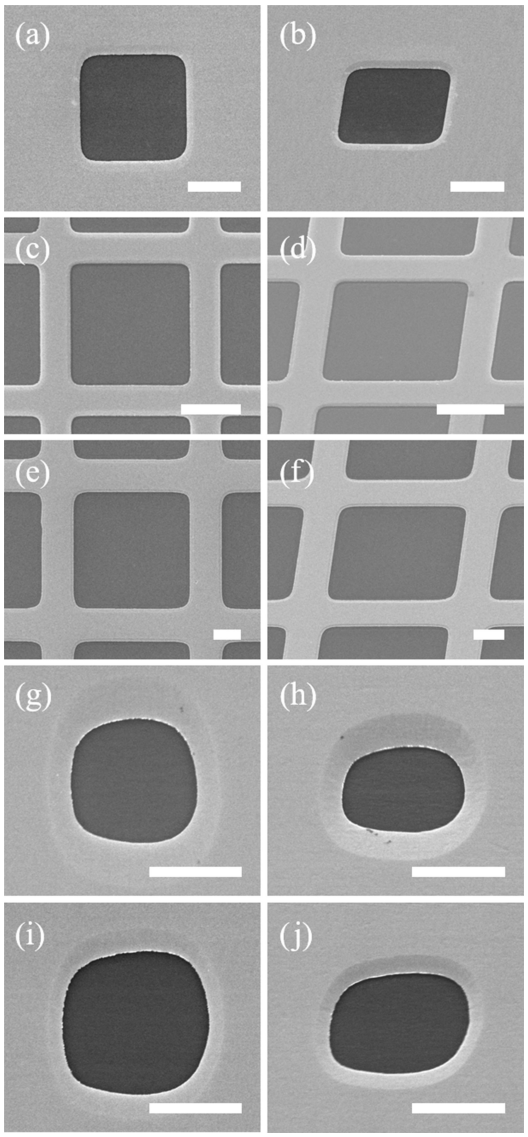

Figure 5.4: SEM images of Au-patterned i-InGaP samples subjected to the I-MacEtch solution (i.e., 6.4 mol/L H_2O_2 and 14.1 mol/L HF) for 20 min, demonstrating consistent I-MacEtch behavior for a variety of catalyst pattern geometries. Considered here is the size of the window or off-metal region, and size of the Au-covered street widths separating windows. Top- (left-side) and tilted-view (right-side) SEM images, respectively, for (a) and (b) $\sim 10 \times 10$ μm^2 off-metal windows and ~ 20 μm Au width (window-to-street-width ratio = 1:2); (c) and (d) $\sim 10 \times 10$ μm^2 off-metal windows and ~ 2 μm Au width (ratio = 5:1); (e) and (f) $\sim 20 \times 20$ μm^2 off-metal windows and 5 μm Au width (ratio = 4:1); (g) and (h) $\sim 5 \times 5$ μm^2 off-metal windows and ~ 5 μm Au width (ratio = 1:1); (i) and (j) $\sim 5 \times 5$ μm2 off-metal windows and ~ 20 μm Au width (ratio = 1:4). All samples have an i-InGaP film thickness of 500 nm, and an Au thickness of 35 nm. Scale bars in (a)-(f) represent 5 μm, and in (g)-(j) represent 3 μm.

Chemical Etching in GaAs.R1

As seen throughout Figures 5.3 and 5.4, the Au layer continues to conform to the underlying etched InGaP in the interfacial regions, resulting in the Au/InGaP interface remaining intact. This is contrary to I-MacEtch behavior previously reported where the metal is suspended over the dissolved regions [13, 40]. This observation may shed some light on the inverse etching mechanisms observed for InGaP. In the case where the catalyst layer is suspended over the etched regions, additional material volume is exposed underneath the Au as the off-metal regions continue to etch, allowing for mass transport pathways. In contrast, for the case where the metal conforms to the underlying profile, mass transport underneath the metal is impeded by a limited path for simultaneous HF access and material removal, thereby leading to reduced etch rates (*vide infra*). The limited path for solution access and mass transport of dissolved products is visible in Figure 5.3e-h as a narrow gap at the Au/InGaP interface at the window edge.

5.5.3 Confirming Catalytic Influence

In order to validate the catalytic role of the metallic layer in the selective oxidation of $In_{0.49}Ga_{0.51}P$, etching investigations were next carried out using Au and Cr masks for comparison. A series of i-InGaP samples were patterned with Cr using the same preparation methods and etched under the same conditions as the Au-patterned InGaP (*vide supra*). The SEM images in panels a and b of Figure 5.5 show Cr-patterned InGaP samples prior to and after being subjected to I-MacEtch, respectively. In the case of the Cr/InGaP system, no observable etching is found; only deterioration of Cr mask is noted (visible cracks in metal layer), likely due to slow dissolution in HF [125]. This supports the understanding that the etching behavior of Au-patterned InGaP is metal-assisted and a consequence of catalytic oxidation, as further discussed below.

A necessary condition for the metal to serve as a catalyst in the redox reaction

between H_2O_2 and the semiconductor is that the redox potential of the metal must lie lower than the ionization potential (i.e., valance band edge) of the semiconductor [21, 22]. Otherwise stated, in order to facilitate the requisite cathodic reaction, the reduction potential (E^0) of the metal must be offset relative to a more negative semiconductor ionization potential, when referenced to the standard hydrogen electrode (SHE). On this basis, while Au (E^0 = +1.50 V/SHE) is commonly used as a catalyst in standard Si MacEtch experiments, Cr (E^0 = -0.74 V/SHE) is known to prohibit catalytic etching [21, 126]. Similar to the case of Si, InGaP has an ionization potential that lies intermediate to the redox potentials of Au and Cr [127]. Thus, a comparison between Au and Cr may determine whether an observed etching effect is simply due to patterned wet chemical etching, or if the metal promotes catalytic etching. Notably, Figure 5.5b and Figure 5.3d show results obtained from identical InGaP samples (composition, thickness, and metal pattern geometry), that were etched under equivalent conditions (solution composition, temperature, and duration), with the only exception being the type of the metal employed. Contrary to the case of the Cr/InGaP system (Figure 5.5), significant etching is observed in the case of the Au/InGaP system (Figure 5.3). This highlights the role of Au as a catalyst that enables a cathodic reaction for the injection of holes into the underlying InGaP film.

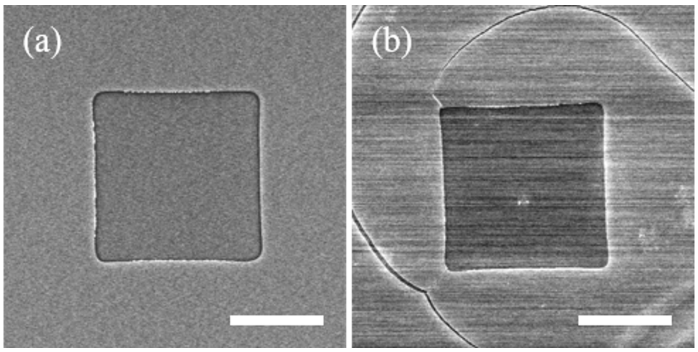

Figure 5.5: SEM images of Cr-patterned i-InGaP (a) before and (b) after being subjected to I-MacEtch for 50 minutes. Scale bars represent 5 μm.

5.5.4 Determining Vertical Etch Rates

Progression of the vertical etch front in off-metal regions is considered next. Figure 5.6 shows VER data collected for InGaP samples of the three distinct doping types. The VER for i-InGaP, p-InGaP, and n-InGaP is determined to be 9.7 ± 0.7 nm/min, 8.7 ± 0.6 nm/min, and 8.8 ± 0.9 nm/min, respectively. Figure 5.6a shows the measured etch depth progression data for i-InGaP samples. A higher etch rate is observed initially (i.e., below 2.5 minutes) due to smaller volumes of oxidized material being consumed by the acid in the I-MacEtch solution near the sample surface. As etching progresses, greater volumes of oxidized material are exposed, and the VER of oxidized material is reduced in comparison to the initial non-linear etching regime. Thus, beyond approximately 2.5 minute etch time, an apparent linear etching regime is observed. A linear etch depth trend was also observed for p- and n-type InGaP samples. Kim and Oh have reported a similar linear I-MacEtch VER evolution (within measured error) during GaP micro-mesa fabrication [40]. In contrast, I-MacEtch of InP demonstrated a saturation of VER over time [13]. Despite the obvious distinctions between the

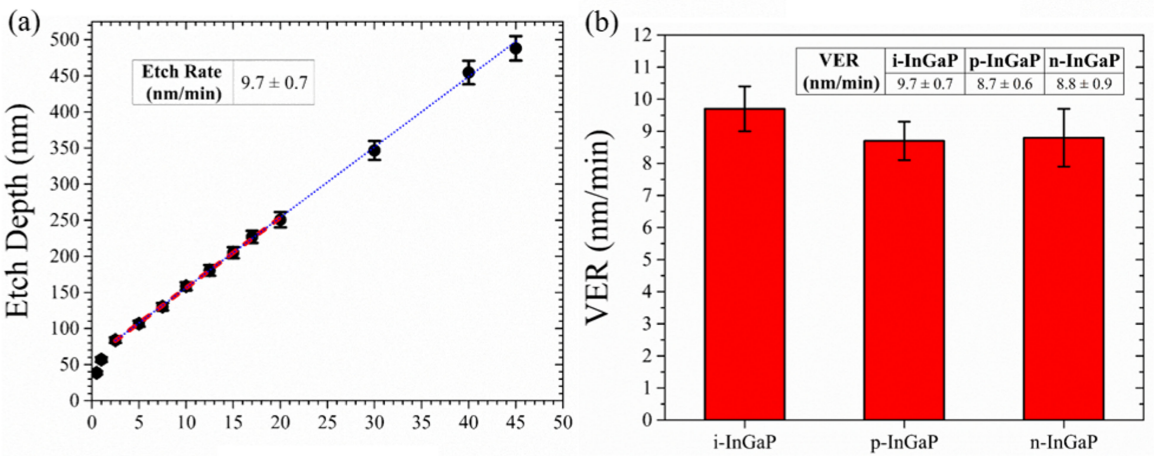

Figure 5.6: (a) Plot of vertical etch depth as a function of I-MacEtch time for i-InGaP. The red dashed line marks the linear regression from which VER is calculated. The blue dotted line shows an extrapolation of the linear regression for longer etch times and demonstrates that the constant etch rate persists for extended etch periods leading toward cavity formation. (b) Comparison of vertical etch rates (VER) for i-, p-, and n-type InGaP samples under common etching conditions.

current study and the experiments reported by Kim and Oh (e.g., catalyst type, thickness, and geometry; etchant solution composition; etc.), which can explain the notable absolute VER differences, the common linear trend for InGaP and GaP may highlight an important difference between the I-MacEtch mechanisms of those systems in comparison to that of binary InP. The VER trend difference between InGaP and InP may potentially be related to the absence of a distinct undissolved oxide layer at the Au/InGaP interface, which was observed in the case of InP I-MacEtch. However, further analysis is required beyond the current study to clarify this point (*vide infra*).

Figure 5.6b summarizes the representative VER for InGaP samples of all three doping types, which is defined as the measured slope of the etch depth vs. etch time trend for each sample set in the linear etch regime. To ensure etch reproducibility and measurement repeatability, each depth data point (e.g., Figure 5.6a) was calculated as the mean value collected from at least six distinct samples etched for the same amount of time, and with at least ten measurements per sample, based on cross-sectional SEM imaging. The error bars in Figure 5.6a represent the first standard deviation from the mean for depth measurements analyzed at a given etch time. Multiple etch times were analyzed to determine the overall etch rate (i.e., Figure 5.6b) for each doping type, based on the slope of a linear fit. Therefore, the data highlighted by the red dashed line in Figure 5.6a shows the linear regime from which the etch rate of i-InGaP was calculated to be 9.7 ± 0.7 nm/min. This linear regression is extended toward data points representative of longer etch durations by the blue dotted line in Figure 5.6a, which indicates a constant etch rate prior to the formation of cavities in the InGaP layer after approximately 50 minutes. In the limit of extended etch times required for the formation of cavities in the InGaP layer, the influence of the non-linear etching regime (i.e., less than 2.5 minutes) becomes negligible. Thus, the linear regime marked by the red dashed line in Figure 5.6a was chosen for the calculation of etch rate because this constant etch rate is representative of the relevant etch depths of

interest for the current study. Etch rates for n- and p-type InGaP were determined in the same manner.

In the I-MacEtch process, the catalyst or plane of hole injection does not sink, in contrast to forward MacEtch. In such a scenario, and due to the finite extent of oxidized material under the catalyst, a corresponding limit to catalytic etching will arise and lead to etch rate saturation, as reported in the case of InP I-MacEtch [13]. Under otherwise constant I-MacEtch conditions, InGaP samples of sufficient thickness (i.e., to prevent cavity formation) are expected to eventually experience such an etch rate saturation. In the current study, since thin InGaP films of 500 nm thickness are used, a saturation effect is not observed prior to cavity formation.

While a comparison of vertical etch rates between i-, n-, and p-type GaAs in the forward progression MacEtch regime has been previously reported [20], no such comparison of etch rate dependences upon doping type has been presented to date (to the authors knowledge) for I-MacEtch of III-V compounds. The current set of measurements have shown that InGaP VER in the I-MacEtch regime is independent of doping type, as all i-, p-, and n-type samples have shown comparable etch rates within the measured errors with no apparent trend favoring enhanced etch rate for one type over another. In comparison to the I-MacEtch VER values reported for n-InP [13] and n-GaP [40], the current study shows a reduced n-InGaP VER by a factor of $\sim$0.44 and $\sim$0.23, respectively. The etch rates reported here are also substantially lower than the I-MacEtch VER values presented by Lee et al. for n-GaAs under exposure to ultra-violet (UV) radiation (i.e., $\sim$130 nm/min) [34]. However, due to the large number of dissimilar experimental parameters across the listed set of most comparable studies (e.g., size, thickness, and type of catalyst features; conformal vs. overhanging catalyst profile; ratio of catalyst area to off-metal area; dopant concentration; I-MacEtch solution composition; with or without UV exposure; etc.) direct I-MacEtch VER-to-composition correlations cannot be made.

5.5.5 Support for Hole Injection into Valance Band

In the absence of consistent VER comparisons in the I-MacEtch regime, etch rate dependences upon doping type are considered from literature pertaining to both III-V and Si systems in the forward MacEtch regime. For forward MacEtch of GaAs, consistently greater VER values were observed for p-type samples, independent of etchant temperature, dilution ratio, and oxidant concentration [20]. In contrast, Lai et al. have shown that for forward MacEtch of Si in solutions with comparable HF proportions of $\rho = [HF]/\{[HF]+[H_2O_2]\} = 0.68$ as in the current study, p-type samples showed reduced etch rates relative to n-type Si, by a factor of $\sim$0.85 [23]. In the case of Si, the lower forward MacEtch rate of p-type samples can be attributed to Schottky barrier-induced hole drift away from the metal/semiconductor interface. However, the same explanation cannot hold for the current InGaP I-MacEtch study, since the etch-front progresses in off-metal areas and evidence for preferential localization of the hole distributions at the Au/n-InGaP interface (i.e., forward MacEtch) has not been observed. Therefore, the VER of InGaP in the I-MacEtch regime appears to be independent of differences in Fermi energy and workfunction. This is consistent with the model for metal-catalyzed etching whereby the offset between metal redox potential and semiconductor ionization energy is more critical than the availability and type of free carriers [21, 22].

5.5.6 Evaluation of Heterostucture Effects

Next, the heterostructure I-MacEtch stage is considered. Figure 5.3d,h shows SEM images obtained immediately after the InGaP layer has been locally etched through, marked by the formation of a cavity in the center of the off-metal window (indicated by a white arrow in Figure 5.3d,h). The InGaP layer becomes progressively thinner towards the center of the window, with an ultra-thin InGaP nanofoil surrounding the cavity location. The nanofoil thickness is tunable with etch time, and Figure

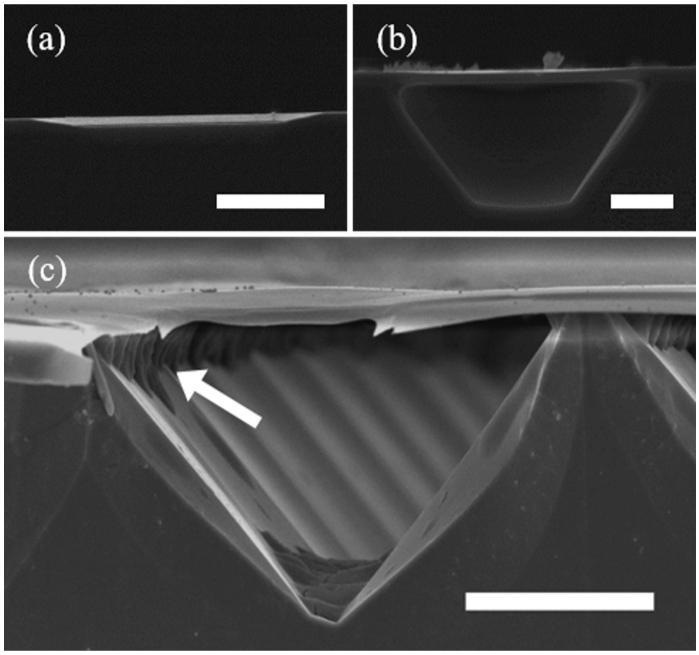

Figure 5.7: Cross-sectional SEM images of Au-patterned i-InGaP showing a sample (a) before central cavity generation (etch time of 20 minutes) and (b, c) after central cavity generation and formation of the suspended InGaP foil (after an etch time of 50 minutes). A cross-sectional view of an ordered array of GaAs micro-trenches and suspended InGaP nanofoils with re-entrant profiles in the GaAs substrate indicated by the white arrow is shown in (c). The Au layer is observed on top of the suspended InGaP foil at the sample surface. Scale bars in (a, b) represent 2 μm, and in (c) represent 10 μm.

5.3d shows the nanofoil suspended above a trench formed in the underlying substrate. The micro-scale trench underneath the overhanging InGaP nanofoil is formed by the rapid dissolution of the GaAs substrate, which is accommodated by HF access and mass transport pathways through the cavity. The SEM images in Figure 5.7 show the cross-sectional etch progression through the InGaP film for i-InGaP samples. Figure 5.7a shows an example of a sample that has been subjected to the I-MacEtch solution, though prior to the time of cavity formation; thus, the InGaP film has not yet been etched through. Alternatively, Figure 5.7b shows a cross-sectional view of a sample subjected to I-MacEtch beyond the point of cavity formation, wherein a micro-trench is generated in the GaAs substrate underneath the InGaP window. Figure 5.7c illustrates the ordered pattern of dissolved GaAs micro-trenches directly below the center of each window in the array. It should be noted that Figure 5.7b was

not cleaved at the center of the window for cross-sectional imaging, which explains why a centrally-located cavity is not apparent in the InGaP layer along the imaging plane and why the trench in the underlying GaAs does not converge to a point at the base (i.e., an inverse pyramid shape). As described above, holes are injected through the metal and into the underlying semiconductor throughout the entire etching process such that hole diffusion forms a hemispherical distribution around each injection site. An interesting consequence of subjecting heteroepitaxial samples to such an I-MacEtch process is the differential catalytic oxidation of the epilayer and the underlying substrate. If the hole diffusion length is larger than the thickness of the epitaxial layer, then the substrate will be continuously oxidized while the epitaxial layer is being etched. The hole distribution is likely to differ from layer to layer based on the material properties; however, an important observation is that without HF access to the underlying oxidized substrate for material dissolution, the substrate becomes heavily oxidized until it reaches a saturation point. Here, with the GaAs substrate being heavily oxidized throughout the InGaP etching phase, upon cavity formation in the epilayers, a rapid dissolution of GaAs is observed with a vertical etch rate of approximately 9 μm/min.

The post-I-MacEtch nanofoil heterostructure is more clearly revealed via EDX mapping. Figure 5.8a shows a cross-sectional SEM image of an i-InGaP sample (i.e., 500 nm i-InGaP film on a GaAs substrate), with a corresponding set of EDX maps representative of elemental In, Ga, Au, P, and As shown in panels b-f, indicating the composition of the final nanofoil structure. Figure 5.8d shows the presence of the Au catalyst layer on the surface of the sample. Panels b, c, and e show the InGaP layer in the same vicinity as the Au film, and panels c and f show the GaAs substrate underneath the InGaP film. It is noted that Au, In, and P are only present along the nanofoil near the surface of the sample. Elemental As is only detected beneath this layer, corresponding to the location of the GaAs substrate, and Ga is detected in both

the InGaP layer and GaAs substrate, as anticipated. Figure 5.7b and Figure 5.8a indicate the etch front in the GaAs substrate progresses along the {111} planes (i.e., micro-trench sidewalls are oriented 54.7° relative to (100) substrate surface plane), which suggests crystallographically preferential etching occurs in the GaAs with the InGaP window acting as a patterned mask. The etching behavior along the GaAs{111} planes agrees with the conventional selective chemical etching behavior of GaAs [128], including the re-entrant profile at the intersection of the InGaP nanofoil and the GaAs{111} planes seen in Figure 5.7c and Figure 5.8a (indicated by white arrows). While the GaAs substrate exhibits masked chemical etching behavior, enhanced etch rates are expected during the early stages of GaAs dissolution, and corresponding to etch depths equal to the hole diffusion length (oxidation range in the I-MacEtch regime). The distinct etch rates and etch progression behavior between the InGaP film and the GaAs substrate demonstrates the advantage of utilizing dissimilar oxidation effects and hole distributions in heteroepitaxial systems for the formation of suspended

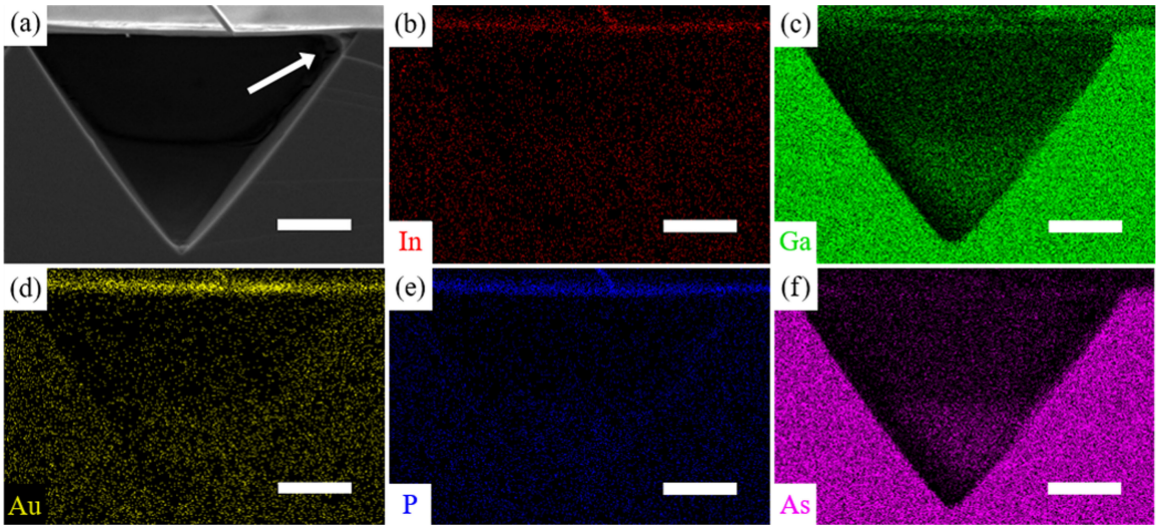

Figure 5.8: (a) Cross-sectional SEM image of Au-patterned i-InGaP nanofoil suspended over a micro-trench in the GaAs substrate after an etching period of 50 minutes. Corresponding EDX maps are shown, which are representative of elemental (b) In, (c) Ga, (d) Au, (e) P, and (f) As. The Au-covered InGaP nanofoil is prominently observed in panels (b), (c), (d), and (e), while absent in the elemental As map (f). The white arrow points to the re-entrant profile formed in the GaAs substrate. All scale bars represent 3 μm.

structures. In the current study, beyond the point of cavity formation by I-MacEtch, the etch rate of GaAs is sufficiently high in comparison to InGaP to allow for the formation of suspended nanofoils.

5.5.7 Model for Etching Behavior

The schematic illustrations shown in Figure 5.9 depict the Au/InGaP/GaAs I-MacEtch mechanisms, processes, and resulting structures. Figure 5.9a is a model of the mechanisms and reactions that occur during I-MacEtch. First, a cathodic reaction occurs with oxidant reduction at the solution/Au interface (black arrow), accompanied by hole injection into the underlying semiconductor at the Au/InGaP interface (blue arrow). An anodic reaction occurs with the dissolution of oxidized off-metal regions (red arrow). The catalytic etching behavior of InGaP, as observed here, can be understood in terms of hole distributions corresponding to adjacent injection sites (i.e., metal/semiconductor interfacial regions). Figure 5.9b depicts hole distributions as regions marked by white dashed arrows, resulting from the catalytic oxidation at

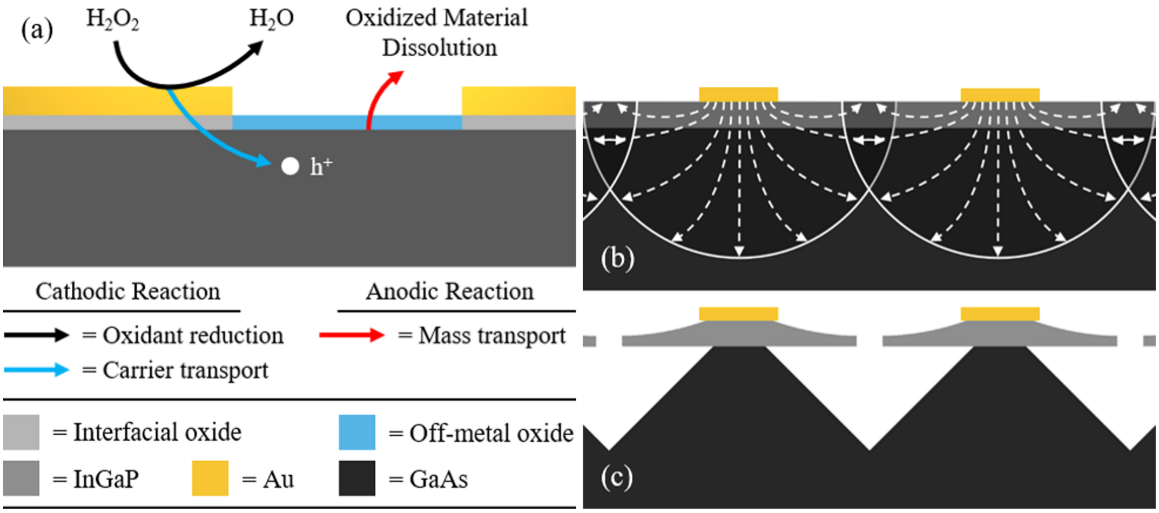

Figure 5.9: Schematics showing (a) the I-MacEtch mechanism and reactions, (b) a qualitative depiction of neighboring hole distributions in the InGaP layer (light gray) and GaAs substrate (dark gray), and (c) a model of the suspended InGaP nanofoil with cavity aligned with the center of the micro-trench generated in the underlying GaAs substrate.

neighboring Au locations. The hole distributions and oxidation profiles can extend beneath the InGaP layer (shown as the light gray film in Figure 5.9b) and into the GaAs substrate (dark gray). Moreover, an overlap of the neighboring distributions at the midpoint between two Au features marks the location of enhanced I-MacEtch and corresponds to the site of cavity formation in the InGaP layer. Figure 5.9c represents the features generated in the oxidized GaAs substrate after the cavity formation and when HF has penetrated the InGaP layer (note: the viewing plane in Figure 5.9c corresponds the center of the off-metal window, and simply depicts a row of neighboring features; thus, no features from background rows are observed, unlike those seen in Figure 5.7c). The InGaP layer acts as a patterned mask for the rapid etching of the oxidized GaAs regions near the interface and deeper substrate regions along the {111} planes. The position of the cavity in the InGaP layer is aligned with the initial GaAs etching location and corresponds to the bottom of the inverse pyramidal micro-trench that is etched in the GaAs substrate. Thus, the mesh-patterned Au catalyst enables I-MacEtch of the InGaP layer, but also determines the location at which GaAs etching is initiated. The morphology of the micro-trenches formed in the GaAs substrate is not expected to vary with changes in the dimensions of the Au catalyst pattern. Dissolution of GaAs beneath the InGaP window also causes the InGaP nanofoil to be suspended over the micro-trench.

5.6 Conclusions

Au-assisted and inverse-progression MacEtch (I-MacEtch) of the heteroepitaxial $In_{0.49}Ga_{0.51}P$/GaAs material system has been demonstrated, along with a method for fabricating suspended InGaP nanofoils of tunable thickness in solutions of hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). Vertical etch rates for nominally undoped, p-type, and n-type InGaP are determined to be ∼9.7 nm/min, ∼8.7 nm/min, and ∼8.8 nm/min, respectively. The VER values are independent of doping type, as all i-,

p-, and n-type samples have comparable etch rates within the measured errors with no apparent trend favoring enhanced etch rate for one type over another. Therefore, the VER of InGaP in the I-MacEtch regime appears to be independent of differences in Fermi energy and workfunction. This is consistent with the model for metal-catalyzed etching whereby the offset between metal redox potential and semiconductor ionization energy is more critical than the availability and type of free carriers.

The evolution of I-MacEtch in the InGaP/GaAs system is tracked, leading to the formation of nanocavities located at the center of off-metal windows. Upon nanocavity formation, additional localized mass-transport pathways to the underlying GaAs substrate permit its rapid dissolution. The unique suspended InGaP nanofoil structures described here demonstrate that differential oxidation and dissolution rates can be exploited during I-MacEtch of III-V heterostructures for single-step nano-fabrication of complex architectures. It is anticipated that this process can be exploited for the fabrication of nanoscale, three-dimensional heterostructure geometries for device applications in photonics (waveguides), photovoltaics (multijunction solar cells), optoelectronics (lasers), and nanoelectronics (HEMTs).

5.7 Future Works

In future work, additional structural characterization via transmission electron microscopy (TEM) and chemical analysis via X-ray photoelectron spectroscopy (XPS) and/or Auger electron spectroscopy (AES) is required to understand the basis of the I-MacEtch mechanism, specifically related to the potential absence of the distinct oxide phase that was observed at the metal/semiconductor interface in the case of InP I-MacEtch. The nature of a suspended catalyst profile, observed previously for GaP and InP, in comparison to the current conformal Au profile can likewise be investing via TEM in future efforts, which would also identify potential crystallographic dependences at the etch front. Lastly, further investigation of etching rate dependences

upon dissimilar micron-scale Au mesh dimensions and exploration of nanometer-scale catalyst features, which may permit enhanced solution access to oxidized regions and potentially modify the inverse etching behavior observed in the current study, are areas of future consideration.

Chapter 6

Au-Catalyzed AlGaAs for Ordered Nanopillar Arrays

6.1 Summary

The ternary III-V semiconductor compound, $Al_xGa_{1-x}As$, is an important material that serves a central role within a variety of nanoelectronic, optoelectronic, and photovoltaic devices. With all of its uses, the material itself poses a host of fabrication difficulties stemming from conventional top-down processing techniques. For example, processing via reactive-ion etching (RIE) can generate highly anisotropic features; however, high energy ion bombardment can cause detrimental sidewall damage and generate lattice defects that degrade optical and electrical properties. These issues can be avoided by using traditional wet etching, although its isotropic nature prohibits formation of features with tunable aspect ratios. On the other hand, metal-assisted chemical etching (MacEtch) is a low-cost and benchtop technique that simultaneously enables anisotropic etching while avoiding the detrimental effects of RIE. Here, inverse-progression MacEtch (I-MacEtch) of Au-patterned $Al_xGa_{1-x}As$ demonstrated for the first time as a method for the fabrication of ordered nanopillar arrays in a solution of citric acid ($C_6H_8O_7$) and hydrogen peroxide (H_2O_2). The I-MacEtch evolution is tracked in time for $Al_xGa_{1-x}As$ samples with compositions defined by $x = 0.55$, $x = 0.60$, and $x = 0.70$. The vertical and lateral etch rates (VER and LER, respectively) are shown to be tunable with Al fraction and temperature of the etching solution, based on modification of catalytically-injected hole distributions (Figure 6.1a). Control

over the VER/LER ratio is demonstrated by tailoring etch conditions for single-step fabrication of ordered AlGaAs nanopillar arrays with predefined aspect ratios. Ordered arrays of post-I-MacEtch $Al_{0.70}Ga_{0.30}As$ nanostructures before and after Au-removal via mechanical exfoliation is demonstrated in Figure 6.1 (panels b and c, respectively). Maximum VER and LER values of ∼40 nm/min and ∼105 nm/min, respectively, are measured for $Al_{0.55}Ga_{0.45}As$ at a process temperature of 65 °C. The nanofabrication methodology outlined here can be directly applied to the processing of devices such as high electron mobility transistors, light-emitting diodes, distributed Bragg reflectors, lasers, and tandem junction solar cells containing AlGaAs components.

6.2 Motivation

Traditional top-down nanostructure fabrication techniques include patterned wet-etching and reactive-ion etching (RIE), though these methods come with a variety of limitations and disadvantages [5, 6]. A major advantage of RIE is its directionality and ability to generate highly anisotropic geometries. However, it often requires processing at elevated temperatures with hazardous gases. Additionally, RIE causes sidewall

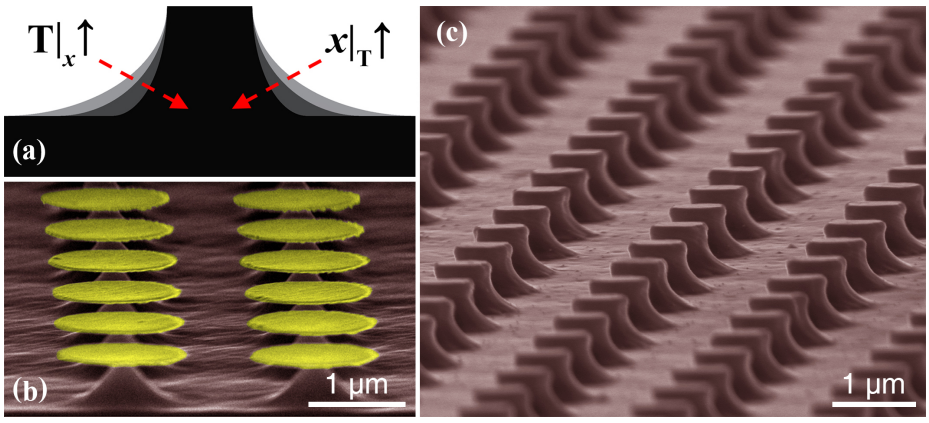

Figure 6.1: (a) Model highlighting that the aspect-ratio of $Al_xGa_{1-x}As$ nanostructures can be tuned with solution temperature (T) for a constant x, and with Al composition (x) at a constant T. (b) Near cross-sectional SEM image demonstrating post-I-MacEtch of Au-patterned AlGaAs. (c) Tilted-view SEM image showing an ordered array of $Al_{0.70}Ga_{0.30}As$ nanostructures after Au-removal via mechanical exfoliation.

damage and lattice defects, which are undesirable as devices continue to move toward smaller dimensions and higher aspect ratio features [7]. Likewise, patterned wet-etching is advantageous for being solution-based and having fabrication compatibility with conventional benchtop semiconductor processing methods. Although its simplicity and cost-efficiency is attractive, patterned wet-etching lacks the ability to generate high aspect ratio features because of its isotropic nature and/or crystallographic etching dependencies [8].

$Al_xGa_{1-x}As$ is a ternary IIIV alloy that remains nearly lattice matched with GaAs for all values of x spanning the compositional bounds of its binary components, GaAs and AlAs. This allows for its electrical and optical properties to be easily tuned as a function of composition [129]. AlGaAs is commonly utilized in nanoelectronics, including heterojunction bipolar transistors and high electron mobility transistors [130, 131]. Additionally, AlGaAs is regularly used in photonic and optoelectronic devices, such as light-emitting diodes (LEDs) [121, 132], lasers [133, 134], distributed Bragg reflectors (DBRs) [135, 136], and tandem-junction solar cells [137, 138]. Despite its usefulness as a tunable and functional ternary alloy semiconductor, AlGaAs processing poses a multitude of challenges, particularly for the fabrication of micro- and nano-structures. Dry etching is capable of accurately generating high-aspect-ratio features, though ion bombardment can be particularly detrimental to the electrical and optical properties of semiconductor nanostructures with high surface-to-bulk-state ratios [139]. Specifically, RIE can increase surface recombination velocity and lower optical output [140], cause scattering losses from sidewall damage [139], and generate high concentrations of carrier trap defects [141]. Likewise, wet etching has its own limitations, with many common etchants capable of isotropically attacking AlGaAs, including hydrofluoric acid (HF) [142, 143], buffered oxide etch (BOE) [144], nitric acid (HNO_3) [145], hydrochloric acid (HCl) [143, 146], sulfuric acid (H_2SO_4) [147, 148], and phosphoric acid (H_3PO_4) [149, 150]. The above acids wet etch $Al_xGa_{1-x}As$ at an

increasing rate with either x, temperature, etchant concentration, or a combination of these three variables [151]. Because of this myriad of processing constraints, AlGaAs-based devices are inherently more difficult to fabricate in comparison to other IIIV alloys, such as InGaP [149]. To that end, Petter et al. outline a conventional, multistep method for the generation of AlGaAs microdisks as follows: photoresist is patterned on the topmost AlGaAs epilayer, followed by mesa etching via dry etching and undercutting of the GaAs substrate with a citric acidhydrogen peroxide solution [152]. Although citric acid-based solutions etch GaAs and InGaAs [130], they are relatively ineffective at etching other semiconductor compounds commonly incorporated with GaAs. For example, AlGaAs and InGaP are used as etch-stop layers due of their excellent selectivity over GaAs in citric acid-based solutions [130, 131]. Solutions consisting of hydrogen peroxide and citric acid etch $Al_xGa_{1-x}As$ slower with increasing x [150], with GaAs etching at 314 nm/min and $Al_{0.30}Ga_{0.70}As$ etching at 2.7 nm/min [153]. Tong et al. also report GaAs etching at ∼321 nm/min and $Al_{0.45}Ga_{0.55}As$ etching at 1.4 nm/min, and note that the reason AlGaAs acts as an etch-stop layer is due to the limited etch rate of the oxide that forms in citric acidhydrogen peroxide solutions (i.e., Al_xO_y) [141].

6.3 Introduction

Inverse-progression MacEtch (I-MacEtch) behavior of Au-catalyzed AlGaAs is reported. The etch progression is tracked in time for $Al_xGa_{1-x}As$ samples with $x = 0.55$, $x = 0.60$, and $x = 0.70$, which are etched in a consistent solution at three different process temperatures of 35, 50, and 65 °C. The I-MacEtch solution consists of a relatively benign mixture of liquid citric acid and hydrogen peroxide. The VER and LER values are quantified for each $Al_xGa_{1-x}As$ composition etched within the overall I-MacEtch parameter space, and the VER/LER ratio is calculated. The VER and LER values are determined to range from 39.8 to 1.1 nm/min and 105.4 to 3.3 nm/min, respectively.

Etch rates, as well as the etch anisotropy (i.e., relative VER to LER ratio), are shown to be tunable with Al composition and the etching solution temperature. The etch rate enhancements can primarily be attributed to the modification of the size of oxidized material distributions surrounding the Au catalysts disks, which increase with time and etch temperature and decrease with Al fraction. The catalytic effect is demonstrated using catalyst layers of substantially disparate reductionoxidation potentials (i.e., Au and Cr). MacEtch conditions and AlGaAs nanostructures are reported here that can be utilized for various device applications in photovoltaics, photonics, optoelectronics, and nanoelectronics. This single-step fabrication method combines many of the advantages of processing by RIE and conventional wet etching and offers the requisite versatility and controllability to generate ordered $Al_xGa_{1-x}As$ nanopillar arrays of controlled dimensions.

6.4 Experimental Details

In this study, all AlGaAs samples were grown via a 3 × 2" Aixtron close-couple showerhead metal-organic chemical vapor deposition (MOCVD) reactor, on GaAs(100)

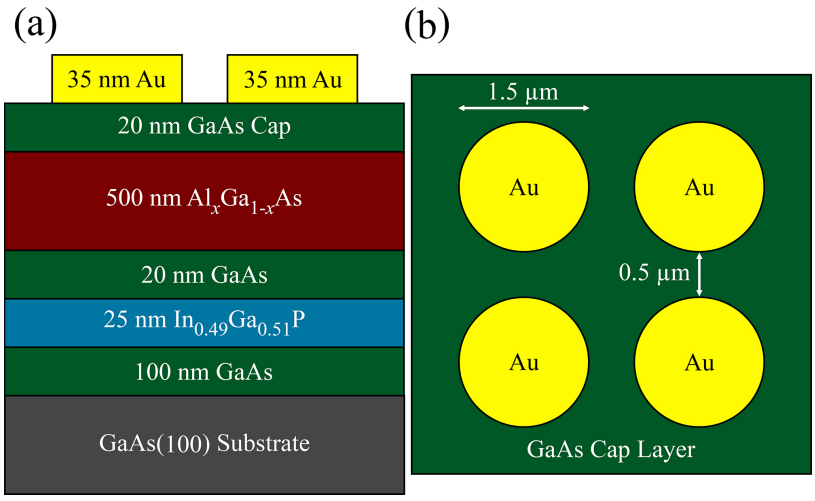

Figure 6.2: Schematics illustrating (a) cross-sectional view of epi-structure and (b) top view of a sample, along with deposited Au catalysts on both.

substrates. A 10 min oxide desorption step was first conducted at 720 °C under a constant supply of arsine (AsH_3). A 100 nm GaAs layer was grown first. Then, 25 nm $In_{0.49}Ga_{0.51}P$ and 20 nm GaAs films were grown prior to AlGaAs growth. All $Al_xGa_{1-x}As$ films were grown at a temperature of 700 °C and had a thickness of 500 nm. Al, Ga, and As were supplied using the precursors trimethylaluminum [TMAl, $Al(CH_3)_3$], trimethylgallium [TMGa, $Ga(CH_3)_3$], and AsH_3, respectively. Following $Al_xGa_{1-x}As$ growth, a 20 nm GaAs cap layer was grown. The InGaP and AlGaAs compositions were measured by X-ray diffraction (XRD; Bruker D8 Discover). A schematic representation of the epi-structures employed in this work is shown in Figure 6.2a.

Acetone, isopropyl alcohol (IPA), and methanol were used to clean the wafers following growth. An i-line photolithographic stepper (GCA Autostep 200) was utilized to generate patterned samples. All metallic catalyst films (i.e., Au and Cr) were deposited via e-beam evaporation (CVC SC 4500) and had a thickness of 35 nm. The Au and Cr patterns were cubic arrays of metallic dots of approximately 1.5 μm diameter, with an approximately 0.5 μm wide spacing between each dot. Thus, otherwise identical samples of Au and Cr dot-patterned arrays were prepared for comparison. A schematic representation of the metallic patterning used throughout this work is shown in Figure 6.2b.

A two-part mixture of a liquid citric acid/deionized water (DI-H_2O) solution (to support the anodic reaction and material dissolution) and hydrogen peroxide (to promote the cathodic reaction and hole injection) were used for all MacEtch trials. First, crystalline citric acid (99.5+% $C_6H_8O_7$) was mixed with DI-H_2O, with a volumetric ratio of 2 g:1 mL ($C_6H_8O_7$:DI-H_2O). For simplicity in later discussion, "citric acid crystals" or "anhydrous citric acid" will refer to crystalline $C_6H_8O_7$ powder and "liquid citric acid" or "citric acid" will refer to the solution of 2 g $C_6H_8O_7$:1 mL DI-H_2O. Because of this reaction being endothermic, the solution was stirred on

a hot plate at 35 °C for 1 hr to ensure complete dissolution. Then, 30% hydrogen peroxide (H_2O_2) was mixed into the citric acid solution at a volume ratio of 5 parts citric acid to 1 part H_2O_2. The mixture was raised to the target etching temperature, and the desired temperature was maintained for 15 min before any experiments were performed. The solution temperature was maintained throughout the duration of each experiment to ensure consistency. Elemental mapping was performed using energy dispersive X-ray spectroscopy (EDS; Zeiss Supra 55VP), and all samples were imaged using scanning electron microscopy (SEM; Zeiss Ultra 55 and Hitachi S-4000). Representative EDXS elemental mapping can be found in Figure 6.3.

6.5 Results and Discussion

In the discussion that follows, experimental data are presented for I-MacEtch trends leading to quantitative analyses of VER and LER. The quantitative trends are

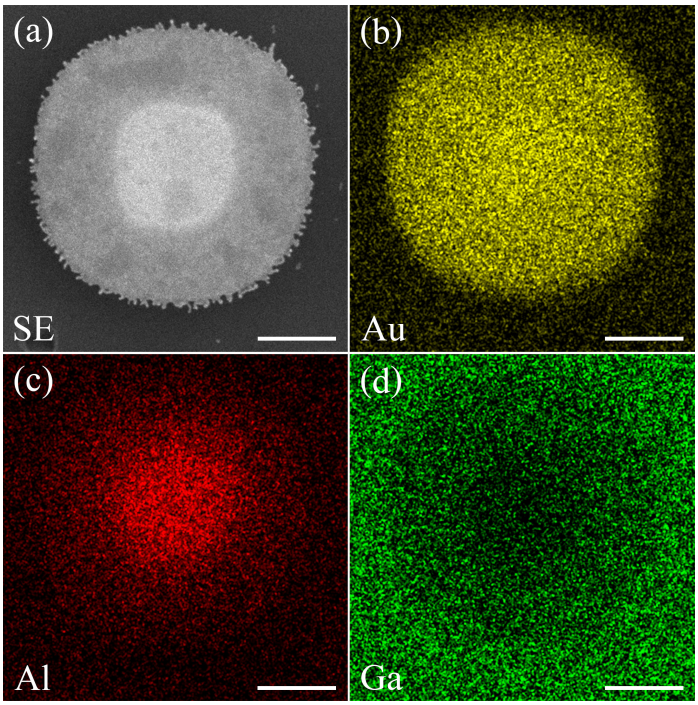

Figure 6.3: (a) Top-view SEM image of an Au-patterned $Al_{0.70}Ga_{0.30}As$ sample after being subjected to the I-MacEtch solution for $t = 60$ min at $T = 50$ °C. Corresponding EDX maps represent elemental (b) Au, (c) Al, and (d) Ga. Scale bars represent 500 nm.

described with respect to several experimental variables, including the etch evolution with time, and the effect of Al concentration and etch solution temperature. Next, the basis for catalytic etching is presented through a comparison of identical samples patterned with Au and Cr and etched under constant conditions. Lastly, a qualitative model is provided to summarize all experimental results.

6.5.1 Observable Inverse-Progression

The etch progression was tracked in time, t, for $Al_xGa_{1-x}As$ samples with $x = 0.55$, $x = 0.60$, and $x = 0.70$. Figure 6.4 shows SEM images obtained at 45° stage tilt that demonstrate the inverse MacEtch behavior of Au-patterned $Al_{0.70}Ga_{0.30}As$ samples that were etched at a temperature of $T = 50$ °C over durations ranging from $t = 20$ min to $t = 60$ min. The vertical etch depth and lateral etch width, both in the

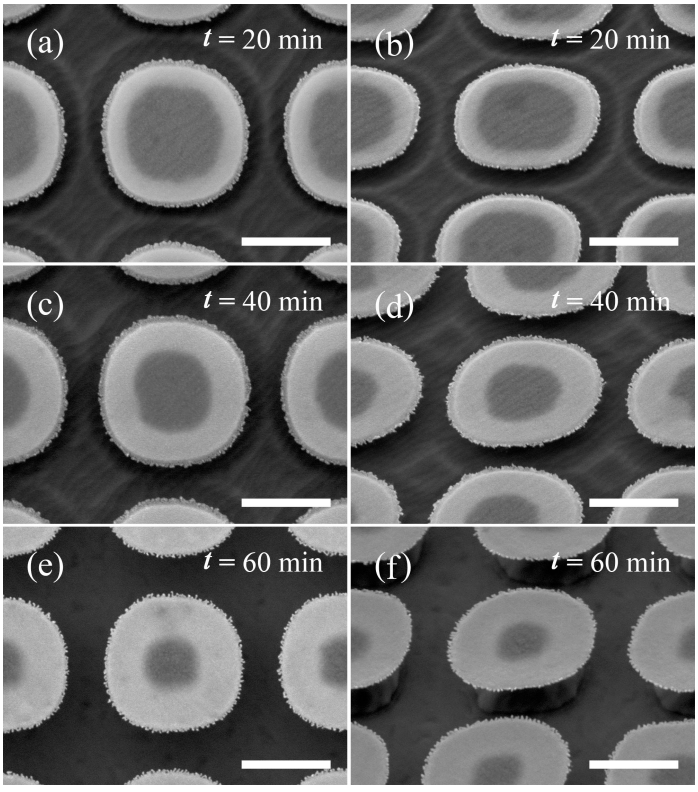

Figure 6.4: Top-view (left-side column) and 45° tilted-view (right-side column) SEM images of Au-patterned $Al_{0.70}Ga_{0.30}As$ samples etched at 50 °C for (a, b) 20 min, (c, d) 40 min, and (e, f) 60 min. Scale bars represent 1 μm.

Au-interfaced and off-metal regions, increase with time. The same inverse-progression MacEtch behavior is observed for $x = 0.55$ and $x = 0.60$ sample sets etched under identical conditions and for all three AlGaAs compositions etched in the same solution at $T = 35$ °C and $T = 65$ °C. All samples either are discussed below or can be found in Figure 6.5.

The extent of injected hole distributions can be identified in Figure 6.4a,b as the disk-shaped etched region immediately surrounding the Au catalyst pads. The lateral extent of hole distributions about their injection sites (i.e., about the Au catalysts) is observed to increase with time, until the hole distribution dimensions are hidden by the overlap of neighboring profiles (i.e., after $t = 40$ min) and followed by the complete dissolution of off-metal regions (i.e., after $t = 60$ min). Figure 6.4e,f shows a smooth surface exposed between the bases of the AlGaAs nanostructures after extended etch times, which is likely the underlying InGaP layer. InGaP is known to serve as an effective stop-etch layer in citric acid-hydrogen peroxide solutions [130, 131], and its function as such appears to hold true in the catalytically enhanced system explored

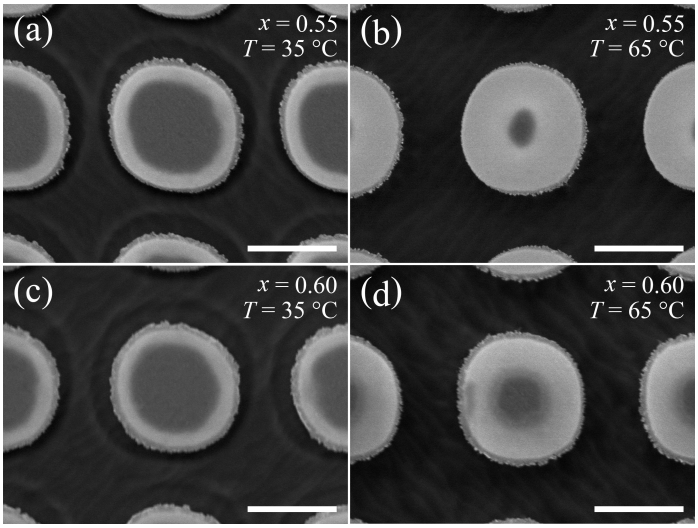

Figure 6.5: Top-view SEM images of Au-patterned $Al_xGa_{1-x}As$ samples, with (a) $x = 0.55$ etched at $T = 35$ C for t = 60 min, (b) $x = 0.55$ etched at $T = 65$ °C for t = 10 min, (c) $x = 0.60$ etched at $T = 35$ °C for 75 min, and (d) $x = 0.60$ etched at $T = 65$ °C for 10 min. Scale bars represent 1 μm.

here. Although the etch rate of InGaP could not be quantified here, the layer did not completely dissolve with prolonged etching after it was first exposed. The lateral extent of the I-MacEtch fabricated nanostructures can be identified by the dark regions at the center of the Au disks. The bright regions at the periphery of the metallic disks indicate the underlying material has been dissolved. That is the dark contrast within the Au disks represents the remaining AlGaAs structure underneath, as seen in the tilted-view images (right-hand column). Notably, in Figure 6.4 the rigid Au catalyst is shown to overhang about the underlying etched profile; this increases solution access to oxidized regions (i.e., the anodic reaction) compared to systems in which the catalyst remains interfaced with the etched profile [42]. The trend observed here is consistent with that reported by Kim et al. for InP [13] and may suggest a similar etching mechanism. That is, distinct oxides may be generated in the Au-interfaced and off-metal regions that are nonsoluble and soluble in the I-MacEtch solution, respectively. Furthermore, as the oxide formed in citric acidhydrogen peroxide solution hinders the dissolution of AlGaAs without the presence of Au [141], the layer formed by catalytic oxidation is likely distinct from the noncatalytically formed phase and supports preferential dissolution in the current I-MacEtch solution.

6.5.2 Influence of Al Fraction

The influence of Al composition on the size of injected hole distributions and therefore the extent of oxidized material volume available for dissolution is considered next. Figure 6.6 shows top-view (left-side column) and tilted-view (right-side column) SEM images of Au-patterned $Al_xGa_{1-x}As$ samples etched under constant conditions. The top, middle, and bottom rows represent $x = 0.55$, $x = 0.60$, and $x = 0.70$ samples, respectively, that have been etched in identical solutions (i.e., constituents and concentrations), at $T = 50$ °C, and for $t = 20$ min. Notably, $Al_{0.55}Ga_{0.45}As$ samples (i.e., panels a and b) experience greater vertical and lateral etching in comparison to

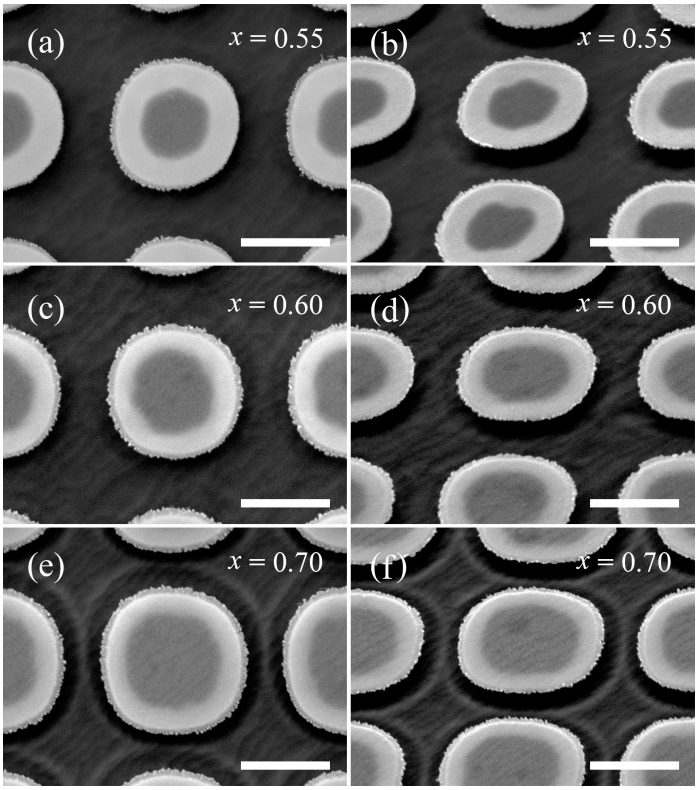

Figure 6.6: Top-view (left-side column) and 45° tilted-view (right-side column) SEM images of Au-patterned AlxGa1-xAs samples, with (a) and (b) $x = 0.55$, (c) and (d) $x = 0.60$, and (e) and (f) $x = 0.70$, etched in a solution at 50 °C for 20 min. Scale bars represent 1 μm.

$Al_{0.70}Ga_{0.30}As$ samples (i.e., panels e and f). Thus, the dissolution profiles extend at a lower rate and become more discernible as x increases due to lack of overlap with neighboring profiles, indicating that VER and LER are inversely proportional to Al content. The same trend was also observed at $T = 35$ °C and $T = 65$ °C and over various etch durations.

6.5.3 Influence of Solution Temperature

Lastly, the role of temperature on the extent of the injected hole distributions is considered. Samples are etched in a consistent solution at varying temperatures of $T = 35$, 50, and 65 °C for comparison. Figure 6.7 shows top-view SEM images of Au-patterned $Al_{0.70}Ga_{0.30}As$ samples etched in the same solution. Figure 6.7a shows a

sample etched at $T = 35$ °C for 60 min, and panels b and c show samples etched for $t = 10$ min at process temperatures of $T = 50$ and 65 °C, respectively. Negligible etching is observed at room temperature. However, comparable etch times are captured for $T = 50$ and 65 °C (i.e., $t = 10$ min). Longer etch times (i.e., $t > 60$ min) are required for the realization of structure formation at $T = 35$ °C. The extent of the dissolved catalytically oxidized material corresponding to each etch temperature and time is seen as a region of dark contrast about the perimeter of the Au disks. Comparing $T = 50$ °C and $T = 65$ °C, a clear increase in the extent of the etched region beyond the catalyst disk is observed at the higher temperature. Likewise, even at extended etch times (i.e., $t = 60$ min), samples processed at $T = 35$ °C exhibit a reduced lateral etching profile. In panels a, b, and c, the total diameter of the catalytically oxidized region (i.e., injected hole distribution) stemming from a single Au disk is measured to be ∼1975 nm, ∼2125 nm, and ∼2325 nm, respectively. Figure 6.7c shows the onset of overlap of neighboring injected hole distributions, whereas Figure 6.7a demonstrates etching prior to the enhancement of overlapping distributions.

Combining the influences of AlGaAs composition and etching temperature on the size of the hole distributions as they progress in time allows for accurate design of etching conditions necessary for fabricating features of targeted dimensions. Figure 6.8 shows a near-cross-sectional SEM image of a post-I-MacEtch $Al_{0.70}Ga_{0.30}As$ sample, following 60 min of etching at $T = 50$ °C and subsequently having the Au catalyst

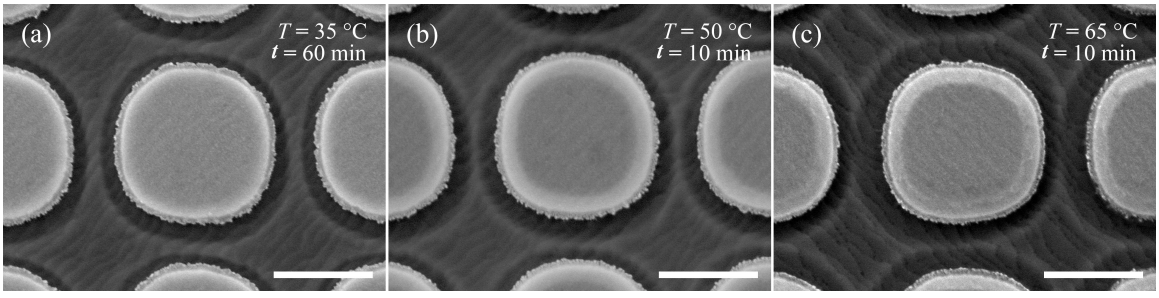

Figure 6.7: Top-view SEM images of Au-patterned $Al_{0.70}Ga_{0.30}As$ samples etched for (a) 60 min at 35 °C and for 10 min at (b) 50 and (c) 65 °C. Scale bars represent 1 μm.

disks removed from the top of the pillars via mechanical exfoliation. Thus, long-range and precisely ordered arrays of nanopillars having diameters of ∼700 nm and heights of 500 nm can be fabricated under these conditions. That is, the entire 500 nm thick layer of AlGaAs has been etched in the off-metal regions, resulting in discrete nanopillar features. It should also be noted that the top of the AlGaAs nanopillars is not believed to be damaged during Au exfoliation, as it is protected by the GaAs cap layer, which can subsequently be removed using a polishing etch. Figure 6.9 below shows a top-view SEM image of an AlGaAs nanopillar following Au removal, and both the GaAs cap layer and the exposed AlGaAs at the periphery of the structure appear to be smooth and free of damage.

6.5.4 Determining Lateral and Vertical Etch Rates

Next, etch rate variations are considered as a function of $Al_xGa_{1-x}As$ composition and I-MacEtch solution temperature. Figure 6.10 summarizes the representative VER and LER, and Figure 6.11 is representative of the VER/LER ratio, for all combinations of x and T explored in the current parameter space. $Al_xGa_{1-x}As$ samples with $x = 0.55$, $x = 0.60$, and $x = 0.70$ are reported for varying amounts of time in the $T = 35$ - 65 °C

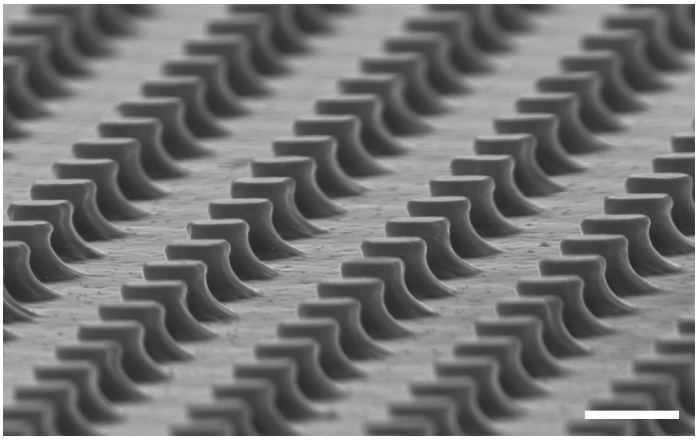

Figure 6.8: 85° tilted-view SEM image showing an Au-patterned $Al_{0.70}Ga_{0.30}As$ sample etched for 60 min at 50 °C. The Au catalysts has been removed from the nanopillars to better illustrate the etched features. Scale bar represents 1 μm.

range. The vertical etch depth and lateral etch width are measured from sample sets consisting of multiple etch times for each $Al_xGa_{1-x}As$ composition and each etching temperature. Multiple samples are analyzed at each etch time, and a minimum of 50 measurements are taken under each condition (i.e., t, x, and T for VER and LER) to ensure etch reproducibility and measurement reliability. The vertical etch depth is captured by cross-sectional SEM imaging and measured from the top of the pillar

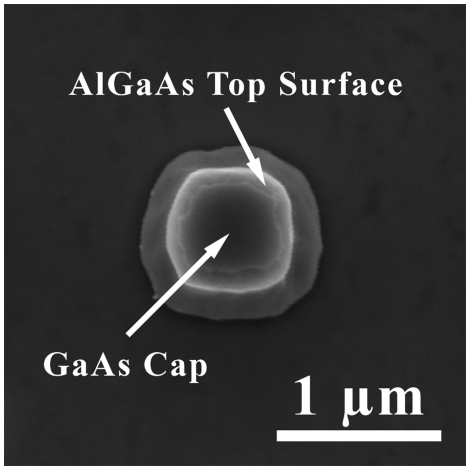

Figure 6.9: Top-view SEM image of Au-patterned $x = 0.70$ $Al_xGa_{1-x}As$ after the Au had been removed via mechanical exfoliation with adhesive tape. The Au catalyst was adhered to the GaAs cap layer. Neither the GaAs cap layer, nor the top surface of the exposed AlGaAs appear damaged.

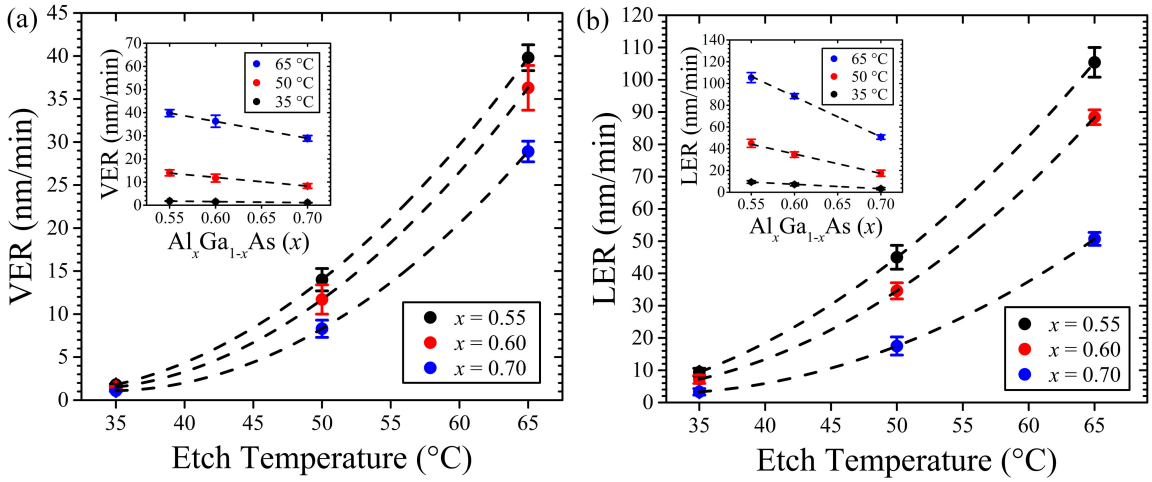

Figure 6.10: Graphs showing exponential dependence upon Al content and linear dependence upon etch temperature (insets) of (a) VER and (b) LER. All regressions are guides to the eye only.

to the bottom-most location at the base of each pillar. As discussed previously for Figure 6.4, the dark region at the center of the Au disks represent the extent of the remaining AlGaAs structure. The lateral etch width is realized by top-view SEM imaging and is measured as the difference between the diameter of the unetched Au catalyst and the diameter of the top of the pillar.

The VER and LER values are extracted from the linear fit of the vertical etch depth or lateral etch width dimensions, as a function of time. The first standard deviation from the regression is represented by the error bars. Both VER and LER were noted to rapidly increase with temperature. Panels a and b of Figure 6.10 show the exponential dependence of VER and LER upon T, respectively, while the insets illustrate the linear dependence of VER and LER upon $Al_xGa_{1-x}As$ composition. A similar nonlinear relationship between temperature and etch rate for Si MacEtch was found by Cheng et al. over a similar temperature regime [154]. Si MacEtch exhibits a forward-progression behavior, which has a fundamental difference from I-MacEtch in that the plane of hole injection is continuously moving. That is, the metal sinks into the substrate as a consequence of preferential dissolution of the oxidized material directly beneath the catalyst [9]. However, it appears forward- and inverse-progression MacEtch share a nonlinear etch rate trend as a function of temperature. This can be explained by considering the role T plays in the catalytic oxidation and dissolution of oxidized material, which is common to both etch progressions. Thus, increasing temperature improves hole injection, hole diffusion, and dissolution rates independent of forward- or inverse-progression MacEtch.

6.5.5 VER-to-LER Ratio: Etch Anisotropy

Figure 6.11 shows the VER/LER ratio as a function of T and its dependence upon x in the inset. The plotted VER-to-LER ratio trend is intended to demonstrate the combined influence of VER and LER on the etch anisotropy. The trends observed here

indicate that both VER and LER increase exponentially with etch temperature and decrease linearly with Al fraction. Moreover, etch anisotropy increases with Al fraction at a constant etch temperature and also with etch temperature at a constant Al fraction. Although etch temperature has a stronger influence than x on both VER and LER over the experimental range studied here (Figure 6.10), the etch anisotropy (i.e., relative VER-to-LER) increases more rapidly with x but tends toward a saturation trend with increasing etch temperature (Figure 6.11). It should be noted that vertical etch depth is inherently bound by the thickness of the AlGaAs epilayer. That is, once off-metal regions have etched completely through the vertical extent of the $Al_xGa_{1-x}As$ layer, then lateral etching may only continue in the regions under the Au disks.

The increase in etch rate with etch temperature can be explained by considering two key consequences: (1) the increased size of hole distributions, and therefore extent of oxidized material, and (2) the greater probability of bond liberation for oxidized material dissolution. Catalytic oxidation increases with temperature due to a larger number of holes being generated through thermally activated catalytic decomposition of H_2O_2 as well as enhanced hole diffusion from the metal/semiconductor interface [49, 50]. That is, the number of holes generated at the solution/Au interface and

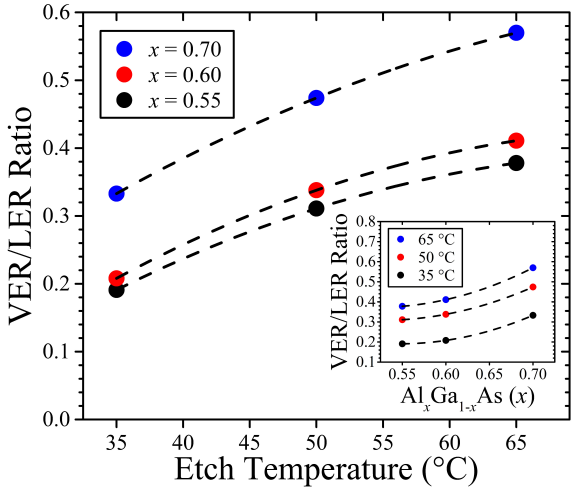

Figure 6.11: Graph showing VER-to-LER ratio dependence on T and x (inset). All regressions are guides to the eye only.

the number of holes injected at the Au/semiconductor interface both increase with temperature. As injected holes diffuse from their injection sites at a higher rate with increasing temperature [51], the size of hole distributions expands correspondingly and provides additional material in an oxidized state that is exposed to and soluble in the I-MacEtch solution. With all other conditions held constant, increasing temperature raises the LER relative to the VER due to a larger lateral area of exposed semiconductor becoming oxidized, simply based on the AlGaAs layer thickness and the dimensions of the Au catalyst disks. Moreover, the VER also increases as the LER becomes more rapid with T. An enhancement of lateral etching uncovers regions of oxidized material that would otherwise remain unexposed to the I-MacEtch solution at lower etching temperatures and otherwise subject to slower LER values. Additionally, elevated temperatures enable enhanced dissolution of oxidized materials, associated with elevated rates of mass transport for both dissolution reactants and products [155], as well as a reduced energy barrier to bond liberation [49]. Another consideration is the overlap of neighboring hole distributions with increasing temperature. Overlapping hole distributions enhance etch rates by more rapidly oxidizing the overlapped regions to a chemical state that is soluble in the etchant [42]. As the hole distribution overlap depends on the extent of the spacing between injection sites, the dependencies and relationships demonstrated here hold true for a fixed catalyst diameter, d, and spacing, s. In this study, all samples consist of Au disks of $d = 1500$ nm and $s = 500$ nm in the substrate surface (x-y) plane. Conversely, the trends shown here can be considered analogous to decreasing s while holding x or T constant, which introduces yet another etch profile variable for nanostructure aspect ratio engineering.

The influence of Al content on etch rates can also be explained by two main contributing mechanisms, namely (1) the etch rates of GaAs-like and AlAs-like constituents in citric acid-hydrogen peroxide solutions and (2) the offset in the semiconductor energy band edges relative to the catalyst (i.e., Au) reductionoxidation potential.

While mixtures of hydrogen peroxide and citric acid wet etch GaAs, the addition of Al decreases the etch rate of ternary $Al_xGa_{1-x}As$ [150]. The catalytically enhanced etch rates follow the same trend; VER and LER decrease with Al content over the range investigated in this study. Moreover, the decrease in etch rates for more AlAs-like samples indicates that the I-MacEtch solution dissolves the relevant oxides at different rates. While the concentration of AlO bonds increase with x [150], the Al_2O_3 oxide formed during standard wet etching of AlGaAs becomes more resilient to citric acid solutions [141]. Although further studies are required to establish the stoichiometry of the specific oxides generated during the Au-catalyzed wet etching process (e.g., Ga_xO_y and Al_xO_y), we note that their solubility in the current I-MacEtch solution is inversely proportional to Al content. Additionally, energy band edge alignments must be considered. While the offset in the conduction band edge of GaAs and AlAs is relatively small (i.e., ∼0.13 eV), the valence band edge (VBE) of AlAs is shifted ∼0.6 eV toward the redox potential of Au in comparison to that of GaAs [21, 156]. This results in a lower valence band density of states for the accommodation of hole injection at higher x. Therefore, the oxidation capacity is reduced, resulting in a decrease in catalytic oxidation for higher Al content samples etched under constant I-MacEtch conditions. It should be noted that while VER and LER are shown to be dependent on x and T, the VER/LER ratio will likely be more dependent upon pattern geometry (e.g., catalyst size, spacing, etc.).

6.5.6 Confirming Catalytic Influence

To test if the observed etching behavior is the result of catalytic oxidation, identical sets of $Al_{0.55}Ga_{0.45}As$ samples were processed using the same procedure for preparations of Au- and Cr-patterned catalyst arrays for direct comparison. Identical etching conditions were used for the Cr- and Au-patterned samples. Post-I-MacEtch SEM images are shown in Figure 6.12 for comparison between the two disparate metal layers.

Cr has been identified as a material that prohibits MacEtch from occurring for Si and InGaP [21, 42, 155]. This can be explained through an analysis of the established cathodic reaction that is necessary for MacEtch [9, 21]. The cathodic reaction requires the VBE of AlGaAs (i.e, its ionization potential) to lie higher (i.e., offset toward less positive potential) than the redox potential of the metal, when referenced to a common electrode [21, 22, 42]. Thus, the semiconductor must possess an ionization potential that resides closer to the vacuum level than the redox potential of the catalyst to accommodate hole injection. The reduction potentials (E^0) for Au and Cr are +1.50 and -0.74 V, respectively, relative to the standard hydrogen electrode [21], and the ionization potential of each binary component of AlGaAs (i.e., GaAs and AlAs) lies between these two values [156]. Therefore, the valence band edge for all $Al_xGa_{1-x}As$ compositions resides at potentials that enable Au to promote the necessary redox reaction, while Cr may not serve as a catalyst for the oxidation of the underlying ternary substrate. Figure 6.12 shows identical sets of $Cr/Al_{0.55}Ga_{0.45}As$ (panels a and

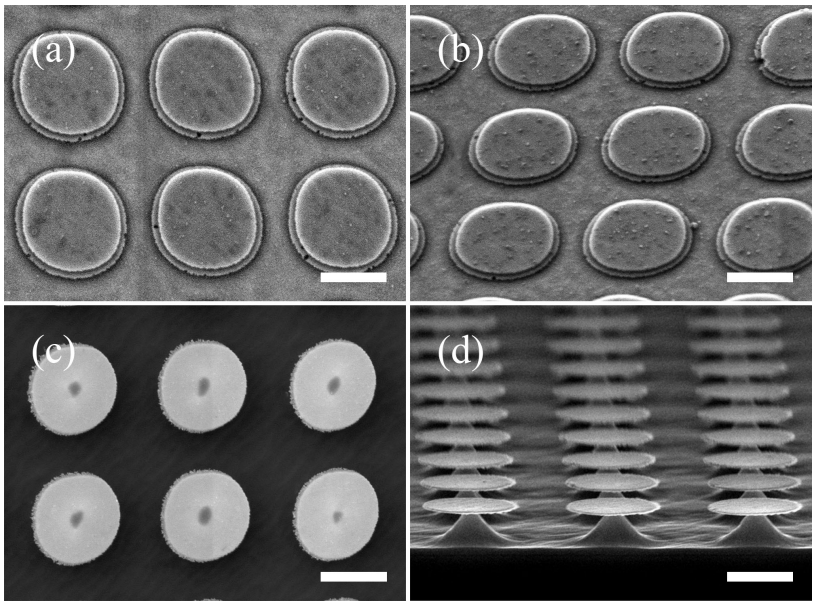

Figure 6.12: SEM images showing (a) top-view and (b) 45° tilted-view SEM images of Cr-patterned and (c) top-view and (d) 85° tilted-view SEM images of Au-patterned $Al_{0.55}Ga_{0.45}As$ samples etched in identical I-MacEtch solutions at 65 °C for 30 min. Scale bars represent 1 μm.

b) and Au/$Al_{0.55}Ga_{0.45}As$ (panels c and d) etched in the same I-MacEtch solution for 30 min at 65 °C. The Cr-patterned samples exhibit wet etching of only the GaAs cap layer, which is attributed to noncatalytic wet etching of GaAs in the mixture of hydrogen peroxide and citric acid. In contrast, the Au-patterned samples show significant vertical and lateral etching. This illustrates the ability of Au to facilitate the cathodic reaction and allow hole injection not only through the GaAs cap layer but also into the underlying $Al_xGa_{1-x}As$ film. This point is highlighted in support of the Au-catalyzed etching behavior of $Al_xGa_{1-x}As$.

6.5.7 Model for Etching Behavior

The schematics in Figure 6.13 demonstrate the I-MacEtch mechanisms and illustrate the ability to target a final structure with desired geometry by tuning the etching conditions. Figure 6.13a details the I-MacEtch mechanisms; the cathodic reaction reduces the oxidant and injects the resulting holes into the substrate, and the anodic reaction dissolves the catalytically oxidized semiconductor. Figure 6.13b demonstrates the influence of t, T, and x on the extent of hole distributions (dashed blue arrows)

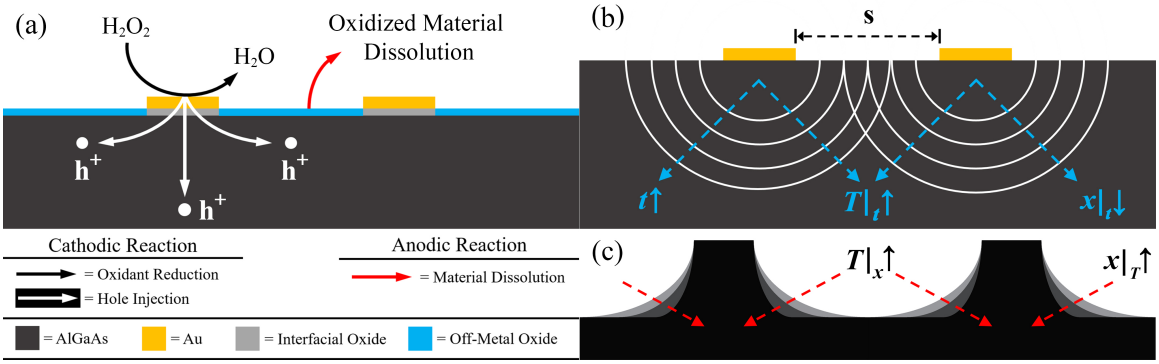

Figure 6.13: Schematic illustrations demonstrating (a) mechanisms for AlGaAs I-MacEtch and associated reactions, (b) the ability to extend hole distributions by increasing time (t), increasing temperature for a fixed etch time ($T|_t$), and decreasing Al content for a fixed etch time ($x|_t$). Adjusting the size of the hole distributions with T or x is analogous to changing the spacing (s) between catalysts at a constant T and x. (c) A qualitative model of the ability to tune the etch anisotropy with increasing Al composition for a fixed etch temperature ($x|_T$) and increasing temperature for a fixed Al composition ($T|_x$).

for samples with identical catalyst patterns that are etched in an I-MacEtch solution of consistent concentration. The progression in the size of hole distributions is shown in Figure 6.13b as concentric white hemispheres extending from the Au disks. Figure 6.13c is a visual representation of the etch anisotropy (i.e., VER/LER ratio), which increases with x at a constant T ($x|_T$) and increases with T at a constant x ($T|_x$), as denoted by dashed red arrows. The extent of these profiles increases over time under constant conditions. Furthermore, for a constant etch time, the extent of the hole distributions and therefore oxidation profiles increases with etch temperature ($T|_t$) and decreases with Al fraction ($x|_t$).

6.6 Conclusions

The I-MacEtch process outlined here provides a single-step technique for the fabrication of vertically oriented and ordered $Al_xGa_{1-x}As$ nanostructures of tunable dimension and aspect ratio. Although most common etchants attack AlGaAs in an isotropic manner, an I-MacEtch system consisting of Au-patterned AlGaAs in a mixture of hydrogen peroxide and liquid citric acid is conducive to anisotropic etching control via selective oxidation. This benchtop technique can be realized using standard planar semiconductor processing equipment, and can be performed in conventional wet-benches. Following nanostructure formation and Au removal, a subsequent polishing etch (e.g., 1:8:80 H_2SO_4:H_2O_2:H_2O [148] or more dilute for slower etching) can be employed to further reduce the diameter of the features without altering their overall shape. The fabrication method outlined here may be utilized to generate ordered arrays of nanometer-scale features for devices in nanoelectronics, optoelectronics, and photovoltaics.

6.7 Future Works

In future work, further exploration of etching conditions will be carried out. Not all parameters that contribute to the etch conditions are within the scope of this study. Areas for further exploration include, but are not limited to, modification of the relative concentration of I-MacEtch solution constituents toward room-temperature processing, tuning carrier transport via illuminated MacEtch, and modeling of the dynamic dependences of hole distributions upon etching parameters during the formation of nanopillar structures. X-ray photoelectron spectroscopy, electron energy loss spectroscopy, or Auger electron spectroscopy may be used for further chemical analysis of the distinct oxides formed during I-MacEtch of AlGaAs as Al content is increased. Transmission electron microscopy will be performed in future work to investigate the sidewall crystallinity. Lastly, investigation of AlGaAs systems beyond the scope of this study (e.g., extended composition range, layer thickness, DBR structures, etc.) and varied Au pattern geometries are also areas for future work.

Chapter 7

CNT-Catalyzed Si MacEtch Towards CMOS Compatibility

7.1 Summary

Metal-assisted chemical etching (MacEtch or MACE) has been heralded as a robust and cost-effective semiconductor fabrication technique that combines many of the advantages of both wet- and dry-etching, while simultaneously overcoming their accompanying limitations. However, widespread use of MACE processes has been hindered partly due to the use of metallic catalysts such as Au that potentially introduce deep-level trap defects into Si processing. Moreover, alternative noble metal catalysts (e.g., Ag or Pt) embed an optically reflective film within the etched substrate, which can be detrimental to devices that rely on MACE-generated structures for improved light absorption. Here, a versatile process is detailed whereby carbon nanotube (CNT) composite films are used as catalysts for site-selective etching of Si. The so-called carbon nanotube-assisted chemical etching (CNT-ACE) method enables solution-based and room-temperature fabrication of vertical Si micropillar arrays. Vertical etch rates (VERs) of Si samples etched using nominally undoped CNTs and potassium tetrabromoaurate ($KAuBr_4$)-doped CNTs are compared. An enhancement of VER from ∼28 nm/min to ∼142 nm/min is observed for $KAuBr_4$-doped CNTs compared to undoped films, which is attributed to a shift in the aggregate reduction potential of the catalyst film toward that of pure Au. Raman spectroscopy and Auger electron spectroscopy reveal that the catalytic CNT layer is not degraded during etching. A

solar-weighted reflectance of ∼2 % is found using UV-Vis spectrophotometry for Si micropillar arrays with surface-embedded catalytic CNT membranes. This represents over 94 % reduction in solar-weighted reflectance compared to bare Si, and 33 % reduction compared to Si micropillar arrays fabricated via conventional MACE with embedded Au catalyst layers. A physical model is provided for the CNT-ACE mechanisms, including additional mass transport pathways for dissolution products through the CNT film. The CNT-ACE method outlined here enables complementary metal-oxide-semiconductor (CMOS)-compatible fabrication of Si micro- and nanostructures with device applications in optoelectronics, photonics, and photovoltaics, and is particularly beneficial for applications wherein non-reflective embedded contacts are desired.

7.2 Introduction and Motivation

The increasing demand for complex devices that utilize three-dimensional nanostructures has incentivized the development of adaptable semiconductor nanofabrication strategies. Without the introduction and refinement of processes that overcome challenges associated with modern semiconductor device engineering, nanofabrication sequences will continue to be the prominent bottleneck for advancing the feasibility of next-generation architectures. For example, while crystallographic wet-chemical etching has historically been sufficient for production of textured Si surfaces, physical and chemical plasma etching evolved to allow for the creation of vertical structures within integrated circuits. However, the ballistic nature of dry etching introduces undesired imperfections, particularly within the micro- and nano-scale regimes.

Current nanofabrication methodologies can be categorized as being either bottom-up or top-down, each with a host of strengths and limitations. Although well-defined and pristine nanostructures may be realized through bottom-up epitaxial growth, this involves costly tools that use hazardous gases at elevated temperatures in vacuum

chambers [157–160]. Conventional top-down approaches include wet-chemical etching and plasma etching. Wet etching is advantageous for its simplicity and cost-efficiency, though it lacks the ability to yield high aspect-ratio features due to isotropic progression of etch-fronts or crystallographic etch rate dependences [8]. Conversely, reactive-ion etching (RIE) is directional and highly anisotropic, at the expense of using hazardous gases and vacuum instrumentation. Moreover, the high energy ion bombardment associated with RIE can cause detrimental lattice and sidewall damage [5].

Metal-assisted chemical etching (MacEtch or MACE) is a relatively new semiconductor nanofabrication methodology that provides an alternative processing scheme to overcome traditional limitations [12, 43]. It is a solution-based and anisotropic technique that induces or enhances semiconductor etching in the presence of a suitable catalyst [8]. A thin metallic catalyst (e.g., Au, Ag, Pt, or Pd) is commonly deposited in intimate contact with a semiconductor, which is then submerged in a solution containing an etchant (e.g., hydrofluoric acid or sulfuric acid) and an oxidant (e.g., hydrogen peroxide or potassium permanganate) [9].

The MACE process is modeled after a galvanic cell, with cathodic and anodic half reactions occurring at the solution/catalyst and catalyst/semiconductor interfaces, respectively [42]. The oxidant is reduced at the cathode, thereby generating charge carriers that are locally injected into the semiconductor at the anode. The solution interacts with the ionized substrate, creating an oxide that is preferentially attacked by the etchant [42, 43]. The metal sinks into the substrate as the underlying, catalytically generated, oxide is dissolved, leaving behind vertical structures defined by the non-interfaced regions. Therefore, MACE offers a nanofabrication alternative that is both anisotropic and solution-based. While the MACE technique has predominantly focused on Si [21, 23, 24, 51, 124, 161–163], there have been recent advancements in the catalytic etching of III-V alloys and functional oxides, such as InP [13, 17], GaAs [20, 27, 29, 38, 164, 165], InGaAs [41], AlGaAs [43], InGaP [42], and β-Ga_2O_3

[166, 167].

The main challenge that has inhibited MACE from becoming a mainstream process is the common use of Au as a catalyst, which effectively disqualifies the method from many Si foundry front-end process lines and common cleanroom laboratories. Although Au serves as an excellent catalyst due to its relatively high reduction potential and stability in common etchant solutions [21, 42, 43], its prevalent use within MACE is a two-fold issue. First, many cleanroom facilities impose blanket regulations that restrict the introduction of Au into their equipment. Second, Si nanofabrication foundries may be reluctant to employ a process that requires a deep-level trap (e.g., Au) to be in contact with their substrates. Therefore, developing Si MACE schemes that replace Au with alternative catalysts that do not introduce deep-level traps is highly sought after.

Additionally, use of alternative noble metals such as Ag or Pt still presents the challenge of embedding an optically reflective film into the MACE-micropatterned surface. This is undesired for certain device applications in optoelectronics and photovoltaics, where micro/nanotexturing is specifically employed to minimize reflection loss. While embedded catalyst layers may be wet-etched during device fabrication, this adds additional process complexity, and imperfect etching selectivity may result in damage to the active device structures. Thus, a pressing need exists for development of alternative catalysts that are compatible with standard processes, and that do not introduce deep-level trap defects or surface reflection loss.

Researchers have recently made strides towards CMOS-compatible MACE processes, including utilizing copper- [168–172] graphene-,[173], graphene- [173], carbon nanotube- [174], and titanium nitride-based catalysts [175]. The work presented here aims to build upon these recent advancements towards creating viable avenues for carbon-induced catalytic etching with CMOS-compatibility [176, 177]. To that end, a room-temperature method for carbon nanotube-assisted chemical etching (CNT-

ACE) is detailed here. Ordered Si microstructure arrays are achieved by utilizing vacuum-filtered CNT membranes as the catalytic medium in the MACE process. Vertical etch rates (VERs) are compared for the various catalyst layers, including pure CNT membranes, potassium tetrabromoaurate ($KAuBr_4$)-doped CNT membranes, and pure Au. The enhanced VER for $KAuBr_4$-doped CNTs compared to undoped CNT films is attributed to a shift in their aggregate reduction potential towards that of pure Au. Raman spectroscopy and Auger electron spectroscopy are performed to show no degradation of the CNT-film occurs during etching. Use of CNTs as a MACE catalyst precludes the introduction of deep-level traps during fabrication of periodic and vertically-oriented Si micropillar arrays. Moreover, it is anticipated that the embedded CNT films can simultaneously serve as a non-reflective contact layer for micropillar arrays-based device applications in electronics, optoelectronics, and photovoltaics.

7.3 Experimental Details

The CNT catalyst films were prepared through the following approach. First, 86 μg of commercially available single-walled carbon nanotubes (SWCNTs; NanoIntegris, Inc.) were mixed with 15 mL chlorosulfonic acid (CSA) in a resodyn LabRAM mixer for 30 min with an acceleration of 10.7 m/s^2. Next, CNT films were created using a vacuum filtration process to collect the SWCNTs, which allows for CNT film thickness to be controlled [178–180]. The CNTs were extracted onto an adhesive Teflon binder for vertical alignment in a membrane-like structure. Films were then transferred from a liquid solution onto the adhesive, which was then exfoliated to yield thin CNT films. All CNT films prepared in this manner had a thickness of approximately 50 nm. CNT films were then thermally oxidized at 400 °C to remove any remaining CSA.

Three different sets of CNT samples were prepared for this study, as summarized in Table 7.1. Sample A consisted of undoped CNT films, while samples B and C

Table 7.1: Overview of sample preparation conditions for CNT-catalyzed etching trials.

Sample	Catalyst Type	Catalyst Thickness (nm)	$KAuBr_4$ Doping (mmol/L)
A	CNT	50	0
B	CNT	50	5
C	CNT	50	15
D	Au	35	N/A

consisted of CNT films that were doped with 5 mmol/L and 15 mmol/L $KAuBr_4$, respectively. Doping of $KAuBr_4$ (Sigma Aldrich) was performed in de-ionized (DI) water for 1 hr, and subsequently rinsed with DI water prior to solution transfer to Si substrates.

Separately, the p-type Si(100) wafers used for all experiments were first subjected to a standard RCA cleaning process prior to being degreased with solvents. Si samples were then subjected to an additional 30 second, 10:1 buffered oxide etch (BOE) for removal of any surface oxide layers formed in ambient air after RCA cleaning. The Si wafers were then used for direct solution transfer of CNT membranes. Additional details for this process have been reported in prior work [181].

The CNT films transferred to Si substrates were patterned through photolithography to yield the desired geometry of Si nanopillars after catalytic etching. First, an array of circular windows with $\sim$3 μm diameters were exposed through a photoresist layer to uncover CNT film in predefined locations. Next, CNT membranes exposed through circular windows were removed via oxygen plasma reactive ion etching (RIE) prior to dissolution of the remaining photoresist film. Thus, a planar CNT mesh consisting of $\sim$1 μm street width and $\sim$3 μm circular openings were formed, which revealed the underlying Si substrate.

For direct comparison of CNT-ACE and Au-catalyzed MACE processes, an additional sample set was fabricated, hereafter referred to as Sample D. Here, a 35 nm-thick Au mesh pattern was defined through a photolithography, Au thermal

evaporation, and liftoff procedure. Sample preparation conditions for Sample D are summarized in Table 7.1. All CNT-ACE and Au-assisted etching trials were performed in identical solutions consisting of 6.26 mol/L hydrofluoric acid (HF), 8.52 mol/L hydrogen peroxide (H_2O_2), and 1.45 mol/L isopropyl alcohol (IPA).

Etched samples were imaged via scanning electron microscopy (SEM) using a Hitachi S-4000 instrument. Room-temperature Raman spectroscopy (RS) was performed using a Horiba LabRAM HR Confocal Raman Microscope with the 633 nm excitation line of a He-Ne laser. Auger electron spectroscopy (AES) was performed in a chamber with a base pressure of 1×10^{-10} T using a double pass cylindrical analyzer. Measurements we taken at 60° incidence from the surface normal and beam current was kept below 5 nA to minimize charging effects. The beam diameter at the sample was set to 0.5 mm to obtain a large, reliable ensemble measurement. Total hemispherical reflectance (i.e., specular and diffuse) spectra were collected using a Shimadzu UV-2600 sphectrophotometer with an integrating sphere, and solar-weighted reflectance was calculated using the Air Mass 1.5 spectrum.

7.4 Results and Discussion

7.4.1 Pre-Etch CNT Imaging

Figure 7.1 shows a set of top-view SEM images demonstrating the CNT films prior to etching. A patterned mesh of CNTs can be seen in Figure 7.1a, with spacing (s) of $\sim$1 μm between neighboring circular windows. An interconnected catalytic network of CNT bundles is directly interfaced with the Si substrate along the patterned mesh. Circular windows with diameter (d) of approximately 3 μm expose the underlying Si surface. Figure 7.1b shows a high-magnification view of non-aligned CNT bundles comprising the catalyst membrane. Compared to conventional MACE catalyst layers deposited by physical vapor deposition [21] or electrodeposition [27], the CNT network

is non-uniform in areal coverage and possesses a series of pores, which serve to (1) anchor the catalyst to the Si substrate [24], and (2) provides additional pathways for mass transport of dissolved CNT-ACE products through liquid phase diffusion. Both features are necessary for the CNT-ACE process to proceed uniformly, which will be considered in later discussions of the etching mechanism.

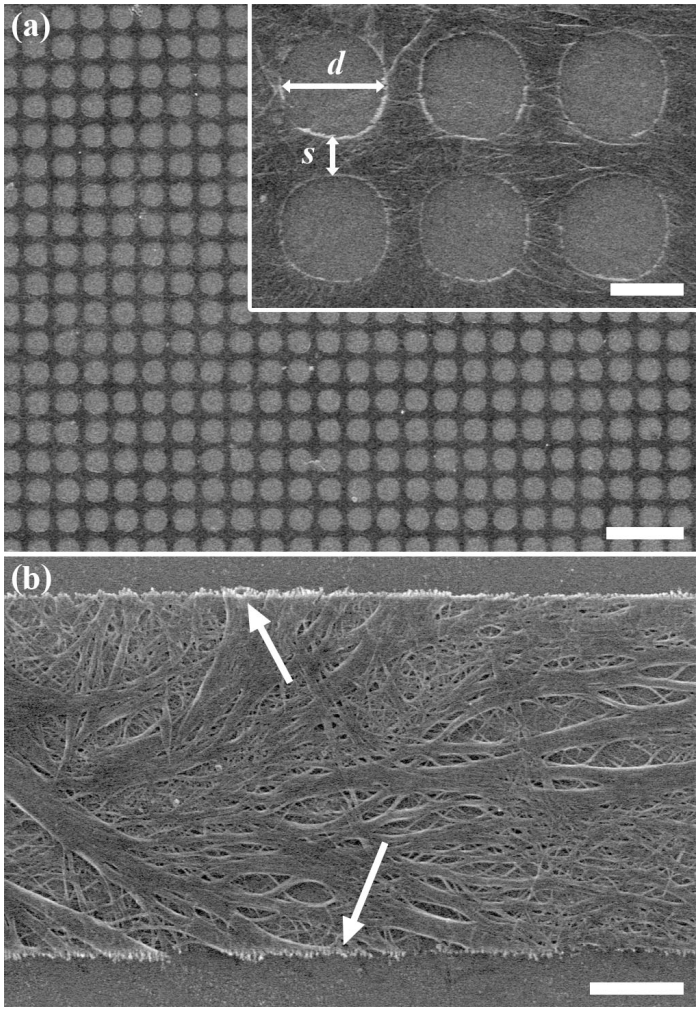

Figure 7.1: Top-view SEM images of CNT-patterned Si prior to etching. (a) Shows a patterned array of CNTs with street width (s) of 1 μm and non-interfaced Si regions of diameter (d) 3 μm, and (b) shows a high-magnification view of the CNT fibers which act as a catalyst, with white arrows indicating serrated CNT perimeters that translate to roughened Si sidewalls after etching. Scale bars represent (a) 10 μm and (inset) 2 μm, and (b) 1 μm.

7.4.2 Confirming CNT-Catalyst Suitability

Etching trials have been performed to evaluate the performance of CNTs as a suitable selective-etching catalyst. Tilted-view SEM images of samples etched in the same solution are shown in Figure 7.2. Figure 7.2a shows Si micropillars formed in Sample A, where an undoped CNT composite membrane was used as the etching catalyst layer. The interconnected CNT membrane is seen along the bases of individual Si micropillars, consistent with the conventional forward-progression MACE mechanism whereby the catalyst-interfaced regions are selectively etched. This is further supported through energy-dispersive X-ray spectroscopy (EDXS) maps collected from post-CNT-ACE samples, which are shown in Figure 7.3.

The sidewalls of the resulting Si micropillars are observed to be engraved with vertical serrations. The serrations coincide with indentations in the CNT membrane along the interior of the patterned windows (indicated by white arrows in Figure 7.1b), which are formed during the RIE step of the mesh fabrication process. Similar serrations have been observed along the sidewalls of GaAs nanopillars formed via

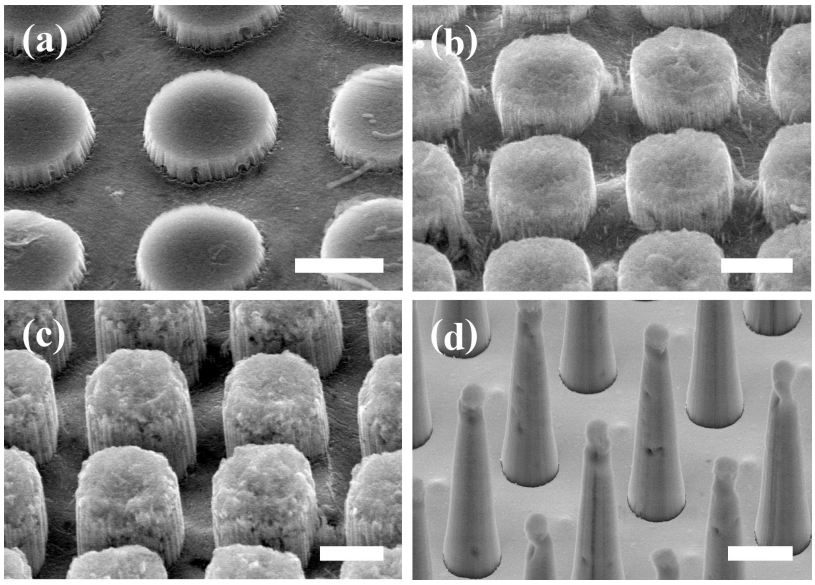

Figure 7.2: Tilted-view SEM images showing (a) undoped CNTs, CNTs doped with (b) 5 mmol/L $KAuBr_4$, (c) 15 mmol/L $KAuBr_4$, and (d) Au-catalyzed MACE. Scale bars represent 2 μm.

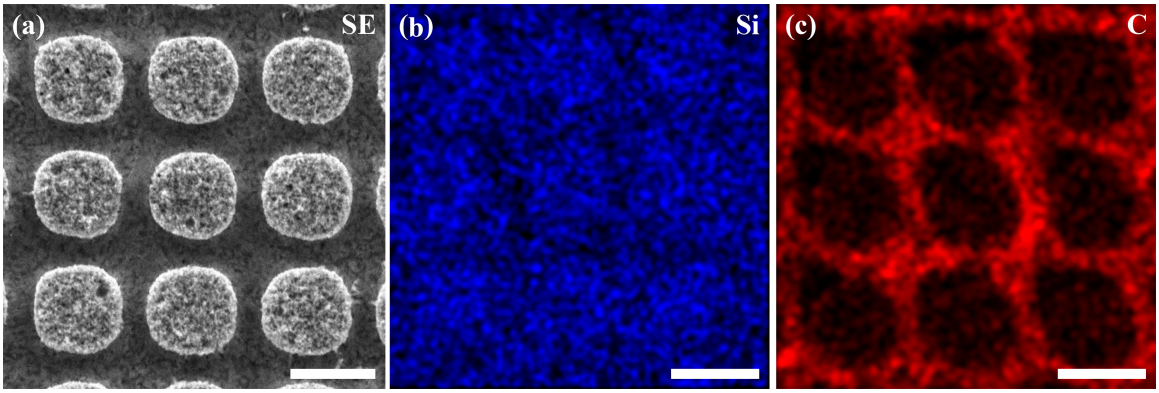

Figure 7.3: (a) Top-view SEM image of a CNT-patterned sample after etching. Corresponding EDX maps represent elemental (b) Si and (c) C. Scale bars represent 3 μm.

Au-assisted MACE, where the catalyst mesh pattern was defined in a similar manner to the current process [20]. Thus, the vertical indentation lines seen as sidewall roughness on Si micropillars (also observed for Samples B and C) are simply a product of the catalyst geometry and not an inherent product of the CNT-ACE mechanism itself. For Sample A, a vertical etch rate (VER) of 27.5 ± 1.8 nm/min is measured.

7.4.3 Vertical Etch Rate: Undoped- and Doped-CNTs, and Pure-Au

Next, samples etched using doped CNT membranes are considered. Figure 7.2b and 7.2c show as-etched Si micropillar arrays formed using Samples B and C, where the catalyst CNT film is doped with 5 and 15 mmol/L $KAuBr_4$, respectively. While a VER of 59.2 ± 4.5 nm/min is observed in the case of Sample B, a more than two-fold VER of 141.5 ± 6.6 nm/min is measured for Sample C. This represents over 5× enhancement of etch rate in the case of Sample C compared to Sample A (i.e., undoped CNTs). Finally, Sample D demonstrates Si micropillars fabricated using an evaporated film of pure Au, as seen in Figure 7.2d. A VER of 234.3 ± 4.5 nm/min is measured for Sample D, and is considered the upper limit for the current study. This agrees well with existing literature for Au-catalyzed Si MACE; for example, Lai et al. found an etch rate of ∼250 nm/min for p-Si using a comparable solution [23]. Figure 7.4 shows a VER comparison for all four sample sets.

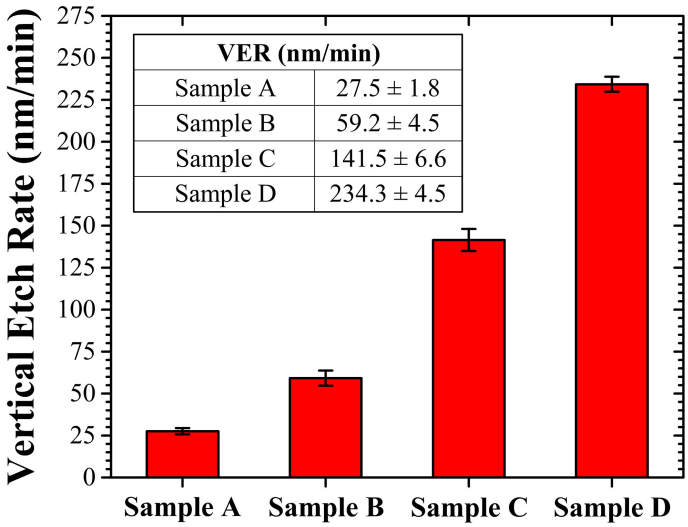

Figure 7.4: Plot showing measured vertical etch rates (VERs) for Si samples using undoped CNT catalysts (Sample A), CNTs doped with 5 and 15 mmol/L $KAuBr_4$ (Samples B and C, respectively), and Au-catalyzed MACE (Sample D).

Since all CNT catalyst mesh layers used in this study are prepared with comparable thickness and porosity, the VER differences between Samples A through C cannot simply be attributed to variations in the mass transport rate of dissolved product. Instead, it is anticipated that $KAuBr_4$ doping shifts the aggregate reduction potential of CNT membranes towards that of pure Au [21, 181]. Consequently, enhanced oxidant reduction and carrier generation rates in doped CNT samples can account for the greater VER observed in the case of Samples B and C, in comparison to that of Sample A. Higher concentrations of $KAuBr_4$ (i.e., Sample C) also induce the deposition of randomly distributed Au nanoparticles in the CNT membranes, as shown in Figure 7.5. The deposition of Au nanoparticles with comparable size and number density to those found in Sample C has been shown in prior work on fabrication of CNT membranes through similar methodologies [179]. The presence of such nanoparticles further locally enhances the cathodic reaction and leads to an overall enhancement of VER, stemming primarily from charge carrier generation contributions.

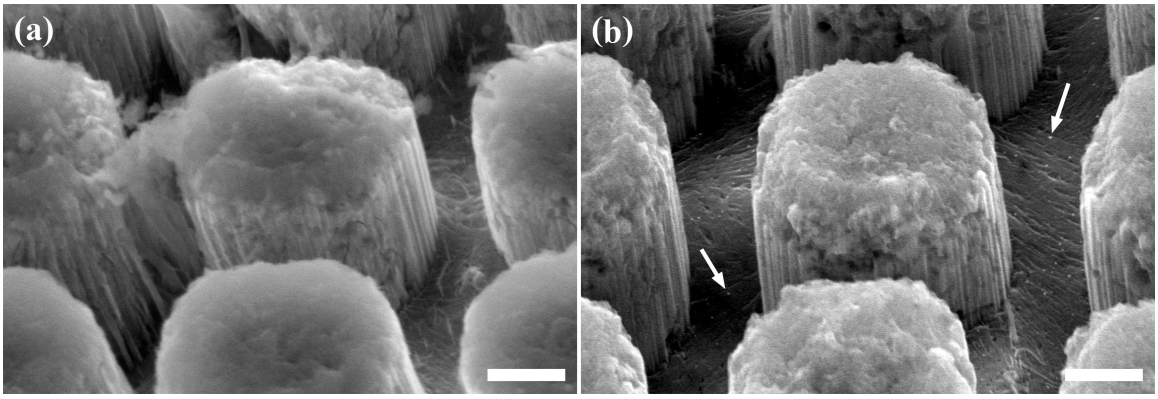

Figure 7.5: Tilted-view SEM image of (a) 5 mmol/L, and (b) 15 mmol/L $KAuBr_4$-doped CNT films after etching. Higher concentrations of $KAuBr_4$ (i.e., Sample C) result in randomly distributed Au nanoparticles in the CNT membranes, as indicated by white arrows. Scale bars represent 1 μm.

7.4.4 Evaluating CNT Degradation via Raman Spectroscopy

To evaluate the CNT membrane and to assess the possibility of its degradation as a result of etching, EDXS, RS, and AES analysis was performed. As shown in the Figure 7.3, EDXS mapping reveals the CNT membrane remains intact, and that it can only be found along the base plane between Si micropillars (i.e., where catalytic etching took place). Figure 7.6 shows Raman spectra collected from regions corresponding to exposed Si before and after the CNT-ACE process. The bare Si curves, before and after etching, show only the signature crystalline Si phonon resonance peak at 520 cm^{-1}, which undergoes neither a shift, nor linewidth broadening, during CNT-ACE. This indicates that the bulk Si integrity has not been compromised, and that additional parasitic phases have not been introduced.

Similarly, Figure 7.7 shows the Raman spectra collected from Si regions covered by the catalytic CNT membrane, with the black and red-dashed curves representing pre- and post-etch samples, respectively. In addition to the characteristic transverse optical (TO) phonon resonance of crystalline Si at 520 cm^{-1}, CNT phonon modes are observed, corresponding to the characteristic radial breathing modes (RBM) below 300 cm^{-1}, D-band at /sim 1340 cm^{-1}, G-band at $\sim$1580 cm^{-1}, and 2D-band at $\sim$2680

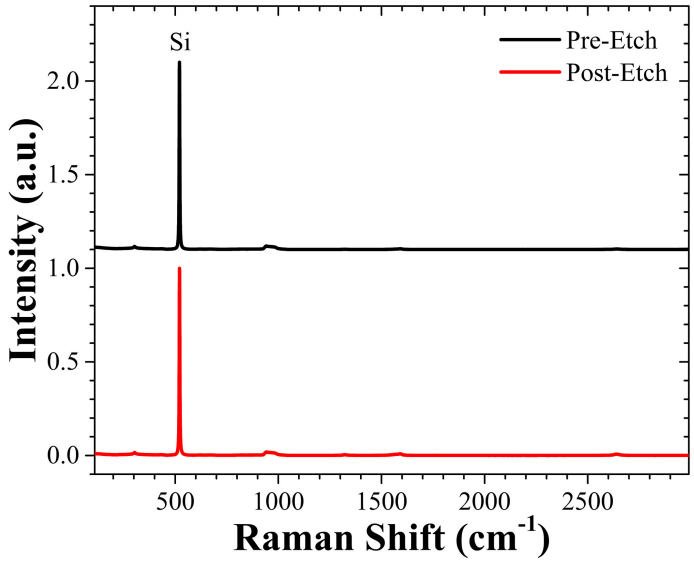

Figure 7.6: Raman scattering spectra for (black curve) pre- and (red curve) post-etch bare Si samples (i.e., a Si region not interfaced with CNTs).

cm^{-1} [182]. First, we note that the pre- and post-etch spectra reveal G-band peaks that are perfectly aligned and of equivalent linewidth and intensity, indicating that the CNT crystallinity has been preserved after etching. Next, G-/D-band intensity ratios (I_G/I_D) of 3.7 and 4.2 are measured before and after the CNT-ACE process, respectively. The comparable intensity ratios indicate that the purity of the CNTs

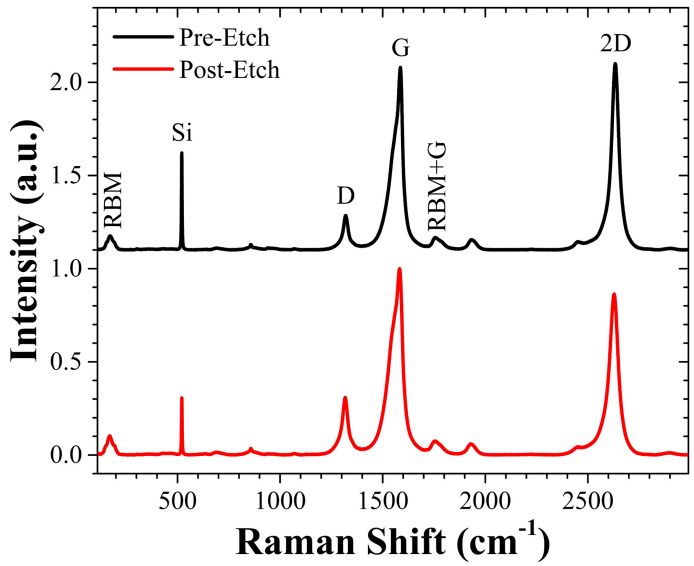

Figure 7.7: Raman scattering spectra for (black curve) pre- and (red curve) post-etch CNT-covered Si samples.

comprising the catalyst layer remain unmodified with respect to defect density. Small variations in $I_G G/I_D$ may also stem from local differences in defect density from one region to the next. Lastly, the coincidence of pre- and post-etch CNT Raman spectra show that intermixing of C with Si, O, F, or other CNT-ACE reaction products does not occur.

7.4.5 Evaluating CNT Degradation via Auger Electron Spectroscopy

CNT film degradation was also evaluated using Auger electron spectroscopy. Figure 7.8 shows the Auger electron spectra for pre- and post-etch samples (black and red curves, respectively). Three characteristic peaks are observed in the differential AES plots, which correspond to Auger electron emission from SiO_2 (81 eV), C (272 eV), and O (508 eV) [183]. The C peak does not shift or change in shape, indicating that the surface chemistry of the CNT film and the C-to-C bonds are unaffected. As expected, the SiO_2 peak remains the same before and after etching. This peak is associated with surface oxidation, and relays no information regarding the underlying bulk Si.

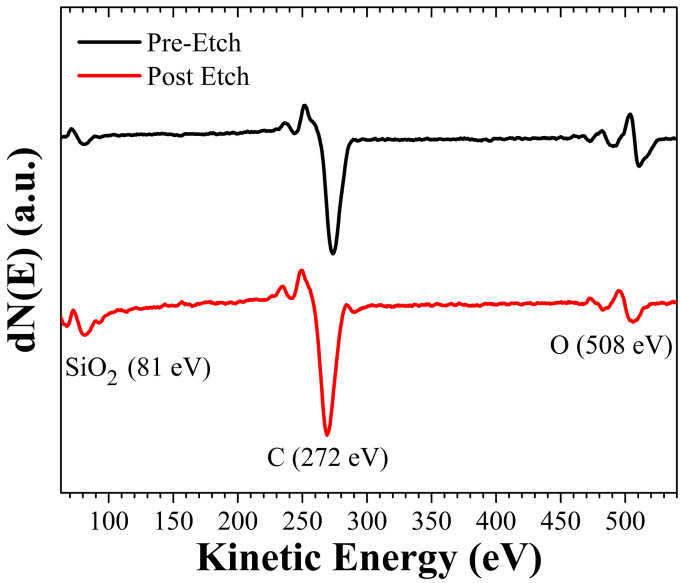

Figure 7.8: Auger electron spectra for (black curve) pre- and (red curve) post-etch samples. Three peaks corresponding to Auger emission of SiO_2 (81 eV), C (272 eV), and O (508) eV.

Notably, the Si Auger signal, which is expected at 92 eV, is absent in both the pre- and post-etch spectra. This indicates the oxide formed during CNT-ACE is thicker than the Auger electron escape depth (i.e., < 2 nm). Lastly, the differences in relative intensity of the O peak can be caused by local differences in surface adsorbates after exposure to air. Since these samples were not kept under vacuum at any point, the exposure to air introduces oxygen-based complexes that can adsorb on the surface of the sample. This can cause a fluctuation in the observed oxygen energy peak intensities [183].

7.4.6 Reduced Reflectance with CNT-Catalyst

Figure 7.9 shows total hemispherical reflectance spectra for bare Si (black curve), and spectra representative of samples subjected to CNT-ACE (blue curve) and Au-catalyzed MACE (red curve). Total hemispherical reflectance includes contributions from both specular and diffuse reflections. Hemispherical solar-weighted reflectance (SWR) is found by applying an appropriate scaling factor (i.e., Air Mass 1.5 solar

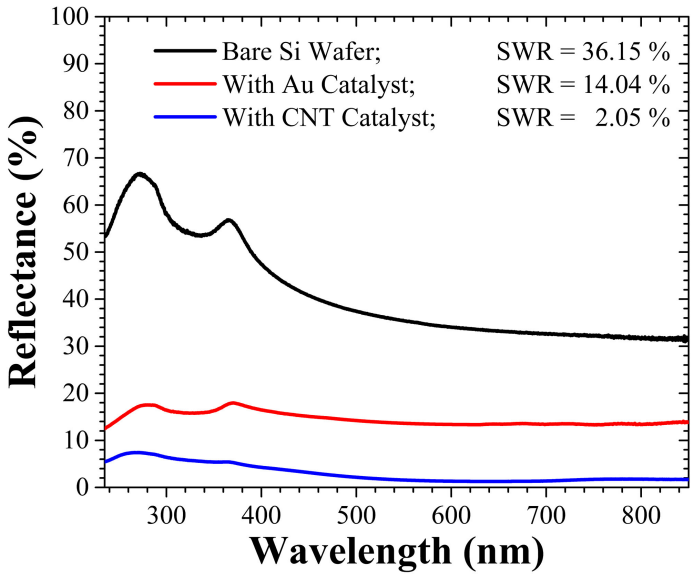

Figure 7.9: Total hemispherical reflectance (i.e., specular and diffuse) spectra for bare Si, CNT-ACE, and Au-enhanced MACE (black, blue, and red curves, respectively). Solar-weighted reflectance (SWR) values, calculated using Air Mass 1.5, for bare Si, CNT-ACE and Au-MACE are 36.15 %, 14.04 %, and 2.05 %, respectively.

irradiance spectrum) to hemispherical reflectance data [27]. Importantly, the catalyst layers were not etched or otherwise removed prior to reflectance measurements. Thus, the blue and red curves are representative of measurements collected from samples with embedded CNT and Au layers, respectively, along the base of the Si micropillars. For bare Si, SWR is determined to be 36.15 %, which is considered to be a baseline of comparison for CNT-ACE and Au-catalyzed MACE trials. Post-etch SWR values for Au- and CNT-catalyzed samples are found to be 14.04 and 2.05 %, respectively. Au-MACE samples reduce SWR by 61.2 %, whereas CNT-ACE samples reduce SWR by 94.3 %, compared to that of bare Si. Therefore, a 33.2 % reduction in SWR is gained by utilizing CNT-catalysts instead of Au. The reflectance reduction measured from post-etch samples using CNT catalysts is attributed to the membrane itself having lower reflectance properties in comparison to Au films [184, 185]. Thus, the CNT layer does not need to be removed for device applications requiring a minimization of reflection loss. This is in contrast to Au-MACE, which requires additional processing steps to remove the metallic catalyst after etching is complete. Therefore, it is envisioned that CNT-ACE may simplify device fabrication processes wherein integrated CNT films serve as embedded contact layers or components in active heterojunctions.

7.4.7 Model for Etching Behavior

Figure 7.10 shows schematic illustrations of the catalytic etching mechanism using (a) Au and (b) CNT catalysts. Pre- and post-etch depictions are shown in the left and right columns of the figure, respectively. The cathodic (blue arrows) and anodic (white arrows) half reactions are highlighted on the pre-etch samples. The red arrows on the post-etch schematics represent mass transport pathways for dissolved etch products. While continuous Au films only allow mass transport along the periphery of the metal, CNT membranes allow for additional mass transport pathways through the porous film itself. During MACE fabrication of Si microstructures, features with vertical

sidewalls result from localized hole injection, and subsequent preferential dissolution of the selectively oxidized regions. However, injected holes have a tendency to be swept away from Au catalyst layers in contact with p-type Si substrates due to Schottky barrier formation along the metal-semiconductor interface, which causes oxidation of off-metal regions and formation of micropillars with tapered morphologies [23]. Figure 7.2d shows Si micropillars with characteristic tapered morphologies resulting from Au-catalyzed MACE of p-Si [21, 23, 24, 124]. A surplus of charge carriers are generated during the Au-mediated MACE process. These holes are swept away from their injection sites, which oxidizes non-interfaced Si regions (e.g., micropillar

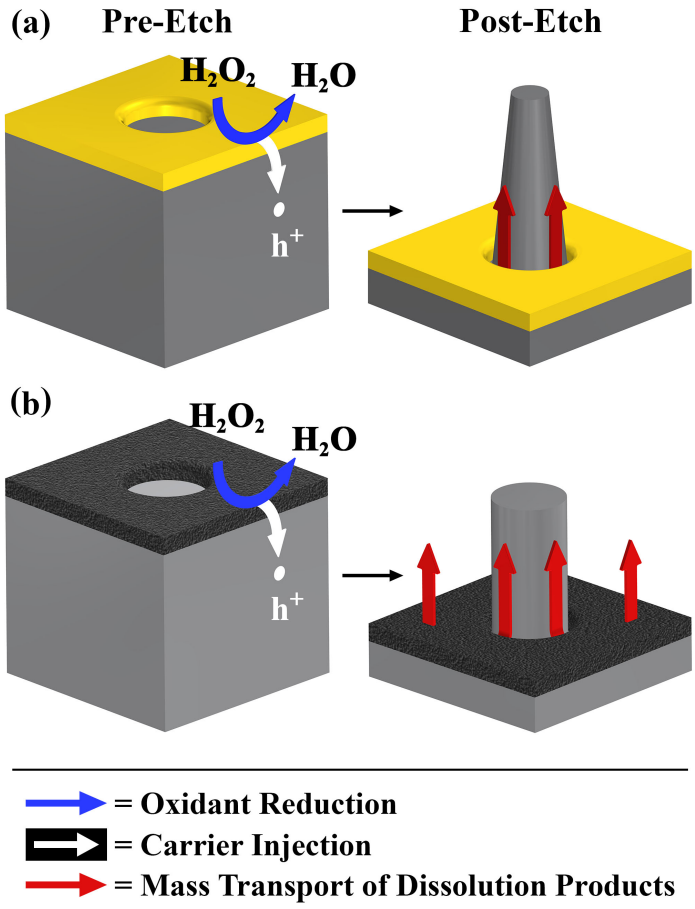

Figure 7.10: Schematics showing (left) Pre-etch and (right) post-etch samples using (a) Au- and (b) CNT-catalysts. The blue and white arrows represent cathodic (i.e., charge carrier generation) and anodic (i.e., hole injection) half reactions, respectively. The red arrows indicate mass transport pathways for dissolved material, with additional pathways through the CNT film.

sidewalls) and permits material dissolution beyond the Au/Si interface. As a result, Au-catalyzed MACE is limited by mass transport under the current etching conditions (e.g., relative solution concentrations, catalyst geometry, etc.). Given the comparable work function values of Au and CNTs used here [185], it is anticipated that a built-in potential stemming from interfacial Schottky barrier formation may similarly sweep excess injected holes away from the CNT/Si junction and result in tapered micropillars. Yet, such an effect is not observed, as evidenced by the vertical sidewalls of CNT-ACE-fabricated micropillars shown in Figures 7.2a-c. This may likely be attributed to the additional mass transport pathways provided by the porous catalytic CNT membrane. That is, the catalytically formed oxide is likely dissolved before injected holes have an opportunity to be swept away to the non-CNT-interfaced regions. Thus, the etching behavior observed here for CNT-ACE is likely charge carrier generation-limited for undoped CNT membranes, while a carrier transport-limited regime may be enabled for doped CNTs with aggregate reduction potentials approaching that of Au.

7.4.8 Comparison with Existing Literature

Lastly, we compare the current study to other reports of Si MacEtch that use unconventional C-based catalysts. Graphene-assisted chemical etching (GaCE) was demonstrated by Kim et al. in 2015 [173]. The authors use chemical vapor deposition to grow graphene films that are then transferred to Si substrates. An anodic aluminum oxide (AAO) mask was patterned using a copper(II) chloride solution. The AAO was then used as a hard mask to transfer its patterning to the graphene film using O_2 plasma etching. Several etching regimes were found while using a GaCE solution containing HF and H_2O_2; namely, porous Si was generated with solutions consisting of a low ratio of HF to H_2O_2, whereas no etching was observed for relatively high concentrations of HF. However, nanowire formation was induced by increasing the etching temperature to 50 °C while using a solution that otherwise resulted in porous

Si [173]. Carbon nanotube-assisted chemical etching was first reported by Hu et al. earlier this year [174]. The authors deposited an aqueous CNT solution onto Si wafer substrates, followed by etching in an aerated HF/H_2O vapor. During etching, the CNT bundles showed a tendency to float away from the Si surface, due to a lack of substrate adhesion. The authors enhanced the etching rate by plating Ag onto the CNTs via electrodeposition, which successfully resulted in randomly textured Si surfaces with reflectance of $\sim$7 % [174]. The work presented in the current work aims to build upon these initial studies towards establishing viable paths for MACE schemes utilizing C-based catalysts. Room-temperature CNT-ACE is demonstrated to successfully generate ordered Si micopillar arrays with solar-weighted reflectance of $\sim$2 %, while simultaneously achieving process simplification through use of standard lithography and liquid-phase etching. Moreover, fabrication of periodically ordered and large-area micropillar arrays is realized by direct solution transfer of the CNT membranes with tunable $KAuBr_4$ doping.

7.5 Conclusions

A room-temperature and solution-based semiconductor fabrication process has been detailed here that uses CNT membranes to catalyze the reduction of H_2O_2, while HF simultaneously and preferentially dissolved the selectively oxidizes substrate regions. Uniform CNT films were generated using a vacuum filtration technique, which were then deposited onto Si substrates via solution transfer. Vertical etch rates for CNT-ACE and Au-catalyzed MACE were been found to be 27.5 and 234.3 nm/min, respectively, whereas CNT-doping with $KAuBr_4$ shifted their aggregate reduction potential towards that of pure-Au. This resulted in enhanced VERs of 59.2 and 141.5 nm/min for 5 and 15 mmol/L $KAuBr_4$, respectively. Raman spectroscopy and Auger electron spectroscopy were performed, and no degradation of the CNT films was detected throughout etching. UV-Vis spectrophotometry was performed as well, with

solar-weighted reflectance found to be 14.04 % for Au-MACE, and 2.05 % for CNT-ACE samples. Thus, CNT-catalyzed etching reduces solar-weighted reflectance by 94.3 % compared to bare Si, which is a 33.2 % improvement over similarly etched Au-catalyzed MACE. Therefore, utilizing CNT-ACE does not require post-etch catalyst removal for devices with low reflectance criteria. A model for the observed mechanism has been presented, with additional mass transport pathways available for dissolved material through the CNT-catalyst fibers. CNT-ACE is anticipated as a practical route towards CMOS-compatible, solution-based, and anisotropic etching of Si, as well as a process-simplifying scheme for optoelectronic devices requiring low-reflectance embedded contacts. Additionally, it is envisioned that CNT-ACE can be expanded for fabrication of III-V micro- and nano-structures for scenarios benefiting from Si and III-V integration, as well as III-V fabrication limited by Si processing constraints.

Chapter 8

Au-Catalyzed MacEtch for Lithography-Free Black GaAs

8.1 Summary

A practical nanofabrication process is detailed here for the generation of black GaAs. Discontinuous thin films of Au nanoparticles are electrodeposited onto GaAs substrates to catalyze site-specific etching in a solution of $KMnO_4$ and HF according to the metal-assisted chemical etching mechanism. This provides a solution-based and lithography-free method for fabricating sub-wavelength nanostructure arrays that exhibit solar-weighted reflectance approaching 4%. This two-step benchtop process can be entirely performed at room-temperature without lithographic patterning, vacuum instrumentation, or bottom-up epitaxial growth, providing an alternative high-throughput nanotexturing approach for thin-film photovoltaics applications.

8.2 Motivation

Metal-assisted chemical etching (MacEtch) techniques are simple and cost-effective semiconductor nanofabrication methodologies whereby selective wet-chemical etching occurs in the presence of a metal catalyst (e.g., Au, Ag, etc.) [8, 12, 43]. First, a thin catalyst layer is deposited in direct contact with a semiconductor, followed by submersion in a solution consisting of an acid and an oxidant [20]. MacEtch mechanisms may be interpreted based on a galvanic cell model, whereby the metal catalyzes the reduction of oxidant species within the solution, causing site-specific hole

injection and localized oxidation of the substrate [42, 164]. The MacEtch solution is then tailored to preferentially dissolve the selectively oxidized substrate [38, 164].

GaAs is used in a wide variety of applications, such as optoelectronic [20] and photovoltaic [186] devices, which highlights the need for alternative GaAs micro- and nano-structure fabrication techniques. GaAs nanostructure fabrication can be realized through both wet- and dry-etch processing, each with a slew of advantages and limitations. For example, inductively-coupled plasma reactive-ion etching (ICP-RIE) often requires hazardous gases and high vacuum conditions [187, 188]. Moreover, most GaAs MacEtch processes involve high-vacuum metal deposition [20] and/or nanoparticle catalyst formation via thermal agglomeration under annealing conditions approaching the substrates congruent sublimation temperature [30, 39]. Alternatively, Lova et al. have outlined a room-temperature MacEtch process whereby micrometer-scale structures are generated using electroless Au deposition for catalyst formation [164].

8.3 Introduction

Here, an entirely solution-based, lithography-free, and low-temperature nanofabrication process is presented for the generation of black GaAs with hemispherical solar-weighted reflectance (SWR) less than 5%. Specifically, electrodeposition and MacEtch are coupled such that every fabrication step may be performed in a conventional wet-bench without the need for elevated temperatures, hazardous process gases, high vacuum instrumentation, or epitaxial growth. This nanofabrication technique can be utilized as an efficient method to improve spectral absorbance for GaAs photovoltaics.

8.4 Experimental Details

All experiments were performed on semi-insulating GaAs(100) substrates. All wafers were cleaned with solvents prior to native-oxide removal in ammonium hydroxide (NH_4OH). Au was deposited via electrodeposition using sulfite gold plating solution at 60 °C, and with constant current density of 50 mA/cm^2. Three samples, denoted A, B, and C, were prepared with different fabrication parameters. Electrodeposition times (t_{ED}) were 24 min for Sample A, and 12 min for Sample B and Sample C. It should be noted that electrodeposition conditions (i.e., time and current density) may be adjusted to accommodate the use of doped substrates. All MacEtch experiments were performed at room temperature using a solution containing 14.072 mol/L hydrofluoric acid (HF) and 0.011 mol/L potassium permanganate ($KMnO_4$). MacEtch times (t_{ME}) were 30 min for Sample A and Sample B, and 60 min for Sample C. Sample preparation and etching conditions can be found in Table 8.1. Imaging was performed by scanning electron microscopy (SEM), and total (specular and diffuse) hemispherical reflectance spectra were measured using a spectrophotometer with an integrating sphere. Raman spectroscopy was performed using laser light at 532 nm, focused on the sample using a long-working-distance microscope objective with numerical aperture of 0.6 and 40× magnification. The incident power at the sample was 300 μW with a spot size diameter of 1 μm. The Raman scattered light was passed through a laser line filter into a

Table 8.1: Overview of sample preparation conditions for Au-catalyzed GaAs etching trials.

Sample	Electrodeposition			MacEtch			
	Time (t_E; min)	**Current Density** (mA/cm^2)	**Solution Temp.** (°C)	**Time** (t_M; min)	**HF Conc.** (mol/L)	**$KMnO_4$ Conc.** (mol/L)	**Solution Temp.** (°C)
A	24	50	60	30	14.072	0.011	Room Temp.
B	12			30			
C	12			60			

monochromator and dispersed onto a 1340 × 100 pixel CCD array photodetector.

8.5 Results and Discussion

8.5.1 Tuning Catalyst Size and Surface Coverage

Figure 8.1 shows top-view SEM images of pre-MacEtch samples wherein the catalyst geometry is modified using two Au electrodeposition times (t_{ED}). Figure 8.1a shows t_{ED} = 24 min and corresponds to Sample A with an average Au nanoparticle diameter of ∼195 nm. Figure 8.1b shows t_{ED} = 12 min and represents Samples B and C with an average Au diameter of ∼65 nm. Thus, a contiguous and porous Au film is formed

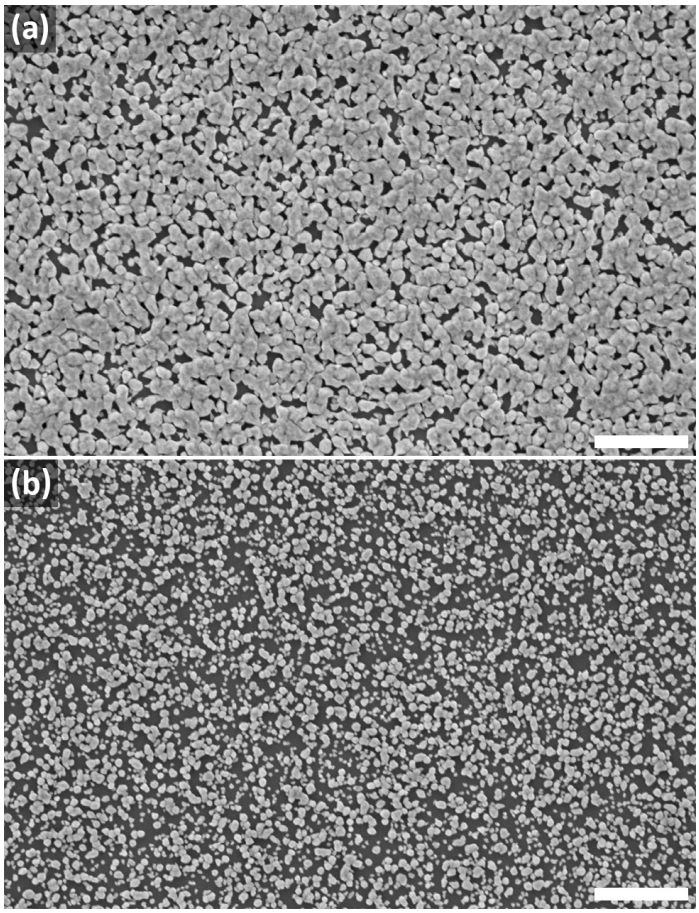

Figure 8.1: Top-view SEM images showing pre-MacEtch GaAs after Au electrodeposition for (a) t_{ED} = 24 min (Sample A) and (b) t_{ED} = 12 min (Samples B and C). Scale bars represent 1 μm.

after t_{ED} = 24 min, whereas only discrete particles are deposited after t_{ED} = 12 min. Deposition times longer than 24 min result in continuous Au film formation with increased overall substrate surface coverage, which is undesirable for the current MacEtch process.

8.5.2 Controlling Nanostructure Size and Morphology

MacEtch trials are performed over two different process periods, as seen in the tilted-view (top row) and cross-section (bottom row) SEM images in Figure 8.2. Sample A (Figure 8.2a,d) and Sample B (Figure 8.2b,e) show comparable etch depths, and both samples provide vertical arrays of GaAs nanowires after t_{ME} = 30 min. Importantly, the discrete Au nanoparticles of Sample B are not observed to deviate from vertical etch directions (i.e., detouring effect) after a 30 min MacEtch step. However, the distinct catalyst size and substrate coverage on Samples A and B yield etched nanowires of disparate sizes; the average nanowire diameters for Samples A and B are ∼325 nm and ∼170 nm, respectively, with aspect-ratios of ∼6.5 and ∼14, respectively. Although, Sample B and Sample C (Figure 8.2c,f) have equivalent Au size and coverage (t_{ED} = 12 min), they result in dramatically dissimilar nanostructure morphologies due to differing values of tME (30 and 60 min, respectively). In the case of Sample C, the longer MacEtch time results in exaggerated Au nanoparticle detouring and generation of non-vertical structures. Moreover, smaller dimension nanostructures (< 500 nm) are lost in the case of Sample C as catalyst etching paths begin to cross. Here, the role of catalyst detouring is expected to be more influential in the loss of smaller structures than lateral etching. That is, the effects of lateral etching are present throughout all MacEtch trials, regardless of nanoparticle detouring. The effects of lateral etching are more noticeable for longer etch times. However, the resulting structures would be conical, with the top of the nanowires having smaller diameters than their base. Therefore, considering lateral etching alone would not explain the loss of smaller (i.e.,

$<$ 500 nm) structures. Instead, excluding the influence of nanoparticle detouring, and considering only exaggerated lateral etching, would result in nanocones, potentially with shorter lengths than those observed nanowires in Figure 8.2a,b.

While only semi-insulating (SI) GaAs(100) has been employed in the current study, it is anticipated that doped GaAs substrates of alternative orientations can also be used for MacEtch fabrication of similar nanowire arrays, albeit at modulated lateral and vertical etch rates depending on dopant type and concentrations [20, 23, 42, 43]. To that end, discussion of doping must be separated into two steps during the MacEtch process; that is, (1) whether holes are catalytically injected into the semiconductor substrate, and (2) whether holes are affected once they have been injected. First, the accepted MacEtch model is based on a galvanic cell, whereby the oxidant within the solution is reduced at the metallic catalyst, which generates charge carriers that are locally injected into the substrate. Here, the value of merit is the relative alignment of the catalyst reduction potential and the semiconductor ionization potential (i.e., valence band edge). Therefore, hole injection is independent of doping (i.e., work-

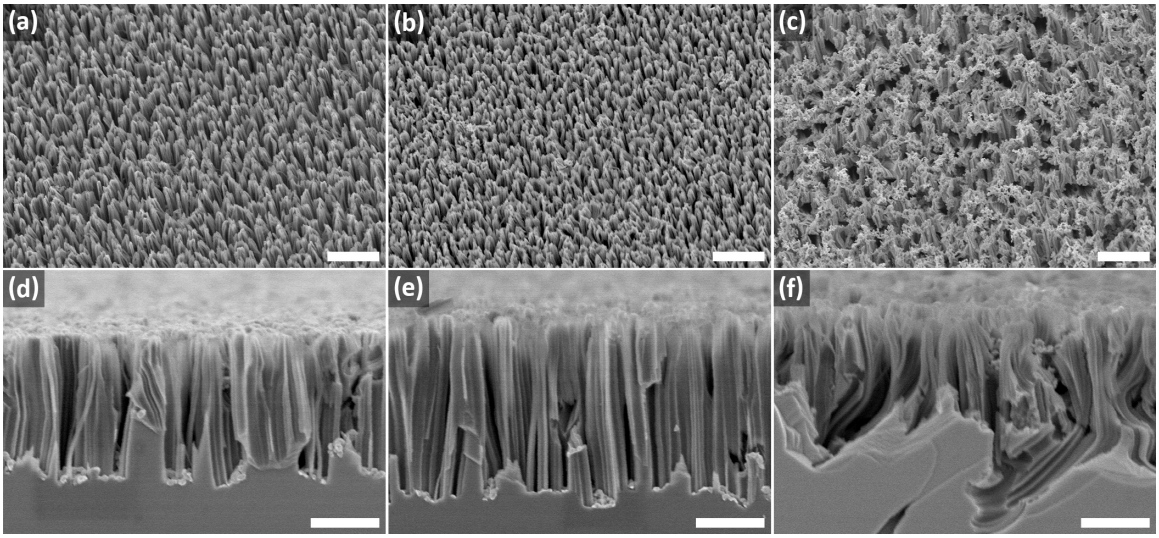

Figure 8.2: Tilted-view (top row) and cross-sectional (bottom row) SEM images showing (a,d) Sample A after $t_{\mathrm{ED}} = 24$ min and $t_{\mathrm{ME}} = 30$ min, (b,e) Sample B after $t_{\mathrm{ED}} = 12$ min and $t_{\mathrm{ME}} = 30$ min, and (c,f) Sample C after $t_{\mathrm{ED}} = 12$ min and $t_{\mathrm{ME}} = 60$ min. Scale bars in (a-c) represent 3 μm, and in (d-f) represent 1 μm.

function or Fermi level). Second, we must consider whether holes that have been injected are affected by doping. This point was studied at length by Lai et al [23]. In short, the metal-semiconductor interface creates a Schottky barrier that dictates the spatial distribution of injected holes. That is, n-type semiconductors trap injected holes near the catalyst and result in enhanced vertical etching, whereas p-type substrates encourage holes to drift away from their injection sites and result in additional lateral etching. This analysis is particularly relevant in the forward-progression MacEtch regime, which is defined by a catalyst that sinks into the substrate during etching. In this current study, doping also plays a major role during the electrodeposition process. That is, Au will be deposited at a higher rate for doped GaAs substrates, which can be offset by tuning the electrodeposition conditions (i.e., time and current density) to achieve a desired deposition rate.

8.5.3 Reducing Solar-Weighted Reflectance

Figure 8.3 shows total hemispherical reflectance (i.e., specular and diffuse) spectra for bare GaAs (black curve; pre-MacEtch) and MacEtched black GaAs Samples A, B, and C (red, cyan, and blue curves, respectively). The inset shows a photograph of side-by-side specular (pre-MacEtch, left) and matte (post-MacEtch, right) samples. The hemispherical SWR is calculated by weighing hemispherical reflectance with an appropriate solar irradiance spectrum11, in this case Air Mass 1.5. Bare GaAs is determined to have 35.87% ± 0.19% SWR over the measured range of 280 nm to 800 nm, with the uncertainty representing the first standard deviation from the mean for at least three SWR measurements. The introduction of random nanostructures induces a graded refractive index and reduces Fresnel reflections, leading to SWR values of 5.21% ± 0.11%, 4.070% ± 0.059%, and 8.20% ± 0.13% for Samples A, B, and C, respectively. Thus, Sample B exhibits an 89% reduction in SWR compared to bare GaAs. Although Samples A and B have comparable overall etch depths, a more Lambertian surface

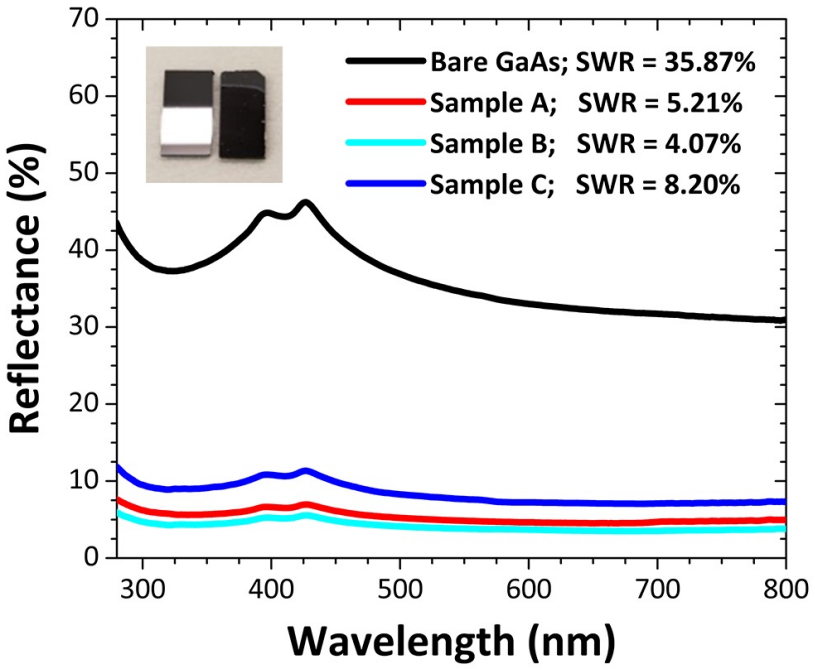

Figure 8.3: Total hemispherical reflectance for bare GaAs (pre-MacEtch) and MacEtched GaAs (Samples A C). Corresponding hemispherical SWR values are shown in the legend. Inset: photograph of specular pre-MacEtch (left; fluorescent lamp reflection visible) and matte post-MacEtch (right) samples.

results from shorter t_{ED} and smaller Au nanoparticles. At extended t_{ME} (Sample C), the light-absorbing quality of the surface is ultimately hindered, which is attributed to catalyst detouring and consequent exposure of non-vertical reflective surfaces. The ability to generate random features for improved light trapping is a critical strength of MacEtch over ICP-RIE. Reported reflectance values at 550 nm for GaAs nanowire arrays generated with ICP-RIE range from approximately 3.9% [186] to 6.7% [188] for nanowires of diameter 60 nm to 70 nm and 500 nm, respectively. In contrast, MacEtched GaAs reflectance values at 550 nm range from approximately 3% at normal incidence for structures with diameter of 5 m (reported by Lova et al. [164]), to 3.8% with sub-wavelength nanostructures (demonstrated here).

8.5.4 Evaluating Parasitic Phases via Raman Spectroscopy

Figure 8.4 shows the Raman scattering spectrum for Sample C (blue curve), while the inset shows a comparison with bare GaAs (black curve). The position and full-width at half-maximum (FWHM) of Raman peaks are determined using Lorentzian fitting of the deconvolved spectra (inset, grey curves). Crystal orientation determines which mode(s) are excited within bulk samples, based on selection rules [38]. Bare zinc-blende GaAs(100) exhibits a strong longitudinal optical (LO) peak at 292.3 cm^{-1} with a FWHM of 3.1 cm^{-1} (inset, black curve), as expected for the bulk substrate [189]. However, the anisotropic nature of MacEtch-generated nanostructures modulates modal angular dependencies and permits orthogonal polarization scattering that is forbidden by bulk selection rules [190]. Consequently, distinct transverse optical (TO) phonon modes are observed in the MacEtched sample (blue curve). Additionally, phonons that are confined along the free surfaces of nanowires induce an additional surface optical (SO) phonon mode in the Raman spectrum of the MacEtched sample. Thus, Sample C shows TO, SO, and LO peaks centered at 268.8 cm^{-1}, 288.4 cm^{-1},

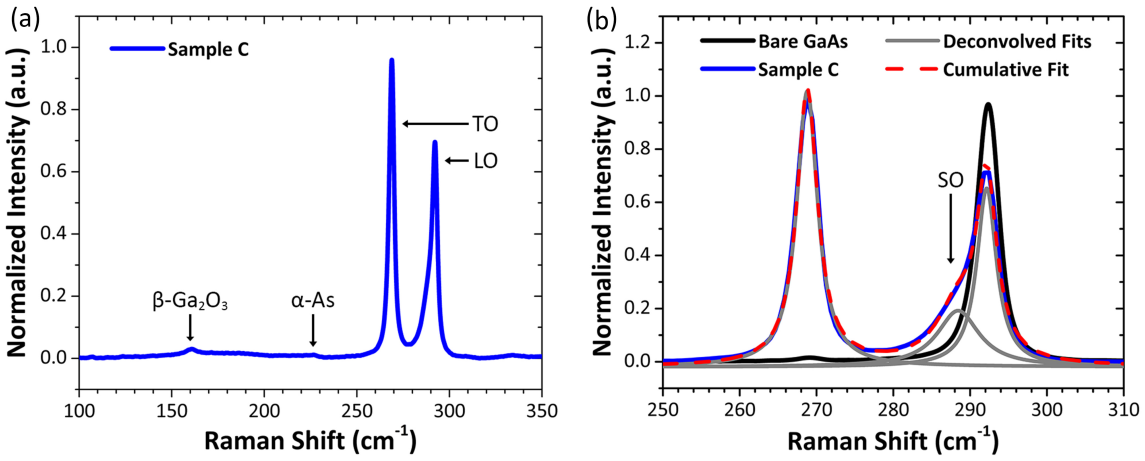

Figure 8.4: (a) Post-MacEtch Raman spectrum for Sample C (blue curve) with only trace amounts of β-Ga_2O_3 and α-As phases. (b) Spectral deconvolution and Lorentzian fitting (grey curves) of Sample C to determine frequency and FWHM of TO, SO, and LO peaks. The red dashed curve shows the cumulative fit. The bare GaAs(100) Raman spectrum (black curve) for comparison.

and 291.1 cm^{-1}, respectively, with corresponding FWHM values of 3.3 cm^{-1}, 6.5 cm^{-1}, and 3.1 cm^{-1}. All values are in agreement with previously published theoretical and experimental values reported for top-down GaAs nanowires [191]. Unlike prior reports of GaAs nanowires fabricated by MacEtch using similar solutions, [38] no broadening or redshift in the LO peak is observed here, and a significant amount of TO and SO scattering is found in post-MacEtch GaAs. This can be explained by the disparity in structural orientation (e.g., ordered and random arrays) and morphology (e.g., diameter and height). Lastly, the current black GaAs samples do not show substantial formation of β-Ga_2O_3, crystalline As (c-As), or amorphous As (α-As) phases, which is in contrast to previously reported GaAs nanowires after MacEtch under similar conductions [38] and ICP-RIE-fabricated GaAs nanowires after photo-thermal excitation [191]. The absence of such parasitic phases holds promise for integration of MacEtch-fabricated black GaAs in thin-film and flexible membrane photovoltaic devices.

8.6 Conclusions

An entirely solution-based and lithography-free nanofabrication process has been described using a two-step method involving electrodeposition and MacEtch. The generation of black GaAs with hemispherical solar-weighted reflectance of 4.07% was demonstrated, which represents an 89% reduction compared with bare GaAs. This approach has potential as a straightforward and cost-efficient means of engineering nanotextured solar cell surfaces.

8.7 Future Works

Although the current study relates specifically to semi-insulating (SI) GaAs, it is envisioned that this process may be applied to degenerately-doped substrates to

create antireflective layers and back-surface reflectors for solar cells of various material systems. To that end, see Chapter 10 for an example of this process applied to AlGaAs.

Chapter 9

Summary of Work

9.1 Summary

The work presented here details alternative semiconductor nanofabrication methodologies that combine many of the advantages of both wet- and dry-etching, while simultaneously overcoming their limitations. Metal-assisted chemical etching of the ternary allows InGaP and AlGaAs were demonstrated for the first time, for viable pathways towards the formation of suspended III-V nanofoils and ordered nanopillar arrays. An entirely solution-based and lithography-free method has been outlined for the fabrication of black GaAs with solar-weighted reflectance of ∼4 %. Lastly,

9.2 Research Contributions

9.2.1 Peer-Reviewed Publications

9.2.1.1 First-Author Publications

1. **T. S. Wilhelm**, C. W. Soule, M. A. Baboli, C. J. O'Connell, and P. K. Mohseni, "Fabrication of Suspended III-V Nanofoils by Inverse Metal-Assisted Chemical Etching of $In_{0.49}Ga_{0.51}P$/GaAs Heteroepitaxial Films", *ACS Appl. Mater. Interfaces* 10 (2), 2058-2066 (2018)

2. **T. S. Wilhelm**, Z. Wang, M. A. Baboli, J. Yan, S. F. Preble, and P. K. Mohseni, "Ordered $Al_xGa_{1-x}As$ Nanopillar Arrays via Inverse Metal-Assisted Chemical

Etching", *ACS Appl. Mater. Interfaces* 10 (32), 27488-27497 (2018)

3. **T. S. Wilhelm***, A. P. Kolberg*, M. A. Baboli, A. Abrand, K. A. Bertness, and P. K. Mohseni, "Black GaAs with Sub-Wavelength Nanostructures Fabricated via Lithography-Free Metal-Assisted Chemical Etching", *ECS J. Solid State Sci. Technol.* 8 (6) Q134-Q136 (2019)
   *Equal contribution authorship

4. **T. S. Wilhelm***, I. L. Kecskes*, M. A. Baboli, A. Abrand, M. S. Pierce, B. J. Landi, I. Puchades, and P. K. Mohseni, "Fabrication of Ordered Si Micropillar Arrays via Carbon Nanotube-Assisted Chemical Etching", Submitted to *ACS Applied Nano Materials* on September 23, 2019, manuscript ID: an-2019-01838h
   *Equal contribution authorship

9.2.1.2 Co-Author Publications

1. M. A. Baboli, M. A. Slocum, H. Kum, **T. S. Wilhelm**, S. J. Polly, S. M. Hubbard, and P. K. Mohseni, "Improving Pseudo-van der Waals Epitaxy of Self-Assembled InAs Nanowires on Graphene via MOCVD Parameter Space Mapping", *CrystEngComm* 21 (4), 602-615 (2019)
   **This work was selected as the back cover article of CrustEngComm, January (Issue 4), 2019.

2. S. Biria, **T. S. Wilhelm**, P. K. Mohseni, and I. Hosein, "Direct Light-Writing of Nanoparticle-Based Metallo-Dielectric Optical Waveguide Arrays Over Silicon Solar Cells for Wide-Angle Light Collecting Modules", *Adv. Optical Mater.* 1900661 (2019)

9.2.2 Conference Presentations

1. **T. S. Wilhelm**, S. Lakshminarayanamurthy, C. J. O'Connell, M. A. Baboli, and P. K. Mohseni, "Parameter Space Exploration of Metal-Assisted Chemical Etching for Si Micro- and Nano-Fabrication", *40th Annual IEEE EDS in Western New York Conference*, Rochester, New York, United States. November 2016

2. **T. S. Wilhelm**, M. A. Baboli, C. J. O'Connell, S. Lakshminarayanamurthy, and P. K. Mohseni, "Generation of Si and III-V Micro- and Nano-Structures via Metal-Assisted Chemical Etching Techniques", *17th Annual CEIS Technology Showcase*, Rochester, New York, United States. April 2017

3. **T. S. Wilhelm**, Z. Wang, C. W. Soule, M. A. Baboli, J. Yan, S. F. Preble, and P. K. Mohseni, "Inverse Metal-Assisted Chemical Etching of Ternary III-V Alloys", *42nd Annual IEEE EDS in Western New York Conference*, Rochester, New York, United States. November 2018

4. **T. S. Wilhelm**, Z. Wang, C. W. Soule, M. A. Baboli, J. Yan, S. F. Preble, and P. K. Mohseni, "Versatile Nanomanufacturing of Ternary III-V Nanostructure Arrays via Inverse Metal-Assisted Chemical Etching", *2018 Materials Research Society Fall Conference*, Boston, Massachusetts, United States. November 2018

5. **T. S. Wilhelm**, A. P. Kolberg, Z. Wang, C. W. Soule, M. A. Baboli, A. Abrand, J. Yan, S. F. Preble, and P. K. Mohseni, "Metal-Assisted Chemical Etching for Simple, Cost-Effective, and Large-Scale III-V Semiconductor Nanofabrication", *235th Electrochemical Society Conference*, Dallas, Texas, United States, May 2019

6. **T. S. Wilhelm**, A. P. Kolberg, Z. Wang, C. W. Soule, M. A. Baboli, A. Abrand, J. Yan, S. F. Preble, and P. K. Mohseni, "Simple and Cost-Effective III-V Compound Semiconductor Nanofabrication via Metal-Assisted Chemical

Etching", *2019 Electronic Materials Conference*, Ann Arbor, Michigan, United States, June 2019

Chapter 10

Future Works

10.1 Carrier-Selective GaAs Photovoltaics

10.1.1 Planar Carrier-Selective Asymmetric Heterojunction

10.1.1.1 Motivation and Introduction

Improving todays photovoltaic devices comes down to considering a dollars-per-watt (DPW; \$/W) metric. While marginal increases in power conversion efficiency (PCE; η) continue to be reported for single-junction III-V photovoltaics due to innovative device

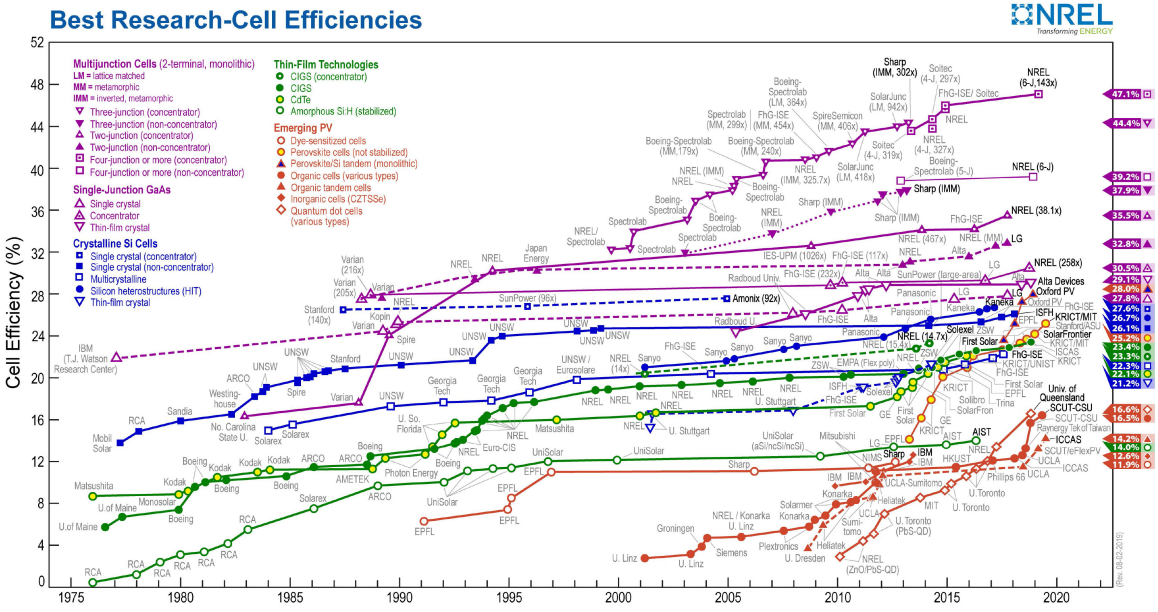

Figure 10.1: Chart showing the best recorded power conversion efficiencies for various photovoltaic structures [192].

designs (see Figure 10.1, which shows the most recent PCE chart published by the National Renewable Energy Laboratory [192]), the primary focus is now on reducing the fabrication costs without sacrificing PCE or reliability. Initially, cost-reduction was promoted by decreasing solar cell thickness [90], thereby reducing the cost of material. However, conventional device processing requires a relatively high thermal budget, which became a limiting factor for device thinning due to wafer bending and lattice strain at elevated temperatures [91]. For the past several decades, one approach for cost reduction is the transition from traditional p-n junctions towards heterojunction designs, as the latter can use transition metal oxides (TMOs) for carrier selectivity. This allows for processing temperatures less than 200 °C [92, 93] and wafer thinning below 100 μm [91].

Transition metal oxides are large band gap semiconductors with high work functions, and are leading contenders as a replacement for the a-Si:H emitter in silicon heterojunction (SHJ) devices [108]. TMOs can provide high carrier inversion and tunable electrical properties [109], along with a variety of material compositions to choose from. Although TMOs act as n-type semiconductors due to their inherent oxygen vacancies, their large work functions allow them to serve as n- or p-contacts due to band alignment with the substrate [110]. These layers are referred to as carrier selective layers, or electron selective layers (ESLs) and hole selective layers (HSLs). That is, ESLs promote electron transport across the interface while repelling holes, and likewise HSLs allow holes to pass while rejecting electrons. For example, MoO_x, V_2O_5, and WO_3 are common HSLs, and TiO_2, LiF_x, KF_x, and CsF_x can serve as ESLs [110].

Using transition metal oxides (TMOs) as carrier-selective layers has the potential to reduce solar cell fabrication costs and their thermal budget [96]. TMOs can promote carrier separation without the need for expensive growth, or high temperature implantation [91, 96]. TMOs are routinely incorporated into organic [193, 194],

perovskite [73, 194], and SHJ [96, 108, 110] photovoltaic devices; however, very little work has been demonstrated for III-V solar cells using TMOs for carrier separation [114].

The goal for this project is to establish a viable path towards fabrication of carrier-selective asymmetric heterojunction (CSAH) GaAs photovoltaics. Once a process flow is established, MacEtch will be applied to generate a black GaAs (see Chapter 8) front surface.

10.1.1.2 Experimental Details

All experiments were performed on single-side polished p-type GaAs(100) wafers (UniversityWafer) with $p = 4 \times 10^{16}$ - 1×10^{17} cm^{-3}. All wafers were cleaned with standard solvents prior to native-oxide removal in dilute (1:1) ammonium hydroxide (NH_4OH). In order to form an Ohmic contact, Au/Zn/Au (25, 25, and 150 nm, respectively) was deposited on the back side of the substrates by thermal evaporation (Lesker PVD Nano38 Thermal Evaporator). The contacts were then alloyed using a tube furnace under nitrogen environment at 407 °C for 6 min. Following anneal, each wafer was cleaved into quarters for subsequent processing of individual pieces.

Atomic layer deposition (ALD) was used (Ultratech S200 ALD) to deposit titanium dioxide (TiO_2) using tetrakis(dimethylamido)titanium (TDMAT) and DI-H_2O as precursors. The TDMAT precursor manifold was kept at 75 °C throughout deposition, while the chamber itself (i.e., inner and outer rings) were kept at 100 °C. First, a 10 min stabilization step was performed, followed by an iterative process consisting of: a 0.1 s TDMAT pulse and 10 s purge, then a 0.015 s H_2O pulse and 10 s purge. This results in a 0.55 Å/cycle deposition rate for TiO_2 at 100 °C.

Following ALD of TiO_2, samples were immediately loaded for indium-tin-oxide (ITO) sputter (CVC 601). An 8 in ITO target was used in pulsed-DC (250 kHz) mode at 180 W power (i.e., 3.58 W/in^2), with 1616 ns pulse widths, 5 mT chamber pressure,

and with 40 sccm Ar. All samples had a 80 nm thick ITO film deposited, with a deposition rate determined to be 5.5 nm/min after a 1 hr deposition. A follow-up anneal at 250 °C on a hotplate was performed to improve the as-deposited ITO optical and electrical properties.

A 35 nm thick Au film was deposited by thermal evaporation (Lesker PVD 75 Thermal Evaporator) at a rate of ∼1 Å/s to serve as a seed layer for Au electrodeposition. Photolithography was used to pattern the front contacts; a positive photoresist (Shipley 1813) was spin-coated, followed by a 100 °C soft-bake. Exposure and development were performed using a broadband contact aligner (Kuss MA56 Mask Aligner) and CD-26 (Microposit), respectively. Three 0.5 × 0.5 cm^2 solar cells (one-sun configuration, with 4% contact coverage) were patterned per quarter wafer. Au was then deposited via electrodeposition using sulfite gold plating solution (Transene TSG-250) at 60 °C, with a constant current density of 7.64 mA/cm^2 and a duration of 10 min. Residual photoresist was then stripped using an acetone bath. The final fabrication step involved removing the 35 nm thick Au seed layer between the grid fingers. This was achieved by submerging the samples in a Transene TFA solution for 15 s. Lastly, device isolation was achieved via cleaving. An overview of the fabrication process flow for this device is depicted in Figure 10.2.

Solar cell performance was determined using illuminated and dark I-V, as well

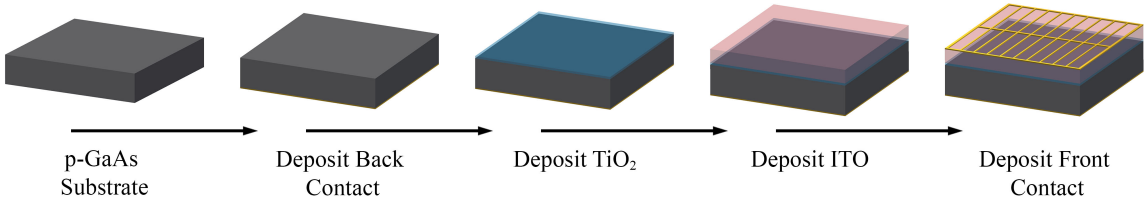

Figure 10.2: Schematics showing the fabrication process flow for planar GaAs carrier-selective photovoltaic devices. First, lightly doped p-GaAs(100) wafers are used as substrates, followed by depositing a p-type (Au/Zn/Au) back contact onto the backside of the wafer. Then, TiO_2 and ITO are subsequently deposited onto the top surface of the wafer via ALD and sputtering, respectively. Lastly, photolithography and Au electrodeposition are used to realize the front grid.

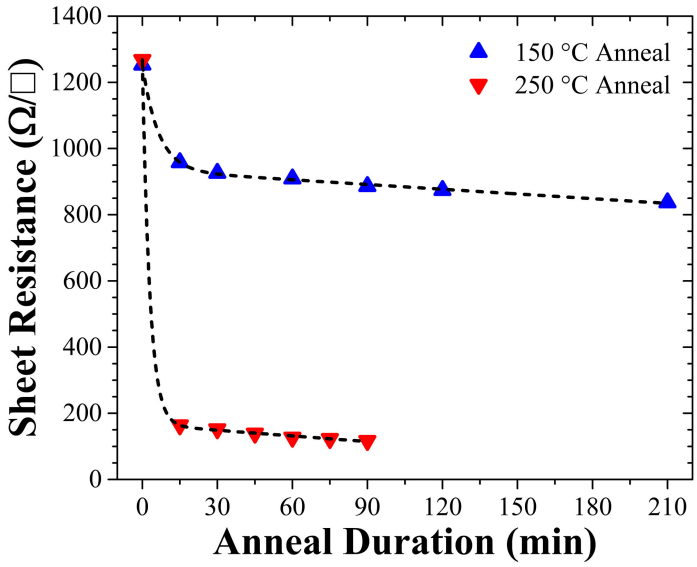

Figure 10.3: Sheet resistance for 80 nm thick ITO films after being subjected to post-deposition anneals at (blue triangles) 150 °C and (red triangles) 250 °C.

as spectral response and quantum efficiency. A dual source 18 kW solar simulator (TS Space Systems), with additional Air Mass (AM) 1.5 filters installed, was used to measure the I-V characteristics under illumination. A 6 kW mercury halide arc lamp is used to create the ultraviolet and visible portions of the spectrum, and a 12 kW quartz tungsten halogen lamp is used to generate the infrared portion. Dark I-V and J_{SC}-V_{OC} were performed using a Kiethley 2400 SMU was, which also extracts dark series resistance, idealities, and dark saturation currents. Finally, spectral response was measured using a Newport IQE-200 Automated EQE/IQE measurement system with a focused spot size of 1 × 2 mm^2.

ITO electrical properties (i.e., sheet resistance) were measured using 4-point probe mapping (CDE ResMap), as well as optical characterization via UV-Vis spectrophotometry (Shimadzu UV-2600) with an integrating sphere.

10.1.1.3 Results and Discussion

Lightly-doped (i.e., 4 × 10^{16} - 1 × 10^{17} cm^{-3}) p-type GaAs(100) wafers are used as substrates for this study. Carrier-selectivity is achieved by employing TiO_2 deposited

Table 10.1: Solar-weighted transmittance (SWT), reflectance (SWR) and absorbance (SWA) for as-deposited and post-anneal ITO films subjected to anneals at 150 and 250 °C for 210 and 30 min, respectively.

	Pre-Anneal	Post-Anneal		
ITO	SWT = 63.81 % SWR = 0.12 % SWA = 36.08 %	150 °C	4 hr	SWT = 64.85 % SWR = 0.17 % SWA = 34.99 %
	SWT = 63.92 % SWR = 0.08 % SWA = 36.01 %	250 °C	30 min	SWT = 69.85 % SWR = 0.12 % SWA = 30.03 %

via ALD, followed by sputtering a 80 nm thick ITO contact layer. Finally, the front contact is realized through photolithography and Au electrodeposition.

A 80 nm thick ITO contact layer is employed on these devices. The electrical and optical characteristics of the as-deposited films are measured. Then, the films are annealed at two different temperatures, namely 150 and 250 °C, to determine if their properties change. The as-deposited sheet resistance for a 80 nm thick ITO film is found to be over 1250 Ω/□, as seen in Figure 10.3. Employing a 150 °C (blue triangles) reduces the sheet resistance to ∼950 Ω/□ after 15 minutes, which then

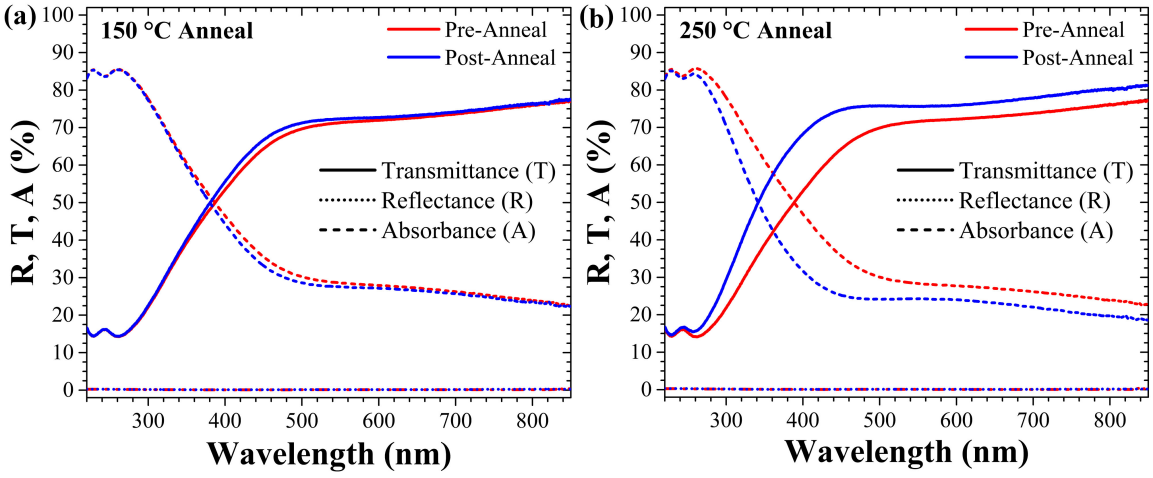

Figure 10.4: Total hemispherical (i.e., specular and diffuse) reflectance (dotted lines), absorbance (dashed lines), and transmittance (solid lines) for as-deposited (red lines) and post-anneal (blue lines) ITO films subjected to anneals at (a) 150 °C for 210 min, and (b) 250 °C for 30 min.

Table 10.2: Illuminated J-V cell performance for planar GaAs CSAH devices.

	001-1	011-3	003-3	008-1	010-3
TiO_2 Thickness (nm)	20	15	10	5	0
Cell Area (cm^2)	0.302	0.304	0.286	0.265	0.256
J_{SC} (mA/cm^2)	19.77	17.67	20.15	19.36	16.70
V_{OC} (mV)	273.3	241.7	304.5	235.5	233.9
FF (%)	64.57	63.60	60.94	61.21	59.98
η (%)	3.49	2.70	3.74	2.79	2.34

drops linearly with time. After an extended anneal at 150 °C for 210 min, the sheet resistance is found to be 837 Ω/□. In comparison, the sheet resistance drops to 164 Ω/□ after a 15 minute anneal at 250 °C (red triangles), which is further reduced to 117 Ω/□ after a total of 90 min.

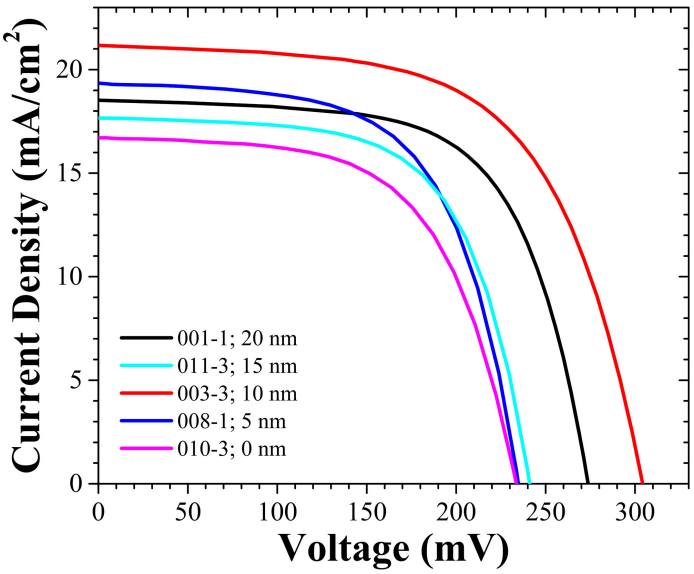

Figure 10.5: Illuminated J-V curves for planar GaAs CSAH devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm.

The optical properties of the as-deposited and annealed ITO films are characterized as well. Figure 10.4 shows total hemispherical (i.e., specular and diffuse) reflectance (dotted lines), absorbance (dashed lines), and transmittance (solid lines) for as-deposited (red lines) and post-anneal (blue lines) films after being subjected to a 150 °C (panel a) and 250 °C (panel b) anneal. Following a 150 °C anneal for 210 min, transmittance is slightly increased and shifted towards the UV. As seen in Table 10.1, solar-weighted (using the AM1.5 spectrum) transmittance (SWT) is increased by 1%, from 63.81 to 64.85%. After a 250 °C anneal for 30 min, transmittance is increased and shifted more substantially towards the UV. Here, SWT increases almost 6%, from 63.92 to 69.85%.

Figure 10.5 shows illuminated J-V curves for planar GaAs CSAH photovoltaic devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm. The illuminated J-V performance of these devices is tabulated in Table 10.2.

Figure 10.6 shows dark J-V curves for planar GaAs CSAH photovoltaic devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm.

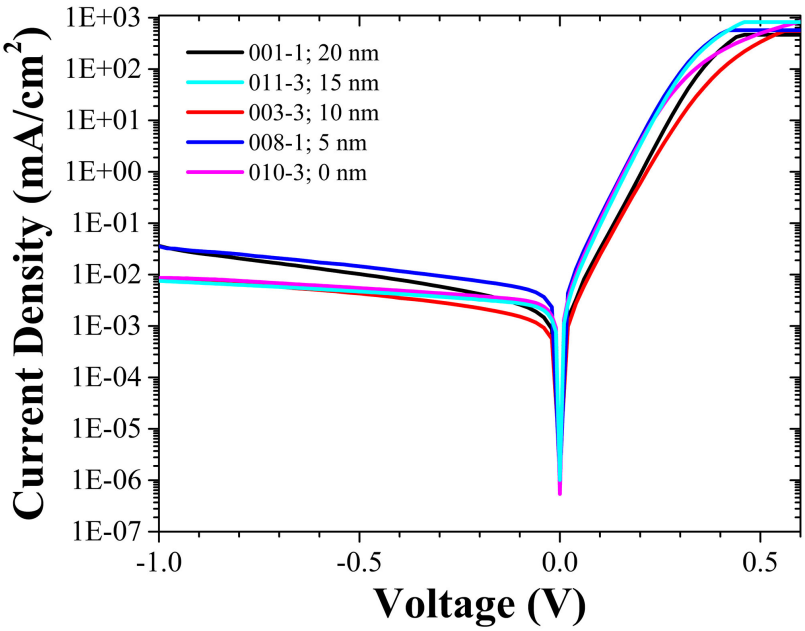

Figure 10.6: Dark J-V curves for planar GaAs CSAH devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm.

The ideality factor (n) is determined to be 1, which is expected for a Schottky device. This is found by plotting J_{SC} as a function of V_{OC} on a semi-log plot, and finding the slope of the linear regime. Figure 10.7 shows an example of this, with the blue lines representing 60 mV/decade, which equates to n = 1. J_0 is determined to be $\sim 3 \times 10^{-6}$ A/cm^2, which is found by extrapolating the linear regime of Figure 10.7 to the y-axis (red dashed line). The reduced open-circuit voltage (V_{OC}), and therefore the power conversion efficiency (η), observed with these devices (Figure 10.5) is attributed to the cells being dominated by leakage current (i.e., J_0; see Equation 3.42).

Figure 10.8 shows the external quantum efficiency (EQE; panel a), internal quantum efficiency (IQE; panel b), and reflectance (R; panel c) for planar GaAs CSAH photovoltaic devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm. Based on the quantum efficiency spectra, these devices perform better towards the UV-end of the spectrum, which is likely the result of the ITO contact layer acting as an anti-reflective coating. Moreover, carrier-selective geometries inherently result in relatively shallow junctions due to the rectification occurring at

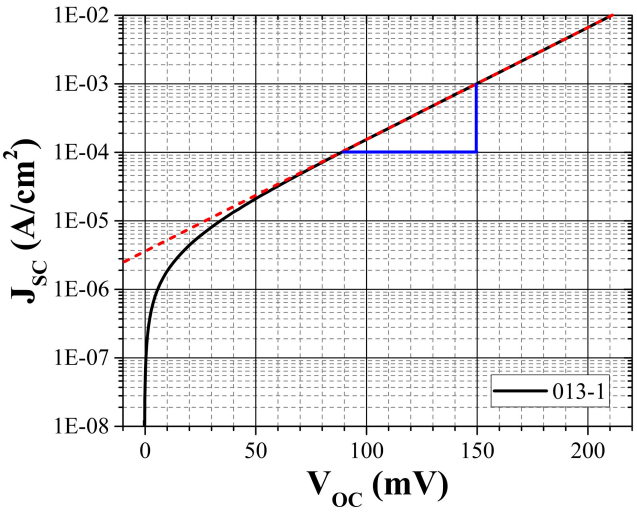

Figure 10.7: Plot demonstrating how to determine the ideality factor (n) and leakage current (J_0). Ideality is calculated from the slope of the linear regime, depicted by blue lines. J_0 is the y-intercept of an extrapolated line from the linear regime (depicted by a red dashed line).

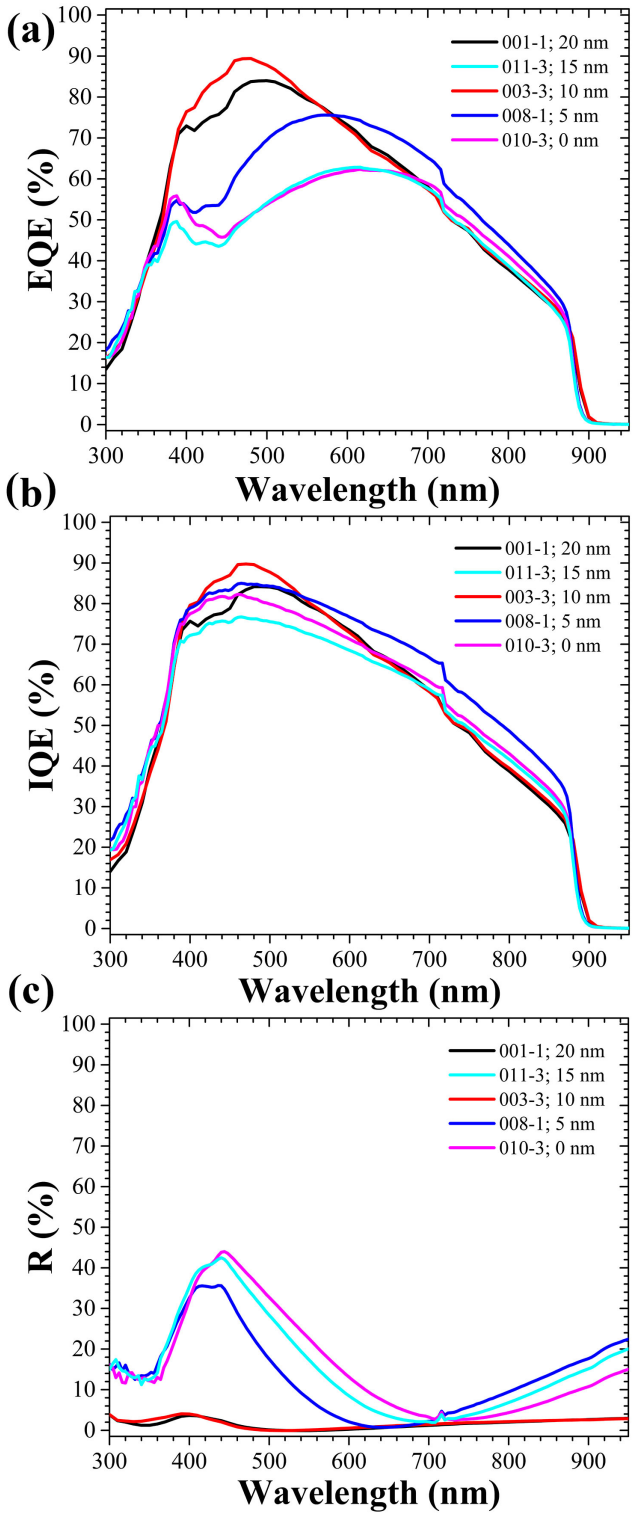

Figure 10.8: (a) External quantum efficiency (EQE), (b) internal quantum efficiency (IQE), and (c) reflectance (R) data for planar GaAs CSAH devices with TiO_2 thickness of (black) 20, (cyan) 15, (red) 10, (blue) 5, and (magenta) 0 nm.

(or near) the surface, which also results in greater blue response.

While initial proof-of-concept for this device structure has been demonstrated here, a continuation and optimization of this work would be useful towards establishing carrier-selective GaAs photovoltaics. Improving upon the work presented here can be broken up into two categories, (1) fabrication and device engineering, and (2) characterization and device physics.

Reproducibility has been a major issue with these devices, which has been the pivotal obstacle impeding optimization of the fabrication process. Figure 10.8a and 10.8c demonstrate an example of this point perfectly. The first round of devices that were fabricated are represented by black and red curves (i.e., samples 001 and 003, respectively), the blue curve illustrates one of the middle rounds of fabrication (i.e., sample 008), whereas the magenta and cyan curves (i.e., samples 010 and 011, respectively) come from the later rounds. Although each round of fabrication was performed identically, a stark difference can be seen in the reflectance (Figure 10.8c) spectra based on the general timeline in which the cells were fabricated. The distinct reflectance spectra translates to disparate EQE spectra as well, with the earlier devices exhibiting superior blue response. This variation over time is attributed to a modification of the ITO film, which is potentially a consequence of the ITO sputtering target being changed in the interim. A dedicated ITO deposition tool would be advantageous in this regard, particularly if the tool relied on RF sputtering instead of pulsed-DC [195].

Another potential solution to some of the reproducibility concerns would be to epitaxially grow a low-doped (e.g., $p = 5 \times 10^{16}$ cm^{-3}) active layer to ensure the crystal quality of the device material. The underlying substrate could be left in place, else eliminated via substrate removal or epitaxial liftoff.

Device modeling should also be performed in parallel with the fabrication process optimization. It is difficult to compare device results with those that are expected

(i.e., modeled) if it is unclear whether the fabrication is inadvertently skewing the data.

Once a reproducible process has been established, the next phase of this project would be a thorough characterization and optimization of the device structure. Varying the carrier-selective layer (in this case TiO_2) would be a worthwhile evaluation. This would be used to determine the minimal thickness required to achieve sufficient rectification, while simultaneously reducing absorption losses within the TiO_2 film. An additional material property to examine would be the affect of the TiO_2 crystallinity. Amorphous and anatase phases could be evaluated by modifying the ALD deposition temperature (i.e., inner and outer rings). These, along with the rutile phase, could also be considered via a post-deposition anneal step.

The essential device attribute in need of future development is the recovery of open-circuit voltage. The short-circuit current density observed here is less problematic than V_{OC}. That is, these devices are generating electron-hole pairs, but they are recombining before leaving the circuit through its terminals. The reduction in V_{OC} is attributed to excessive reverse saturation, or leakage, current (i.e., J_0). One reason this could be unintentionally high is related to the zero-bias barrier height (Φ_b). Depending upon the alignment of the bands at the TiO_2/GaAs interface, Φ_b may be unnecessarily high such that the flow of valance electrons (either by thermionic emission or tunneling) is impeded. Φ_b can be determined by employing Norde's function [196, 197]. If the barrier height is found to be excessively large, GaAs could be grown with an appropriate doping concentration to compensate. Capacitance-voltage (C-V) measurements would also be performed to determine the barrier height, as well as the interface state density (D_{it}) [197]. Furthermore, Schottky devices are known to have significantly reduced V_{OC}, and therefore η, if the back contact is not perfectly Ohmic [198].

10.1.2 Nanostructured Carrier-Selective Asymmetric Heterojunction

10.1.2.1 Motivation and Introduction

Chapter 8 focused on fabrication of black GaAs through an entirely solution-based MacEtch process whereby the Au catalysts are introduced via electrodeposition. This project aims to marry the GaAs CSAH structure with the light-trapping benefit associated with the nanostructures generated via MacEtch. More specifically, both MacEtch and the CSAH architecture are intended to serve as alternative fabrication schemes towards simple and cost-effective processing methodologies.

10.1.2.2 Experimental Details

All experiments were performed on single-side polished p-type GaAs(100) wafers (UniversityWafer) with $p = 4 \times 10^{16}$ - 1×10^{17} cm^{-3}. All wafers were cleaned with standard solvents prior to native-oxide removal in dilute (1:1) ammonium hydroxide (NH_4OH). In order to form an ohmic contact, Au/Zn/Au (25, 25, and 150 nm, respectively) was deposited on the back side of the substrates by thermal evaporation (Lesker PVD Nano38 Thermal Evaporator). The contacts were then alloyed using a tube furnace under nitrogen environment at 407 °C for 6 min. Following anneal, each wafer was cleaved into quarters for subsequent processing of individual pieces.

Then, front surface texturing was achieved using a similar approach to that used in Chapters 8 and 9 (*vide infra*). A positive photoresist (Shipley 1813) was painted onto the back Au/Zn/Au contact for protection during MacEtch, which was then baked in an oven at 100 °C for 10 min. Au nanoparticles were deposited onto the front surface via electrodeposition using sulfite gold plating solution (Transene TSG-250) at 60 °C with a constant current density of 0.64 mA/cm^2 for 30 s. Samples were then MacEtched at room-temperature using a solution containing 14.072 mol/L hydrofluoric acid (HF) and 0.011 mol/L potassium permanganate ($KMnO_4$) for 30 min.

Atomic layer deposition (ALD) was used (Ultratech S200 ALD) to deposit titanium dioxide (TiO_2) using tetrakis(dimethylamido)titanium (TDMAT) and DI-H_2O as precursors. The TDMAT precursor manifold was kept at 75 °C throughout deposition, while the chamber itself (i.e., inner and outer rings) were kept at 100 °C. First, a 10 min stabilization step was performed, followed by an iterative process consisting of: a 0.1 s TDMAT pulse and 10 s purge, then a 0.015 s H_2O pulse and 10 s purge. This results in a 0.55 Å/cycle deposition rate for TiO_2 at 100 °C.

Following ALD of TiO_2, samples were immediately loaded for indium-tin-oxide (ITO) sputter (CVC 601). An 8 in ITO target was used in pulsed-DC (250 kHz) mode at 180 W power (i.e., 3.58 W/in^2), with 1616 ns pulse widths, 5 mT chamber pressure, and with 40 sccm Ar. All samples had a 330 nm thick ITO film deposited, with a deposition rate determined to be 5.5 nm/min after a 1 hr deposition. A follow-up anneal at 250 °C on a hotplate was performed to improve the as-deposited ITO optical and electrical properties (*vide supra*).

Photolithography was used to pattern the front contacts; a positive photoresist (Shipley 1813) was spin-coated, followed by a 100 °C soft-bake. Exposure and development were performed using a broadband contact aligner (Kuss MA56 Mask Aligner) and CD-26 (Microposit), respectively. Three 0.5 × 0.5 cm^2 solar cells (one-sun configuration, with 4% contact coverage) were patterned per quarter wafer. A 300 nm

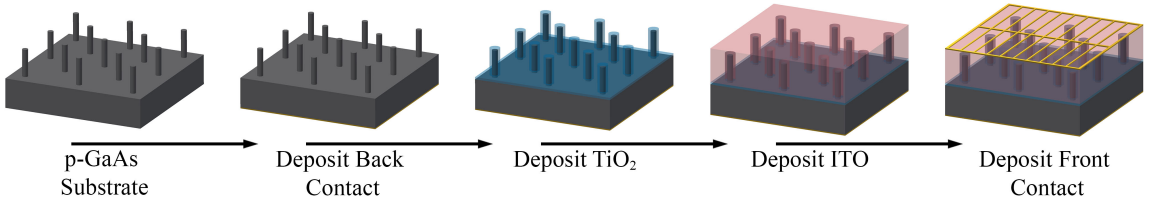

Figure 10.9: Schematics showing the fabrication process flow for nanostructured GaAs carrier-selective photovoltaic devices. First, a p-type (Au/Zn/Au) back contact is thermally evaporated onto the backside of the wafer, followed by the generation of nanostructures - via MacEtch - on the front surface of lightly doped p-GaAs(100) substrates. Then, 20 nm TiO_2 and 330 nm ITO is sequentially deposited onto the top surface of the wafer via ALD and sputtering, respectively. Lastly, photolithography and liftoff are employed to realize the 300 nm thick Au front contact, which itself is deposited via thermal evaporation.

thick Au front contact was then deposited by thermal evaporation (Lesker PVD 75 Thermal Evaporator) at a rate of ∼2 Å/sec, and liftoff was performed in a bath of N-Methyl-2-pyrrolidone (NMP). Lastly, device isolation was achieved via cleaving.

An overview of the fabrication process flow for this device is depicted in Figure 10.9. It follows similar sequencing as the planar design (*vide supra*); however, several key steps were altered to account for the nanostructures. Most notably, a thicker (i.e., 330 nm thick) ITO layer was sputtered in an attempt to planarize the top surface, and a 300 nm thick Au front contact was thermally evaporated (followed by a liftoff process) to realize the front contact.

Solar cell performance was determined using illuminated and dark I-V, as well as spectral response and quantum efficiency. A dual source 18 kW solar simulator (TS Space Systems), with additional Air Mass (AM) 1.5 filters installed, was used to measure the I-V characteristics under illumination. A 6 kW mercury halide arc lamp is used to create the ultraviolet and visible portions of the spectrum, and a 12 kW quartz tungsten halogen lamp is used to generate the infrared portion. Dark I-V and J_{SC}-V_{OC} were performed using a Kiethley 2400 SMU was, which also extracts dark series resistance, idealities, and dark saturation currents. Finally, spectral response was measured using a Newport IQE-200 Automated EQE/IQE measurement system with a focused spot size of 1×2 mm^2.

Sample imaging was performed using scanning electron microscopy (SEM; Hitachi S-4000).

10.1.2.3 Results and Discussion

Following Au electrodeposition, samples were subjected to a MacEtch solution containing HF and $KMnO_4$ for 30 min. Figure 10.10 shows top- (panel a) and tilted-view (panel b) SEM images of post-MacEtch black GaAs prior to device fabrication. The non-vertical structures generated here resemble those found in Sample C in Chapter 8.

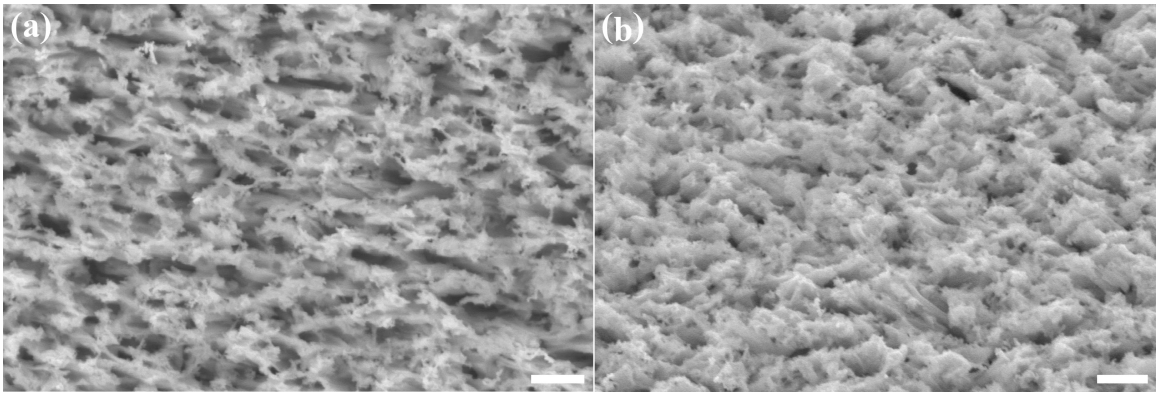

Figure 10.10: (a) Top-view and (b) tilted-view SEM images of nanostructured GaAs via MacEtch. Scale bars represent 500 nm.

It should be noted that the Au nanoparticles are not removed prior to TiO_2 and ITO deposition, because the Au etchant used here attacked the bottom contact. In future, work could be done to protect the contact during this step.

Figure 10.11 shows tilted-view (panel a) and cross-section view (panel b) SEM images of a post-MacEtch GaAs CSAH device after 20 nm TiO_2 and and 330 nm ITO deposition via ALD and sputtering, respectively. Instead of a continuous film, the ITO is shown to form a contiguous film of relatively large islands. The ITO topography results in a modification of the initial fabrication process flow for these devices. Namely, instead of creating the front contact by Au electrodeposition onto a thermally evaporating a 35 nm thick Au seed layer, a liftoff process is employed with

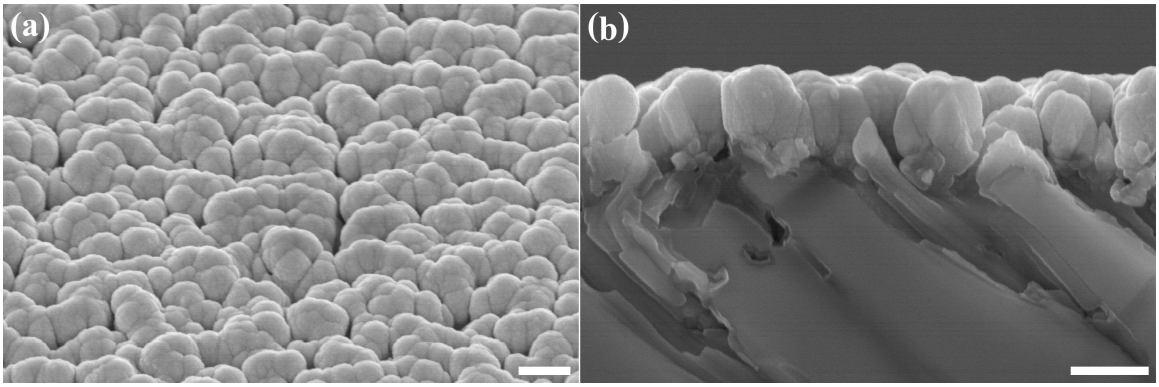

Figure 10.11: (a) Tilted-view and (b) cross-sectional view SEM images of nanostructured GaAs after 20 nm TiO_2 deposition via ALD, and 330 nm ITO deposition via sputtering. Scale bars represent 500 nm.

Table 10.3: Illuminated J-V cell performance for nanostructured GaAs CSAH device.

Sample	TiO2 Thickness (nm)	Cell Area (cm^2)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	η (%)
014-3	20	0.173	3.50	338.2	33.02	0.39

a 300 nm thick evaporated Au film to realize the grid.

Figure 10.12 shows an illuminated J-V curve for nanostructured GaAs CSAH photovoltaic device with TiO_2 thickness of 20 nm. The illuminated J-V performance of these devices is tabulated in Table 10.3. Cell performance is substantially reduced from the planar counterparts (Figure 10.5), particularly the photocurrent generated, as well as the fill factor and PCE. The nanostructured device also exhibits high series resistance and low shunt resistance.

Figure 10.13 shows the diode behavior (i.e., dark J-V curve) for a nanostructured GaAs CSAH photovoltaic device with TiO_2 thickness of 20 nm, with n and J_0 found to be $\sim$1.3 and $\sim 2 \times 10^{-6}$ A/cm^2. An example of determining these values can be found in Figure 10.7.

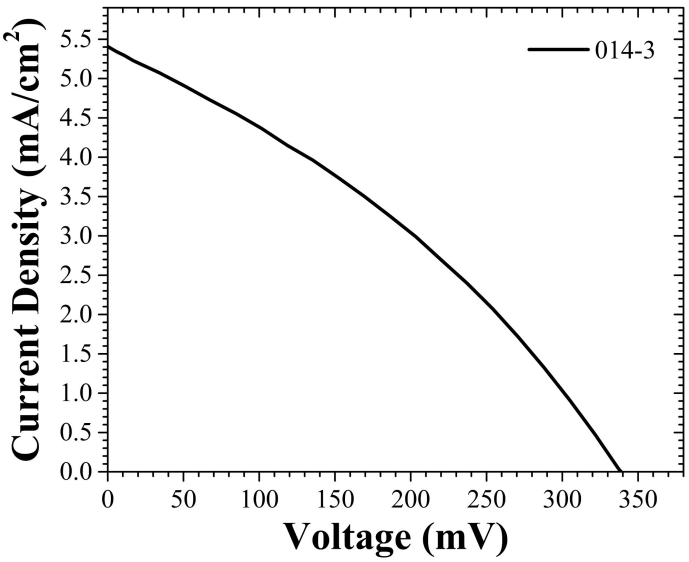

Figure 10.12: Illuminated J-V curve for nanostructured GaAs CSAH device with TiO_2 thickness of 20 nm.

Figure 10.14 shows the EQE (panel a), IQE (panel b), and R (panel c) for a nanostructured GaAs CSAH photovoltaic device with TiO_2 thickness of 20 nm. A substantial reduction in spectral response is exhibited compared to the corresponding planar device (Figure 10.8).

Initial proof-of-concept for this device structure has been demonstrated here; however, a great deal of work remains for this project. Assuming the planar fabrication process has been optimized (*vide supra*), the fabrication sequences and device structure can be improved towards generating an efficient nanostructured GaAs CSAH solar cell. Au deposition and MacEtch conditions should be optimized (see Chapter 8) to achieve a desired structure (e.g., vertical nanowires). Emphasis should be placed on tuning the ITO sputtering conditions, or post-deposition processing steps, to planarize the surface. This would simplify the front contact fabrication, and open pathways to alternative processing techniques (e.g., electrodeposition). Finally, the nanostructured GaAs CSAH solar cell could be exfoliated from the substrate to create a flexible device.

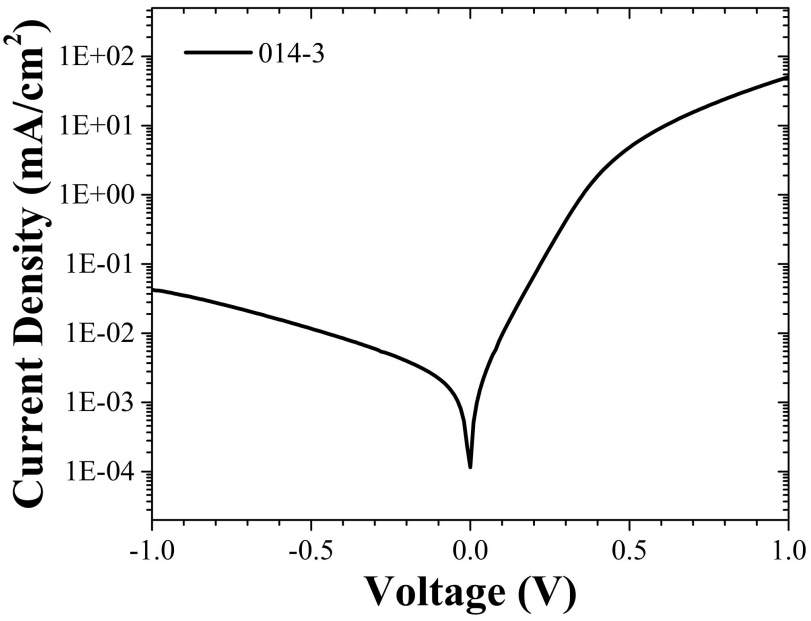

Figure 10.13: Dark J-V curve for nanostructured GaAs CSAH device with TiO_2 thickness of 20 nm.

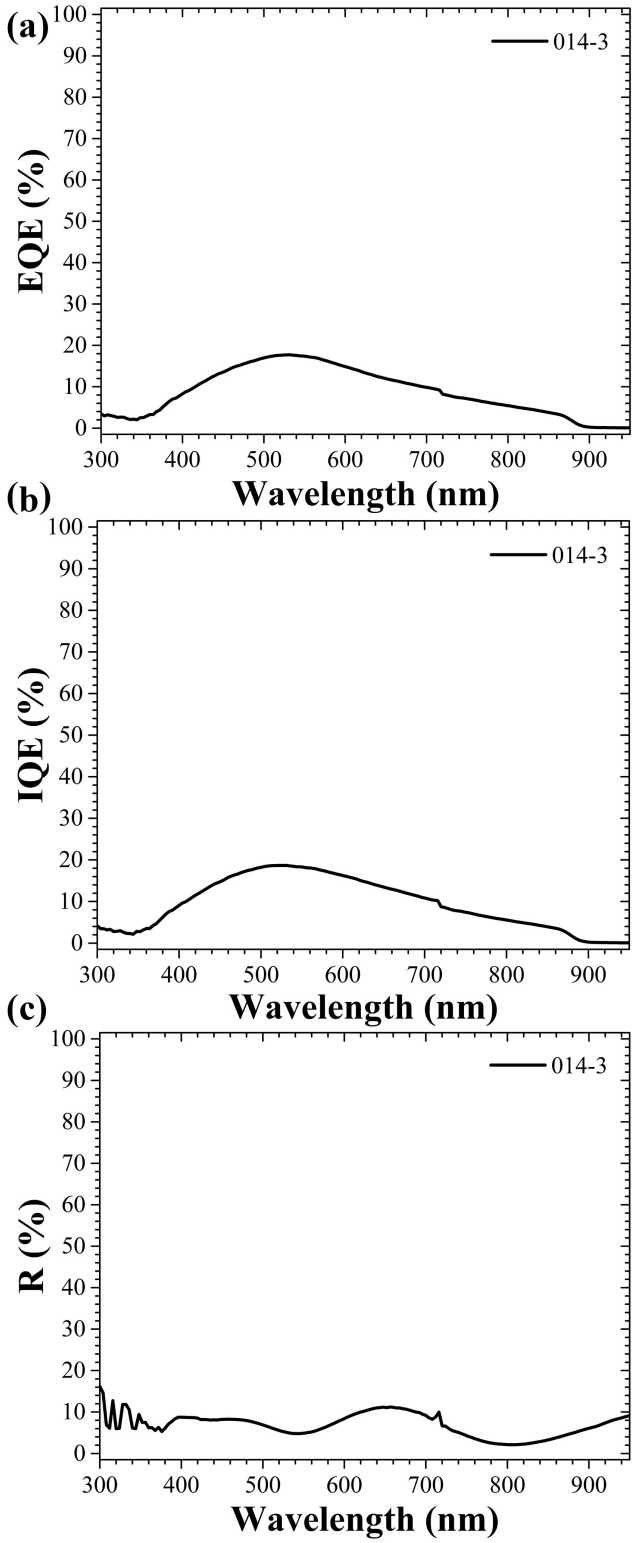

Figure 10.14: (a) External quantum efficiency (EQE), (b) internal quantum efficiency (IQE), and (c) reflectance (R) data for nanostructured GaAs CSAH device with TiO_2 thickness of 20 nm.

10.2 Lithography-Free Black AlGaAs

10.2.1 Motivation and Introduction

Chapter 6 detailed the development of MacEtch conditions for relatively high Al fraction (i.e., 55, 60, and 70% Al) AlGaAs. Chapter 8 focused on combining MacEtch and electrodeposition of Au nanoparticles on semi-insulating GaAs substrates to fabrication black GaAs. The project discussed here aims to combine these two studies, whereby electrodeposition of Au nanoparticles on low Al fraction (i.e., 10% Al) AlGaAs serves as a wet-etch mask to generate black AlGaAs. Ideally, this simple, cost-effective, and high-throughput process could be used to generate textured surfaces to serve as back surface reflectors for III-V photovoltaics [199].

10.2.2 Experimental Details

All AlGaAs samples were grown on GaAs(100) substrates using a 3 × 2 inch Aixtron close-couple showerhead metal-organic chemical vapor deposition (MOCVD) reactor. A 1 μm-thick AlGaAs film was grown with a composition of 10% Al (i.e., $Al_{0.10}Ga_{0.90}As$) and doping concentrations of $p = 4 \times 10^{19}$ cm^{-3}.

Sample preparation and etching conditions can be found in Table 10.4. All wafers were cleaned with standard solvents prior to native oxide removal was performed using

Table 10.4: Overview of sample preparation and etching conditions for black AlGaAs etching trials.

Electrodeposition			**MacEtch**				**Produced Black AlGaAs?**
Time (*s*)	**Current Density** (mA/cm^2)	**Solution Temp.** (°C)	**Time** (min)	**HF Conc.** (mol/L)	**$KMnO_4$ Conc.** (mol/L)	**Solution Temp.** (°C)	
15	0.5	60	15	14.072	0.011	Room Temp.	No
10	0.1		30				Yes
10			60				Yes

dilute (1:1) ammonium hydroxide (NH_4OH). Au was deposited via electrodeposition using sulfite gold plating solution (Transene TSG-250) at 60 °C. Several deposition conditions were attempted, including current densities of 0.1 and 0.5 mA/cm^2, and deposition durations of 10 and 15 s.

All etching trials were performed at room-temperature using a solution containing 14.072 mol/L hydrofluoric acid (HF) and 0.011 mol/L potassium permanganate ($KMnO_4$). Sample imaging was performed using scanning electron microscopy (SEM; Hitachi S-4000).

10.2.3 Results and Discussion

Figure 10.15 shows top-view SEM images (low and high-magnification in panels a and b, respectively) of post-etch $Al_{0.10}Ga_{0.90}As$ that was subjected to 15 s Au electrodeposition at a constant current density of 0.5 mA/cm^2. Under these conditions, the Au electrodeposition rate is sufficiently high to yield a nearly continuous film (thickness ∼200 nm), which does not result in nanostructured black AlGaAs after 15 min of etching.

Next, the electrodeposition conditions are reduced in the hopes of yielding a discontinuous Au film. A constant current density of 0.1 mA/cm^2 for a duration of 10 s is employed. Figure 10.16 shows top-, tilted-, and cross-sectional-view SEM

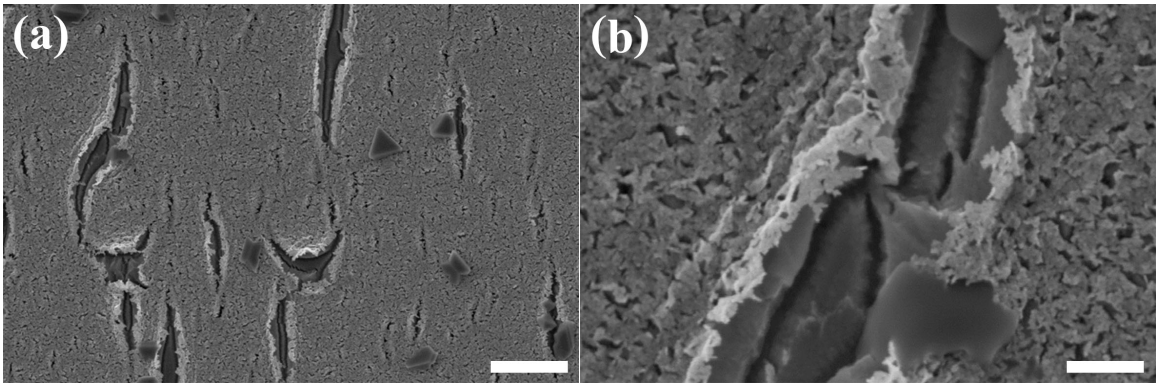

Figure 10.15: Top-view SEM images of post-etch $Al_{0.10}Ga_{0.90}As$ with $p = 4 \times 10^{19}$ cm^{-3}, after 15 s Au electrodeposition at 0.5 mA/cm^2. Scale bars represent (a) 3 μ and (b) 500 nm.

(left-, middle-, and right-columns, respectively) for samples etched for (panels a-c) 30 min and (panels d-f) 60 min. Under these conditions, the discontinuous Au film agglomerates during etching, which serves as a patterned mask for the underlying AlGaAs. Post-MacEtch micro- and nano-structure heights measure ∼500 nm after 30 mins (i.e., a vertical etch rate of ∼16.7 nm/min), and ∼900 nm after 60 min (i.e., 15 nm/min). The slight discrepancy in etch rates could be the result of the 1 μm-thick film being nearly etched completely through after 60 min of etching.

Completion of this work would be useful to establish this process as a viable path towards black AlGaAs. While the initial proof-of-concept and feasibility study has been completed here, additional process development and structural characterization is necessary before this can be applied to III-V photovoltaics.

First, an exploration of the catalytic influence (if any) is needed. Chapter 6 demonstrated AlGaAs MacEtch in a solution containing citric acid and hydrogen peroxide; however, that was for relatively high Al fraction AlGaAs, and a key finding was that the influence of conventional wet-chemical etching increases as the ternary composition becomes more GaAs-like. Therefore, low Al fraction (e.g., 10-30% Al) AlGaAs that is typically employed within III-V photovoltaics is expected to be dominated by traditional, non-catalytic, wet-etching. Instead, the solution used here (i.e., HF and H_2O_2) is commonly used for GaAs MacEtch (see Chapter 8). Cr does not have sufficient reduction potential to inject holes into the valance band of $Al_xGa_{1-x}As$ for any value of x [43], thus can be used to determine if the etching observed here is catalytic in nature. Moreover, if the etching is non-catalytic, or if the catalytic influence is minimal, Cr electrodeposition would serve as a cost-reduction approach to strengthen this process.

Next, etch repeatability and process reproducibility is essential for this project. The process outlined here is unlikely to repeatedly produce identical structures due to inherent fluctuations in electrodeposition (e.g., sample size and contact strength) and

etching (e.g., relative concentration of solution constituents) conditions. Therefore, minimizing these fluctuations is key to establishing a reproducible nanofabrication process. Then, the process should be repeated to determine appropriate uncertainty (i.e., a range of structures expected from following the process).

Finally, UV-Vis spectrophotometry should be performed to investigate the solar-weighted reflectance associated with structures generated using the established process. Then, back surface reflectors can be fabricated on III-V photovoltaics, and device performance can be evaluated.

10.3 Au-Catalyzed GaSb MacEtch

10.3.1 Motivation and Introduction

Although GaP [40] and GaAs (see Chapter 8) MacEtch have both been demonstrated previously (using solutions containing HF and H_2O_2, and HF and $KMnO_4$, respectively), no semiconductor containing antimony has been MacEtched. The goal for this

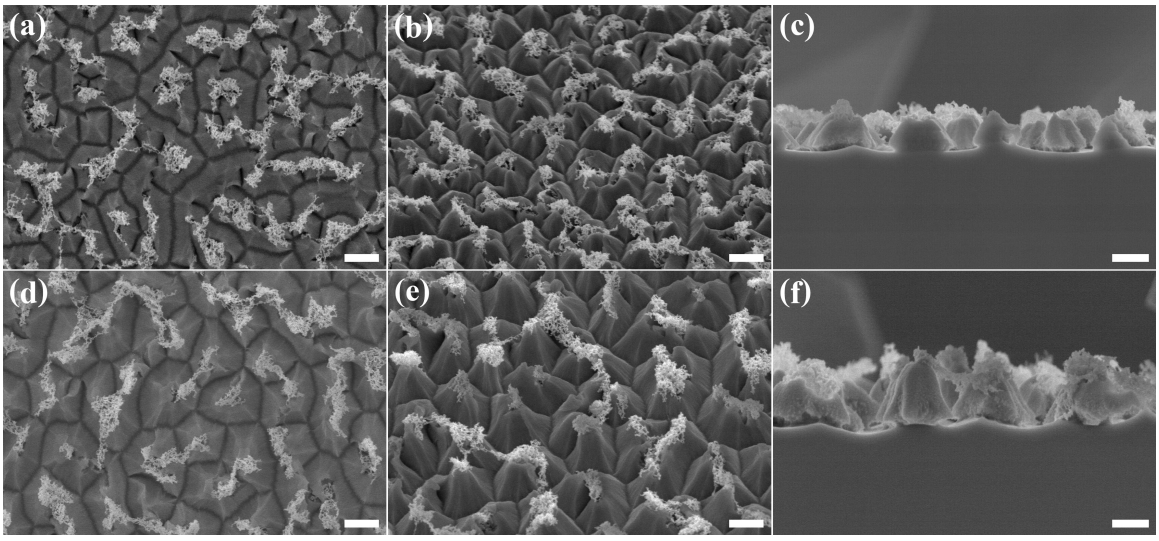

Figure 10.16: (Left column) Top-view, (middle column) tilted-view, and (right column) cross-sectional view SEM images of post-etch $Al_{0.10}Ga_{0.90}As$ with $p = 4 \times 10^{19}$ cm^{-3}. Au electrodeposition for 10 s at 0.1 mA/cm^2. MacEtch durations include (a)-(c) 30 min and (d)-(f) 60 min, which yield structures with height 500 nm and 900 nm, respectively. Scale bars represent (left and middle columns) 1 μ and (right column) 500 nm.

project is to establish MacEtch conditions for the binary III-V semiconductor, GaSb.

10.3.2 Experimental Details

A n-type GaSb(100) wafer (WaferTech) was used for this study. Native oxide removal was performed using dilute (1:1) hydrochloric acid (HCl), followed by degrease with standard solvents. Photolithography was used to pattern the samples; a positive photoresist (Shipley 1813) was spin-coated, followed by a 100 °C soft-bake. Exposure and development were performed using a g-line stepper (GCA 6300) and CD-26 (Microposit), respectively. A 35 nm thick Au film was deposited by thermal evaporation (Lesker PVD 75 Thermal Evaporator) at a rate of ∼1 Å/s, and liftoff was performed in a bath of N-Methyl-2-pyrrolidone (NMP). The size of each metal-patterned array was ∼2.5 × 2.5 mm^2, and they consisted of a mesh-shaped Au grid of ∼2 μm width separated by ∼2 × 2 μm^2 windows (or "off-metal" regions). An example of this pattern is shown in the top-view SEM images in Figure 10.17.

All MacEtch experiments were performed at room-temperature using a common solution containing 14.072 mol/L hydrofluoric acid (HF) and 0.011 mol/L potassium permanganate ($KMnO_4$). Sample imaging was performed using scanning electron microscopy (SEM; Hitachi S-4000).

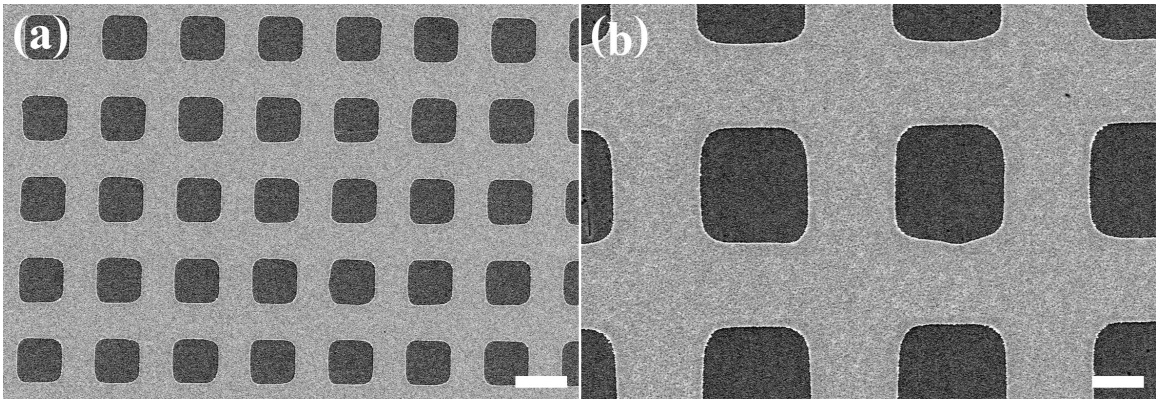

Figure 10.17: Top-view SEM images of post-MacEtch GaSb samples. Scale bars represent (a) 5 μm and (b) 2 μm.

10.3.3 Results and Discussion

Figure 10.17 shows top-view SEM images (low and high-magnification in panels a and b, respectively) of a pre-MacEtch sample.

Figure 10.18 shows top-view (panels a-b) and tilted-view (panels c-d) SEM images of post-MacEtch GaSb samples that were subjected to a solution consisting of 14.072 mol/L HF and 0.011 mol/L $KMnO_4$ for 30 min. The Au catalyst does not sink uniformly into the substrate, as can been seen in Figure 10.18a,b. Instead, the Au along the periphery of the off-metal regions begins to sink, whereas the street regions lag behind. This indicates the MacEtch process observed here is limited by mass transport [29]. Several approaches could solve this issue; either optimizing the relative concentration of solution constituents, and/or reducing the width of the interfaced regions. Both scenarios ensure the rates of oxidation and mass transport (i.e., solution access to, and dissolution of, catalytically oxidized material) are similar, such that the metal sinks uniformly into the substrate [29].

A continuation of this work would be useful towards establishing a solution-based GaSb nanofabrication process that is also highly anisotropic. While proof-of-concept has been demonstrated here, a more robust parameter space exploration of the MacEtch conditions is essential. The work presented here demonstrates that Au-patterned GaSb will undergo MacEtch in a solution containing HF and $KMnO_4$. However, etch rates should be established through a modification of the MacEtch conditions (e.g., relative concentration of the solution constituents), as well as dependencies on catalyst dimension.

Material characterization and device fabrication would also be beneficial. This includes analyzing the electrical properties of the post-MacEtch GaAs samples, to better understand how influential the MacEtch process is device performance. This would be particularly useful to evaluate the affect catalytically generated oxidation has on electrical devices (e.g., tunnel diodes). Additional three-dimensional devices

should be realized through this approach, including infrared photodetectors.

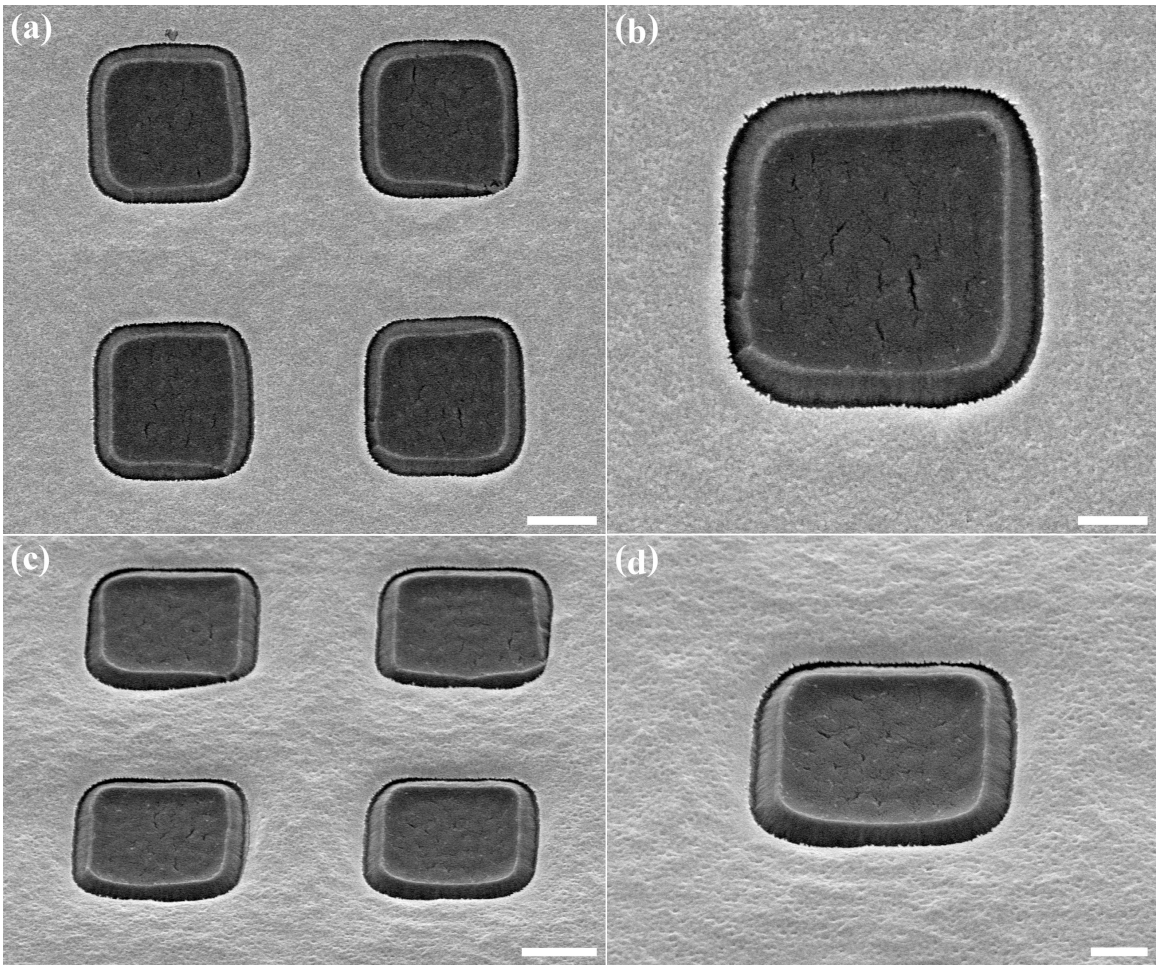

Figure 10.18: (a)-(b) Top-view and (c)-(d) tilted-view SEM images of post-MacEtch GaSb. Scale bars represent (left column) 2 μm and (right column) 1 μm.

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