8-13-2019

A Study on Copper-Gate Integration with Titanium Interface Layers for IGZO TFTs

Harithshanmaa Sethupathi
hxs3991@rit.edu

A Study on Copper-Gate Integration with Titanium Interface Layers for IGZO TFTs

Harithshanmaa Sethupathi

A Study on Copper-Gate Integration with Titanium Interface Layers for IGZO TFTs

Harithshanmaa Sethupathi

August 13, 2019

A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

R·I·T | Kate Gleason
College of ENGINEERING

Department of Electrical and Microelectronic Engineering

A Study on Copper-Gate Integration with Titanium Interface Layers for IGZO TFTs

Harithshanmaa Sethupathi

Committee Approval:

Dr. Karl Hirschman *Advisor* Date
Professor

Dr. Dale Ewbank Date
Senior Lecturer

Dr. Ivan Puchades Date
Assistant Professor

Certified By:

Dr. Karl Hirschman *Advisor* Date
Professor

Dr. Robert Pearson Date
Microelectronic Engineering Program Director

Dr. Sohail Dianat *Electrical and Microelectronics Engineering Department Head* Date

Acknowledgments

To the greatest teachers of my life- from walking, to talking and advice in making life's biggest decisions, for giving me the freedom and for encouraging me, Thank you amma and appa. You will always be my heroes.

I would not have been able to do this without Dr.Karl Hirschman, a fatherly figure away from home.He was there to always make me feel like home, who supported me and guided me throughout both professionally and personally. I'm forever grateful for what you have given me. Thank you Dr.Hirschman. You will always be my go to person.

Dr.Robert Pearson- I wouldn't have been able to do what I wanted to without you. You welcomed me into the department and made it possible for me to learn what I have wanted to for years. Thank you.

Dr.Fuller-My inspiration to get into this department. Having had the opportunity to be in his class was a blessing. I Will always be a proud RIT Microelectronics graduate because of Dr.Fuller. Thank you.

I would like to thank all the technicians at SMFL, Bruce, Rich, John and Patricia and Sean for not giving up on us and helping us in the cleanroom. Working in the cleanroom wouldn't have been fun if it wasn't for any of them. They were a great support to me.

I would like to thank Team Eagle for supporting the work and me throughout. It was a wonderful three years of grad school.I would especially like to thank Glenn and Kabir for their constant support and motivation.

I would like to thank my friends Pratheik, Lilian, Patty, Udita and Viraj and Sanjna for always pushing me to do better and making learning fun. My friends Divya, Mythili, Arun, Sandesh, Abhilash for constantly being by my side and never giving up on me.

Lastly I would like to thank my cousins for lovig me unconditionally.

To Appa and Amma for being my biggest inspiration and support

Abstract

The continuous demand for ultra-high resolution and improved video performance on increasingly larger active-matrix displays has advanced the research field of thin film transistors (TFTs) materials, processes and devices. Performance improvements demonstrated by amorphous Indium-Gallium-Zinc-Oxide (IGZO) TFTs has enabled a commercialized backplane technology adopted for AM-OLED displays, providing advantages in device performance and uniformity at a much lower cost than Low Temperature Poly-crystalline Silicon (LTPS). However as the display size gets larger and the pixel density increases, charge transfer from the column driver to the pixel through the addressed row TFT within the required time interval becomes increasingly difficult. As the pixel size shrinks and the panel size grows, interconnects that must be scaled down in cross-section have to transport charge over longer distances. In addition, as the numbers of rows increase in a display, the time allowed for charge transfer decreases to maintain a high image refresh frequency. These challenges must be addressed by lower interconnect delay, thus the advantage in transitioning to Cu for long interconnect rows and columns. The gate electrodes are usually implemented as an appendage of the row interconnect, thus Cu-gate TFTs would avoid added process complexity while supporting high-speed interconnects and low production costs. The following work presents a study on Cu-gate integration and potential channel contamination on bottom-gate IGZO TFTs with a newly established baseline process. Cu was used in place of Mo as the gate electrode, with an underlying Ti layer to promote adhesion to the oxidized silicon substrate. The experimental design input factors included the option of a Ti capping layer on the Cu-gate, and the anneal conditions of the gate dielectric (PECVD SiO_2) prior to IGZO sputtering. Distinct differences in physical and electrical responses over all treatment combinations were identified. Experimental results demonstrated that while the Ti capping layer promoted adhesion to the gate dielectric, it served as a source of contamination on pre-annealed

treatments causing pronounced electrical characteristic shifting and dielectric failure. The anneal process was found to promote adhesion between the Cu-gate and the gate oxide without the use of Ti capping layer, as well as reduce oxide charge levels. Copper contamination did not appear to be an issue in treatment conditions at or below 400^oC, however pitting of the gate electrode occurred at anneal temperature above 400^oC, as well as electrical results that suggest evidence of Cu contamination. Visual observations and electrical characteristics are presented with a detailed discussion on comparisons between treatment combinations, with reference to the baseline IGZO devices.

Contents

List of Figures

List of Tables

List of Symbols

Term	Description	Units/Value
I_D	Drain current	A
m^*	Carrier effective mass	kg
N_c	Effective density of states in the conduction band	cm^{-3}
S	Subthreshold swing	V/dec
V_{DS}	Drain–Source voltage	V
V_{eff}	Effective reverse bias voltage	V
V_G	Gate voltage	V
μ_n, μ_p	Mobility of electrons and holes respectively	cm/V·s

Chapter 1

INTRODUCTION

1.1 OVERVIEW

Display technology has seen tremendous change over the past two decades from segment type display to active matrix displays. Active matrix liquid crystal displays (AMLCD) are the major devices used for flat panel displays in recent times. Studies state that the display market is expected to grow from 137.7 billion in 2019 to 167.7 billion by 2024 at a compound annual growth rate of 4 % from 2019 to 2024 [16]. The increasing demand for displays of higher resolution, faster response rate and better quality has directed this industry to move towards breakthrough innovations and growth in the field such as bendable and rollable displays for unbreakable rugged displays. This demand for better performance of AMLCDs and Active matrix Organic Light Emitting Diode (AMOLED) displays has advanced research in the field of thin film transistors (TFTs) and materials. The increasing demand for large displays with better resolution and higher refresh rates (240Hz for UHDs), drives the need to find alternative materials for TFTs as amorphous silicon (a-Si) has low mobility (μ $<$ 1-cm^2/(Vs)) which restricts high frequency response for back planes [17].

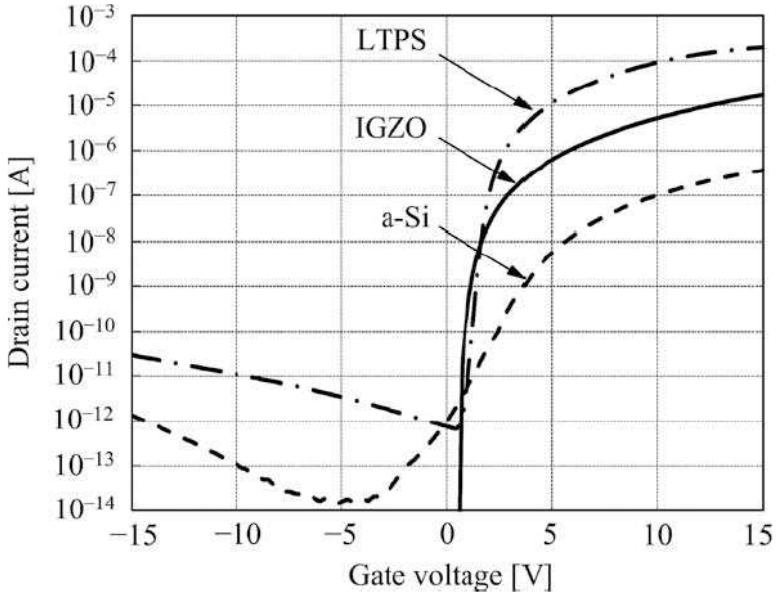


Figure 1.1: Comparison of IV characteristics of TFTs with different active channel materials [1]

Two materials that have been promising as a replacement for a-Si are amorphous oxide semiconductor (AOS) materials and Low-Temperature Poly-crystalline Silicon (LTPS) due to high process compatibility and low process temperature, as these TFTs are fabricated on glass substrates which have a thermal tolerance of around 600 ^{o}C. Large area uniformity is an important factor to be considered for fabrication of TFTs as FPD panel sizes have advanced to Gen10.5 with dimensions are 3370 $\times$ 2940mm which is 180% larger than Gen 8.5. From Fig 1.2 it is observed that manufacturing capacity for Gen 10+ FPDs have increased over the years to meet the demands.[2]

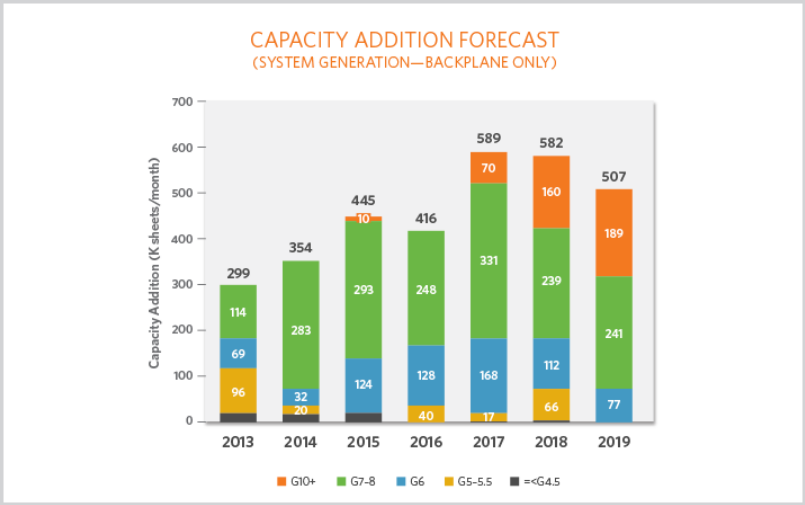


Figure 1.2: FPD manufacturers are adding significant production capacity for Gen10+ FPDs, represented by the orange bar segments. The total production capacity added each year (201819 estimated), in thousands of sheets per month is represented by each bar. [2]

The shipment of 65+ inch displays has increased from 8 million in 2016 to about an expected 30 million in 2020 [2]. Electrical uniformity over such large areas can be challenging. Amorphous Indium Gallium Zinc Oxide (IGZO) has proven to be the most promising AOS, already commercialized for large 8K OLED displays. This has been preferred over its counterpart due to its large area uniformity owing to amorphous nature, large mobility, higher aperture ratio, low leakage current, high on-off ratio for lower power consumption, low cost of fabrication and ease of adoption as a replacement for a-Si.

The growth of display market is expected to grow by double digits in the next five years for applications such as smartphones and other larger display devices. With the growth being doubled, the cost of these are expected to be low which makes it critical for mass production. This can be done by tighter process specifications and adoption of AOS such as IGZO for FPD backplanes.

1.2 RECENT DEVELOPMENT IN BACKPLANE TECHNOLOGY

AMLCDs received lot of attention in the initial transition of displays from CRTs to FPDs. AMOLEDs are now emerging as an alternative technology for display devices. AMOLEDs offer higher brightness due to their ability to eliminate backlight by integrating the OLED with the TFT pixel electrode circuit. Their ease of manufacturing, higher efficiency and wider viewing angle makes it advantageous over the AMLCD displays. The technological and material requirements for both the above-mentioned technologies are tabulated below.

Applications	**Technological Requirements on TFT Backplane**	**Enabling Material Properties**
AM-LCD	Large area	Uniform amorphous phase
	High aperture ratio	Visible light transparency/High mobility
	Fast response	High mobility
AM-OLED	Good current driving capability	High mobility
	Good stability	Low defect and weak bonding density

Table 1: Challenges and material requirements of next- generation TFT backplanes [6]

Conventional AM-LCDs are driven by a-Si TFTs, but due to their low mobility they are not practical for use in advanced displays. The material property requirement of uniform amorphous phase, higher mobility and visible light transparency paves way for the adoption of IGZO TFTs in the active matrix FPD industry. IGZO TFT has received significant attention in a variety of applications such as televisions,

mobile phones, flexible displays, etc. owing to its material properties. Because of its lower power consumption, as low as a tenth that of conventional a-Si screens, IGZO devices contribute to a longer battery life [18]. Their touch sensitivity is very high, and this promotes detection of even the faintest signals. This makes possible ultra-high sensitive displays that enables natural handwriting input like that on paper [18]. Due to its highly sensitive sensors that can transform X-rays into high-resolution images, IGZO imaging arrays are found in medical device application. These properties of a-IGZO add to its advantages over that of low-temperature polycrystalline silicon (LTPS) thin film transistors. LTPS has advantages over a-IGZO in some segments due to higher mobility that can easily exceed 100 $cm^2/(Vs)$ which can provide better resolution over smaller displays, however these devices exhibit poor electrical uniformity over larger substrates due to grain boundaries.

1.3 STRUCTURE OF DISPLAY DEVICES

The purpose of this section is to understand the structure of the display device and the role of TFT in the backplane for a display device. Pixel addressing in both the passive matrix and an active matrix structure is discussed in brief. Hence, this gives us a vivid picture of why an active matrix structure is better for higher resolution display devices.

1.3.1 LIQUID CRYSTAL DISPLAY

A liquid crystal display (LCD) is a device that utilizes the electro-optical characteristics of a liquid crystal which is matter having properties of both a liquid and crystal; to convert an electric stimulus into a visual signal [4]. These liquid crystals can be manipulated by applying appropriate voltage through the thin film transistor (TFT) to the common electrode to either block or transmit light through it to a variable degree. The color filter in the front of each sub-pixel allows only light of a certain

wavelength to pass through it to emit certain color. The unpolarized light emitted by backlight light emitting diode (LED) is passed through a bottom polarizer which allows only light of vertical wavelength to pass through it. The polarized light is then passed through the liquid crystal and passed through another polarizer which transmits only light of horizontal wavelength. The function of the polarizer is to improve color and definition without which it will not be possible to read the display. The entire structure of an LCD display is pictorially shown below in Fig 1.3.

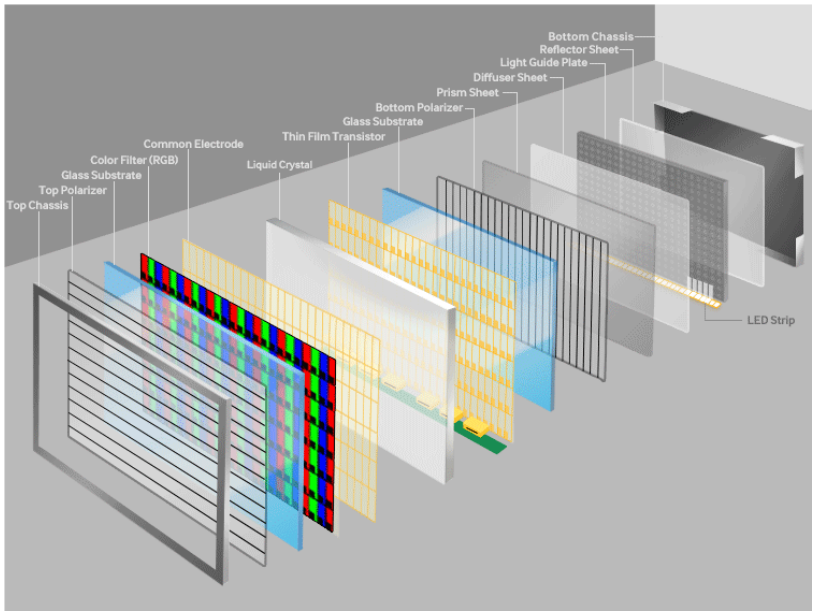


Figure 1.3: Structure of Liquid crystal display [3]

Liquid crystal display does not generate light of their own and hence a strip of LEDs is used for backlight illumination which is shown in the figure above. The adoption of LED for this purpose allows for thinner panels, brighter display, better contrast and low power consumption. Its significance is observed in good color reproduction and broad color gamut.

Addressing is the process of conversion of information to be displayed into sequential pulses to switch on individual pixels. The different methods of addressing pixels in a display device are direct addressing, passive matrix addressing and active

matrix addressing. In a passive matrix display, one electrode is patterned into M columns and the other electrode is patterned into N rows for addressing a matrix of M × N pixels. Bonding pads are fabricated at each end of the rows and column bus lines for applying pulses of voltage to be sent. The contrast of the pixel in a passive matrix addressing reduces with larger number of rows. With larger displays, the power consumption and RC delay increases and becomes unmanageable. In an active matrix structure there is better control of voltage to the pixel and the gray level by exploiting the use of a switching device and a capacitor. The switching device is this case is implemented through thin film transistors whose channel layer is a thin film deposited by plasma enhanced chemical vapor deposition (PECVD) on a non- conducting substrate like glass. Hence with the implementation of AMLCDs, high contrast and fast LC mixture is obtained with minimized crosstalk. This can be used for high information content and graphical applications. Comparison of the pixel addressing using a passive matrix and an active matrix displays is shown by its circuitry in the Fig 1.4a and b.

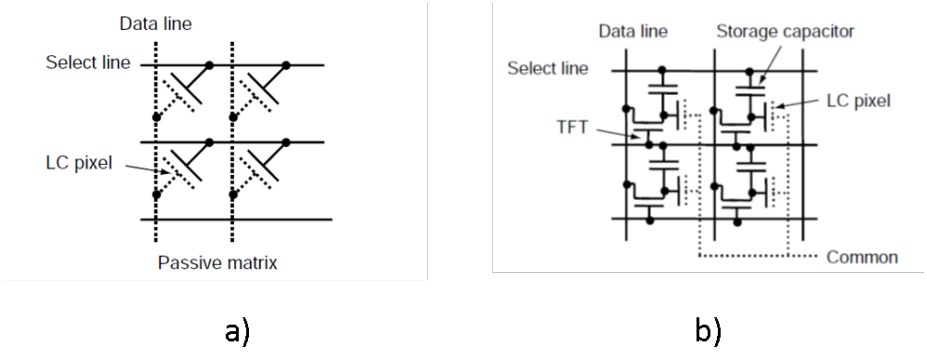


Figure 1.4: Circuit diagram for pixel addressing in a) passive matrix LCD b) active matrix LCD [4]

1.3.2 THIN FILM TRANSISTOR

TFTs are like a conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) except in structure where the devices are fabricated on an insulating

substrate such as glass. The structure of TFT consists of three electrodes, the gate, source and drain. The devices do not have a conducting base substrate and hence they have negligible body bias. The channel between the drain and source is formed by a thin layer of active semiconductor material deposited by PECVD as it is difficult to grow epitaxial silicon on glass substrate. The gate metal is deposited on the glass substrate and a dielectric material is deposited on top of it to avoid contact between the gate and the channel material. The source and drain metal are deposited on top of the semiconductor material to make contact. The operation is like that of a MOSFET where a gate voltage controls the conduction in the channel region.

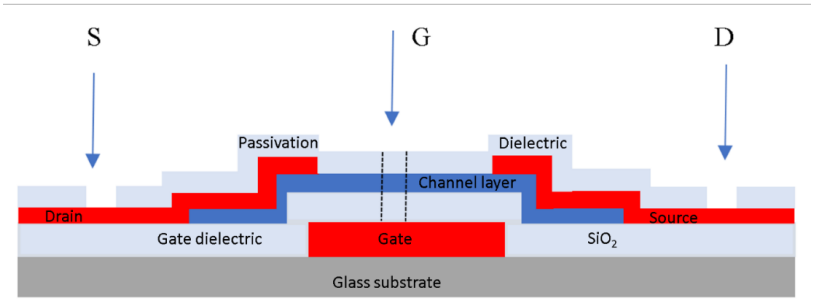


Figure 1.5: Cross section of a thin film transistor (staggered bottom gate structure)

1.3.3 AM-OLED DISPLAY

OLEDs are light emitting diodes whose luminescence is obtained from the organic stack of material that constitutes the structure of the device. The principle of working is that electroluminescence is an optical and electrical phenomenon where light is emitted by the organic material when electric current is passed through it or when it is subjected to strong electric field. The excited electrons emit energy in the form of photon light.

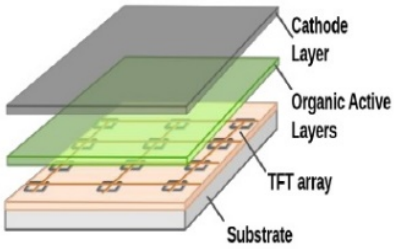


Figure 1.6: Structure of AM-OLED screen [5]

The device consists of a substrate, anode, cathode, emissive layer and a conductive layer. The anode is generally made up of a transparent electrode with indium titanium oxide (ITO) and the cathode is usually metals such as aluminum depending on the type of device. The organic layers between the anode and cathode are made up of several organic layers as seen in Fig 1.7.

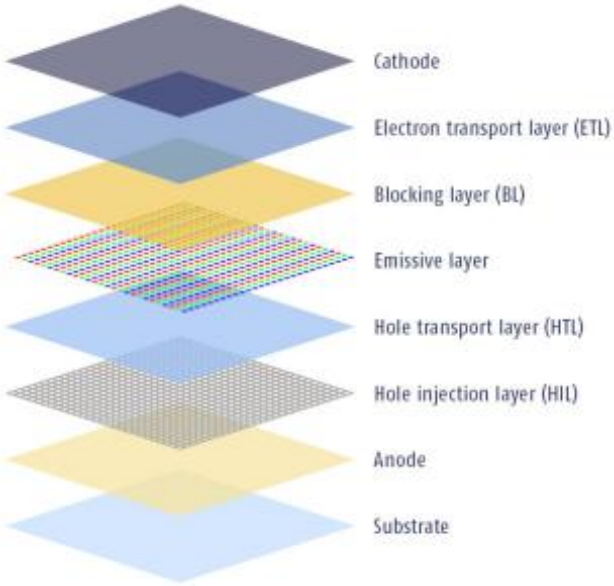


Figure 1.7: Structure of the OLED stack [5]

AM-OLEDs are preferred over the AMLCDs as OLED panels can be thin, light weight and their main significance being they do not require backlight. They can produce true-black contrast ratio. The AMOLED panel consists of fewer layers as seen in Fig than the AMLCD panels which contribute for the thinner and light weight

of the panels.

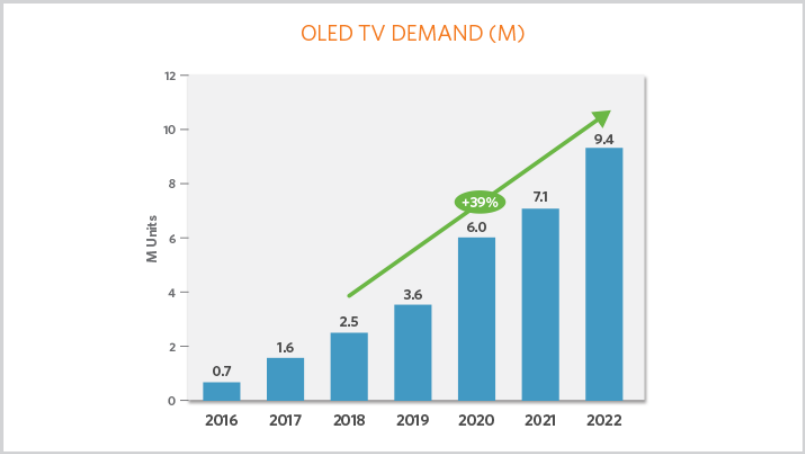


Figure 1.8: The graph represents steady growth in the shipment of OLED display panels each year with an expected 39% growth from 2018 to 2022 [2]

The growth of AMOLED panels in the industry has increased drastically with the shipment of these panels expected to be 39% increase from 2018 to 2022 which can be seen in Fig 1.8 [2].

1.4 MOTIVATION OF STUDY

There has been tremendous interest in thin film transistors with higher mobility and uniform performance over a large display. Amorphous silicon process has been well established as a TFT material in the field of display devices but there is increasing demand for higher resolution, reduced power, and high performance. These become impossible to be adapted for higher resolution displays. IGZO has proven to be a better replacement due to their high mobility of 10- 13 $cm^2/(V.s)^{-1}$ (10 times greater than that of a-Si), low off state leakage current and higher switch ratio of 10^9 which is 100 times greater than that of polysilicon. IGZO has also proven to be more reliable for large displays in comparison with LTPS owing to their amorphous structure. Even though LTPS offers higher mobility of 100 cm^2/Vs the additional recrystallization steps increase the cost of production and adds more complexity. One more problem

with Excimer laser annealing poly silicon is that it has high off- state gate leakage which are major factors to be considered. The ease of fabrication of IGZO adds to all the other advantages as they do not have grain boundary formation issues. IGZO with the high transparency in the visible region and broader bandgap of 3.05eV, opens a wide spectrum of applications such as transparent electronics and sensors. This has significant properties which make it a much better material for TFT than a-Si and LTPS for large panel displays.

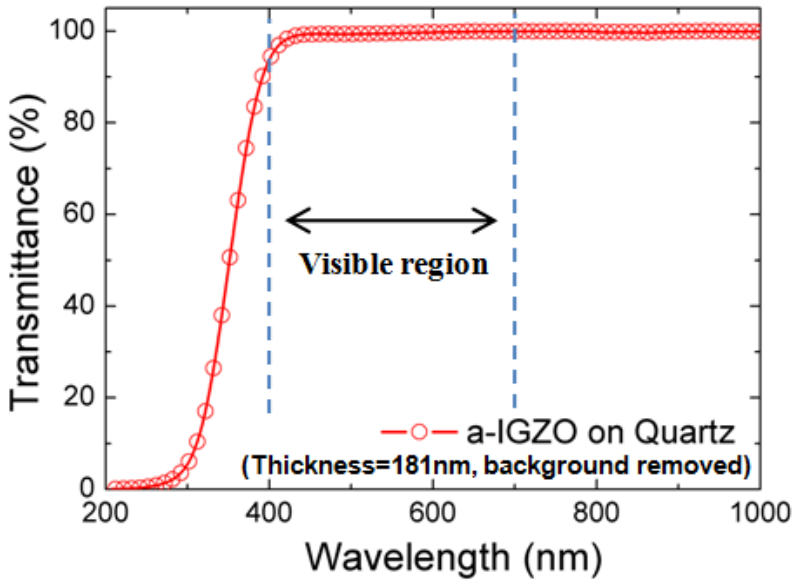


Figure 1.9: Transmittance of IGZO in the visible region of the spectrum

There are certain challenges to fabrication of IGZO TFTs on a large scale. From previous studies, it was observed that the main problem to manufacture these were their instabilities with thermal and bias stress. Shift in the threshold voltage under thermal and bias stress has been observed. This instigated further studies in the thermal instabilities and ways of improving the stability of the IGZO devices.

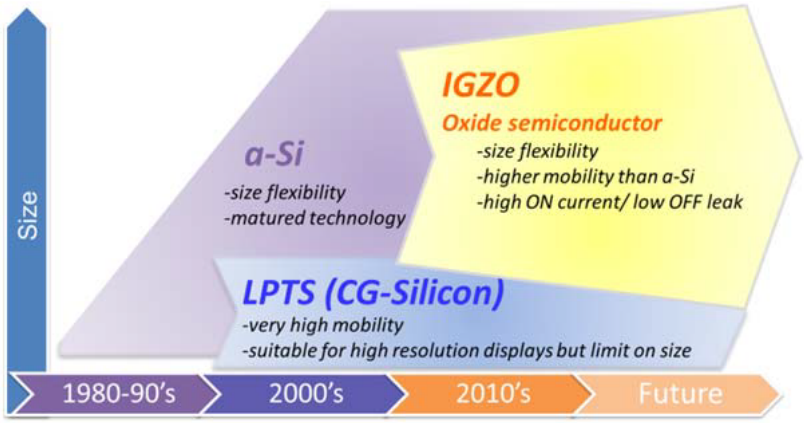


Figure 1.10: Comparison of different channel materials and their scalability along with their incorporation in the display industry [6]

The instability and non-uniformity issues could be compensated in LCDs by using compensation circuit. But with the adoption of OLEDs which require high mobility which emit light by electrical current injection, the a-Si TFTs could not support high current devices. And hence it was necessary to move to a material with high mobility as even the slightest variation in Vt of the TFT would cause significant variation in brightness of the pixels. The luminance would vary by 16% for a +/- 1V change in threshold voltage [2]. AOS were adopted for this purpose and their advantages over a-Si had been mentioned in the previous sections. With increasing panel size and a higher frame rate of greater than 120Hz required for improving video quality and 3D capability, a few challenges need to be addressed. One of the major challenges is the lack of charging time to apply video data to each pixel. As the pixel density increases for large area displays, interconnects are scaled in x-direction. As the number of rows increases, the time for charge transfer decreases to maintain a high image refresh frequency. This can be addressed by either changing the driving architecture to increase the turn on time or by improving the charging capability. Improvements in the RC delay needs to be addressed while transitioning to higher definition panels. With Al/Mo as the gate or Source/ drain metal, this becomes difficult and hence a low resistance metal must be adopted for the gate line. Copper is known to have

higher bulk thermal and electrical conductivities and is a promising candidate as a replacement for Mo/Al as gate metal with appropriate process integration.

1.5 GOALS AND OBJECTIVES

The goal of this study is to investigate the influence of annealing conditions on copper diffusion with and without a titanium interface layer. The objectives are

1. Verify method for copper adhesion.

2. Design of experiment for investigation with treatments that promote a measurable electrical response to metallic contaminants (i.e. V_T shift, SS).

3. Measurement and interpretation of electrical characteristics.

4. Re-establish a baseline TFT process that produces consistent and reproducible electrical characteristics and good stability. [Ensures electrical interpretation is not influenced by process variation or instability which has been a recent problem]

1.6 DOCUMENT OUTLINE

Chapter 1 summarizes the recent developments in the display industry and the role of TFT in the structure of an active matrix display device. The different materials adapted for thin film transistors have been summarized and the advantages of a-IGZO over the other materials have been discussed briefly. Emphasis is given to motivation of this work and the goal and objectives of the study.

Chapter 2 is dedicated to the electronic and material properties of IGZO. The chemical structure of IGZO is discussed along with the conduction mechanism in the material. The motive behind this chapter is to understand the material and its behavior

with different treatments and processes of fabrication. This enhances designing experiments for the devices to study the devices.

Chapter 3 discusses the detailed fabrication process for IGZO TFTs. The different electrode configurations used for the study along with the various process parameters changed to enhance the TFT performance has been discussed along with the changes in its electrical characteristics. The change in the material properties of IGZO motivated designing experiments to re-establish a baseline process for the fabrication of the IGZO TFTs for display devices. The results obtained by varying different parameters such as IGZO thickness, passivation dielectric thickness and anneal conditions are discussed and a new baseline process will be adopted for further study.This chapter also discusses about the thermal stability of the bottom gate and double gate devices. The results of the thermal stability of the devices fabricated with the modified baseline process was compared with the results of the devices fabricated with the previously used baseline process. This was analyzed and discussed briefly.

Chapter 4 discusses the integration of copper as the bottom gate electrode. The motivation behind the incorporation of copper in the IGZO TFT is provided. Copper being a low resistance material is an obvious replacement for molybdenum to obtain low RC delay and faster transmission. But there are challenges to incorporating copper in the process and this is discussed in detail in this chapter. Various process variations such as gate stack, gate dielectric stack and anneal conditions are suggested and experimented to see an enhancement in performance. The experimental results with these variations are provided and compared with the baseline process with molybdenum as the bottom gate electrode.

Chapter 5 provides a summary of work done to incorporate copper as the bottom gate electrode. The process of re-establishing a baseline process and studying the thermal stability of the devices to be able to adopt copper as the gate electrode for IGZO TFTs.

Chapter 2

ELECTRONIC AND MATERIAL PROPERTIES OF IGZO

IGZO has proven to be a promising candidate for the active channel material of the TFT in FPDs. The role of TFT in AMLCD and AMOLED panels have been discussed. The major advantage of using IGZO for large panel displays as discussed previously is its low processing temperature and uniformity over a large area. In this chapter we will dive deep into the structure and characteristics of the material along with its conduction mechanism and TCAD model to better understand the relationship between the electrical characteristics and the material defect state model.

Amorphous oxide semiconductors have mobility higher than a-Si due to the ionic bonding of material. Also, they also have lower values for subthreshold swing (SS) which promotes better overall performance of the device. The lower value for SS and higher mobility are due to lower influence of trap states near the conduction band.

2.1 MATERIAL PROPERTIES OF IGZO

IGZO is an n-type amorphous oxide semiconductor. The amorphous nature of the material is due to the composition of the material. It is a ternary metal oxide with In_2O_3, Ga_2O_3 and ZnO in the ratio of 1:1:2, resulting in an elemental In:Ga:Zn:O ratio of 1:1:1:4.

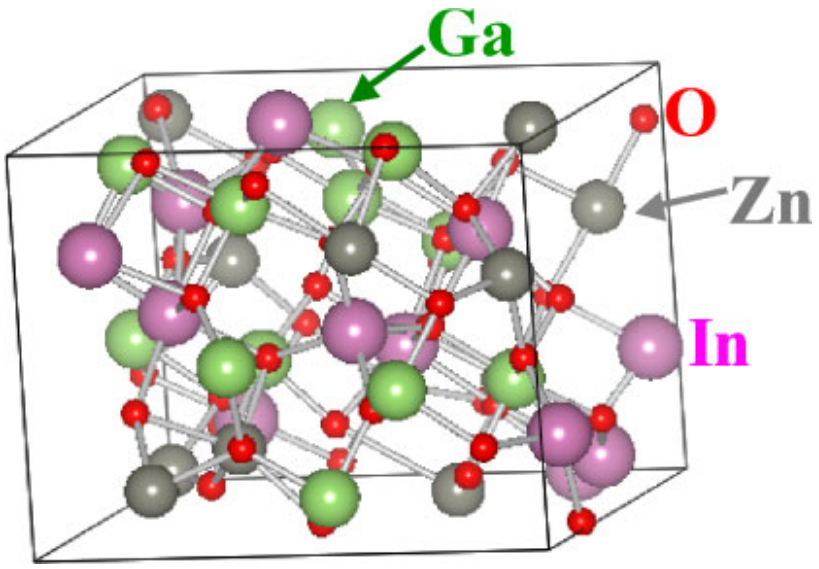


Figure 2.1: Molecular structure of a-IGZO [7]

Amorphous semiconductors are expected to exhibit deteriorated performance such as low mobility in comparison with the crystalline materials due to their strong scattering of the disordered structure. Conduction mechanism in both covalent and ionic amorphous semiconductor is studied.

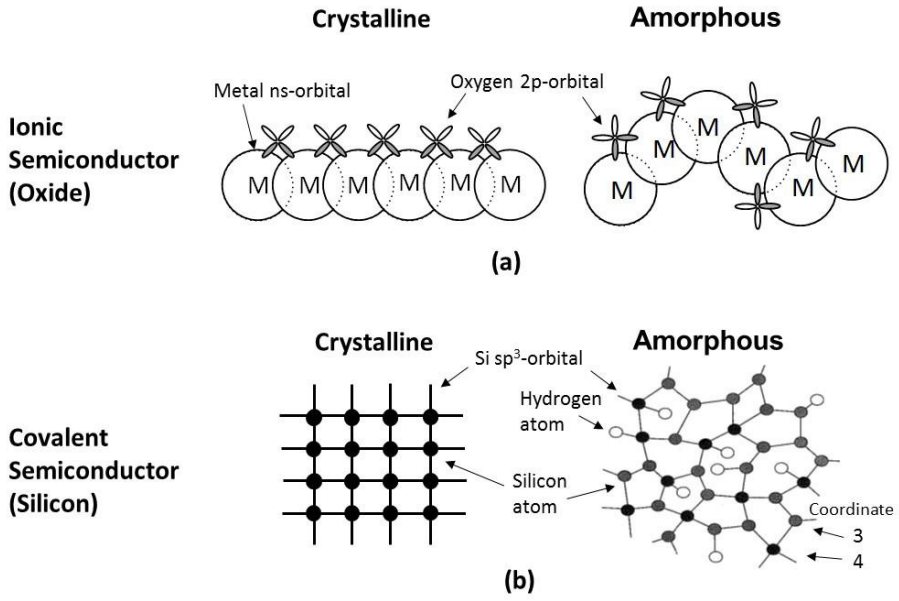


Figure 2.2: Conduction mechanism in ionic and covalent semiconductors in both their crystalline and amorphous phase [8]

Chemical bond in covalent semiconductor such as a-Si is made up of sp^3 orbitals which have strong spatial directivity. Conduction in a-Si is due to overlap of these highly directional sp^3 orbitals which are very sensitive to bond angle variation unlike a crystalline material. The material possess short range order and follows carrier hopping conduction mechanism where the electron is captured in a localized state and re-emitted into extended states significantly affecting carrier mobility. Unlike a-Si (covalent bonding), conduction in an ionic semiconductor material such as a-IGZO is through band conduction [8]. The valence band is formed by filled p-orbitals of oxygen anion and the conduction band is formed by empty s-orbitals of the heavy metal cation. Charge transfer between these results in Madelung potential which is shown in Fig 2.3. The distance between these bands (bandgap) is 3.2 eV with RF sputtering technique. The wide band gap in the structure attributes to the optical transparency of the material[10].

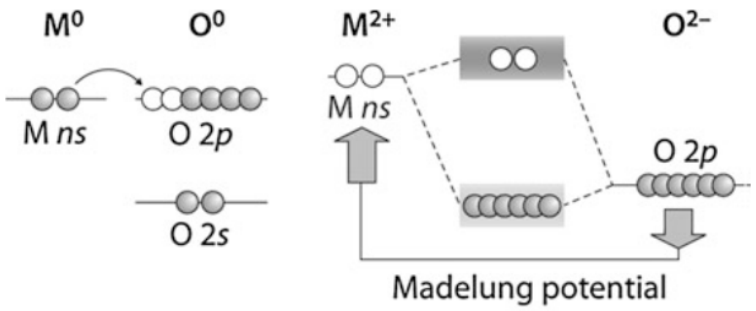


Figure 2.3: Madelung potential resulted from the transfer of electrons from the valence band to the conduction band of amorphous oxide material (a-IGZO)[9][10]

The s-orbitals of the metal cations are spherically symmetric. A significant overlap with the s orbitals of neighbouring metal cations provides a pathway for electron transport. The spatial spread is determined by the principle quantum number, n, of the metal cation. The larger values for n, such as in the case of post transition metals, causes significant overlap between the metal cations which reduces the effective masses of the electron. The lower effective electron mass leads to higher mobility in the

material. The non-bonded metal cation (i.e. oxygen vacancy defect) produces a shallow donor level which contributes to the free electron concentration. The oxygen vacancy formation in IGZO has not been conclusive as there are different theories proposed.

The dependence of Hall mobility on the compositional structure of the material is discussed in detail by several groups. A study by Kamiya et-al. stated that Ga concentration strongly influenced the Hall mobility and free carrier density. With increase in Ga content, both the mobility and carrier density of the material decreased due to the strong Ga-O bond. The strong bond is due to the strong ionic potential of Ga^{+3} which suppresses electron injection. Zinc incorporated materials such as IZO have the highest mobility in comparison with the other binary oxides[4]. However to be adopted for TFTs, the free carrier concentration needs to be controlled. The incorporation of Ga^{+3} suppressed the density of oxygen vacancies. Indium ion (In^{+3}) provides electron transport path in the conduction band through its large 5s-orbital. Amongst the three metal cations, In^{+3} is the only ion that meets the criteria of $(n-1)d^{10}ns^0$ of a heavy post transition metal cation.

Studies conducted by Kamiya et-al on the composition of the material is shown in Fig 2.4. Thus from the above mentioned reasons, IGZO with elemental ratio of 1:1:1:4 (In:Ga:Zn:O) is the adopted composition for TFT channel material.

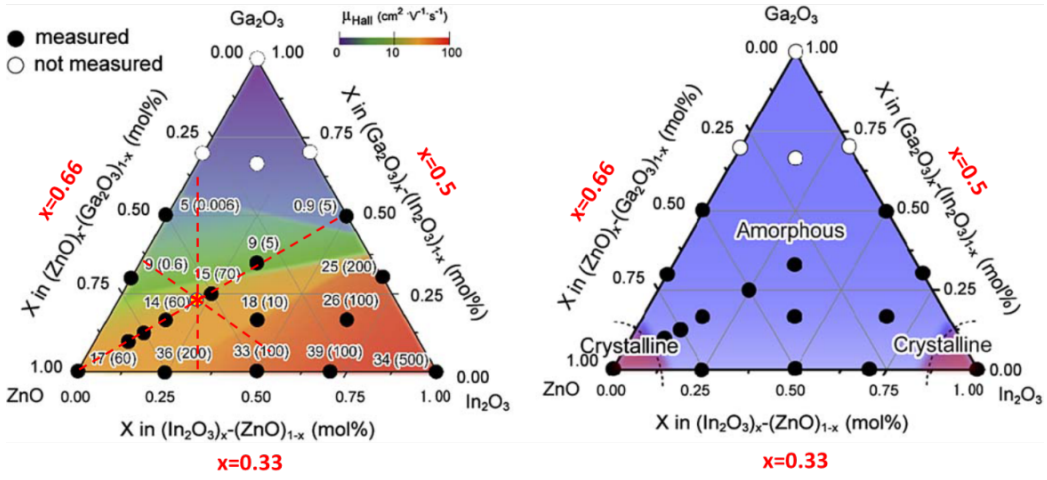


Figure 2.4: Hall mobility dependence on composition of the material (a-IGZO)[11]

Strong ionic nature of bonding in this structure promotes formation of defects easily due to the non-bonding of the transition metal ions with its neighboring ions. This causes poor long-term stability and makes it difficult for doping owing to their self- compensation effect. Studies have proved that the instability might be due to grain boundary effects which deteriorates the short-range uniformity in a poly-crystalline structure. Due to the amorphous nature of IGZO, grain boundary effect is not seen, thus promoting uniformity.

2.2 CONDUCTION MECHANISM IN IGZO

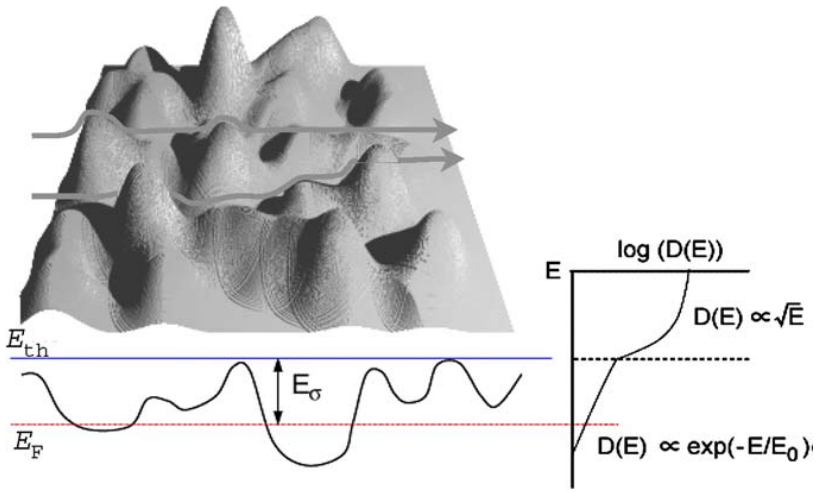


Figure 2.5: Schematic illustration of conduction and electronic structure around conduction band edge. This represents the percolation conduction mechanism in IGZO where the electron path finds lower energy states to travel[12]. An arrow is an electron conduction path. (left bottom) potential distribution cross-section. E_th and E_F denote threshold energy at above which carrier moves freely and Fermi level, respectively. (Right) Density of state [13]

Controllability of the carrier concentration is critical in IGZO (amorphous oxide semiconductors in general) as they can easily form defects. The primary defects formed during deposition are oxygen vacancies (V_o) which act as shallow donors in IGZO. Hall mobility has a functional dependence on the carrier concentration and temperature. Thus, the mobility increases with increase in carrier concentration unlike that of crystalline materials where the mobility decreases with increase in free carrier concentration. This increase in mobility can be explained through a percolation conduction model as seen in Fig 2.5. Due to the strong ionicity of oxides, both the conduction band and valence band are formed by ionic species. As mentioned in the previous section, the conduction band is formed by empty s-orbitals of the heavy transition metal cations and valence band is formed by filled p-orbitals of oxygen anions. The spherical symmetry of the s-orbital has a large spatial spread. This causes a significant overlap with the neighboring cation resulting in a path for electron transport.

The oxygen vacancies defects (V_0) are formed near the conduction band due to the non-bonding of the transition metal ions with the neighboring ions. These V_0 act as shallow donors, typically generating free electrons as follows[13] [8] [12].

$$V_o \rightarrow V_o^{2+} + 2e^- \tag{2.1}$$

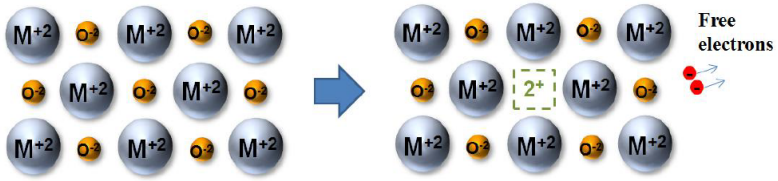


Figure 2.6: Generation of oxygen vacancy (Vo2+) and free electrons from the metal oxide where $M_(+2)$ is the metal cation and $O_(-2)$ is the oxygen anion. [9][10]

This carrier concentration can be controlled by varying the deposition parameters such as oxygen partial pressure or sputter power experimentally [15]. With increase in oxygen partial pressure the density of oxygen vacancies and free electrons decreases [15]. This confirms the source of free electrons as mentioned above in Eq 2.1. Ambient conditions during post metal annealing also has a significant influence on the electronic properties of IGZO and the M-S contact behavior [19]. Optimum degree of oxidant exposure during annealing with the right ambient conditions (time and temperature) will result in reduction of defect state concentration [19]. The ability to control the carrier concentration makes IGZO a good choice of material for TFTs in display devices.

2.3 DENSITY OF STATES

The band structure of as-deposited a-IGZO with density of states distribution within the bandgap is presented in Fig 2.7. Incomplete bonding is observed due to the amorphous structure which causes the formation of a high density of sub-gap states. Trap

states can either be donor-like or acceptor-like. Since IGZO is an n-type channel material, the focus here will be primarily on the sub-gap states near the conduction band which influences the TFT characteristics. Density of sub-gap states can be characterized by contributions from four defect distributions; acceptor-like exponential function, acceptor-like Gaussian function, donor-like exponential function, donor-like Gaussian function. The exponential functions are used to represent tail states and the Gaussian function is used to represent deeper sub-gap states. The tail states in the conduction band are observed due to the variation in bond angle of In-O. The band tail states near the conduction band minimum are very wide, 80-150meV, with these values close to Urbach energy [20]. The width of the band tail states of the conduction band become smaller in the deeper bandgap region. Oxygen vacancies act as donor-like states near in the conduction band. Change in the density of states in this region will cause a shift in the threshold voltage. Increase in the density will make the IGZO more conductive by generating more electrons and acts as metals instead of a semiconductor. Fermi level lies 0.15eV below the conduction band minimum and this shifts towards the conduction band when there is an increase in V_{GS}. This causes electron trapping in these states. The sub-gap density of states 0.15eV below the conduction band are smaller which explains the higher mobility, small subthreshold swing and low operating voltage in a-IGZO TFTs. The amorphous nature of the material breaks the coherent hybridization of 2p orbitals of Oxygen anion and forms strongly localized states isolated from the valence band. The density of this deep sub-gap states is $>5X10^{20}$ cm^{-3} with a width of 1.5eV. The sub gap density of states of a-IGZO annealed at 400^oC is 2-3 orders of magnitude lower than a-Si near the conduction band which results in smaller subthreshold swing. This is an important criterion for turning off the n-channel TFT [14].

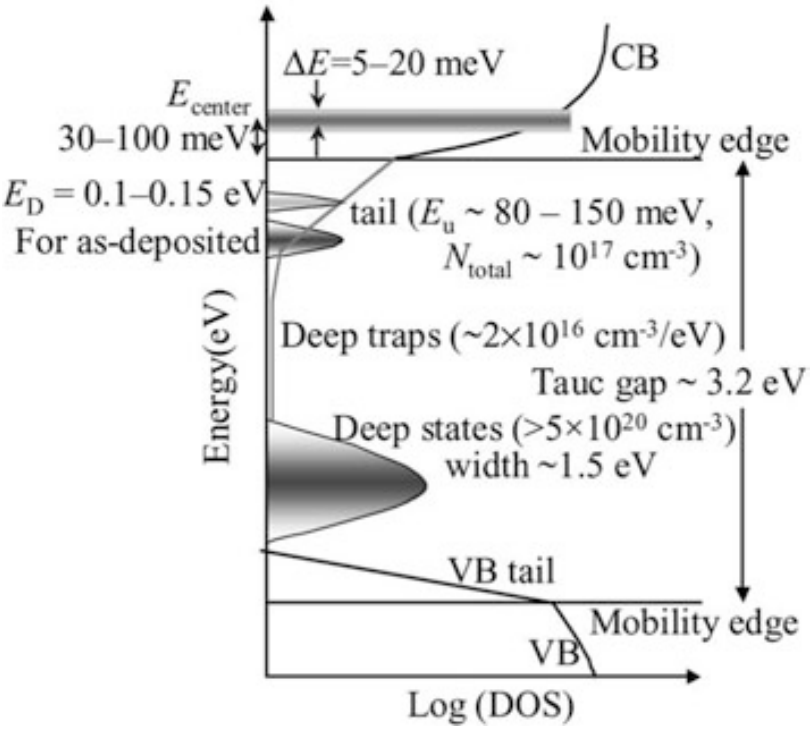


Figure 2.7: Band structure of a-IGZO with tail states and Density of states (DOS) distribution [14]

2.4 IGZO TFT CHARACTERISTICS

The performance of the device can be evaluated from various parameters obtained from the output transfer characteristics of the device. On-current I_{on} and Off-current I_{off} are important characteristics to be determine for current devices like OLEDs as I_{off} is useful for determining the minimum power consumption of the device. Threshold voltage is the gate voltage required to induce band bending at the surface of the semiconductor layer. Threshold voltage V_t of the device is the voltage at which the TFT starts conducting and this is important as fluctuations in this value can cause serious brightness variation in an OLED device which might further affect its performance and lifetime. Hence it is important to understand the fundamentals of physics to determine these parameters. In this section we will discuss in detail about the most important parameters for a TFT.

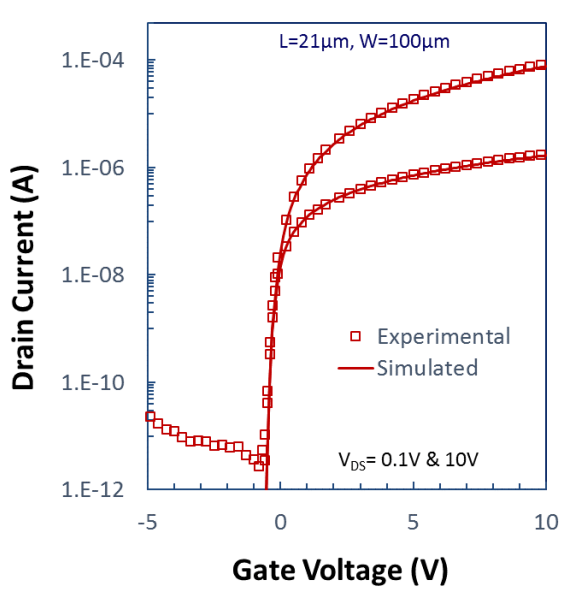


Figure 2.8: Comparison of the transfer characteristics of both experimental and simulated BG TFT with dimensions of L=21μm and W=100 μm

Fig 2.8 shows a comparison of the simulated and measured I-V characteristics of bottom gate passivated device of 21 μm length and 100 μm width. The simulated value matched very well with the measured data. The material and device model used for TCAD simulation of these devices will be discussed in the next section.

2.5 MATERIAL MODELLING FOR TCAD SIMULATION

Device simulation aids in better understanding of the influence of defect states and various other process parameters on the device operation. Visualization of the various effects in the TFT channel and interface region is made possible to understand the basic physics behind these. The presence of band tail states accounts for non-ideal behavior in the electrical characteristics of IGZO TFTs which are not represented well by the conventional models available. Extracting the basic TFT parameters such as mobility and threshold voltage is difficult due to the presence of defect states and gate voltage dependent source-drain resistance (R_{SD}).

In this section, we will discuss the TCAD simulation model developed which

provides an excellent overlay to the measured characteristics. Silvaco Atlas was used for simulating the TFTs interdigitated capacitors (IDC) and the establish material and device model parameters. The density of states g (E) for both acceptor and donor like band tail states and oxygen vacancy donor states defined by exponential and Gaussian distributions are represented as follows

$$g_{TA}(E) = NTA \exp\left(\frac{E - E_c}{WTA}\right) \tag{2.1}$$

$$g_{TD}(E) = NTD \exp\left(\frac{E_v - E}{WTD}\right) \tag{2.2}$$

$$g_{GD}(E) = NGD\, exp\left[-\left(\frac{E - EGD}{WGD}\right)^2\right] \tag{2.3}$$

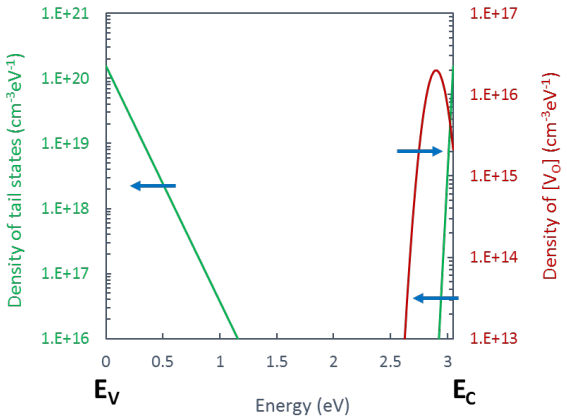
Where $g_{TA}(E)$ and $g_{TD}(E)$ are the density of acceptor-like conduction band tail states and donor-like valence band tail states respectively. E_c and E_v are the energy levels at the conduction and the valence band edge. NTA and NTD represent the density of acceptor-like states in the tail distribution at the conduction band edge and density of donor-like states in the tail distribution at the valence band edge. WTA and WTD is the characteristic decay energy of the conduction and valence band-tail states. $g_{GD}(E)$ is the density of donor-like states (oxygen vacancies). NGD, EGD and WGD are the peak value, mean energy and energy standard deviation, respectively, defining a Gaussian distribution for donor-like states, $g_{GD}(E)$ [15].

The non-ideal characteristics of the TFT were modelled by inclusion of interface defects to have a reasonable fit with the measured data. In this case of a good device, the influence of interface defects on the TFT characteristics was negligible and the bulk state defects. The band tail state density at the valence band edge and the donor-like valence band tail states do not influence the on state of the device.

To account for the defect states in a passivated device, additional parameters were added establishing interface traps and charge centers at the back-channel interface

of IGZO and the dielectric. Fixed charge density of $N_f = -1.9x10^{12}cm^{-2}$ and a Gaussian distribution of donor-like interface traps (N_{vo}) were adopted to provide a reasonable match to the characteristics. These modified parameters were used to account for threshold voltage shift. EGD and WGD values for interface traps were consistent with that provided for bulk states; the peak of the distribution was adjusted to $2x10^{12}cm^{-2}/eV$. The total integrated donor interface trapped charge state density $N_{IT} \sim 5x10^{11}cm^{-2}$ and a net back-channel surface state density $N_{SS} \sim -1.4x10^{12}cm^{-2}$ was obtained.

Symbol	Value
Band gap	3.05 eV
Electron affinity	4.16 eV
Relative permittivity	10
Electron mobility	12.7 $cm^2/V{\cdot}s$ *
NGD	$2{\times}10^{16}$ cm^{-3}/eV *
EGD	2.9 eV
WGD	0.1 eV
NTA	$1.55{\times}10^{20}$ cm^{-3}/eV
WTA	0.013 eV
NTD	$1.55{\times}10^{20}$ cm^{-3}/eV
WTD	0.12 eV



* parameter value modified from the ATLAS default material model.

Figure 2.9: Modified parameter values for material and device model in TCAD [10] [15]

The total space charge in the channel material due to oxygen vacancies integrated over both energy and thickness of the film is $N_{bulk} \sim 2.5x10^{10}cm^{-2}$. The influence of interface charge over the TFT characteristics can be dominant in the case of non-ideal behavior[21] [19].

Chapter 3

IGZO TFT PROCESS DEFINITION AND BASELINE PROCESS MODIFICATION

This chapter outlines the standard IGZO fabrication process in detail. Two different electrode configurations, the bottom-gate (BG) and the double-gate (DG) structure and their electrical characteristics are presented. Electrical characteristics of devices tested recently were inconsistent with results previously established, and so this deviation became a significant piece of this investigation. It was observed that the electrical operation of the TFTs varied from process runs done over several months, with a notable shift towards depletion-mode operation. This suggests that the material properties of IGZO had varied over this time period, hence experiments were designed to vary parameters in the fabrication process such as IGZO sputter conditions and thickness, passivation material thickness and anneal conditions. The results obtained from the design of experiments were used to modify the baseline process for fabrication, which was then used for further experiments in this study. The devices fabricated using the modified baseline process were thermally stressed at high temperatures of 140^oC and 200^oC to investigate the thermal stability of these devices. The results will be discussed along with the future work to be done.

3.1 TFT FABRICATION

A 6-inch silicon wafer with 6500 Å of thermally grown silicon dioxide is used as the base substrate for processing to represent the fabrication of IGZO TFTs on glass. For the bottom gate electrode, 50 nm of molybdenum is sputter deposited by physical vapor deposition using CVC601. Once sub-microtorr base pressure is achieved, the sputter deposition is done in argon ambient at a pressure of 2.7 mT. An 8-inch target was used at 1000 W power for 200 s to obtain the target thickness. The gate electrode is then patterned using a GCA g-line stepper, and subtractive etched using molybdenum etchant which is a combination of acetic, nitric and phosphoric acid. The gate dielectric (100 nm SiO_2) is deposited using plasma enhanced chemical vapor deposition (PECVD) in an AMAT-P5000 with tetraethyl orthosilicate (TEOS) and oxygen as precursors at 390^oC. The oxide is then annealed (densified) in nitrogen ambient at 600^oC for 2 hours. After densification, 50 nm of IGZO is RF sputter deposited at Corning Incorporated using an AMAT Centura system. Reactive sputter is done with the substrate temperature maintained at 200^oC using a target composition of In_2O_3 : Ga_2O_3 : ZnO in the ratio of 1:1:2, in argon with oxygen partial pressure of 7%. The IGZO is patterned and wet etched using H_2O: HCl in the ratio of 6:1. Devices with and without back-channel passivation were fabricated. For an un-passivated device, the gate contact cut is patterned and etched using BOE (10:1) to make contact to the bottom gate. S/D patterning is done using negative resist and then the metal is sputter deposited using the CVC601 in argon flow 20 sccm at 2.7 mT, using DC power of 200 W. A molybdenum/aluminum bilayer stack (each 50 nm thick) was used as the source/drain metal, where the molybdenum serves as the contact metal and aluminum provides resistance to thermal oxidation during annealing. The metal is patterned using a lift off process done by subjecting the wafers to ultrasonic energy in PG remover solvent at 45^oC for 20-25 minutes. The wafers are

then subjected to an anneal at 400^oC for 30 minutes in nitrogen ambient, with an air ramp down. This is done to reduce the IGZO conductivity by reducing the number of oxygen vacancies and in turn reducing the electron concentration, thus providing appropriate semiconducting properties for TFTs. For passivated devices, 100 nm of passivation SiO_2 is deposited following the S/D metal, using the AMAT-P5000 PECVD TEOS process. An anneal is done in an oxygen ambient at 400^oC for 8hours with a 5 hour ramp down. ALD alumina (10-15 nm) is deposited as an optional barrier layer at 200^oC. The substrates are immediately taken for ALD deposition after annealing to minimize exposure to air ambient. The passivation open patterning is then done to contact the electrode pads and wet etched using 10:1 BOE for 5minutes. The devices are then ready for testing.

3.1.1 DIFFERENT ELECTRODE CONFIGURATION

Staggered and co-planar electrode configurations are used for TFT structures [22] [23], but this study will focus on the staggered BG and DG arrangements. These two configurations and their electrical characteristics will be discussed and analyzed.

3.1.1.1 BOTTOM GATE STRUCTURE

The staggered BG structure is shown in Fig 3.1. The TFT is typically fabricated with a passivation dielectric, however devices without back-channel passivation were used for baseline comparisons.

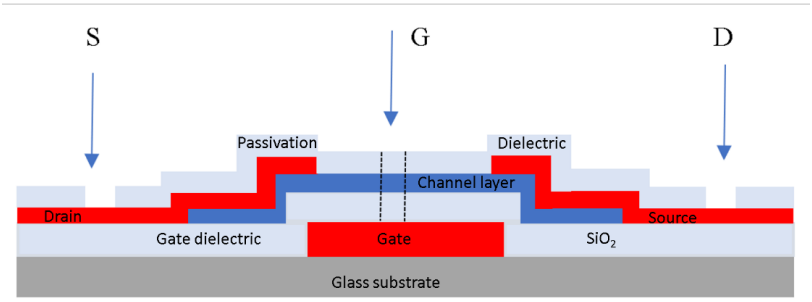


Figure 3.1: Cross sectional view of a bottom gate configuration of IGZO TFT

Fig 3.2 shows the I-V characteristics of a passivated bottom gate device measured using a HP4145 analyzer with a gate sweep of −5 V to +10 V and low drain bias of 0.1 V and a high drain bias of 10 V.

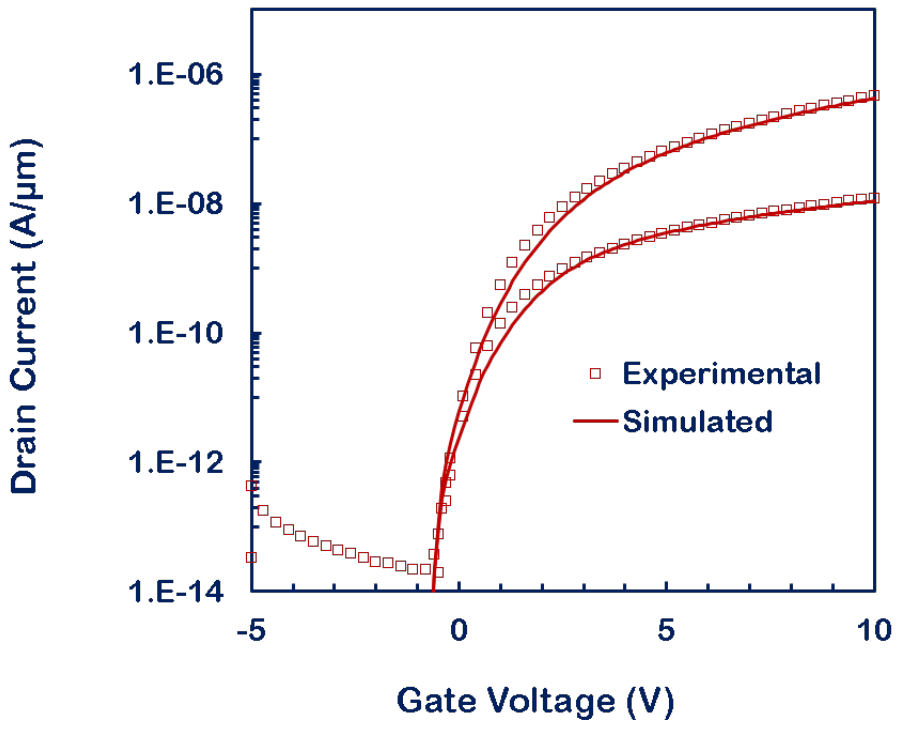


Figure 3.2: Characteristics of a bottom gate passivated IGZO TFT of L=24 μm and W=100 μm

The electrical characteristics of the BG TFT show a minor influence of interface traps at the back-channel which appears as slight degradation in subthreshold operation. This can be overcome by the DG electrode configuration shown in Fig 3.3. Over a year's time the BG passivated devices demonstrated process drift, exhibiting poor electrical characteristics such as poor subthreshold slope, DIBL (drain induced barrier lowering) like separation on long channel devices. They exhibited the weakest ability to overcome the influence of interface trap states and control the TFT operation.

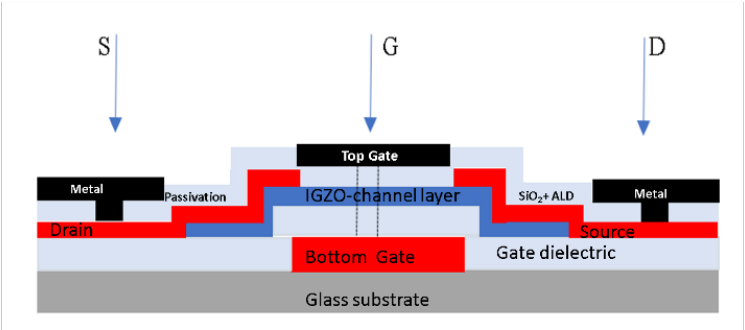


Figure 3.3: Cross sectional view of a double gate configuration of IGZO TFT

3.1.1.2 DOUBLE GATE STRUCTURE

The DG device has a similar process of a bottom gate device with an additional top gate electrode over the ALD passivation material. The top gate electrode is aluminum which is thermally evaporated and patterned using a lift off process. Subtractive etch was replaced with a lift off process to have a controlled patterning of the metal. The double gate structure shows advantage over the bottom gate device as they have better control of the back-channel layer which is prone to trap charges causing instability of the device. A more detailed description of this instability is discussed in the next section of the chapter. Figure 3.4 shows the I-V characteristics of a DG device measured using a HP4145 analyzer with a gate sweep of -5 V to $+10$ V and

low drain bias of 0.1 V and a high drain bias of 10 V.

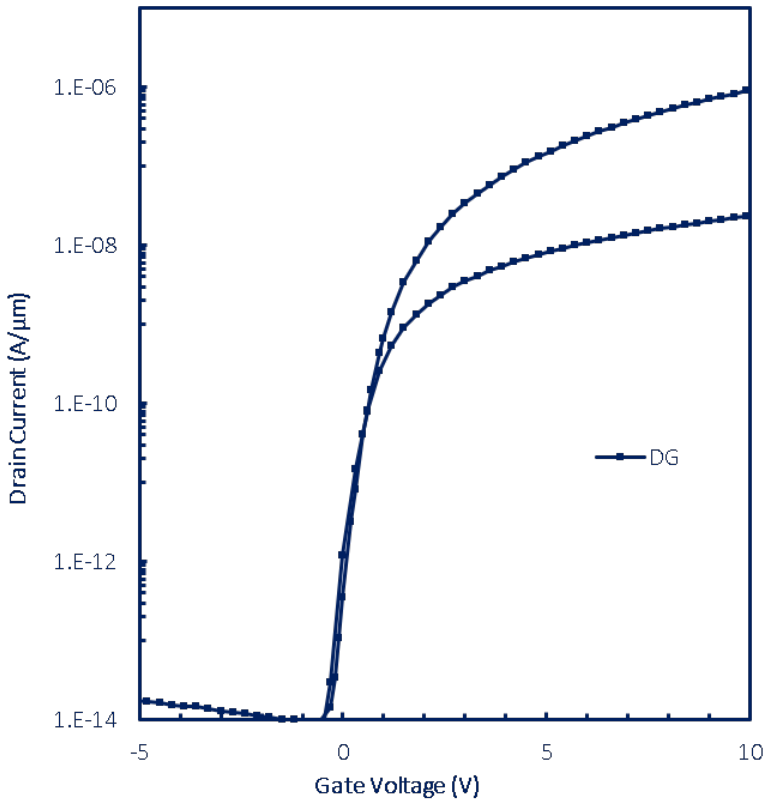


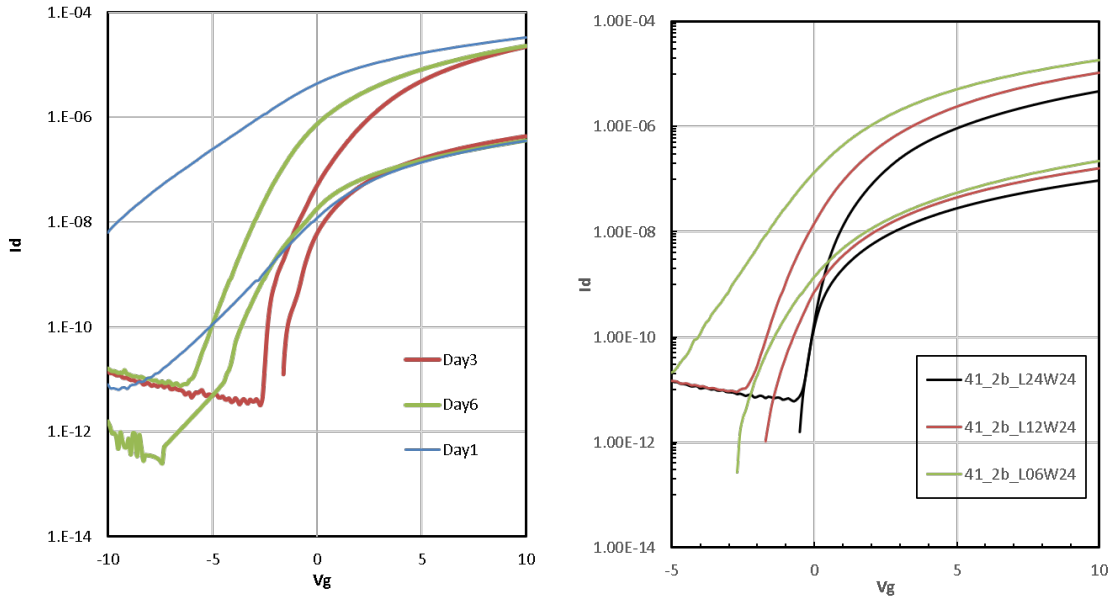
Figure 3.4: Characteristics of a double gate IGZO TFT of L/W= 24/100 μm

The transfer characteristics of the double gate device showed improvement of both the on-state and off-state performance of the TFT due to improved electrostatics. The presence of an additional top gate enhanced the performance of the device by improving the SS from 260 mV/dec to 180 mV/dec and essentially a two-fold increase in channel charge (i.e. drain current).

3.2 PROBLEM STATEMENT

The electrical operation of the TFTs varied from process runs done over several months, with a notable shift towards depletion-mode operation. The BG passivated devices exhibited poor subthreshold behavior and a separation of transfer charac-

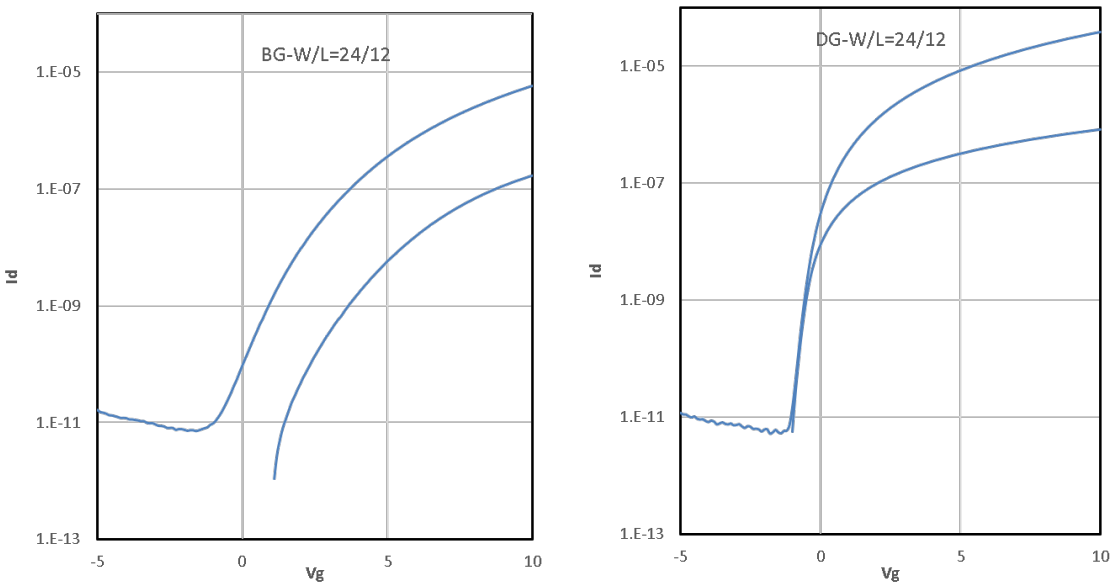
teristics on long channel devices; both indicative of back-channel charge and lack of gate control. While the influence on DG devices was not as pronounced, this source of variation had to be identified and suppressed. The focus initially shifted to the BG unpassivated device process for baseline comparisons. It was observed in the I-V characteristics of an un-passivated device that the standard anneal was not adequate to reduce the sub-gap states in the channel region. The threshold voltage of the device was left shifted drastically. Ripening is the process of exposing the channel to ambient environment; this promotes the self-passivation of high-density trap regions at the back-channel [24]. The devices were left in ambient conditions for ripening process. But after ripening it was observed that the devices seemed to behave like an under annealed device with the threshold voltage left shifted from the ideal value close to 0-V with significant trap associated barrier lowering (TABL) as seen in Fig 3.5. This effect is due to in-homogeneity of donor states at the topside IGZO interface that presents regions with distinctly different effective charge levels In the case of passivated bottom gate devices, the 8hrs anneal in O_2 ambient at 400^oC did not suffice in reducing the number of oxygen vacancies in the channel and the interface. Increased annealing did not seem to be effective in restoring the transfer characteristics. This then steered us to the hypothesis that there could have been a change in the target composition which made the channel very conductive.



(a) (b)

Figure 3.5: Characteristics of an unpassivated BG TFTs with IGZO thickness of 50 nm whose L/W=12/24 μm initial results tested on different days to observe the ripening effect in room ambient with a) standard anneal conditions b) L=24,12,6 μm tested after aggressive annealing conditions .

Figure 3.5a is the characteristic response of unpassivated devices with standard anneal in N_2 ambient for 30 mins and ripening process. It is observed that these devices even after 6 days of ripening in ambient does not yield good characteristics as observed in Fig 1.8 whereas the 24 μm length devices in the Fig 3.5b after aggressive annealing conditions (30min in N_2 ambient, 1hr in O_2 ambient with 4 hour ramp down in O_2) yielded good TFT characteristics with steep subthreshold and threshold voltage of the device close to ideal value. These devices did not exhibit Trap Associated Barrier Lowering,which is the mechanism to describe the long channel DIBL-like separation as observed in Fig 3.5a but short channel devices of L=12 μm and 6 μm showed significant TABL and left shift in the characteristics. This was conclusive of the hypothesis stated above.



(a) (b)

Figure 3.6: Characteristics of a) passivated BG (left) and b) DG (right) devices with channel length L=12 μm with standard anneal conditions in O_2 ambient for 8hrs at 400^oC

The devices exhibited poor electrical characteristics with shallow SS and significant TABL in the case of passivated bottom gate device with standard O_2 anneal at 400^oC for 8hrs as observed in Fig 3.6a. Whereas the double gate devices with the same anneal conditions and without ALD capping layer exhibited good results as shown in Fig 3.4.

3.3 DESIGN OF EXPERIMENTS ON FABRICATION OF TFTs

The devices fabricated with the standard process parameters as stated in the above section exhibited anomalies in their behavior that need to be addressed to yield devices with good TFT characteristics as seen in Fig 3.2 and 3.4. The parameters that influence these anomalies in the device behavior were, thickness of the channel layer, passivation and anneal conditions. This section discusses the experiments designed

Table 3.1: Design of experiments with IGZO thickness and oxygen partial pressure

Device Configuration	IGZO thickness (nm)	Oxygen partial pressure
BG	20	7%
BG	35	7%
BG	45	7%
BG	50	7%
BG	30	13%
BG	50	13%

to modify the electrical characteristics behavior of the TFT and their results.

3.3.1 IGZO THICKNESS AND BACKCHANNEL INTERFACE

The effect of channel thickness on the electrical characteristics of the TFT is investigated in this section. Design of experiments (DOE) with various thicknesses of IGZO and the oxygen partial pressure during deposition was proposed. The characteristic response of the TFTs with the varying conditions will be discussed in detail. Table 3.1 presents the different thickness along with the oxygen partial pressure varied during deposition experimented in this study. Increasing the oxygen partial pressure to 13% by doubling the gas flow was done to reduce the number of defects in the channel (V_o). Increasing the partial pressure increased the deposition rate by 50% thus rendering a thicker film. Thinner channel material was obtained by as-deposited thin layer and back channel etching process. There was significant difference in the device performance of these different treatments.

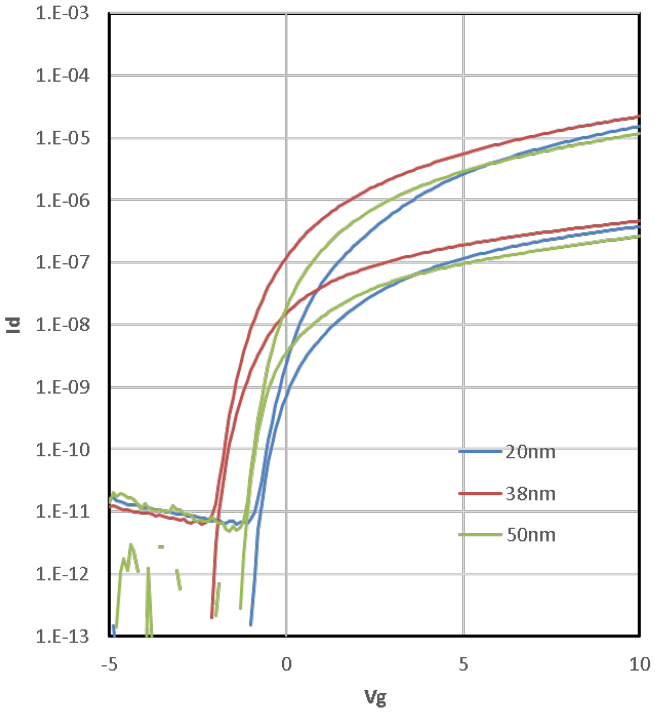


Figure 3.7: I-V characteristics of BG passivated devices with different channel thicknesses of L/W=12/24 μm with 50 nm SiO_2 with 4hr anneal in O_2 ambient

From fig 3.7 it was observed that there was no significant change in the electrical characteristics of the devices with IGZO thinned by wet etch process 20 nm and 38 nm thickness in comparison with the 50 nm device. The thickness of the channel material does not affect the SS but affects the threshold voltage of the device.However the dependence of threshold voltage on thickness is questionable considering the inconsistent shift shown in Fig. 3.7. This can be observed from the results obtained but there is no significant variation in the threshold voltage. Devices with as-deposited thinner channel material showed poor characteristics in comparison to the back-channel etched devices. Wet etch of IGZO is critical and there was inconsistency in the behavior of these devices which is not well understood and hence 50nm as-deposited IGZO was preferred as the standard thickness for future experiments and study.

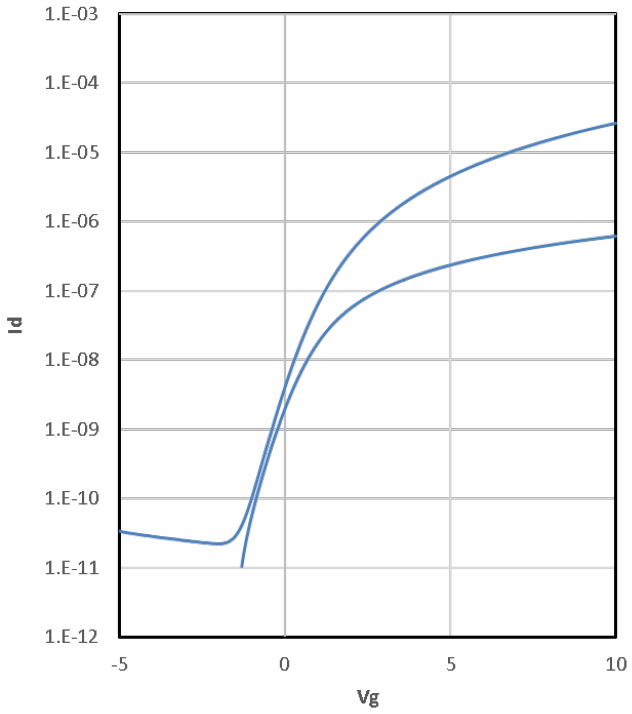


Figure 3.8: IV characteristics of a BG passivated device of W/L of 24/12 μm with 50 nm IGZO annealed at 400^oC for 8hrs in O_2 ambient

Figure 3.8 shows that the electrical characteristics of the passivated BG device with thinner passivation dielectric and standard 8hr anneal but these show poor electrical characteristics with shallow SS. Whereas the BG device as seen in Fig 3.7 with 4hr anneal shows improved electrical behavior.

3.4 PASSIVATION AND ANNEAL CONDITIONS

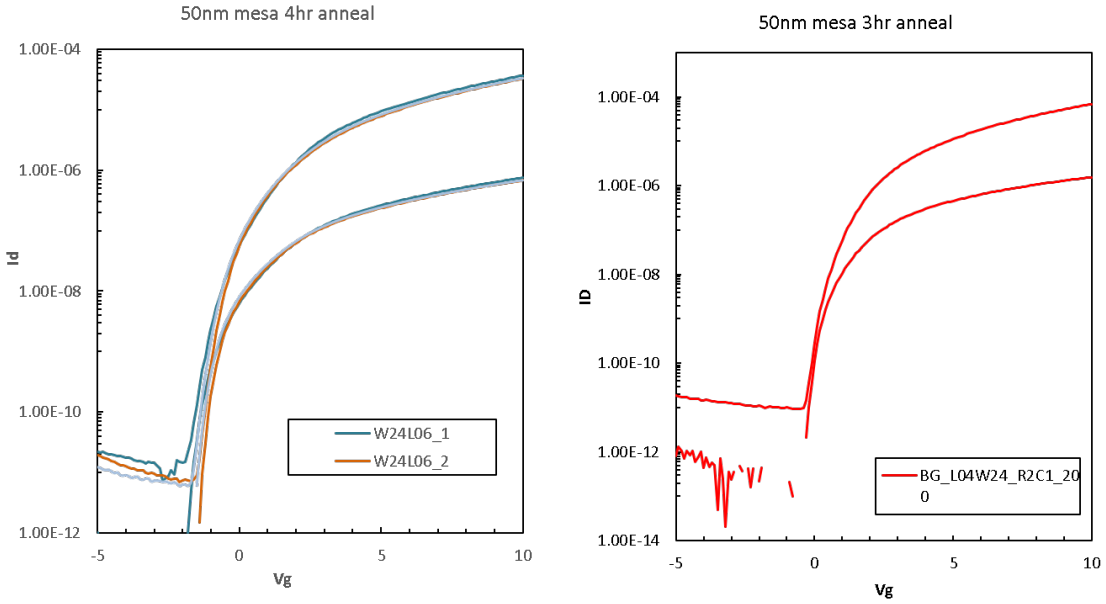
Reducing the thickness of the channel material did not render significant improvement in the electrical characteristics of the device. The experimentation was then focused on the reduction of passivation dielectric thickness and the modification in anneal conditions. From Fig 3.7 it was observed that reducing the passivation dielectric improved the electrical characteristics of the device. Experiments were designed with 50 nm passivation dielectric with 10 nm ALD alumina annealed for different times.

The design of experiments is for different IGZO thickness and anneal conditions are tabulated in Table 3.2. Increasing the annealing was proven not to be effective at restoring the electrical properties of the device as this depleted the devices further (left shifting the I-V characteristics) and exhibited pronounced TABL (separation between the high drain and low drain characteristics).

Table 3.2: Design of experiments with different passivation anneal conditions

Device Configuration	IGZO thickness	Passivation material	Annealing conditions
BG passivated	20,30,50nm	SiO_2 + 10nm Al_2O_3	3-6 hrs at 400^oC in O_2ambient

Annealing in oxygen ambient is done to reduce the electron concentration by reducing the number of sub-gap defect states in the channel material. From Fig 3.7 it was seen that reduction in anneal time to 4 hours, when in combination with the thinner (50 nm) passivation oxide, had a significant significant affect in the reduction of electron concentration which right shifted the characteristics. Anneal times were varied from 3hrs to 6hrs to identify the ideal conditions for the stack mentioned in this study.



(a) (b)

Figure 3.9: Transfer characteristics of BG passivated devices of under different anneal conditions a) 4hr anneal on a BG passivated device of L/W=6/24 μm b) 3hr O_2 anneal on BG passivated devices of L/W=6/24 μm

It was observed from the results in Fig 3.9b that 3hr anneal has characteristics similar to the 4hr anneal with threshold voltage of the device shifted further to the right. Results suggest that the 3hr anneal is ideal for modifying the material properties of IGZO and improves the electrical characteristics of the device with right shift in comparison to the 4hr anneal as seen in Fig 3.9b. It also reduces the time of fabricating the device.

3.4.1 MODIFIED FABRICATION PROCESS FLOW

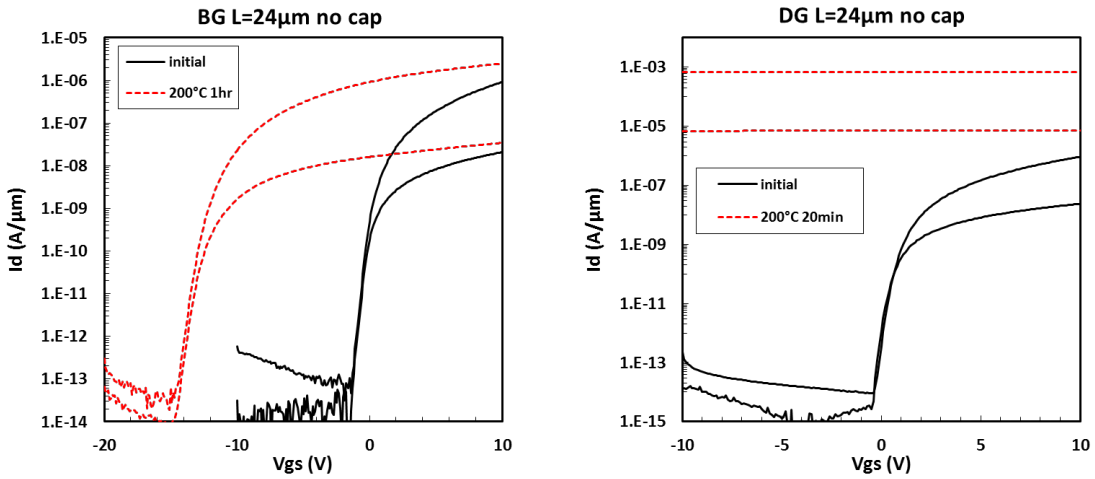
The results of the experimentation done in the previous section has helped re-establish a new process for the fabrication of TFT to yield good devices. The modified process conditions for the process will be summarized in this section to be used for future reference. The process parameters that will be modified are thickness of the passivation dielectric, anneal conditions and source/drain metal stack. The standard thickness of

the channel layer (IGZO) used was 50 nm with the oxygen partial pressure being 7%. In the modified process, the thickness and deposition conditions of IGZO remained the same. The S/D metal deposited is 50/50 nm of Mo/Al by sputter deposition with the deposition conditions as mentioned in fabrication process. The devices are then passivated with 50 nm of SiO_2 deposited by PECVD with TEOS and oxygen as precursors at 390^oC. The anneal conditions were modified from 8hrs to 3hrs at 400^oC in an O_2 ambient. The devices are then immediately deposited with another passivation layer of 10 nm Al_2O_3 by ALD at 200^oC. It is important to not subject the device to ambient conditions with oxygen and water vapor as these when absorbed act like donors in the channel region which will cause instability in the device. The devices fabricated with these modified process parameters showed improvement in the IV characteristics such as steeper subthreshold sweep, right shift in the characteristics which is due to reduction in the number of oxygen vacancies which leads to better control of the density of electron concentration in the channel region. The IV characteristics of the devices fabricated with the modified process is shown in Fig 3.9b.

3.5 THERMAL INSTABILITY OF IGZO TFTs

It is well established that IGZO is extremely reactive to ambient conditions, both during and after TFT fabrication. Long lifetime of the devices is a requirement for display devices and hence stability of the TFTs is important. The stability of the devices with thermal stress is important and must be studied as the devices degrade in performance when subjected to elevated temperature (e.g. T 200^oC) following TFT fabrication during chip-on-glass attachment for the bonding mechanism. Thermal stability of IGZO TFTs were previously studied at applied temperatures of 140^oC and 200^oC, as these temperatures were considered essential for process integration. When the TFTs, both BG and DG were subject to 200^oC on a hot plate with SiO_2 as the

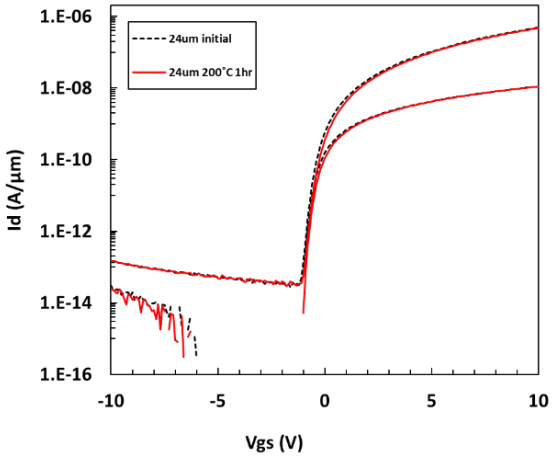
back-channel passivation, significant left shift in the IV characteristics of the BG TFT was observed after an hour of stress. This was more pronounced in the DG devices which upon stress for 20-min on a hot plate showed resistor-like behavior. These results motivated further investigation as the devices showed stable characteristics after the final passivation anneal at 400^oC.



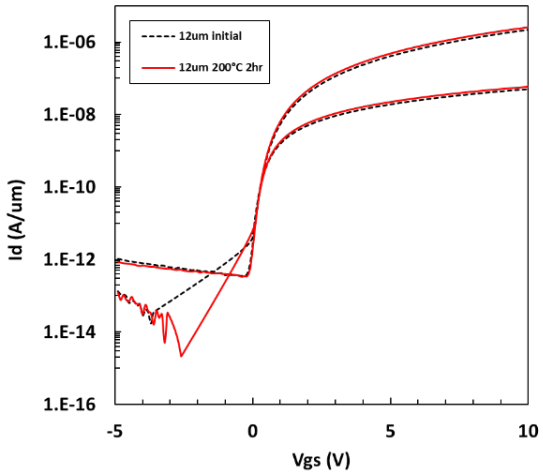
(a) (b)

Figure 3.10: a)BG and b)DG TFTs of L=24μm with SiO_2 as the back-channel passivation material which show degradation in performance when stressed on a hot plate at 200^oC

An additional layer of capping between the SiO_2 and aluminum was deposited using atomic layer deposition at 200^oC which was found to suppress the reaction of water with the top gate. Both the BG and DG TFTs showed good stability when the devices were passivated with an additional capping layer of 10 nm of Al_2O_3 using atomic layer deposition[25].



(a)



(b)

Figure 3.11: a)BG and b) DG devices with 10 nm Al_2O_3 capping layer between back-channel passivation dielectric and the top gate metal (aluminum)

3.5.1 THERMAL STRESS RESPONSE ON MODIFIED BASELINE PROCESS

The devices fabricated with the modified baseline process both bottom gate and double gate devices were stressed at 100^oC, 140^oC and 200^oC to observe their response.

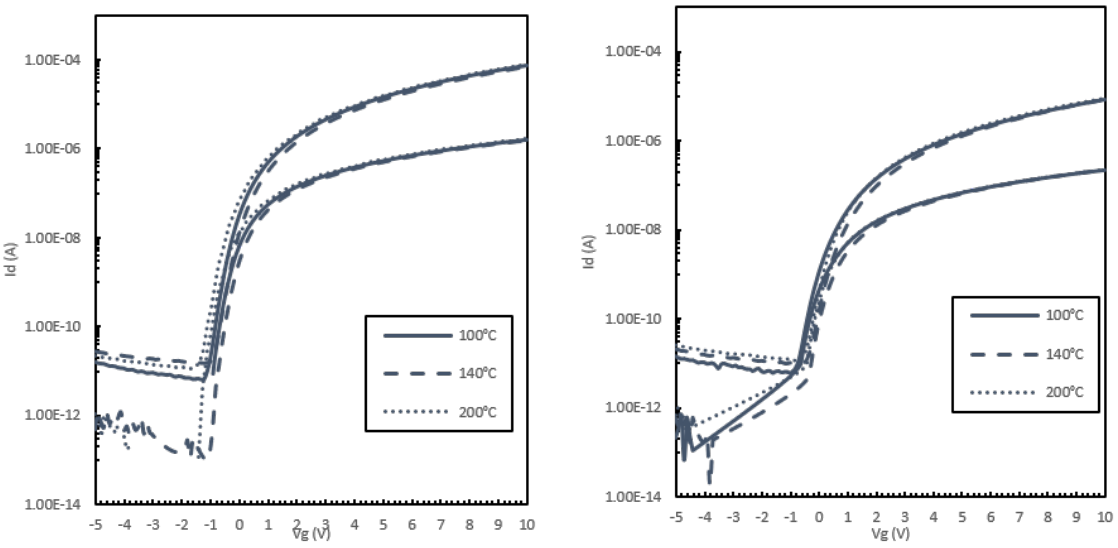
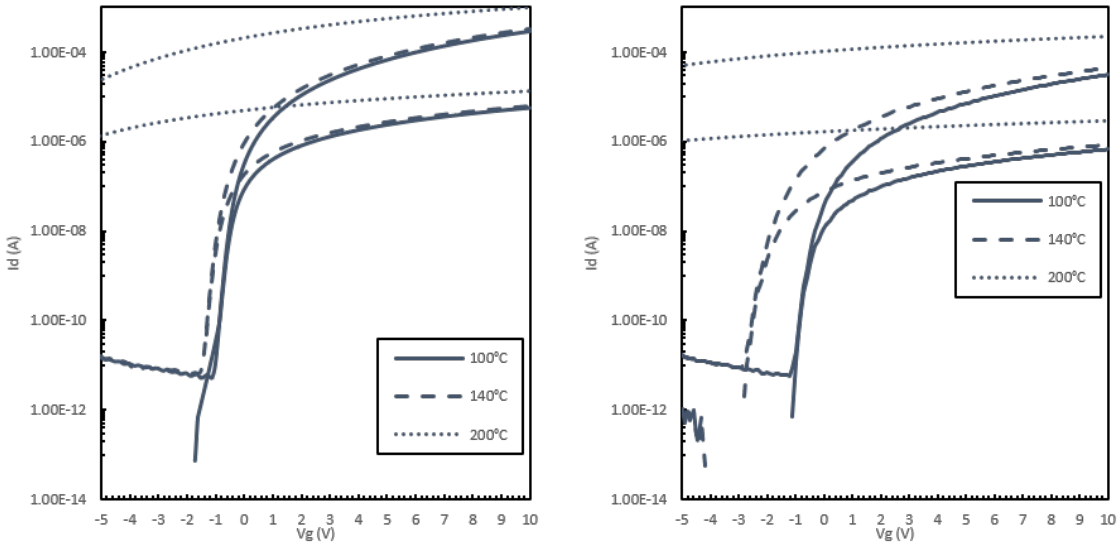


Figure 3.12: a) BG TFTs of L=4 μm and b) L=24 μm thermally stressed at various temperatures as indicated in the plot

From the Fig 3.12a it is observed that the bottom gate devices upon thermal stress of up to 200^oC showed stable behavior without any drastic shift in characteristics. The thermal stability of these devices with the modified process is similar to the results obtained with the old process conditions as mentioned in Fig-3.11a. There is consistency in the device behavior of a BG device when subjected to thermal stress. When the DG devices were subjected to thermal stress, both the short channel and long channel devices degraded by significantly shifting to the left after 140^oC hot plate bake. After 200^oC, the devices failed which can be observed in Fig 3.13. This is inconsistent with the observations made in the previous section as shown in Fig-3.11 where the small channel devices are stable with thermal stress and the longer devices ($L \geq 24\mu$m)fail.



(a) (b)

Figure 3.13: DG devices of a) L=4 μm and b) L=24 μm thermally stressed on a hot plate at various temperatures as indicated in the plot

There is difference in the behavior of the short channel and long channel device as seen in Fig.3.13. The short channel devices of length 4 μm, when subjected to 140^oC hot plate treatment causes a left shift in the characteristics of the device by less than one volt whereas in the case of a longer channel device of L=24 μm shift the characteristics is significant by almost two volts.

3.6 SUMMARY

The chapter summarizes the various experiments done to reestablish a baseline process for the fabrication of IGZO TFTs. The process parameters used initially yielded TFTs that had poor electrical characteristics with significant TABL and poor SS in an unpassivated device. This was inconsistent with the results obtained previously. Multiple experiments with different anneal and passivation conditions were done to study the change in the channel material properties. It was observed that the electrical characteristics of the devices with 3hr anneal time showed steeper SS and a

significant right shift which is evident in Fig 3.9b with their threshold voltage 0V. A baseline process was reestablished with no modifications in the thickness of IGZO and its deposition conditions (50 nm with 7% oxygen partial pressure was used), the thickness of the passivation dielectric reduced from 100 nm to 50 nm and the anneal conditions varied from 8hr to 3hrs at 400^oC in O_2 ambient. This was then used for investigating the thermal instability of the BG and DG devices. Thermal stability of the devices is important as the devices will be subjected to higher temperature processing during bonding mechanism for chip-on glass attachment. In this study, the devices were subjected to higher temperatures of 140^oC and 200^oC on a hot plate in room ambient and their electrical characteristics were measured. It was observed in previous study that the bottom gate devices were stable even after 200^oC hot plate treatment for one hour. Whereas the DG device when subjected to 140^oC, showed channel length dependence on their instability. The longer channel devices failed at 140^oC whereas the shorter channel length device was stable at 140^oC. When the device fabricated with the modified baseline process was subjected to higher temperature, the bottom gate devices remained stable and, in some cases, showed improvement in the behavior of the TFTs. The DG device behavior was inconsistent with the previously obtained results where both the short channel and long channel devices failed. This inconsistency in the behavior of the DG devices needs to be investigated.

Chapter 4

INTEGRATION OF COPPER AS THE BOTTOM GATE ELECTRODE

Large panel size, high resolution and high scan frequency are main factors to be considered in the advanced flat panel display market. With the already existing research and development done with IGZO TFTs for driving large area LCD and OLED panels, RC delay has become an important issue that needs to be addressed. In large displays such as 100 inch displays with 4K resolution the pixel size is 200 μm whereas with an 8K resolution the pixel size is reduced to 90 μm or less. With an 8K display where the number of pixels and gate and data signal lines are increasing, it becomes important to reduce the time constant (RC) associated with moving charge on and off the pixel driver TFT. The time constant depends on three primary factors in a display device; signal line resistance, signal line cross-over capacitance and device parasitic capacitance. Hence it is important to reduce these three factors as faster transmission of signals is required [26]. Reducing the sheet resistance can be done in conventional process by increasing the thickness of the film but this can lead to breakage of glass due to stress of the film, or surface topography issues. This can also be done by incorporation of a metal with lower resistance for the gate bus lines and data bus lines. Amongst the various metals available copper is appropriate for the electrode material for display devices due to their properties such as low resistance, low cost and high corrosion resistance [27].Conventional a-IGZO TFT

uses molybdenum as the gate metal. Incorporating copper as the gate electrode has proven to be advantageous in that copper can be used as both the gate metal and the row enable that transfers charge from each column to the respective pixel in that particular row. This has a significant improvement on the RC delay of the devices as compared to the TFT with molybdenum as the gate electrode. In order for copper to be adopted in large scale manufacturing, certain challenges need to be addressed. These challenges of integrating copper in the IGZO TFT as the bottom gate electrode is studied and discussed in detail in the next section.

4.1 CHALLENGES OF COPPER INTEGRATION

Copper is of high interest in the display industry as an interconnect and electrode material in IGZO TFT backplanes for display panels. Copper is known to have good bulk thermal and electrical conductivities and low electromigration[28] [29], making this a good candidate for larger area displays. High conductivity translates to fast transmission of signals through bus lines. The incorporation of copper in the BG TFT structure poses several challenges of which the primary being the diffusion of copper through the gate dielectric and into the active channel region which has been shown to degrade the TFT characteristics [30], and poor adhesion of copper to the glass substrate. Copper diffusion into the channel region, the gate dielectric and the interface degrade the device performance by inducing interface traps[30]. This causes a negative shift in threshold voltage V_th of the device and degradation of the subthreshold swing and the effective channel mobility of the device. In addition, copper diffusion may result in gate dielectric failure. Hence a diffusion barrier layer may be required to inhibit the diffusion of copper. The adhesion of the gate metal to both the glass substrate and the gate dielectric material is also an issue of great importance. Copper has poor adhesion to dielectric materials which can result in delamination during elevated temperature process due to difference in thermal expansion or changes in

material morphology.

4.1.1 PROCESS INTEGRATION

Copper has emerged as an important metal for interconnects in the display industry. There have been various studies on promoting the adhesion of copper on glass; a few common methods studied are annealing, alloying and use of an interlayer [31]. In this study a design of experiments with different treatments for the gate metal stack and anneal conditions following the gate dielectric deposition are investigated, with details shown in Table 4.1.

Figure 4.1: (a) Ti/Cu and (b) Ti/Cu/Ti gate metal film stacks employed to investigate copper electrode adhesion and copper diffusion effects on the gate dielectric and IGZO channel.

Table 4.1: Design of experiments to study the challenges incorporating copper as the gate electrode for IGZO TFT

Wafer	BG metal	BG dielectric thickness	IGZO thickness	Pre-anneal conditions
1	Ti/Cu	100 nm SiO_2	50 nm	No anneal
2	Ti/Cu	100 nm SiO_2	50 nm	400^oC N_2 anneal
3	Ti/Cu	100 nm SiO_2	50 nm	600^oC N_2 anneal
4	Ti/Cu/Ti	100 nm SiO_2	50 nm	No anneal
5	Ti/Cu/Ti	100 nm SiO_2	50 nm	400^oC N_2 anneal
6	Ti/Cu/Ti	100 nm SiO_2	50 nm	600^oC N_2 anneal

In this study the focus is to experiment on different annealing conditions and use of a metallic interlayer. Much attention has been focused on using refractory metals such as titanium and chromium as interlayers for glass and copper. These refractory

metals have good adhesion to glass and hence a thin layer of these metals between copper and glass is used[32]. But in this study, titanium will be used which has good adhesion to glass. To replicate the process on a glass substrate, 500 nm of SiO_2 was grown on a silicon wafer. The different gate stacks proposed are a)20 nm titanium/ 80 nm copper and b) 10 nm of titanium/ 80 nm of copper/ 10 nm of titanium. 100 nm of SiO_2 is the gate dielectric used for both a) and b). An addition layer of titanium is deposited in b) to study if this promotes adhesion of gate dielectric to the metal and inhibits diffusion of copper to the channel region. One major challenge of incorporating titanium is that when the devices are subject to high temperature process during fabrication, there will be diffusion of titanium into copper which might increase the sheet resistance of the film[33]. This led to the increasing interest in eliminating the use of interlayer metal between copper and glass. This steered way to promoting the adhesion by treating the surface of glass before the deposition of copper. Another common method to promote adhesion is by annealing the film, which was investigated in this study. Annealing decreases the stress of the film by an amount that varies significantly with the thickness of the film**[ref]**. In this study the thickness of the film was not varied, but experiments were done by varying the temperature at which the devices were annealed after the deposition of gate dielectric. This study was done to investigate the different temperatures for pre-annealing with a constant gate electrode thickness. The different annealing temperatures used in this study are shown in table 4.1. Silicon dioxide is not a good diffusion barrier for copper. SiON and SiN_x are used to prevent copper ion diffusion into the channel in a lot of research work done previously. This study investigates the influence of gate stack and the impact of annealing on the diffusion of copper into the channel. Gate dielectric stack of Si_3N_4/SiO_2 is proposed for devices with no metal interlayer for gate electrode. This is proposed to be a good diffusion barrier to copper ions. If a single layer of Si_3N_4 is adopted as the gate dielectric, weakly bonded H+ ions will

inject into the channel layer and will cause serious influence on the threshold voltage of the device by causing a shift and short the channel [34]. Hence it is necessary to have SiO_2 interface with the channel layer. The fabrication process for these devices are described briefly in the next section. The device characteristics for the various processes done will be explained in detail in the following sections.

4.1.2 DEVICE FABRICATION

A base substrate like our conventional process was used where 500 nm of silicon dioxide was grown on a 6-inch silicon substrate to replicate processing on a glass. The substrate is initially coated with HMDS prime and then spin coated with negative resist. Bottom gate lithography is done using g-line stepper and developed. Then the wafers are loaded into the E-beam evaporator for deposition of both titanium and copper as the gate electrode. 20 nm titanium and 80 nm copper is deposited on one case and 10 nm titanium with 80nm copper and 10nm titanium is deposited on another set of wafers. Lift off patterning is done using PG remover to obtain good definition of bottom gate metal. 100 nm of SiO_2 is deposited using PECVD at 300^oC to avoid contamination of the tool. The densification of oxide deposited is done in a nitrogen ambient at temperatures mentioned in the table. Post densification of the gate dielectric, 50 nm of IGZO is RF sputter deposited at 200^oC in an ambient containing 7% oxygen. The channel layer is then patterned using dilute HCl (6:1 of H_2O: HCl) for 15 seconds. Gate vias are patterned for contact with the bottom gate using 10:1 Buffered oxide etch (BOE). Molybdenum/aluminum bilayer is deposited using a DC sputter tool and patterned using lift off process for gate/ source/ drain electrodes. Silicon dioxide SiO_2 with a thickness of 100nm is deposited using PECVD as the passivation material for these devices. This is then annealed in oxygen ambient at 400^oC for 3hrs with a 2hr ramp down in air. This is then immediately taken for ALD deposition to have very little exposure to ambient. This is done to avoid

absorption of water molecules or moisture which can degrade the device performance. 10 nm of Al_2O_3 is deposited. Passivation open patterning is done to open contacts to source, drain and gate electrodes.

4.2 RESULTS

The results obtained from the different fabrication treatment conditions will now be discussed. There were key observations made during visual inspection and electrical characterization which have led to certain conclusions surrounding the treatment combinations investigated. These observations are described, followed by an interpretation on the mechanism(s) involved.

4.2.1 MATERIAL DELAMINATION AND PITTING DEFECTS

4.2.1.1 COPPER/SiO_2 DELAMINATION

The devices fabricated with Ti/Cu as the bottom gate electrode with no annealing done shows large area delamination over copper which can be observed in the Fig 4.2. This occurred during the passivation TEOS PECVD process which was done at 390^oC, and further aggravated by the passivation anneal. This effect on Ti/Cu samples with 400^oC and 600^oC pre-anneal treatments was minimal; it was also minimal on Ti/Cu/Ti treatments.

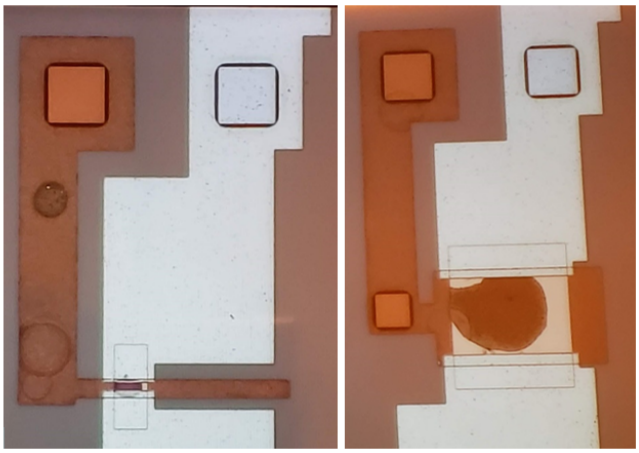


Figure 4.2: Top view of TFT fabricated with Ti/Cu as the bottom gate electrode with no pre-annealing done

Literature supports the enhancement of adhesion between copper and silicon dioxide by annealing [31], done under right circumstances, which appears to be before the IGZO sputter deposition. From the experimentation done, it appears than Ti/Cu samples with 400^oC and 600^oC anneal did not exhibit any delamination as seen in Fig 4.2. All the devices were subjected to passivation dielectric annealing at 400^oC in O_2 ambient after IGZO deposition. This concludes that the bottom gate dielectric anneal plays an important role in the adhesion of SiO_2 to copper.

4.2.1.2 PITTING DEFECTS

Devices with either Ti/Cu or Ti/Cu/Ti gate electrodes that were subjected to pre-annealing at 600^oC exhibited a strange defect effect that was observed only after the passivation anneal, shown in Fig. 4.3. These defects were not observed on samples with no pre-anneal and 400^oC pre-anneal treatments. SEM images as seen in Fig. 4.4 show pitting of the gate electrode film stack appearing to originate from the underlying titanium layer.

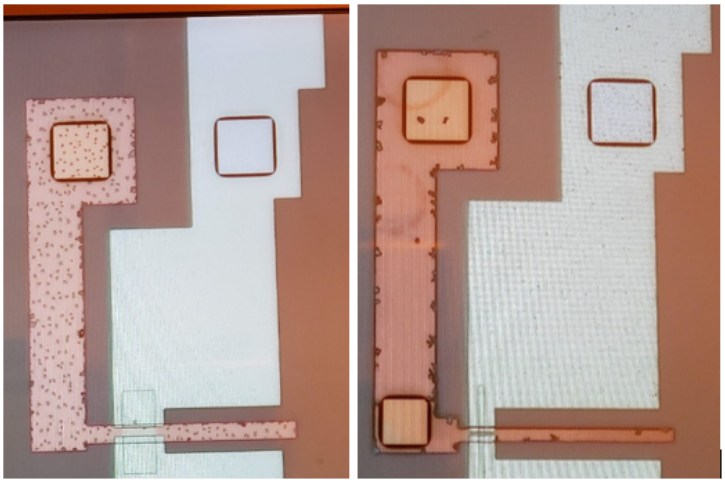
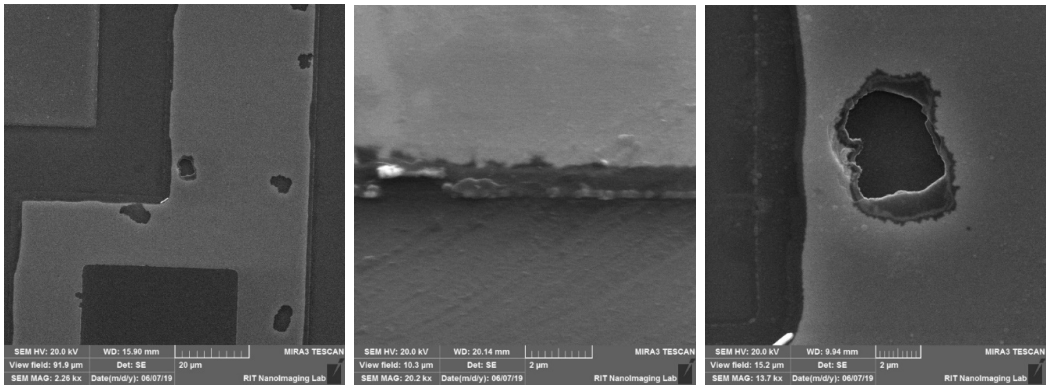


Figure 4.3: Microscopic view of the devices fabricated and annealed at 600^oC a)Ti/Cu and b)Ti/Cu/Ti as the gate electrode stack

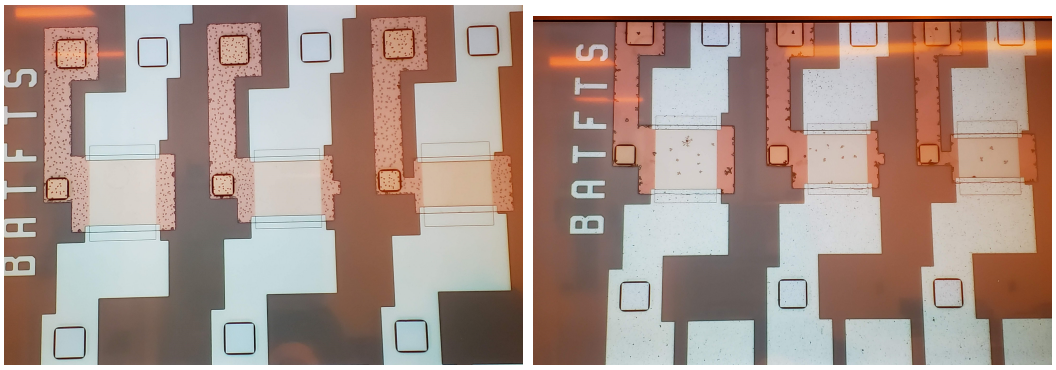


(a) (b) (c)

Figure 4.4: Scanning electron microscopic (SEM) images of defects in the gate stack due to annealing the Ti/Cu/Ti devices at 600^oC a) top view of the gate electrode b) gate stack at 45^o view angle c) defect in the gate electrode.

There is distinct difference in the appearance of the pit defects between the Ti/Cu and Ti/Cu/Ti stacks. The Ti/Cu stack has less pronounced defects uniformly distributed over the electrode area except the channel region, whereas the sample with Ti/Cu/Ti stack shows relatively sparse and pronounced defects that form preferentially at the edge of the gate electrode. The defects are suppressed in the channel region in both the gate metal stacks, however they are notably absent in the channel

region of the sample with Ti/Cu stack. As seen in Fig. 4.5 the Ti/Cu/Ti exhibits visual defects in the channel region of large area channel devices.



(a) (b)

Figure 4.5: Pitting defect distribution of the a) Ti/Cu and the b)Ti/Cu/Ti devices in the large area channel region

The fact that these defects were not observed until the 400^oC O_2 passivation anneal and not immediately following the 600^oC pre-anneal indicates that the origin may be thin-film mechanical stress established as a result of the 600^oC pre-anneal process. These defects may have been apparent after the passivation TEOS deposition done at 390^oC, but the devices are typically not inspected using a microscope between the passivation dielectric deposition and the anneal process. The absence of the defects in the channel region of the Ti/Cu device, and the differences in defect appearance and distribution indicates some interaction with the top Ti layer. Proposed differences in film stress in the channel region could be due to either the IGZO film and/or the overlapping source/drain electrode. It is also observed that there are no defects on the edge of the gate electrode where there is S/D metal overlap, including regions without IGZO present. The pitting mechanism may involve a localized chemical reaction that is stress enhanced or induced. One possible scenario is a reaction of the bottom Ti layer with the underlying SiO_2 during the passivation anneal [32], with suppression in the channel region due to the presence of either the IGZO or the S/D metal. Regardless of the mechanism involved it is clear that pitting defects are

not acceptable, and thus a 600^oC pre-anneal must be avoided.

4.2.2 ELECTRICAL CHARACTERISTICS

The electrical characteristics of devices demonstrated distinct differences between treatment combinations, some of which are directly attributed to the visual defects described. Comparisons of device characteristics are used to provide a comprehensive assessment of each individual treatment. Figure 4.6 shows representative electrical characteristics of five out of the six treatment combinations investigated.

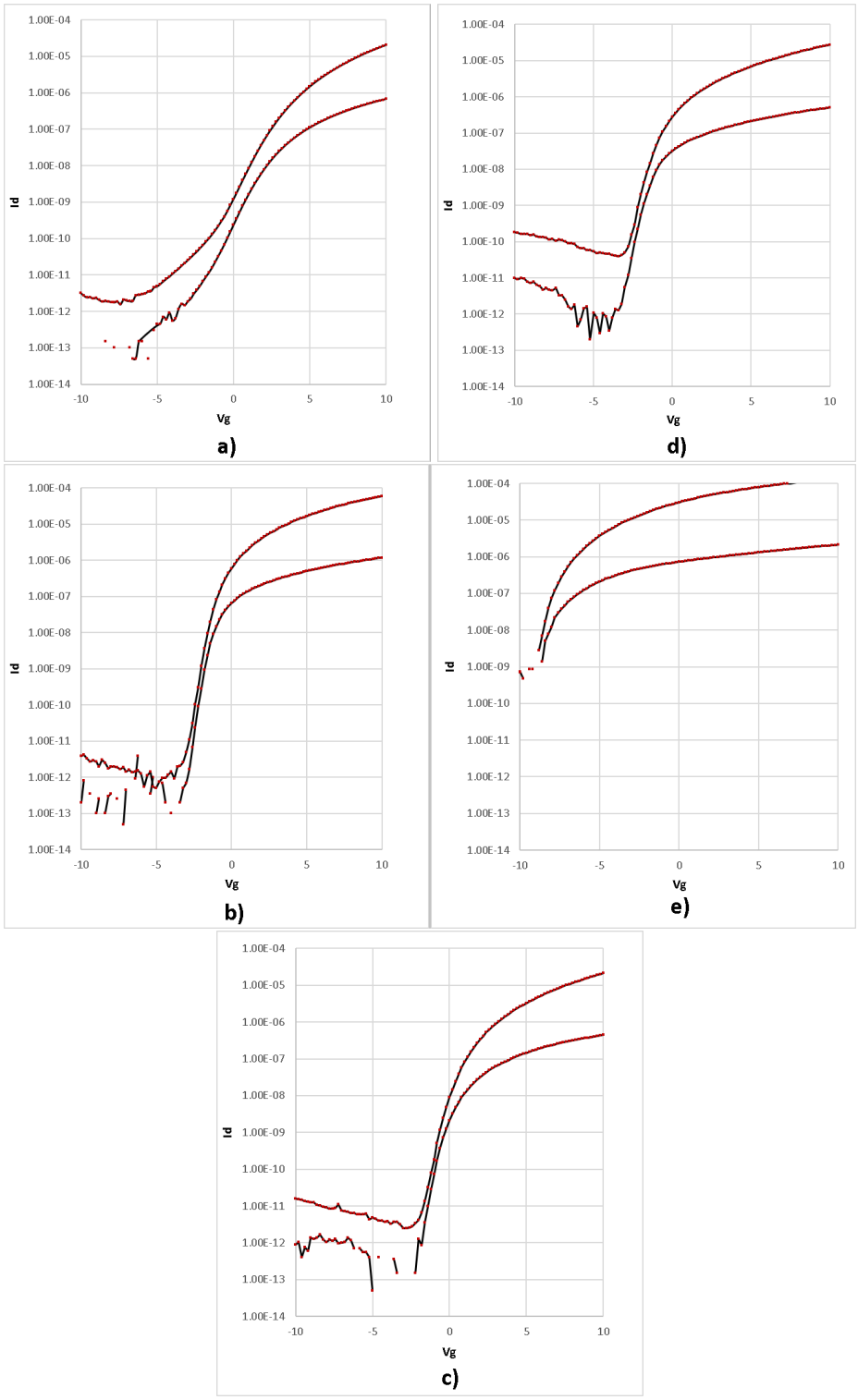


Figure 4.6: Representative electrical characteristics of treatment combinations investigated; all devices are L = 8 μm and W = 24 μm. Note that the Ti/Cu/Ti treatment with 600^oC pre-anneal (TC-6) did not yield operational devices.[a) Ti/Cu with no pre-anneal; b) Ti/Cu with 400^oC pre-anneal; c)Ti/Cu with 600^oC pre-anneal; d)Ti/Cu/Ti with no pre-anneal; e) Ti/Cu/Ti with 400^oC pre-anneal

4.2.2.1 Ti/CU DEVICE OPERATION

Devices from the Ti/Cu sample with no pre-anneal treatment (TC-1) exhibited inferior transfer characteristics in comparison to samples TC-2 and TC-3 that were pre-annealed at 400^oC and 600^oC, respectively. The characteristics were shallow and distorted indicating lack of gate control which may be directly related to the poor interface quality between the Cu gate electrode and the SiO_2 dielectric. The characteristics on pre-annealed Ti/Cu treatments TC-2 and TC-3 were markedly superior. The 600^oC TC-3 pre-anneal treatment is right-shifted in comparison to TC-2, which promotes enhancement-mode operation. Unfortunately this treatment also shows a slightly shallower sub-threshold slope and higher off-state leakage; both of which suggest some influence of Cu contamination. Electrical results have shown that Cu contamination of IGZO devices presents acceptor-like trap states that spread and tilt the transfer characteristics toward the right [35] [36] which is consistent with the electrical characteristics of TC-3.

4.2.2.2 Ti/Cu/Ti

The characteristics on the Ti/Cu/Ti treatment without pre-anneal (TC-4) was notably superior to TC-1, and remarkably similar to TC-2. The subthreshold operation of TC-4 indicated the influence of interface traps, which was not resolved on pre-annealed treatments. Rather, the 400^oC TC-5 pre-anneal treatment was significantly left-shifted, and the 600^oC TC-6 pre-anneal treatment experienced gate-source shorts which resulted in non-functional devices.

4.2.2.3 PITTING DEFECTS AND Ti CONTAMINATION

The pitting defects seemed to have no influence on the electrical characteristics of the Ti/Cu TC-3 devices; however appear to be responsible for the catastrophic gate leakage on Ti/Cu/Ti TC-6. Pitting defects were observed on TC-6 in the channel

regions of large-area devices, whereas they were expressly suppressed on TC-3 which had zero gate shorts. However the short-circuit conditions were also demonstrated by TC-6 on small-area devices which had no observable pitting. Pitting in the channel region and short-circuit behavior may both be associated with the top Ti layer, however the shorting issue may be a response due to Ti contamination rather than pit formation. The TC-5 Ti/Cu/Ti device pre-annealed at 400^oC shows a pronounced left-shift in characteristics compared to the Ti/Cu devices with the same pre-anneal (TC-2) or higher (TC-3), and the Ti/Cu/Ti device with no pre-anneal (TC-4). This result suggests an influence of titanium contamination originating from the gate electrode and diffusing through the gate SiO_2 dielectric to the IGZO channel region [32], eventually leading to device failure at the higher pre-anneal temperature.

4.3 SUMMARY

This chapter has presented research towards adopting copper as the bottom gate electrode for IGZO TFTs. Titanium was used as an interface layer to promote adhesion to SiO_2, and to potentially serve as a barrier to Cu diffusion. Observations and analysis of the experimental results identified distinct differences in physical appearance and electrical response of the treatment combinations investigated. The Ti/Cu treatment without pre-anneal experienced Cu/SiO2 delamination during a subsequent process that was significantly suppressed by gate dielectric pre-annealing prior to IGZO sputter deposition. The Ti/Cu treatments with pre-annealing at 400^oC did not appear to have issues with either delamination or Cu contamination affecting the device operation. The Ti/Cu devices pre-annealed at 600^oC resulted in electrical characteristics that were very similar to the standard molybdenum gate TFT that was pre-annealed at 600^oC, as described in chapter 3 (see Fig. 3.9b). However the shallower sub-threshold slope and distortion are evidence of Cu contaminants. The Ti/Cu/Ti treatment without pre-anneal was operational, however the subthreshold

operation was inferior to pre-annealed Ti/Cu treatments. Pre-annealed Ti/Cu/Ti treatments resulted in characteristics showing either significant left-shifting (400^oC) or gate dielectric failure (600^oC), attributed to Ti contamination. Both metal gate stacks pre-annealed at 600^oC resulted in pitting defects, with associated differences in both visual appearance and electrical response. These defects effectively remove this pre-anneal condition as an option, thus limiting the pre-anneal temperature to not much higher than 400^oC. Unfortunately reducing the pre-anneal temperature to 400^oC appears to result in a compromising characteristic left-shift of 2 V. This is most likely due to oxide charge which is effectively removed during the 600^oC pre-anneal, but remains with process temperature limited to 400^oC.

Chapter 5

CONCLUSION

This chapter will provide a summary of the results and findings in the described study of copper implementation as the bottom gate electrode for IGZO TFTs. The main goal of this study was to investigate the influence of annealing conditions and a titanium capping layer on copper integration and potential channel contamination. An experimental design was defined with factor settings that took into consideration the standard process conditions and the likelihood of promoting an electrical response to metallic contaminants (i.e. V_T shift, SS, distortion) into consideration. To ensure that the electrical interpretation was not influenced by process variation or instability, a baseline process had to be re-established which involved adjustments in the PECVD SiO_2 passivation oxide thickness and the process recipe for the subsequent O_2 passivation anneal at 400^oC. This effort resulted in operating characteristics consistent with previous work [21], as represented in Fig. 5.1. The devices also exhibited good resistance to thermal and bias stress testing.

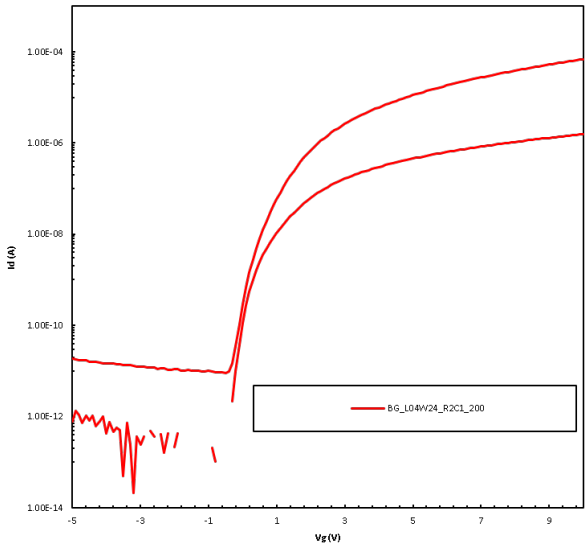


Figure 5.1: Electrical characteristics of a Mo bottom gate passivated device of L/W=4/24 μm with 50nm IGZO and 50 nm passivation dielectric (SiO_2) annealed in O_2 ambient at 400^oC for 3hrs with a 2hr ramp down in O_2

The experimental design that was used for this study identified distinct differences in physical and electrical responses over all treatment combinations. First and foremost was the response of material adhesion between the metal gate electrode and the gate SiO_2 dielectric. The only conditions that experienced significant delamination was the Ti/Cu stack without a pre-anneal prior to IGZO sputter deposition. This resulted in low device yield, and compromised electrical operation on devices that remained intact. The Ti/Cu/Ti stack devices did not have issues with delamination; thus the use of Ti as a capping layer over Cu was successful in that regard. However the application of Ti at the interface to the gate dielectric demonstrated issues with Ti contamination, having a profound impact on pre-annealed devices that was not experienced by the Ti/Cu stack devices. Thus an alternative interface layer should be considered such as refractory nitrides (e.g. TiN, TaN) that are commonly used as Cu diffusion barrier layers in back-end IC fabrication [37], or a metal with proven gate electrode properties such as molybdenum. Pre-annealing the gate dielectric on Ti/Cu devices had benefits in both material adhesion and device operation. Both

pre-anneal conditions demonstrated good adhesion, thus the 400^oC treatment was a sufficient temperature for that specific purpose. In addition, the 400^oC pre-anneal treatment (TC-2) demonstrated steep subthreshold operation indicating a reduction in interface traps in comparison to the Ti/Cu/Ti device without pre-anneal (TC-4), shown in Fig. 5.2. Having this pre-anneal performed prior to IGZO and the passivation oxide deposition seems important, considering that the passivation anneal is also done at 400^oC for an extended time period. Considering the similarity between TC-2 and TC-4, issues with Cu or Ti contamination in either of these samples appear unlikely.

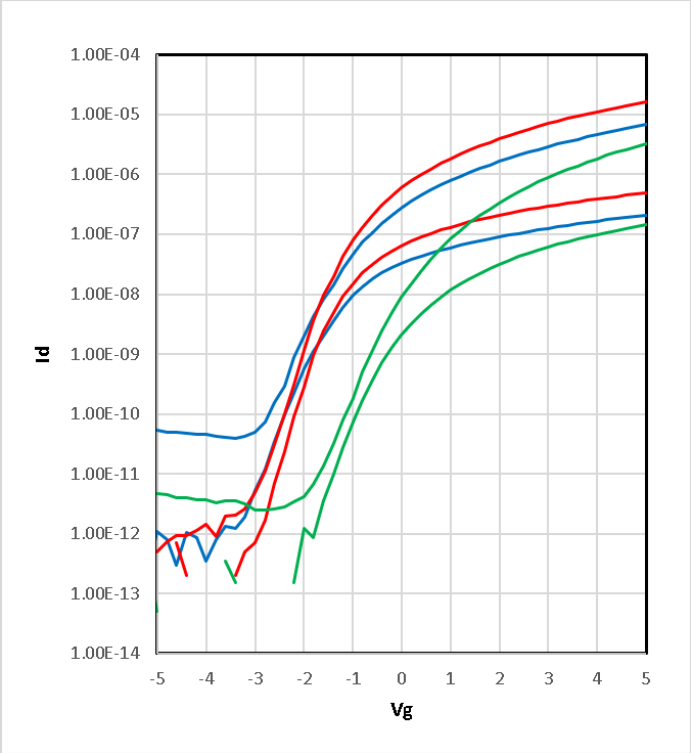


Figure 5.2: Transfer characteristic overlay of select treatment combinations. Comparisons between TC-4 (blue diamond, shallow subthreshold), TC-2 (red squares, steep subthreshold) and TC-3 (green circles, right-shifted) are made in the narrative.

The Ti/Cu 600^oC pre-anneal treatment (TC-3) had a shallower subthreshold, however was right shifted by 1 V from the 400^oC anneal, indicating a reduction in fixed charge or bulk oxide charge that requires the higher temperature process. The

origin of the compromise in subthreshold operation is possibly due to Cu contamination, which has been shown to degrade electrical characteristics in an equivalent manner[35]. Regardless, it was established that 600^oC would not be an option for the pre-anneal process due to pitting that occurred on the gate electrode, potentially contributing to zero yield on the Ti/Cu/Ti device. Alternative gate dielectric and pre-anneal options must be considered to provide lower charge levels while maintaining a temperature limit of 400^oC, and demonstrate comparable performance as the baseline device shown in Fig. 5.1.

References

[1] S. J. Hong, S. Lee, H. J. Yang, H. M. Lee, Y. K. Ko, H. N. Hong, H. S. Soh, C. K. Kim, C. S. Yoon, K. S. Ban, and et al., "Effects of the dissolved oxygen in ti films on ti reactions in cu/ti/sio2/si system upon annealing," *Semiconductor Science and Technology*, vol. 19, no. 11, 2004.

[2] "New generation 10 fabs enable bigger, brighter, better tv displays." [Online]. Available: http://www.appliedmaterials.com/nanochip/nanochip-fab-solutions/july-2018/new-generation-10-fabs-enable-bigger-brighter-better-tv-displays

[3] "Understanding today's lcd screen technology," Aug 2017. [Online]. Available: https://pid.samsungdisplay.com/en/learning-center/blog/lcd-structure

[4] Elsevier, "Active matrix liquid crystal display," *1st Edition*, Sep 2005. [Online]. Available: https://www.elsevier.com/books/active-matrix-liquid-crystal-displays/den-boer/978-0-7506-7813-1

[5] "Active matrix organic light emitting diode," Jul 2019. [Online]. Available: https://en.wikipedia.org/wiki/AMOLED

[6] T. Matsuo, S. Mori, A. Ban, and A. Imaya, "8.3:invited paper: Advantages of igzo oxide semiconductor," *SID Symposium Digest of Technical Papers*, vol. 45, no. 1, p. 8386, 2014.

[7] T. Kamiya, K. Nomura, and H. Hosono, "Subgap states, doping and defect formation energies in amorphous oxide semiconductor aingazno4 studied by density functional theory - kamiya - 2010 - physica status solidi (a) - wiley online library," *physica status solidi (a)*, May 2010. [Online]. Available: https://onlinelibrary.wiley.com/doi/full/10.1002/pssa.200983772

[8] H. Hosono, "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application," *Journal of Non-Crystalline Solids*, vol. 352, no. 9-20, 2006.

[9] T.-C. Fung, "Amorphous in-ga-zn-o thin film transistor for future optoelectronics," 2010. [Online]. Available: https://deepblue.lib.umich.edu/bitstream/handle/2027.42/75856/tcfung_1.pdf

[10] "The kanicki laboratory - displays and detectors." [Online]. Available: http://vhosts.eecs.umich.edu/omelab//publications/index.html

[11] J. Kanicki, "Amorphous ingazno dual-gate tfts: Currentvoltage characteristics and electrical stress instabilities," *IEEE Transactions on Electron Devices*. [Online]. Available: https://www.academia.edu/18014374/

Amorphous_In_and_x2013_Ga_and_x2013_Zn_and_x2013_O_Dual-Gate_TFTs_Current_and_x2013_Voltage_Characteristics_and_Electrical_Stress_Instabilities

[12] H.-H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C.-C. Wu, "Modeling of amorphous ingazno4 thin film transistors and their subgap density of states," *Applied Physics Letters*, vol. 92, no. 13, 2008.

[13] "Electronic structures above mobility edges in crystalline and amorphous ingazno: Percolation conduction examined by analytical model - ieee journals magazine," *O*. [Online]. Available: https://ieeexplore.ieee.org/document/5331948/

[14] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous in-ga-zn-o thin-film transistors," *Science and technology of advanced materials*, Sep 2010. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC5090337/

[15] T. Mudgal, N. Walsh, N. Edwards, R. G. Manley, and K. D. Hirschman, "Interpretation of defect states in sputtered igzo devices using i-v and c-v analysis," *ECS Transactions*, vol. 64, no. 10, 2014.

[16] "Display market," Tech. Rep., September 2018. [Online]. Available: https://www.marketsandmarkets.com/PressReleases/display.asp

[17] "Comprehensive review on the development of high mobility in oxide thin film transistors." [Online]. Available: https://www.researchgate.net/publication/320549843_Comprehensive_review_on_the_development_of_high_mobility_in_oxide_thin_film_transistors

[18] "Sharp global." [Online]. Available: http://www.sharp-world.com/igzo/

[19] K. D. Hirschman, T. Mudgal, E. Powell, and R. G. Manley, "A 2d empirical model for on-state operation of scaled igzo tfts exemplifying the physical response of tcad simulation," *ECS Transactions*, vol. 86, no. 11, 2018.

[20] K. Nomura, T. Kamiya, E. Ikenaga, H. Yanagi, K. Kobayashi, and H. Hosono, "Depth analysis of subgap electronic states in amorphous oxide semiconductor, a-in-ga-zn-o, studied by hard x-ray photoelectron spectroscopy," *Journal of Applied Physics*, vol. 109, no. 7, 2011.

[21] T. Mudgal, N. Edwards, P. Ganesh, A. Bharadwaj, E. Powell, M. S. Pierce, R. G. Manley, and K. D. Hirschman, "Investigation on the gate electrode configuration of igzo tfts for improved channel control and suppression of bias-stress induced instability," *ECS Transactions*, vol. 75, no. 10, 2016.

[22] E. P. Powell, "The infuence of alternative electrode configurations and process integration schemes on igzo tft operation," 2017.

[23] N. R. Edwards, "Engineering sio2 passivated indium-gallium-zinc-oxide tfts for improvement in channel control," 2016.

[24] "An amorphous oxide semiconductor thin-film transistor route to oxide electronics," Tech. Rep., Jul 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1359028613000491

[25] P. Ganesh, "Investigation of thermal stress degradation of indium gallium-zinc oxide tfts," 2017. [Online]. Available: https://scholarworks.rit.edu/cgi/viewcontent.cgiarticle$=$10798&context=theses

[26] Y. Hara, T. Kikuchi, H. Kitagawa, J. Morinaga, H. Ohgami, H. Imai, T. Daitoh, and T. Matsuo, "Igzotft technology for largescreen 8k display - hara - 2018 - journal of the society for information display - wiley online library," Apr 2018. [Online]. Available: https://onlinelibrary.wiley.com/doi/full/10.1002/jsid.648

[27] "Improvement in device performance of a-ingazno transistors by introduction of ca doped cu sourcedrain electrode." [Online]. Available: https://www.researchgate.net/publication/280353816_Improvement_in_Device_Performance_of_a-InGaZnO_Transistors_by_Introduction_of_Ca-Doped_Cu_SourceDrain_Electrode

[28] T. O. et al., "large-electromigration-resistance copper interconnect technology for sub-half-micron ulsi's."

[29] D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. Mcdevitt, W. Motsiff, A. Simon, and et al., "Full copper wiring in a sub-0.25 m cmos ulsi technology," *International Electron Devices Meeting. IEDM Technical Digest.*

[30] C. W. Wu, S. Y. Yoo, C. Ning, W. Yang, G. L. Shang, K. Wang, C. H. Liu, X. Liu, G. C. Yuan, J. Chen, and et al., "10.4: Improvement of stability on aigzo lcd - wu - 2013 - sid symposium digest of technical papers - wiley online library," Jul 2013. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/j.2168-0159.2013.tb06150.x

[31] "Effects of annealing and interlayers on the adhesion energy of copper thin films to sio2/si substrates," Dec 1998. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1359645498002778

[32] e. a. Russell, S.w., "Enhanced adhesion of copper to dielectrics via titanium and chromium additions and sacrificial reactions," 1995.

[33] S. J. Hong, S. Lee, H. J. Yang, H. M. Lee, Y. K. Ko, H. N. Hong, H. S. Soh, C. K. Kim, C. S. Yoon, K. S. Ban, and et al, "Effects of ti thickness on ti reactions in cu/ti/sio2/si system upon annealing," 2002.

[34] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structure of the amorphous oxide semiconductor aingazno4x : Tauclorentz optical model and origins of subgap states - kamiya 2009 physica status solidi (a) - wiley online library," *physica status solidi (a)*, Apr 2009. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.200881303

[35] Liu, Xiang, Wang, L. Ling, Ning, Yang, Wei, Wang, Ke, Yoo, and et al., "Gate bias stress-induced threshold voltage shift effect of a-igzo tfts with cu gate," *IEEE Transactions on Electron Devices*, Dec 2014. [Online]. Available: http://adsabs.harvard.edu/abs/2014ITED...61.4299L

[36] C. K. Lee, D. Y. In, D. J. Oh, S. H. Lee, J. W. Lee, and J. K. Jeong, "Ca-doped cuo diffusion barrier for high-performance a-igzo transistors with cu-based source/drain material," *IEEE Transactions on Electron Devices*, vol. 65, no. 4, p. 13831390, 2018.

[37] e. a. Baumann, J., "Tin diffusion barriers for copper metalization," 1997.

[38] "An amorphous oxide semiconductor thin film transistor route to oxide electronics," Jul 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1359028613000491

[39] S. D. Brotherton, *Introduction to Thin Film Transistors Physics and Technology of TFTs*. Springer International Publishing, 2013.

[40] T. Mudgal, "Interpretation and regulation of electronic defects in igzo tfts through materials and processes," 2017. [Online]. Available: http://scholarworks.rit.edu/cgi/viewcontent.cgi?article$=$10712&context$=$theses

[41] T. Matsuo, S. Mori, A. Ban, and A. Imaya, "8.3: Invited paper: Advantages of igzo oxide semiconductor - matsuo - 2014 - sid symposium digest of technical papers - wiley online library," *SID Symposium Digest of Technical Papers*, Jul 2014. [Online]. Available: http://onlinelibrary.wiley.com/doi/10.1002/j.2168-0159.2014.tb00023.x/abstract