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Etching Processes for GaN Nanowire Fabrication and Single Photon Emitter Device Application

Gildas Ouin
gxo8434@rit.edu

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Gildas Ouin

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Approved by:

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Dr. Jing Zhang, *Thesis Advisor*

_____

Dr. Karl Hirschman

_____

Dr. Santosh Kurinec

_____

Dr. Parsian Mohseni

_____

Dr. Robert Pearson, *Program Director*

DEPARTMENT OF ELECTRICAL AND MICROELECTRONIC ENGINEERING

KATE GLEASON COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

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Abstract

As they have exhibited great potential for light emitting devices, Gallium Nitride (GaN) nanowire (NW)-based devices have attracted a lot of interest over recent years. Ultra-thin GaN NWs can be used to manufacture many novel devices for future communication and encryption systems, such as single photon emitters (SPEs). However, the conventional growth techniques have limitations in terms of manufacturability, creating the need to explore top-down, etch reliant GaN NW fabrication processes.

This work focuses on improving the fabrication methods for top-down GaN nanowires and lay out a potential process for the manufacturing of SPEs. Using a combination of dry and wet etching, the existing process for top-down GaN nanowire fabrication was improved to achieve features with a sub 50nm diameter. An initial process for SPE manufacturing is proposed and an electrochemical etch setup is introduced to broaden the processing capabilities and applications. Preliminary experiments for these new processes show promising results.

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Glossary

DI: De-Ionized

EC: Electrochemical

GaN: Gallium Nitride

HBT: Hanbury-Brown and Twiss

MBE: Molecular Beam Epitaxy

MOVPE: Metal-Organic Vapor Phase Epitaxy

NW: Nanowire

PL: Photoluminescence

QD: Quantum Dot

SEM: Scanning Electron Microscopy

S/MQW: Single/Multiple Quantum Well

SPE: Single Photon Emitter

UV: Ultra-Violet

Chapter 1: Introduction

Optoelectronics is an ever-increasing area of research. Over the past century, it has revolutionized many aspects of everyday life and applications such as lighting, displays or telecommunications which play a major role in society. There is also a large potential in future use of optoelectronic devices for quantum information science. Advancements in these areas may be an essential step towards rendering our communications faster and more secure as well as meeting the growing need for more efficient displays and connected devices.

Optoelectronic devices rely on the ability of materials to emit light under certain conditions. Semiconductors, when electrically stimulated, can give off light of varying wavelength depending on material properties. III-Nitride semiconductors, particularly Gallium Nitride have shown tremendous potential for light-emission, translating into revolutionary applications in solid state lighting and telecommunications [1] [2]. This is due to multiple properties, such as a tunable wavelength of emission, making III-Nitride materials versatile [3]. These materials can be shaped in the form of nanowires to increase light extraction, making nanowire fabrication a rapidly growing technique for GaN-based optoelectronics [4].

Over the past few decades, a type of optoelectronic device known as single-photon emitter (SPE) has been increasingly studied due to its important potential for quantum communications, quantum cryptography, and more [5] [6]. While SPEs can be manufactured in many different ways, a recently explored fabrication method has been the use of GaN nanowires [7]. A lot of progress has been achieved using bottom-up (growth) fabrication [8] [9]. However, not much has been done with regards to top-down applications relying on patterning and etching. The top-down approach has the advantage of creating similar structures for a smaller cost and with a more easily-achieved uniformity [10]. Therefore, exploring this avenue for GaN NW-based SPEs could be highly beneficial.

However, GaN is a particularly hard material to process. There are several issues such as the difficulty of etching. For GaN to reach its full potential for not just SPEs but all nanoscale light emitting devices, a heavy focus on processing is necessary.

The purpose of this work is to optimize etching processes for the fabrication of very thin (sub 50nm) GaN nanowires. Expanding upon existing fabrication methods using nanosphere lithography, dry and wet etching, the goal is to find ideal process conditions to obtain thinner NWs with top-down fabrication and use them for nanoscale devices such as single photon emitters. In parallel, an electrochemical etching set-up is introduced to the facilities in order to achieve a conductivity selective etch of GaN. This process has a lot of potential for applications requiring a porous or smooth etching of regions with higher conductivity and will be studied for potential lift-off applications.

Chapter 2: Background and theory

Understanding the work performed here requires a review of a few different aspects of GaN. This section first focuses on the intrinsic properties of GaN and semiconductor physics for light emitting devices. Then, dry and wet etching processes as they apply to GaN are reviewed. Finally, an overview of the process is provided.

2.1 Gallium nitride

As mentioned in the introduction, GaN is a particularly interesting material for optoelectronics and it has been a popular choice for novel applications. To understand why, its basic characteristics must first be laid out.

GaN is a III-V semiconductor, which means it is composed of a combination of triels and pnictogens (elements from the 13th and 15th column of the periodic table, respectively). A semiconductor is a material that can behave like an insulator or a conductor depending on electrical parameters. They can be obtained from single elements with four valence electrons or by combining materials.

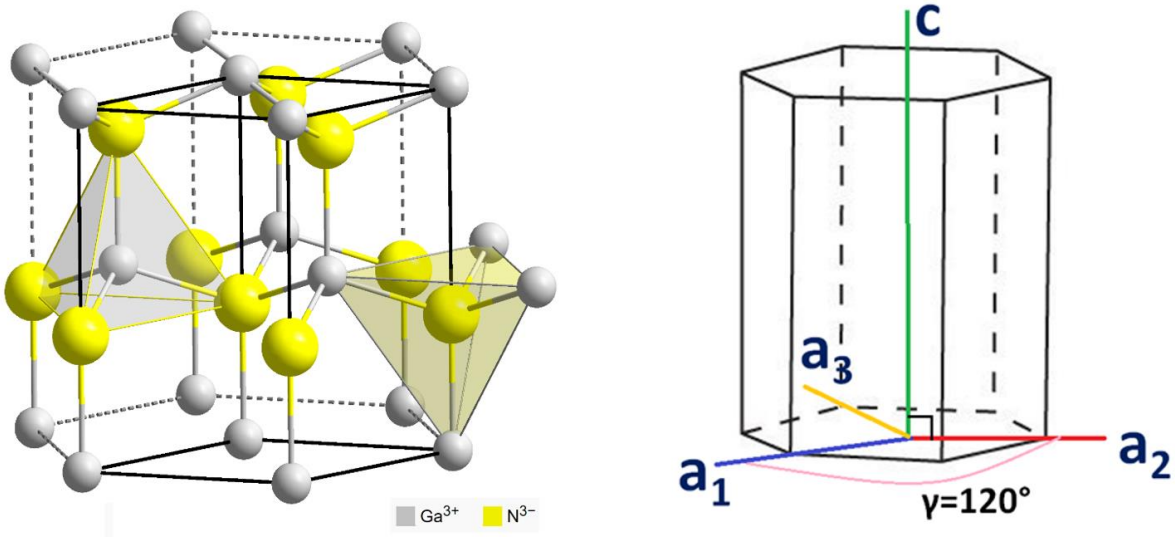

Figure 1: GaN arranged in a Wurtzite structure [102] (left), hexagonal crystal lattice [111] (right)

If triels and pnictogens are mixed, it results in an electronic imbalance between the elements, as the pnictogens provide extra electrons while triels provide fewer electrons (or extra holes). This

generally results in materials with higher electrical mobility, making III-V semiconductor compounds an excellent choice for high speed applications [11].

GaN typically has a wurtzite crystal structure with a hexagonal lattice, as shown in Figure 1. It has been deemed difficult to etch, with a binding energy of 8.9 eV/atom, compared to the much lower value shown for other materials such as Silicon with a binding energy over three times as low [12].

For optoelectronics, GaN also has a major advantage: it is a direct bandgap semiconductor. Carriers (electrons and holes) in semiconductor materials tend to occupy energy levels located in the valence band or the conduction band, which are separated by a region of unallowed states referred to as the bandgap. In order for electrons to be excited from the low-energy levels of the valence band to the conduction band, an energy input is required [13]. Similarly, when electrons relax from the conduction band to the valence band, energy must be released. In the case of direct bandgap semiconductors, this energy is released in the form of photons (light particles). If a material has an indirect bandgap, then only part of this energy is emitted as photons, the rest being released as phonons, quasiparticles representing excitation of the lattice [14]. GaN being a direct bandgap material, it is much more efficient for light emission than any indirect bandgap semiconductor such as Silicon or Germanium.

GaN also has a particularly wide bandgap of approximately 3.4eV [15]. The wavelength of a light emission created by carrier recombination is inversely proportional to the bandgap energy. It is determined by the following formula:

$$E = \frac{hc}{\lambda} \tag{1.1}$$

Where E is the energy, h is Planck's constant and c is the velocity of light. Compared to the other direct bandgap semiconductor such as GaAs (with a bandgap of 1.42eV [16]), GaN can emit light at a lower wavelength. This means that UV emission, which has many applications in terms of telecommunications, sensors and more, is easily achieved with GaN [17] [18].

When adding other materials to a semiconductor material to create an alloy, it is possible to customize the bandgap of the resulting compound. In the case of GaN, the addition of elements such as Indium and Aluminum allow for bandgap optimization. By varying the composition of the alloy, the semiconductor bandgap and thus the emission wavelength can be changed. This customization allows GaN-based devices to emit light with wavelengths ranging from infra-red to the deep UV region. The latter is particularly useful due to all the aforementioned applications for UV light emission. The different wavelength available for III-Nitride compounds are shown in Figure 2.

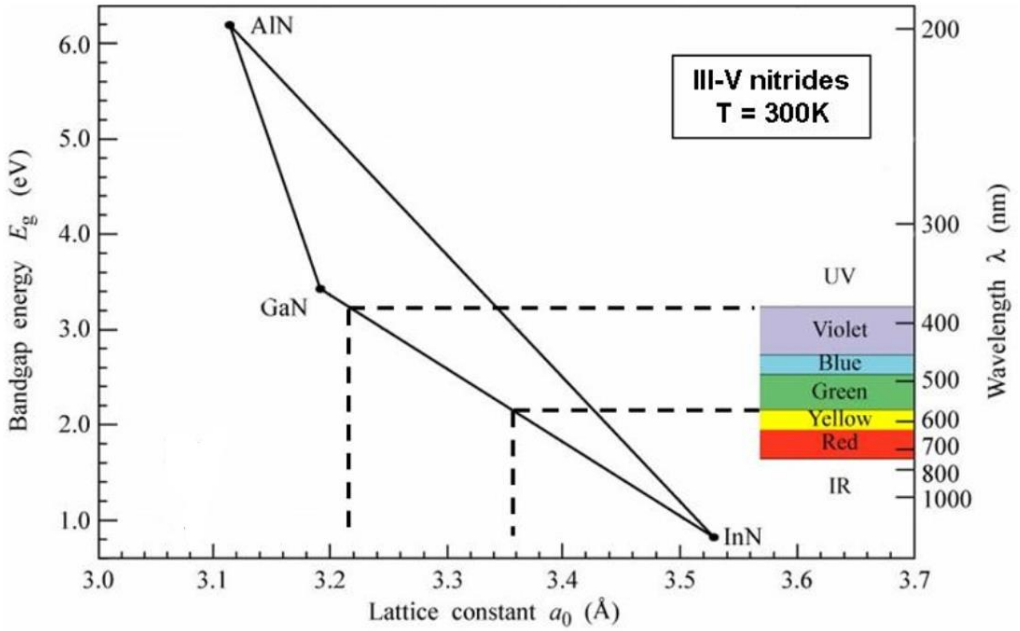

Figure 2: Bandgap variation as a function of lattice constant for different III-Nitride alloys [3]

The combination of high mobility, direct bandgap and wide bandgap makes GaN a very powerful material for optoelectronic applications. However, to unlock its full potential, there is a need for shape optimization.

2.2 LED structures

To extract light from III-Nitride materials, a specific structure must be used. Diodes are typically formed by creating a pn junction. This is done by juxtaposing a semiconductor doped with elements with fewer valence electrons/more holes (p-doped) or additional valence electrons (n-doped). When current flows through the junction, the electrons in the n-region can flow towards the p-region and

recombine with the holes. As mentioned previously, the recombination process can result in light emission.

Light emitting diodes are based on this principle, usually with the addition of quantum wells at the interface between the n and p region. Quantum wells are created by alternating thin layers of semiconductor with different bandgaps, resulting in a confinement of the carriers to certain energy levels. The location of the energy levels in quantum well is defined partly by the well's width, which allows for tunability of the energy differences, thus of the wavelength of the emission. Quantum confinement also offers higher efficiencies, due to the stepwise density of state observed in quantum wells. This step variation results in lower noise and better recombination at the desired level, since only specific energy states are available [19].

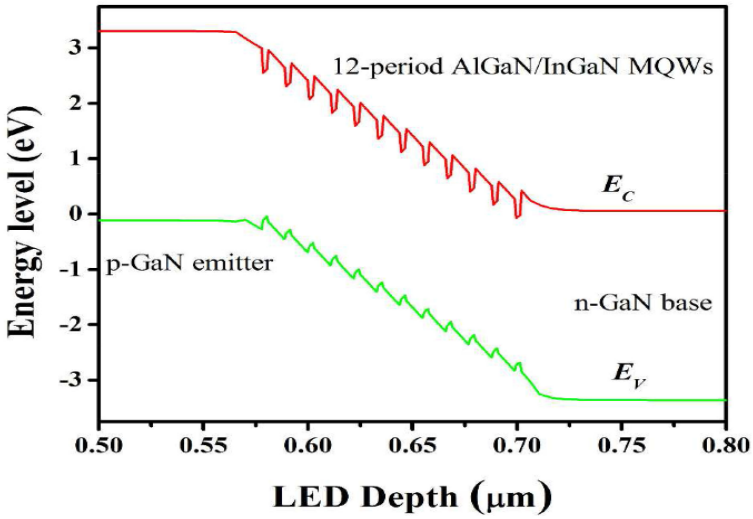

Figure 3: Band structure of a standard GaN-based LED device [106]

The conventional structure for a GaN LEDs is a layer of p-GaN, a layer of multiple quantum wells (MQWs), a layer of n-GaN and a layer of u-GaN (unintentionally doped GaN due to diffusion of dopants from the n-GaN layer) on a sapphire substrate.

If a planar structure is used, a large portion of the light emitted by the active region cannot be collected due to optical loss phenomena such as reflection. This creates a need to optimize the device's shape. If the material is patterned with small cylinders in the shape of wires instead, a higher surface area is available, which allows for more efficient light extraction. If the features are sufficiently small,

they are referred to as nanowires (NWs). NWs have shown tremendous potential for state-of-the-art optoelectronics [4].

NWs are generally fabricated in one of two ways: bottom-up or top-down [20]. The bottom-up method relies on growing the materials on a substrate. The two main ways to grow GaN are Molecular Beam Epitaxy (MBE) and Metal-Organic Vapor Phase Epitaxy (MOVPE, sometimes called MOCVD for Metal-Organic Chemical Vapor Deposition). Epitaxy works by slowly growing a crystal film over a crystal substrate, building upon the previous lattice.

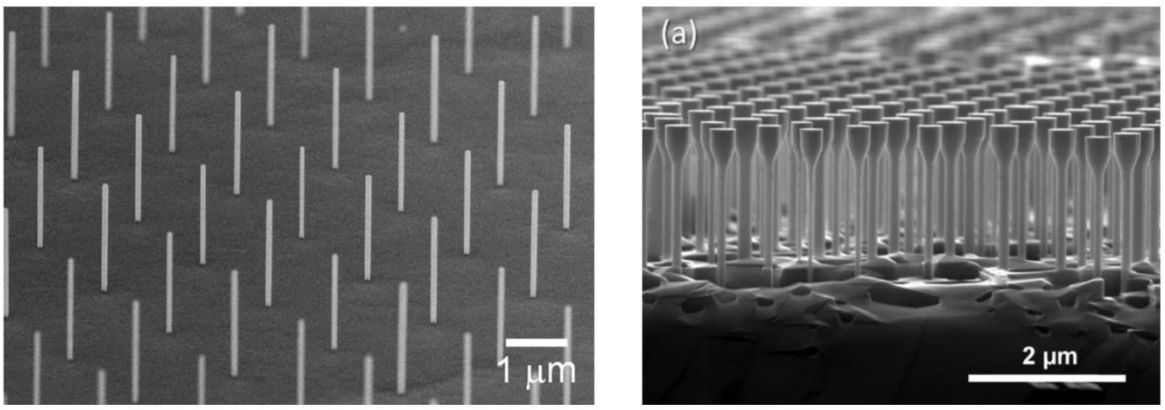

Figure 4: Bottom-up(left) [107] and top-down (right) [108] GaN NWs

Selective area growth is typically achieved by using a dielectric/oxide mask, where the growth only occurs on the substrate and not on the mask. This allows for the growth of wires if the proper mask is used.

However, there are several issues with bottom-up fabrication, both in terms of materials and processes. Due to the large set-ups it requires, NWs growth tends to be much more expensive and necessitate more manpower. This processing method is therefore less accessible for smaller scale facilities. There are also problems that may arise on the materials side. During growth, there is a chance that the NWs will be grown with a higher density than desired and merge into islands if selective area epitaxy is not used or in the presence of defects [21]. Due to the nature of the controlled growth, epitaxy is also a very slow process. This slowness constitutes an obstacle for producing larger volumes, making the transition from research-scale operations into mass manufacturable devices difficult. Moreover, parameters used for GaN growth, especially the low temperature used to favor a higher quality NWs, make the final sample prone to a higher defect density and impurities contamination [22] [23].

On the other hand, top-down fabrication relies on selectively etching parts of the structure to obtain NWs. Using top-down manufacturing will circumvent the previously mentioned growth-related issues [24]. Additionally, top-down fabrication can be set-up for a much lower cost, since it does not rely on epitaxy equipment.

2.3 Process summary

To fabricate GaN NWs, top-down manufacturing can be performed using a simple combination of dry and wet etching. In order to carve a wire shape in the material, certain areas must be protected before an anisotropic etch is performed. This unidirectional carving of the material is done using a plasma-based dry etching process. Dry etching does not, however, result in a perfect wire shape. The fabrication can be completed by using a subsequent wet etch step. Figure 5 details each step of the process used in this work.

The structure depicted is akin to the one used for testing fabrication processes in the upcoming chapters of this work. The lack of a p-doped GaN layer means it will not function as an LED. However, for processing intents, the structure is adequate and will yield identical results to a full p-GaN/MQW/n-GaN structure. For the purpose of this work, the initial flat structure is grown by external organizations using MBE.

The original wafer is first treated with an O_2 plasma and coated with SiO_2 spheres. It is then dry etched using a $Cl_2/Ar/CHCl_3$ plasma. Finally, the sample is subjected to a wet etch step in KOH with time/temperature/concentration condition suited to the needs of the application. The process detailed here is the foundation of GaN fabrication and was developed earlier and characterized by other members of the group. [25] The main objective of this work is to expand on the capabilities of this process to create ultra-thin NWs and lay-out the fabrication process for devices such as SPEs.

In the following sections, each step will be detailed to provide a complete understanding of the fabrication process.

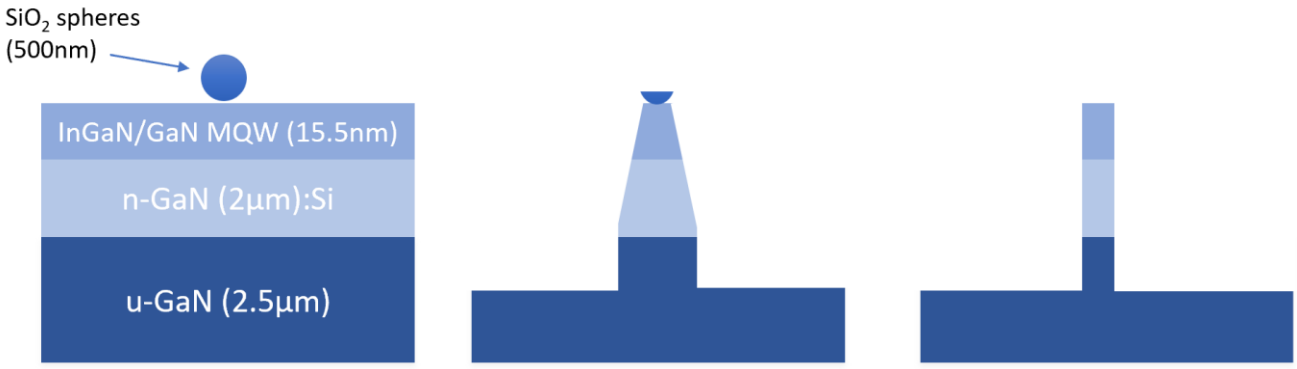

Figure 5: Summary of the NW fabrication process: nanosphere deposition (left), Cl2-based RIE (middle), KOH wet etch (right)

2.4 Nanosphere lithography

To create a NW shape through etching, certain areas of the sample must be protected, such that a vertical etch leaves pillars of materials on the surface.

Conventionally, surfaces are protected during etches by using a hard mask combined with photolithography. However, photolithography has its drawbacks. Its resolution can be increased by reducing exposure wavelength. This comes with additional processing challenges. [26] Moreover, light-diffraction also causes limitations in the resolution. [27] While these limitations have been overcome and photolithography is used to create features down to 10nm, these improvements come with extra processing steps and require capabilities that are harder to access for small-scale facilities. As such, photolithography may not be an ideal way of achieving this and another faster, cheaper patterning method can be explored.

Creating a protective layer for wire formation can be done with the use of nanosphere lithography [28]. Instead of relying on light exposure to pattern resists, small silicon dioxide spheres can be coated over a sample. An easy way to deposit the spheres is through spin coating, ensuring the surface of the sample is coated evenly. By using the right plasma for dry etching (see section 2.4 for more details), GaN can be etched much faster than SiO_2, resulting in the spheres acting like a hard mask.

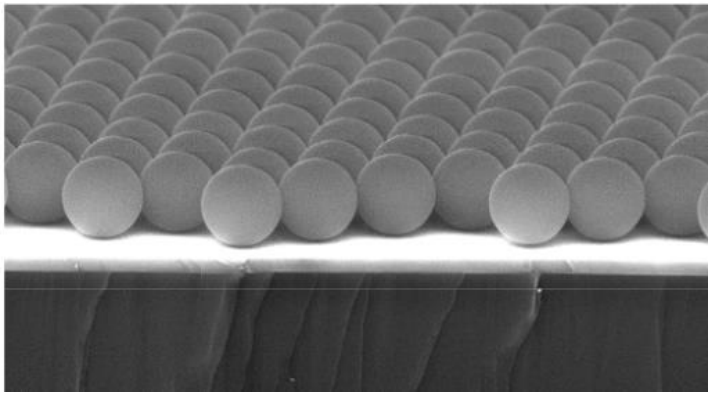

Figure 6: Silica spheres spin coated onto a GaN sample [24]

A commercially available solution of SiO_2 spheres suspended in liquid can be spin coated on the sample. For the spheres to stick to the surface, the surface of the sample must be hydrophilic. Nitride compounds, including GaN, tend to be naturally hydrophobic and creating a hydrophilic surface from these materials can be challenging [29]. However, it is possible to change the surface properties of the sample through an O_2 based plasma. The treatment creates a thin layer of oxide that allows the aqueous sphere solution to stick to the surface. This GaN oxide is weak and does not impact the functioning of the device as it will easily be removed during subsequent processing steps.

2.5 Dry etching

Dry etching relies on the principle that surfaces can be etched by generating a physical ion bombardment on a material. This creates a displacement at the top of the sample surface, resulting in a removal of the top layers of the material.

In order to create the ions, a plasma must be generated. This can be done by introducing an inert gas in a chamber containing the sample attached to a cathode and an anode at the opposite part of the chamber. By introducing a bias between the two electrodes, free electrons will collide with the gas molecules to form ions, turning the gas into a plasma [30]. The electrons will keep flowing towards the anode, creating more free radicals. These ions will flow towards the opposite direction. As they strike the cathode, atoms will be physically dislodged resulting in the etching of the surface. A transfer of momentum occurs, resulting in the formation of secondary electrons. These newly created charges are used to replenish the flow of electrons, thus sustaining the plasma in the process [31].

However, if the material used as a cathode is insulating, then no secondary electrons will be supplied. To circumvent that, some etching systems rely on the use of alternative current. By flipping the polarity of the electrodes, the electrons will oscillate and produce free radicals much more efficiently.

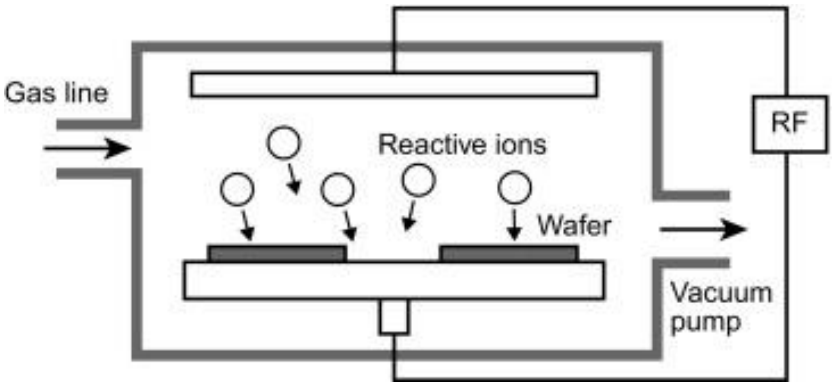

Figure 7: Representation of a simple plasma etcher [110]

As the ions are hitting the surface of the sample unilaterally, the etch can be effectively described as anisotropic, in that it only strips away atoms in one direction. It is generally useful for creating features with a high aspect ratio, making dry etching a particularly useful technique for nanowire formation. However, for better etching and directionality, another form of etching can be used: Reactive Ion Etching (RIE) [32]. It relies on combining the dry etching method previously described with chemical reactions in order to perform a more efficient etch. RIE is particularly useful for a material like GaN, since it is a difficult material to etch.

To apply this type of etching to GaN, several different gas combinations can be used. The most common etchant for GaN are Cl_2/Ar and Cl_2/BCl_3. [33] The combination of gas used depends on the specificity of the desired application. For instance, the addition of BCl_3 to Cl_2 will result in a better anisotropy of the etch [34]. A Cl_2/Ar combination will result in a fast etch rate, valuable to counteract the resilience of GaN to etching.

Chloroform ($CHCl_3$) can be introduced for additional chemical etching. It can be used to protect against part of the sidewall damage. It also creates a polymer build-up around the wire, as the $CHCl_3$ deposits everywhere but amass at the base. This accumulation creates a cone shape.

However, this type of etch can still create damage in the sample. Dry etching often results in the formation of non-radiative recombination centers. These surface defects can have a negative impact of LED performances with regards to markers such as quantum efficiency [24]. Other GaN-based devices have been shown to have increased gate leakage current by up to 6 orders of magnitude and decrease drive current by up to 15% when the dangling bonds created by the etch are not passivated [35]. This is especially a problem for NWs, which have small diameters. Thinner NW (below 80nm) LEDs will be especially affected, as increased recombination is observed at the surface, caused by Fermi level pinning [36]. The combination of surface states, surface Fermi level pinning effects and non-radiative recombination level effects can heavily impact the efficiency of light emitting devices [37]. This means that after being dry etched, the sample will most likely show performances-altering defects that will need to be corrected at a later step.

Chlorine-based etchant for GaN have been shown to have a high selectivity over SiO_2, about 10:1 [38]. Under these conditions, the SiO_2 spheres will still be etched, albeit much more slowly. During the etch, the SiO_2 will eventually shrink to a point where less of the GaN surface is protected. As more than half of an individual sphere is etched, its effective mask diameter will start to decrease. This results in NWs being formed with a pencil shaped tip at the top of the wire. The dry etch step therefore leaves the wires with an inadequate shape and some remaining dangling bonds, creating the necessity for an additional process step.

2.6 Wet etching

As explained earlier, dry etching GaN results in two main issues. Damages that worsen the final device performance and an inadequate NW shape due to the etching of the nanospheres during the plasma etch step. These can both be corrected at once thanks to a wet etch step.

Wet etching refers to a manufacturing technique where samples are immersed in a liquid. The solution is meant to target and remove materials from the sample. This removal is generally achieved by turning the material into a liquid or gaseous compound through a reaction between said material and the chemistry used for wet etching [39]. Unlike dry etching techniques, wet etching is isotropic, meaning that it etches equally horizontally and vertically. Exceptions for this include crystallographic etch, where

the properties of the material-chemistry interaction cause the etch to be occur along certain crystal planes or if the etch is stimulated through other means such as light or electrical bias. Both will be detailed in the coming sections of this report.

Hydroxyl-based chemistries have been shown to be able to passivate the surface states formed by dry etching. This is due to their ability to passivate the previously introduced surface dangling bonds [24] [40] [41]. The etch peels away the damaged sidewalls, resulting in the outer surface being made of unaltered GaN. For this reason, a potassium hydroxide (KOH) wet etch can provide an adequate solution to the damage created during the previous step. Additional work on the characterization of KOH-based passivation has been conducted by this group and is in the process of being published. It has shown that up to 90% of photoluminescence lost by a dry etching step can be recovered through a KOH wet etched step.

KOH has very favorable etching properties when it comes to forming vertical NWs structures. Hydroxyl-based chemistries will first target the $<1\bar{1}01>$ plane, which is etched at a very fast rate. This diagonal plane etch is favorable, as it will remove the base build-up and pencil-shaped tip of the NWs. Etching the $<1\bar{1}01>$ plane results in a smooth, adequate NW shape. After this first step, the etch continues by targeting the $<1\bar{1}00>$ plane, albeit at a much slower rate.

This is once again advantageous, as it slowly shrinks the fully-formed NW shape, at a rate where the final device size can be controlled. Other planes, such as the <0001> gallium plane will be left unetched, which is desirable as it would otherwise decrease NW height. The mechanism behind the different plane targeting and etch rate is the polarity selectivity of KOH. It etches N-polar, semi-polar and non-polar planes, while the Ga-polar plane is untouched due to having a different surface binding energy [41]. This means the $<1\bar{1}01>$ will be etched quickly, and the <0001> plane will not be etched. The $<1\bar{1}00>$ plane etches slowly as it exhibits an equal distribution of N and Ga at the surface, due to the wurtzite crystal structure of GaN [42] [43].

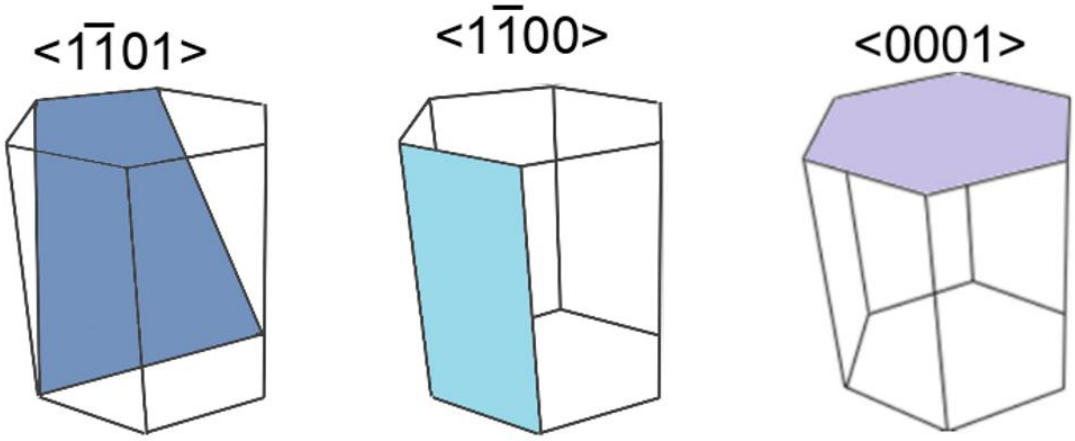

Figure 8: GaN planes targeted (<1101> and <1100>) and untouched (<0001>) by KOH etching. Adapted from [25]

This slow etch rate is critical. The upcoming section partly focuses on the optimization of wet etch experimental conditions in order to obtain ultra-thin NWs. Etching the <1$\bar{1}$00> plane at a slow pace allows for a precise control of the final rate. If a sample is etched for too long, the NWs may be destroyed or rendered too frail to handle. If it is etched for a short time, then the wires may not be sufficiently thin. Note that other chemistries, such as TMAH, have been shown to be suitable for GaN wet etching. However, they were not preferred due to the processing difficulties associated with TMAH (high toxicity, slow etch rate) [44].

For these reasons, a KOH solution can be used to complete NW fabrication. The combination of crystalline planes it targets ideally creates a perfect cylinder from a cone-shaped wire. This KOH etch constitutes the last step to obtain thin GaN NWs that are ready to be used for devices.

While this covered most of the background necessary to understand the experiments that were undertaken for this work, other information and theoretical explanations will be added as they become relevant throughout the rest of the report.

Chapter 3: Nanowire Fabrication

This section focuses on the optimization of experimental conditions for the fabrication of ultra-thin GaN NWs.

3.1 Sample composition

The samples in these sections are MQW samples. The top-layer is a 15.5nm layer of MQW $In_{0.13}Ga_{0.87}N$/GaN with 6 pairs of MQWs (total thickness of 30Å) and a 12.5nm GaN barrier. This structure is grown on a 2 µm thick layer of Si-doped GaN (n-type). Below it is a 2.5µm layer of undoped GaN. Figure 5 displays a drawing of the structure.

3.2 Processing tools

For all the processes presented here, the exact recipe can be found in the appendix section.

Before any processing step is taken, samples are first treated with an O_2 plasma. In the Rochester Institute of Technology Semiconductor and Microsystems Fabrication Laboratory, this is achieved using a LAM 490 plasma etcher. Note that for GaN, the use of oxygen plasma is not a concern but a feature. In many devices, including silicon-based ones, exposure to oxygen results in the formation of a performance altering native oxide [45]. However, for nanosphere lithography application, the thin layer of GaN oxide that is created during the treatment is used to turn the hydrophobic surface into a hydrophilic surface, allowing spheres to stick to the sample.

For the first step of nanosphere lithography, a commercially available solution of 500 nm silica spheres suspended in solvent from Polysciences, Inc. is used. To deposit them evenly across the sample, a SCS spin coater is used. The liquid is dropped on the sample before the latter is spun at a fast pace to spread the spheres.

The following step, RIE, is accomplished using a LAM 4600 Aluminum Etcher. For the purpose of this work, a combination of Cl_2, Ar and $CHCl_3$ is used. Cl_2 and Ar provide a high quality, fast etch while $CHCl_3$ is used as a protection against sidewall damage. This results in conic wires with a pencil-shaped tip.

Finally, the wet etching experiments are done under a fume hood, using a hot plate to control the process temperature. The KOH source was a commercially available AZ400K developer, which contains 2% by weight concentration of KOH [46]. It is then diluted with De-ionized (DI) water to achieve proper concentration. Samples are immersed in the heated KOH solution for various times in order to optimize the etching to obtain the desired thin NWs.

3.3 Characterization tools

Characterizing the samples is an essential step in ensuring that the thin GaN NWs were properly fabricated. For this section of the work, one main characterization method is used: Scanning Electron Microscopy (SEM). It is an imaging technique that will help determine the diameter and height of the wires.

An electron microscope makes use of an electron beam in order to create an enlarged image of a sample. They are conventionally composed of an electron gun, a condenser lens system, scanning coils and an objective system. As the condensed electron beam hits the sample, the formation of secondary electrons, backscattered electrons, X-Ray. By using a secondary electron detector, a magnified rendition of the sample can be displayed. This image is generated by converting the density of electron into a data point on a Cathode Ray display Tube (CRT). The higher the density of electrons, the brighter the image of the region. This difference in density allows for an accurate depiction of the real sample topography without the limitations of optical imaging [47].

Figure 9: Hitachi S-4000 SEM

For this work, two different SEMs were used. The first one was a Hitachi S-4000, used for most common images. For finer characterization, a Tescan Mira3 SEM belonging to the RIT Nanoimaging Laboratory was used. It has a higher accuracy for sub 100nm dimension measurements.

Since GaN is particularly sensitive to charging effects, a low accelerating voltage was used. It is necessary to use a sufficiently high voltage for the obtention of a proper image; however, a high voltage can rapidly introduce errors in measurements due to charging effects. [48] While the typical range is closer to 10 to 30keV for most samples, an accelerating voltage of 5keV was picked for all measurements [47].

3.4 Results and discussion

In this section, results of all experiments conducted in order to optimize the fabrication of GaN NWs for future device fabrication are discussed.

3.4.1 Nanosphere lithography

After the plasma treatment, the first critical fabrication step is nanosphere lithography. Conventional nanosphere lithography is performed with a closed-packed coating of the spheres. For this application, a sparse coating of spheres is desired instead. The SPEs presented in chapter 4 require a metal contact for electrical characterization to be performed. Since each device must only contain one NW, it is crucial that the sphere coating is sparse. This ensures that there is sufficient space between each wire for the deposition of metal contact (see section 4.2). Since the commercial solution of silica spheres produces only a close-packed array, it cannot be used as provided. To fix this, the solution can be diluted.

Sparse coating is achieved by performing several dilutions using DI water of the original solution were performed. The diluted solution was spin coated onto various samples and imaged with optical microscopes and SEMs. This process was first tested on glass samples, and then on MQW GaN samples.

For all samples following this step, the final concentration that was decided on was a dilution of 1-part original SiO_2 solution to 30 parts of DI water, repeated three times. 50µL of the original solution are taken and mixed with 1.5 mL of DI water. Then 50µL of that new solution is taken and mixed with another 1.5mL of DI water. After performing this dilution for a total of 3 times, the final concentration ratio will be 1 part original solution to 27000 part DI water. This concentration was found to provide a good compromise between an adequate distance between wires while providing a sufficiently high amount of wires to properly characterize the samples.

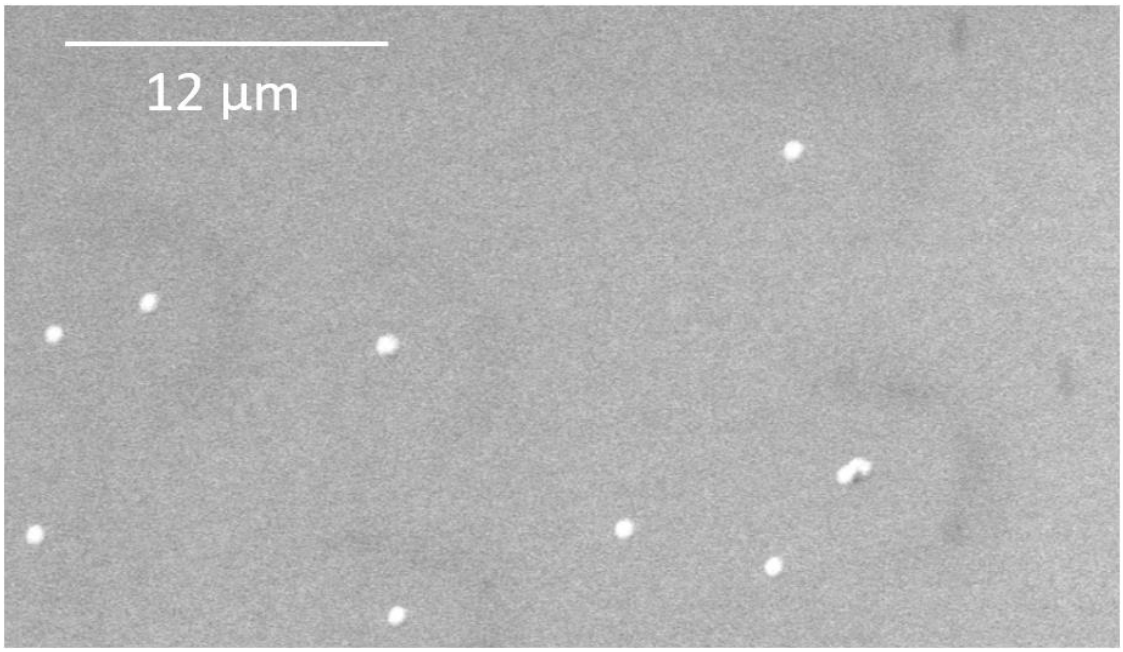

Figure 10: SEM image of the sphere repartition over a GaN sample for a 1:27000 dilution

While this is the concentration that was chosen, it can be altered in the future. Initial tests in device manufacturing shown in chapter 4 suggests that a lower density would be beneficial with regards to the proper manufacturing of devices such as SPEs for proof of concept purposes. A lower concentration of spheres would be beneficial to separate devices. Since sphere density is inversely proportional to dilution of the original chemistry, then a lower density can be obtained by simply having a higher DI water proportion.

3.4.2 Initial NW fabrication

After the nanosphere lithography was finalized, initial steps for NW fabrication were taken to create simple GaN NWs. This was done using the process outlined previously. Following the sphere

coating, a first dry etch was accomplished. The results can be observed in Figure 11. The shape observed is consistent with what was detailed in section 2.4. The addition of chloroform results in a polymer build-up, which, combined with shadowing effects, results in a wire with a conic base. The material is depleted at the top of the wires due to the etching of the spheres during RIE, creating a pencil-shapes tip.

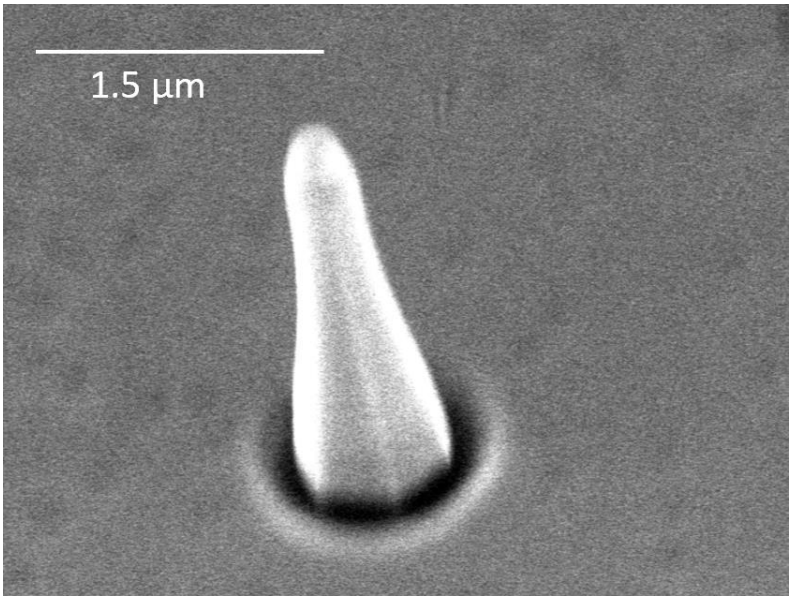

Figure 11: Post-dry etch GaN NWs

The damage observed at the bottom of the NW (black region in Figure 11) is due to trenching effects. During the dry etch step, atoms from the physical bombardment may bounce off and glide along the side of the wire and hit the substrate instead. This causes damage at the base of the wires, and can be seen for almost every NW. It is not known to impact device performance in a significant way in the context of this work.

Following the dry etching step, samples were then wet etched using the KOH chemistry. Based on what had been previously developed by the group and the estimated etch rates, short etch time were chosen, ranging from 2 to 7 minutes. For consistency, samples were maintained at a temperature of 80°C and a solution with a 40% AZ400K concentration was used. The 40% AZ400K concentration, which is used throughout this work corresponds to a 0.8% by weight concentration of KOH. This resulted in wires conform to what had previously been achieved, with longer etches yielded NW diameter ranging from 100 to 300nm on average. The results of this etch can be seen in Figure 12. The same trenching

effect that was seen in Figure 11 can be observed here. The damage's shape is different due to the crystallographic KOH etch. The other damages adjacent are thought to be caused by local crystal defect and are not observed throughout the sample.

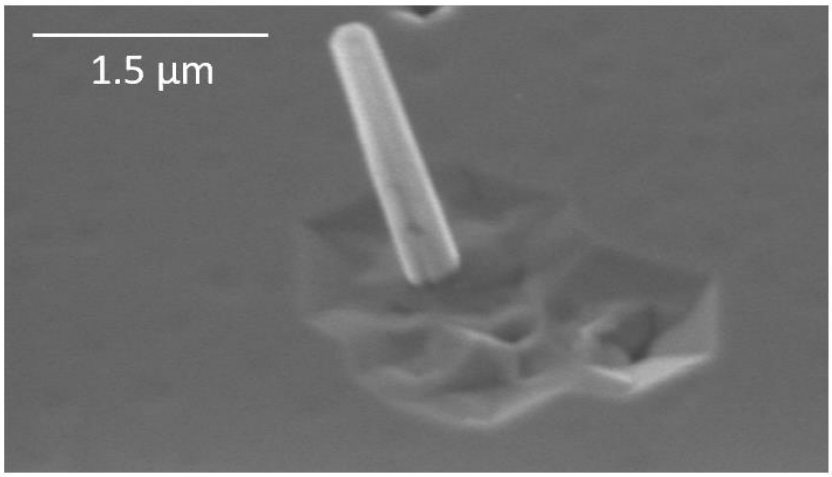

Figure 12: GaN NW after a 4-minute wet etch step

3.4.3 Optimization of NW fabrication

Obtaining a process that can reliably produce sparsely coated GaN NWs is the first essential step. Following this, the main goal of this study is to optimize the process to obtain ultra-thin NWs.

Throughout these tests, the temperature was kept constant at 80°C. Previous studies having shown that the etch rate is dependent on temperature, [25] 80°C was found to be a good compromise has it allowed for a good control of the rate while not unnecessarily prolonging the etch.

Samples were prepared again with longer etching times: ranging from 12 minutes to 20 minutes. A 20 minute etch time was found to produce high quality nanowires. This etch time reliably resulted in NW diameter down to 30 to 50nm. This represents a tremendous improvement over the past processes as a sparse coating was combined with sub 50nm NWs. An example of a very thin NW can be seen in Figure 13. It exhibits similar trenching-induced damages on the substrate, however, this is not a concern for device performance.

While this method produced many ultra-thin NWs, a portion of the wires remained thicker, with diameters closer to 100nm on average. More details on etch uniformity is provided in chapter 6. The goal set for this chapter has been reached with the obtention of sub 50nm GaN NWs.

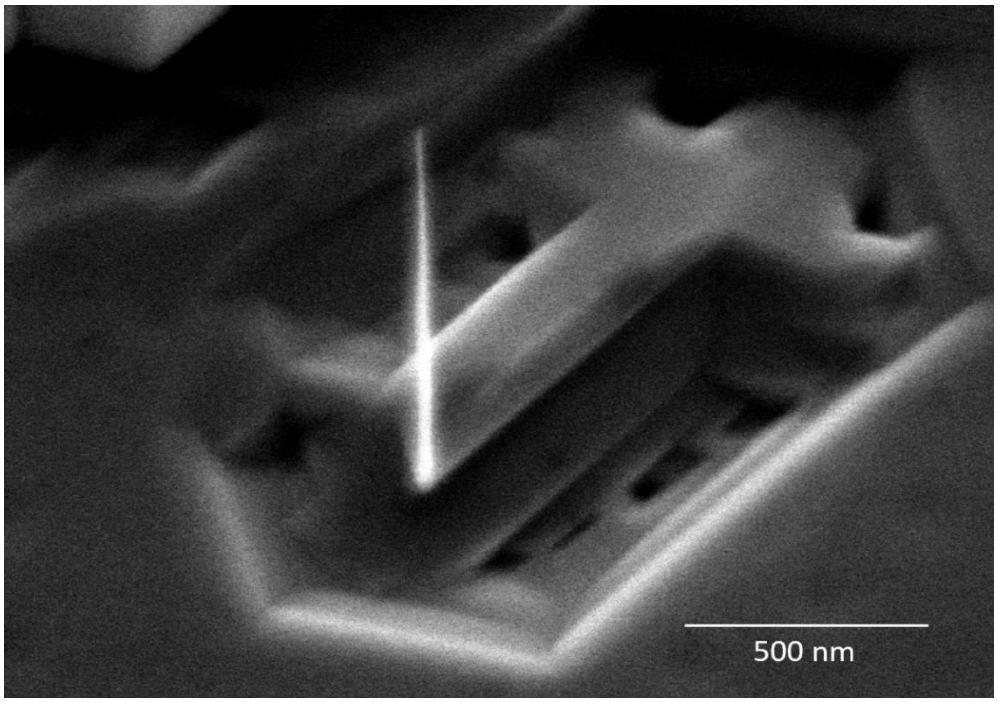

Figure 13: GaN NW with a sub 50nm diameter

3.4.4 Effect of sample handling

While GaN tends to be a sturdy, mechanically resilient material, putting care into sample handling is essential. The initial samples always retained a large portion of the NWs; however, extensive transportation of the sample was found to be damaging. If a sample is imaged several times, NWs tend to be detached from the sample. Yield can be an issue, especially if the sample has a lower density of devices. Therefore, steps must be taken to alleviate this concern.

The first step that was found to reduce the amount of destroyed wires is to tape the samples to their storing boxes using double-sided tape. If the samples are attached to the box, then no contact is made with the sides of the box. The top surface of the sample, covered in NWs, is particularly sensitive to contacts with the top of the box, thus making the tape method effective.

The second step that improved device yield was the use of air drying. Samples are typically dried using a N_2 gun in order to accelerate the drying process after the wet etch step. Drying samples by waiting for complete evaporation was found to preserve the NWs much more efficiently.

This concludes the results and discussion section for optimization of NW fabrication. Ultra-thin GaN NWs were fabricated with a sparse repartition and are ready for nanoscale device applications.

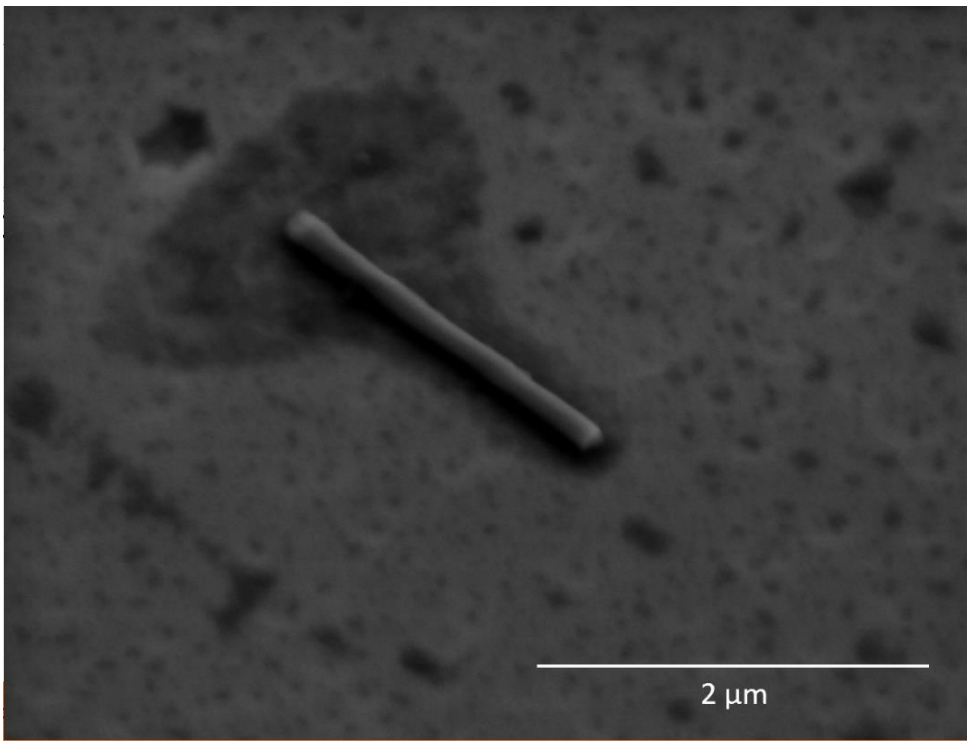

Figure 14: Example of a GaN NW knocked over due to handling, taken via SEM

Chapter 4: Fabrication of Single Photon Emitters

After fabricating extremely thin NWs, they can be used for nanoscale devices. In the previous chapter, a process was laid out to obtain GaN NWs with a sub 50nm diameter, which is believed to be thin enough to achieve single photon emission [8].

4.1 Background and theory

Over the last few decades, non-classical light sources have been the source of increasing research interest. Unlike classical light-emitting devices such as LEDs or lasers, ideal SPEs are devices that emit one particle of light at a semi-regular interval [49]. They have shown tremendous potential for quantum communication as well as general quantum computing aspects [49] [50]. The non-classical nature of photons emitted by SPEs may allow for highly secure quantum encryption, as the no-cloning theorem states that producing an exact copy of a quantum state is not possible [51].

In order to fulfil its function, an ideal SPE should behave identical to a single atom. Single photon sources emit tend particles of light following a sub-Poissonian distribution [52]. This statistical distribution is conventionally used to describe the distribution of subatomic particles but also apply to certain non-classical light sources. If a photon source emits a certain number of photon (n) and is determined by a sub-Poissonian distribution, then the associated variance (Δn^2) will be smaller than the mean ($\langle n \rangle$). [53] Emission from SPE can be triggered through either optical or electrical pumping.

There are several ways to fabricate SPEs. Single atom systems conventionally rely on trapping a single ion or atom in a cooling system. The ion is then excited via a laser, emitting photons at relaxation. The photon production is triggered through pulsing of the cooling and pumping beams, which can be reflected thanks to a mirror and lens system, thus ensuring continuous single photon emission [54]. Crystal defect systems rely on exploiting point defects in a bulk material. By exciting the defect state through optical pumping, it is possible to achieve single photon emission [55].

These conventional SPE systems present several disadvantages. They generally require a large set-up and the cost may be prohibitive. Moreover, the application potential of SPEs may be hindered if

a bulky system is required, as fully-fabricated components will need a high density of SPEs to be efficient.

Other approaches exist, such as the use of weak coherent laser pulses and spontaneous parametric down conversion but neither are yet able to reliably emit single photons in a satisfactory way [56].

Another possibility is the use of QD-based SPEs. By confining the material in every direction, the density of states turns into a δ-function. [57] This quantum confinement creates a local system analogous to a single atom, provided than the dimensions of the quantum dot are smaller than the De Broglie wavelength of an electron, which is determined by: [56]

$$\lambda_{de\ Broglie} = \frac{h}{m\nu}\sqrt{\left(1-\frac{\nu^2}{c^2}\right)} \tag{4.1}$$

Where m is the mass and ν is the velocity.

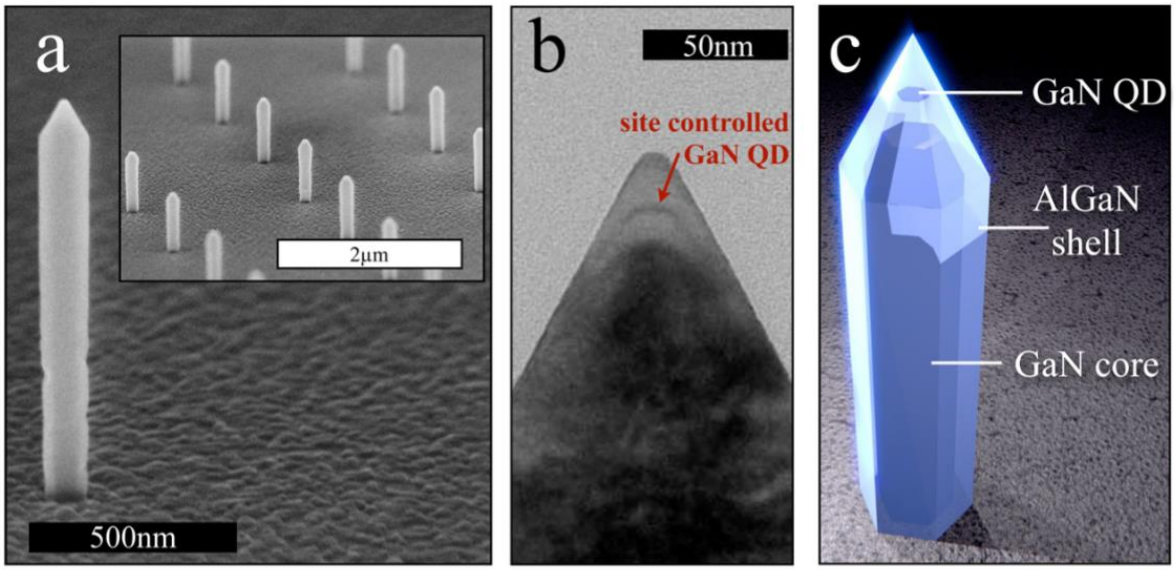

Figure 15: (a) SEM images of bottom-up grown NWs (b) TEM image of a GaN QD at the tip of a NW (c) schematic of the NW [8]

At the beginning of the 1990s, QDs were grown using a modified version of the Stranski-Krastanow growth mechanism to obtain self-organized quantum heterostructures via MBE or MOVPE [57]. However, generating a proper array with this method may be difficult, and single-photon emission can only be achieved using cryogenic temperatures with these conditions [56]. In recent years, progress has been made by using NWs instead, which can function as SPEs even at room-temperature [8] [9].

Using this method, NWs are grown with a single quantum well embedded in the structure, which creates a 1 dimension (1D) vertical confinement. By ensuring that the diameter of the wires is sufficiently small, then horizontal confinement in 2D can be achieved. This combination can result in 3D confinement, creating a quantum dot. Most QD-based SPE are optically pumped, however, it is also possible to achieve the emission through electrical pumping [58]. Overall, it appears QD NW SPEs have great in terms of manufacturability, allow for room-temperature operation and could easily be integrated within complete systems.

Figure 15 shows an example of QD NW SPEs manufactured with a bottom-up fabrication. It features an SEM image, a transmission electron micrograph of the NW tip and a diagram of the NW structure. Based on this figure, a sub 50nm NW should have the capacity to result in sufficient quantum confinement.

A potential concern when emitting single photon is the emission direction. If the emission is performed at different angles, then the photon may be lost. However, the thinning of the NW at the top creates a cone-shaped tip that has been found to increase extraction efficiency. It may be helpful to control the profile of the emission [59]. A similar shape is found in the wires fabricated here (see Figure 13).

While bottom-up growth has been used to create these novel SPEs, the top-down avenue has yet to be explored. In the coming sections, the previously introduced ultra-thin NWs will be used to lay out a fabrication process for QD NW SPEs.

4.2 Fabrication process

As mentioned earlier, SPEs can be either electrically or optically driven [58]. Samples are set aside for optical testing (see section 4.3 for more details regarding the structure). For electrical testing, devices must be prepared adequately to ensure contact. It should be noted that the goal of this process is not to create a large array of devices, but rather to demonstrate a process flow for SPE fabrication using top-down fabricated GaN NWs. A process flow diagram for this experiment is provided in Figure 17.

Starting with the wires obtained in section 3.4.3, the first step is to deposit a bottom contact. Using conventional photolithography, pads of resist can be placed over the sample. Since the wires are sparsely coated, each area of resist will have a low number of NWs, increasing the likelihood of obtaining individual photon emission for each of them. The whole sample is then coated with a thermally evaporated metal contact. Consecutive layers of Ti/Al/Ni/Au (bottom to top) or Ti/Al/Ni/Ag can be used, with respective thicknesses of 10/200/30/50nm. This combination is used for several reasons. Titanium reacts with GaN to form TiN, which acts as a donor to create an electrical connection with the GaN bottom layer [60]. Titanium and aluminum bond together, gold acts as a protection for oxidation of the contact and nickel is used as a barrier to prevent gold from diffusing into the aluminum [61]. Silver can also be used as a cheaper substitute for gold, filling the same role.

Once metal is deposited, the resist can be lifted off using a conventional lift-off developer. The next step is to coat the samples using PDMS. This can be achieved by a simple spin coating step, then followed by a dry etching step used to reduce the thickness of the polymer layer. Since the material is quite viscous, the process used for coating PDMS can hardly deposit a layer thinner than approximately 7µm. To achieve contact with the top of the wire, the PDMS layer must not be taller than the wire. The NWs are typically about 2µm tall, which means the PDMS must carefully be etched until it reaches the top of the wire. It is crucial to avoid over-etching, as this would cause the SQW region to be exposed to the metal, thus shorting the device and preventing it from functioning properly. An SEM image of a sample after step e) from Figure 17 can be seen in Figure 16 as an illustration.

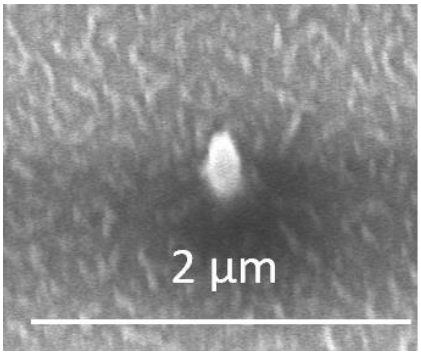

Figure 16: GaN NW embedded in PDMS with exposed top

After the PDMS layer is completed, a second patterning step is done to deposit a top contact. Since the MQW do not have a p-GaN layer, the top metal contact was a Ti/Al layer with a thickness of 30nm for each. After the resist is removed, the sample can then be contacted easily after the PDMS covering the bottom contact is removed using a simple fluorine-based RIE process.

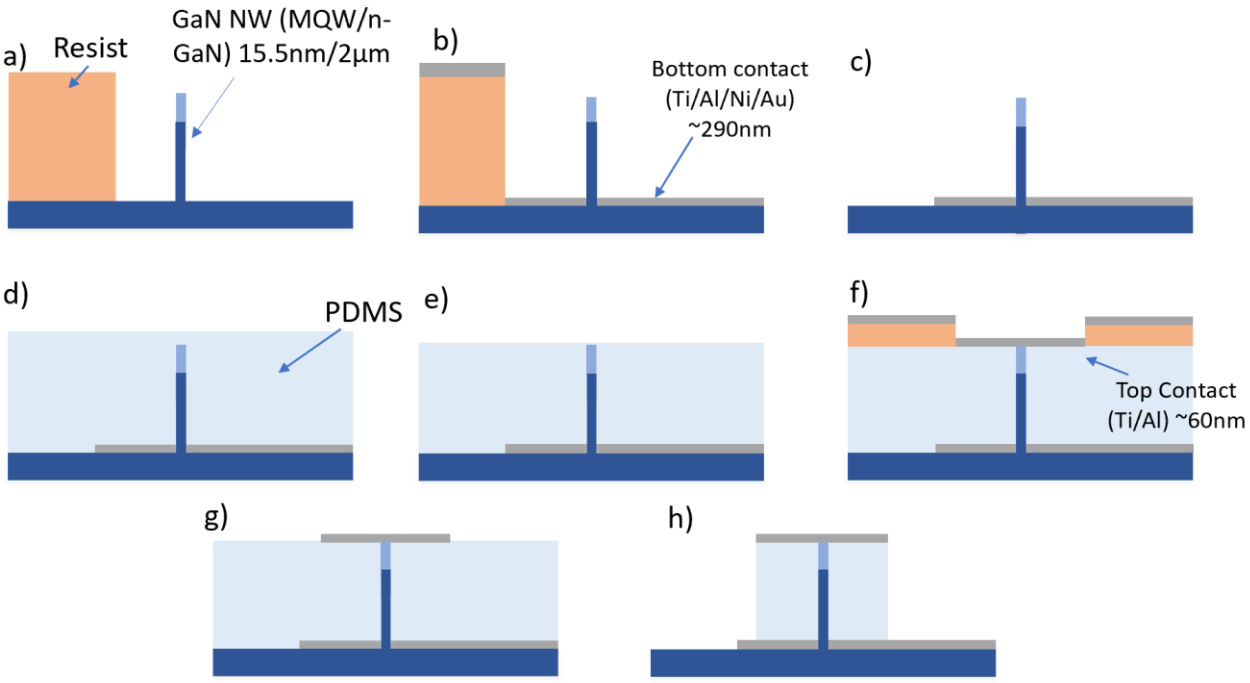

Figure 17: Summary of the metal contact deposition process flow: a) resist deposition, b) bottom contact metal deposition, c) resist lift-off, d) PDMS deposition, e) PDMS etch, f) resist patterning and top metal deposition, g) resist lift-off, h) PDMS etching

4.3 Experimental setup

4.3.1 Sample structure

Since this chapter is meant to lay out a process flow for the fabrication of electrically-driven SPEs, test structures are used for preliminary testing purposes. MQW/n-GaN structures identical to what was presented in section 3.1 are used.

For the purpose of single photon emission, having multiple quantum wells susceptible to emit photons would likely cause interference when attempting to detect single photon emission. As such, a structure akin to the ones used previously would be counterproductive. Future samples used for the fabrication of SPEs will have a top layer of 120 p-GaN. Next is a single $In_{0.13}Ga_{0.87}N$/GaN quantum well of 27nm. The bottom layer is a 3000nm thick layer of GaN.

4.3.2 Process equipment

To fabricate SPEs, the following processing equipment are needed. NWs were fabricated using the same processing equipment as in the previous chapter. An SCS Spin coater was used for nanosphere lithography and resist coating for photolithography. A LAM490 O2 plasma etcher was used for plasma treatment and a LAM4600 was used for the CL_2/Ar/$CHCl_3$ dry etching. Photolithography for metal contact deposition is performed using a Süss MA55 Mask Aligner. Metal deposition is achieved using a CVC Thermal Evaporator.

4.3.3 Characterization equipment

Imaging is performed thanks to the Hitachi S-4000 SEM presented in chapter 3.

Electrical testing is performed using a Cascade M150 4-point probe station, with data being collected by a B1500A device analyzer developed by Agilent Technologies. Optical characterization of the fabricated devices is done using photoluminescence (PL).

When a semiconductor material is hit by a light beam, carriers can be excited before relaxing back down and releasing more photons. This can be exploited to detect the different components in a structure as well as material impurities. This phenomenon, known as PL, is therefore very useful for characterization of direct bandgap semiconductor, as it provides information on material quality in a non-destructive way. Any energy state that will produce a radiative recombination can be detected using PL. A typical setup consists in the use of a laser beam reflected with a mirror onto the sample. The emission produced by the sample is then collected with a detector. A basic set-up akin to the one used in this work is shown in Figure 18. Note that the sample is sometimes placed in a cryostat and maintained at a low temperature, as it provides higher quality measurements for impurities. Low temperature PL is however not required for basic characterization [47].

The PL system that was used is a Horiba system, relying on the use of a He-Cd laser with a 325nm wavelength and a power of 33mW.

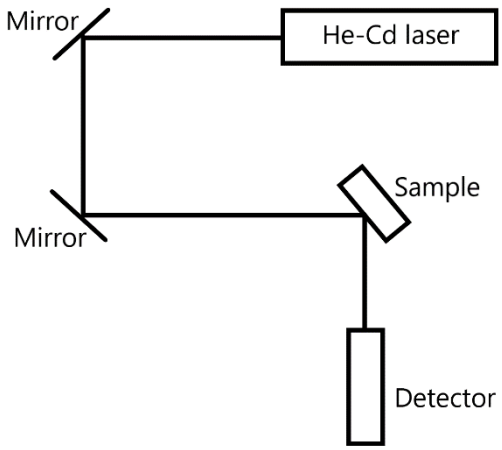

Figure 18: Conventional PL Setup

4.4 Results and discussion

The preliminary SPE fabrication testing can be carried out in two ways: optically and electrically. This section focuses on reporting the optical testing on the wires used for SPEs, a description of the fabrication process results and preliminary electrical testing.

4.4.1 Optical results

Before fabricating the devices, optical characterization can be performed on NW samples. Using an MQW sample with sub 50nm NWs as presented in chapter 3, PL is performed at several different positions on the sample. Since the set-up does not allow for selection of specific areas when performing PL characterization, a large number of measurements are taken. From these measurements, different regions of the sample can be examined, and PL spectra can be associated with certain structures. The PL spectra of 2 representative locations on the sample are plotted and represented in Figure 19.

Multiple information can be extracted from the data presented in Figure 19. The first position at which the PL spectrum was collected corresponds to the substrate (orange spectrum in the figure). The spectrum collected at a NW is similar, however, it displays a peak around 450 nm. This is due to the presence of an MQW layer in the wire. This confirms the difference between the wires that were fabricated and the substrate of the sample. Results from Figure 19 also indicate that NWs fabricated using the process that was developed in chapter 3 are able to adequately emit light.

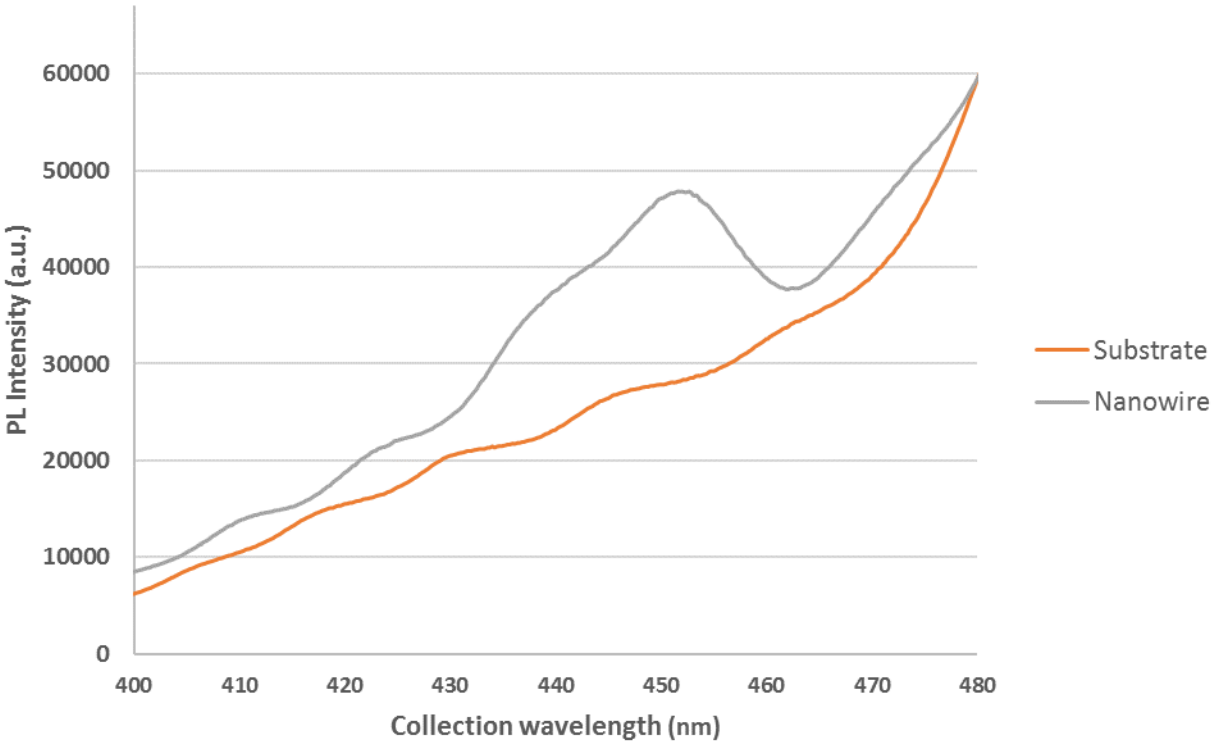

Figure 19: PL spectra of a GaN NW sample

Only two positions were represented in this characterization step. However, compiling more measurements indicates a slightly different position of the MQW on the wavelength axis. This corresponds to different amounts of quantum confinement. When confinement occurs, the corresponding energy will also increase due to the shift in density of states shape. A thinner wire will have an MQW layer-induced emission that is slightly blue-shifted (at a lower wavelength) than a thicker wire. This showcases that quantum confinement occurs in the wires to a certain extent, which is a preliminary indication that a QD NW can be achieved with this method, eventually leading to possible single photon emission.

It should be noted that the intensity on a PL spectrum is measured with arbitrary units. As such, they can only provide a qualitative analysis.

Single photon emission detection requires accuracy in many measurement aspects. Preventing noises in the measurements is therefore essential. In Figure 19, both spectra show an increased signal as

the collected wavelength is increasing. This appears to be caused by a defect peak from the bulk GaN in the signal. Therefore, masking the substrate may be very beneficial.

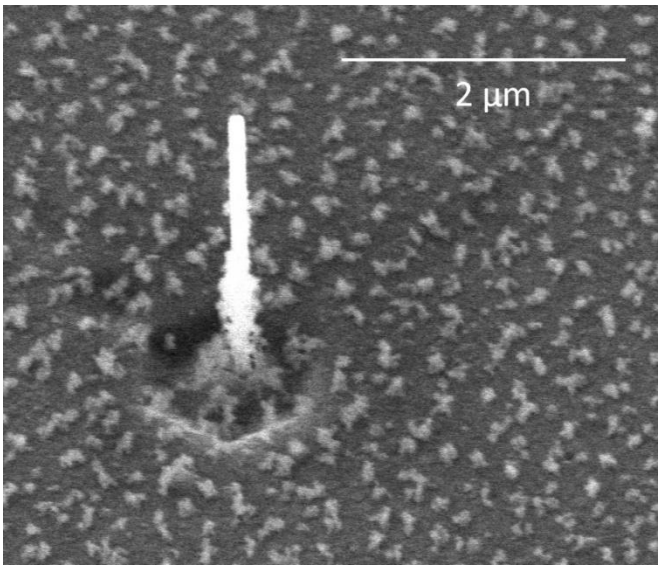

Figure 20: SEM image of a GaN NW sample coated with Al for optical characterization

NWs can be isolated by coating the whole sample in aluminum. An opaque aluminum layer would prevent the undesired detection of a bulk GaN signal. However, this also covers the NWs. To avoid hiding light emission from the wire, the aluminum layer can be etched. To protect the layer, photoresist can be used as a mask if spin coated over the substrate. Then, by simply etching the aluminum layer, the substrate will be covered while the NWs are exposed. Part of the NW bases may also be covered in aluminum, which is advantageous as the QW region is responsible for emission, not the n-GaN base.

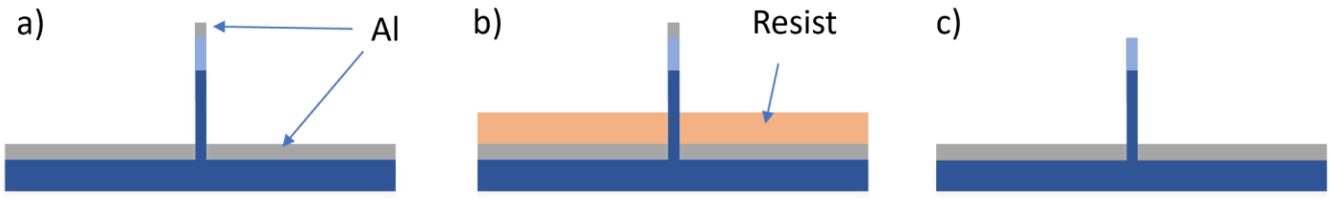

Figure 21: Al coating process flow, a) aluminum deposition, b) resist coating, c) Al etch and resist stripping

The process flow for this operation is shown in Figure 21. This process was then applied to a NW sample. An example of the result can be seen in Figure 20. It displays a NW on a aluminum coated

substrate. The residue that can be observed is a polymer deposit cause by photoresist deposition and removal.

To ensure that the layer is playing its role, a second PL set of measurement was performed. Corresponding results are displayed in Figure 22.

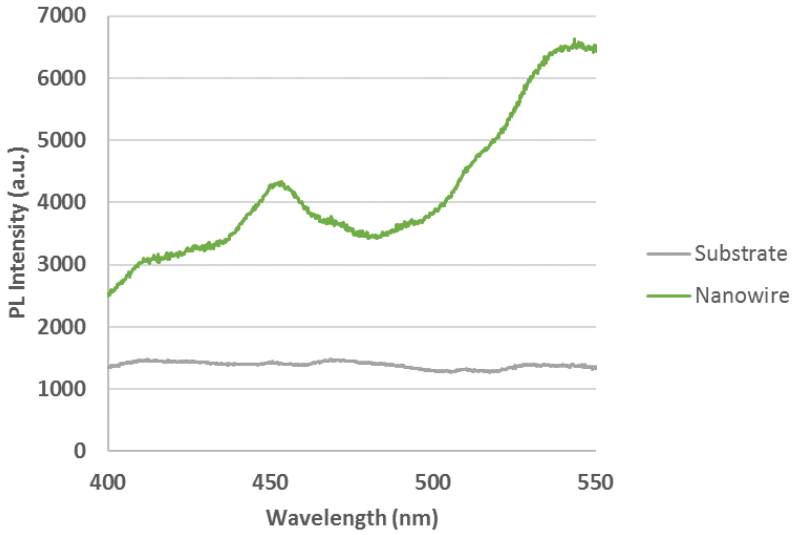

Figure 22: Post-Al coating PL measurement

The spectrum at a substrate point is now flat, no peak observed can be observed. The other spectrum, which corresponds to a NW emission, a peak around 450nm can be observed. It corresponds to the signal from a MQW layer. The second peak at higher wavelength corresponds to the bulk GaN found in the rest of the NW structure. This second experiment confirms the ability of the NWs to emit light, which is necessary for SPE fabrication, and represents a step towards more accurate optical characterization through the masking of the substrate spectrum.

To detect single photon emission, the set-up for single photon detection via interferometry is still in preparation (see section 6). A preliminary version is shown in Figure 23.

It contains a laser that is projected onto the sample via optical fiber. The emission can then be captured by a microscope linked the filters, which narrows the detection to the desired wavelength(s). The signal is then deflected onto a camera using a mirror, to detect emission from the NWs.

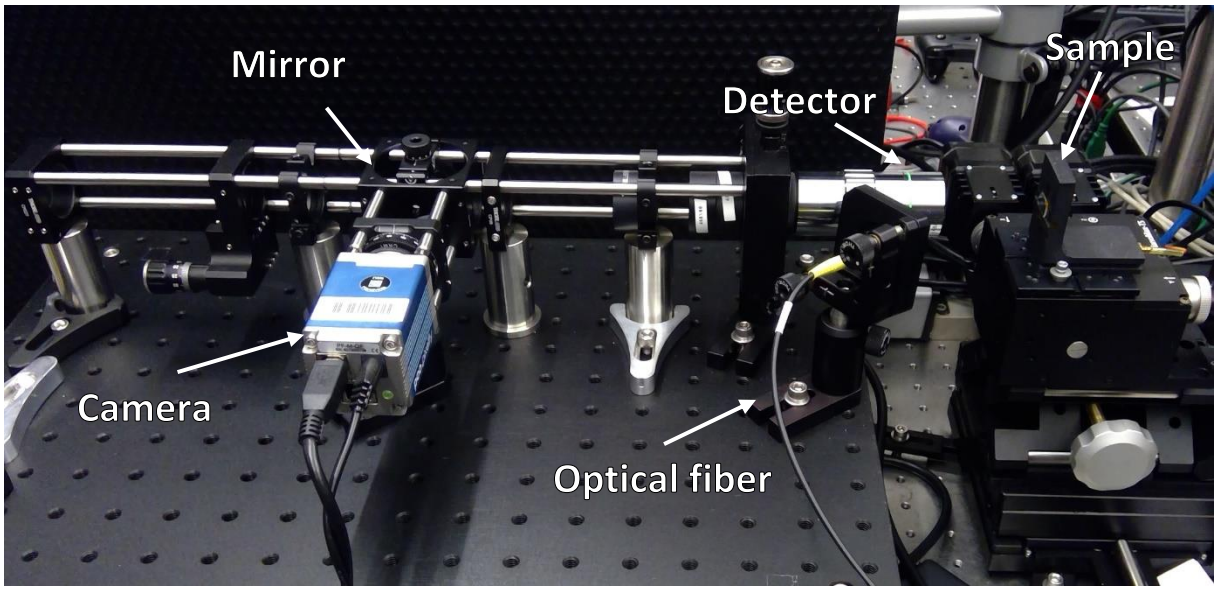

Figure 23: Preliminary version of the interferometry set-up

This version only allows for capture. The set-up that is currently being assembled works slightly differently. Instead of reflecting the signal onto a camera, it can be transported to a beam splitter. Each output is then put through photodetectors. Splitting the emission in such a way allows for the detection a single photon, which may not be possible with a single detector due to detector downtime [52]. This type of collection technique is referred to as a Hanbury-Brown and Twiss (HBT) interferometer [62].

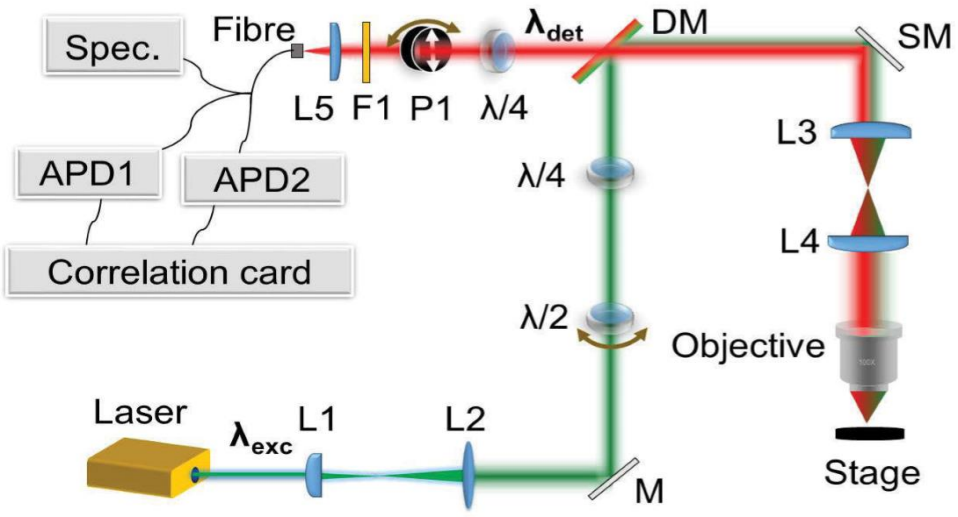

Figure 24: Diagram of an HBT interferometer for single photon emission detection [109]

A diagram of an improved version of the Figure 23 set-up is shown in Figure 24.

4.4.2 Fabrication results

The goal of this section of the work is to lay out the process for SPE fabrication. Instead of the SQW sample, the fabrication process was tested using an MQW sample.

The process flow presented in Figure 17 is used to test its viability. In the process flow, the contacts are not perfectly aligned. This is because Figure 17 shows a 2D representation. A 3D figure can more accurately display the full structure, as the top and bottom contact were made to overlap in the vertical direction. It was done for mask simplicity, as it was assumed to yield identical electrical contact. A representation of the stack can be seen in Figure 25. The SEM image from Figure 25 is taken from the device after going through the whole process flow.

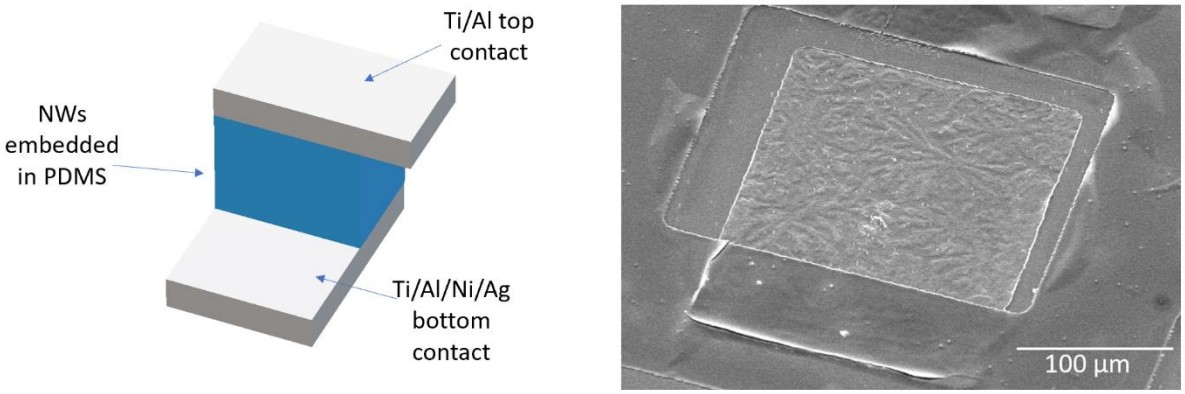

Figure 25: Metal contact test, representation (left) and SEM image (right)

After the process is complete, the fabrication seems to conform to what was expected. While the process was successful, small amounts of metals were deposited on the sides of the NWs during bottom contact metallization. This is believed to be caused by the self-heating of NWs [63]. Due to the materials deposition via evaporation not being perfectly vertical, metal covers the whole sample during evaporation, including NWs. As certain spots in the wire act as a heat sink, the temperature difference causes metal to coalesce in spots on the sidewalls. A solution for this issue is presented in chapter 6 and Figure 35.

A concern that could be raised is the frailness of the wires as shown in section 3.4.4. Since the sample goes through multiple process step that may damage the NWs, it was hypothesized that the wires

may be removed during steps such as spin coating. Several tests on samples along with the fully fabricated sample indicated that this was not the case. Spin coating both resist and PDMS was not found to damage wires. Assuming proper care is taken when processing the samples, it appears that the process flow presented earlier allows for the obtention of a sufficiently high number of devices.

4.4.3 Electrical results

Since the experiments are was done on test structures, electrical pumping with the aim to achieve single photon emission is not yet feasible. The fabrication process will be replicated with an SQW sample to fabricate functional SPEs. (see section 6)

However, there are still electrical measurements that can be performed to better understand the process. When aiming to achieve any electrical characterization of semiconductor-based devices, it is beneficial to ensure that the contacts are functioning as intended. This can be achieved with Transmission Line Measurement (TLM).

TLM functions by measuring the resistance between several metal pads on a semiconductor sample placed at different distances. For each data point, the measured resistance is equal to twice the contact resistance (once for each pad) plus the series resistance between the two pads.

$$R_m = 2R_c + R_s \tag{4.2}$$

Where R_m is the measured resistance, R_c is the contact resistance and R_s is the series resistance. When changing the distance, R_s will vary but not R_c which allows for the acquisition of the contact resistance values. By repeating this experiment for several distances, resistance can be plotted against

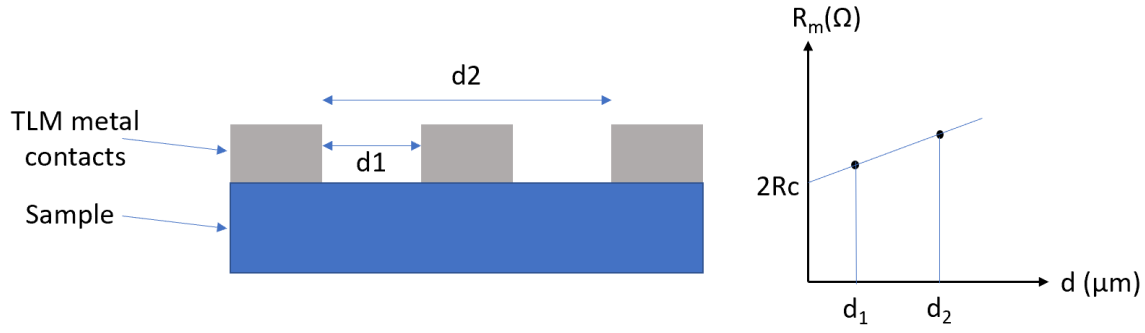

Figure 26: TLM principle representation, sample (left), plot (right)

distance. For ideal contacts, the intersection of the slope with the y axis yields the value of twice the contact resistance. The slope corresponds to the sheet resistance.

For the bottom contact, measurements were taken both pre and post annealing (at 850°C for 30 seconds with N_2). The data can be found in Figure 27. Note that a logarithmic scale was used for the resistance in order to properly display both the annealed and unannealed sample results.

For the unannealed contact, the contact resistance is 387kΩ and the sheet resistance is 45Ω/sq. After annealing for 30 seconds, the contact resistance drops drastically to 3.3kΩ, with a sheet resistance of 2.3Ω/sq. While the contact resistance values are high, the metal pads were fairly large (all on the order of 10^4 µm²). The bottom contact resistance after annealing therefore drops below 1Ω/µm². This makes a strong case for the use of the 4-layer contact described in section 4.2 combined with annealing.

After finalizing the fabrication, another contact test can be performed. The final stack shown in Figure 25 should behave as a resistor.

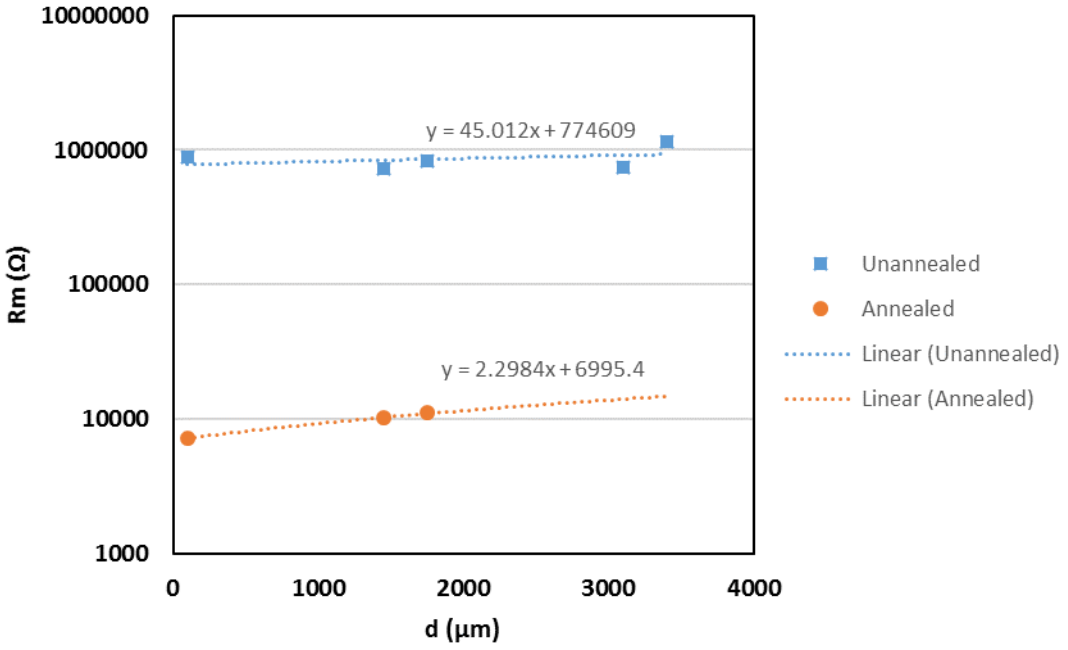

Figure 27: Bottom contact TLM

This is confirmed by the data presented in Figure 28. It showcases a clear ohmic current-voltage characterization, which is desirable as this is the behavior expected from metal contacts. As the samples

were test structures, no more characterization towards single photon emission can be performed at this time. The low current values (and therefore, high resistance values) can be explained by both the large surface area of the contact and the simpler metal structure that was used for the top metal contact. A simpler Ti/Al layer was used, resulting in poorer contact. For SPE fabrication, the top contact will be deposited on p-GaN instead of an MQW layer, calling for a different metal structure. As such, optimizing the top contact for MQWs would not be beneficial.

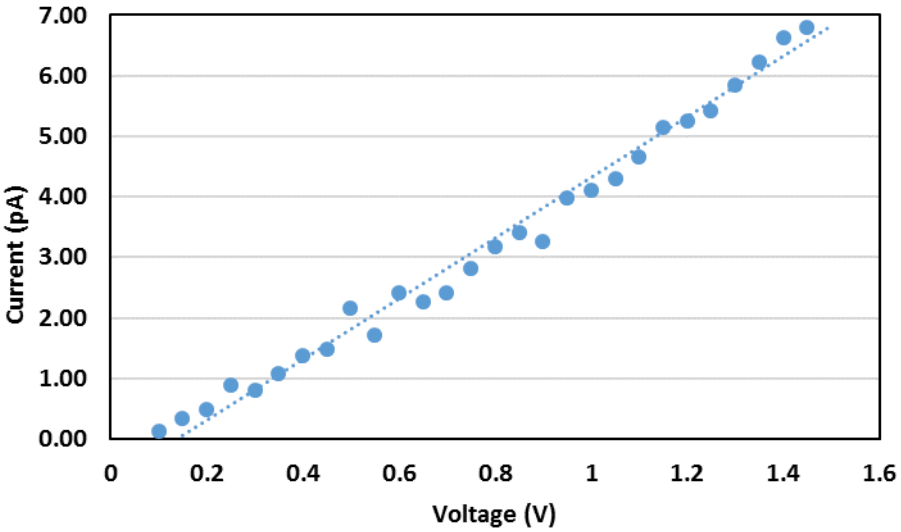

Figure 28: Current-voltage characterization of the metal contact test structure

Chapter 5: Electrochemical Etching

In parallel to the fabrication of ultra-thin GaN NWs and the processing details for SPE fabrication, another, novel way to etch GaN was explored. As mentioned previously, GaN is particularly difficult to etch due to its high binding energy [12]. Expanding on the etching capabilities therefore requires more powerful methods. This section focuses on establishing new electrochemical etching capabilities through literature research on GaN electrochemical etching, experimental set-up and preliminary results discussion.

5.1 Background and theory

5.1.1 Motivation

With GaN-based devices gaining from broadening their application scope, novel processing methods are necessary.

When building the structure of a GaN device, sapphire is conventionally used as a substrate. However, this type of substrate has multiple shortcomings, such as the presence of material dislocations and low thermal/electrical conductivity [64]. Due to these undesirable properties, investigating alternatives for sapphire may be useful. A recent method relies on the growth of GaN structures on a GaN substrate combined with a lift-off process to allow for substrate reutilization, keeping costs down while avoiding the defects induced by the use of sapphire [65].

The conventional lift-off method generally relies of laser cutting, which can be responsible for multiple issues, such as structural damages, reverse bias leakage, and more in GaN-based devices [66]. This creates the need for alternative lift-off methods. One way of doing this is through the use of a relatively new method: electrochemical (EC) etch.

While EC etching is generally used to create nanoholes in a semiconductor through a porous etch, recent progress has shown that a smooth etch (or electropolishing) is possible. Recent experiments done to achieve GaN lift-off have been making use of either the porous etching, the electropolishing, or both. However, they relied on the use of re-growth, which means an additional MEB/MOVPE growth

step is required [67]. The use of epitaxy comes with additional disadvantages as presented in Chapter 2. As such, an alternative route could be taken.

Like with other semiconductors, EC etching of GaN is conductivity selective. It could therefore be used to target the base of the nanowire, which has the highest n-type doping. By sputtering a protective layer on a close-packed array of NWs, the base remains largely uncovered due to the proximity of other features. EC etch can then be used to target the base of the NWs. Once the diameter of the base is reduced (but not completely etched away), NWs would become much less resilient and could easily be removed from the substrate. To preserve the wires, they could be embedded in PDMS, which is optically transparent and would not meaningfully impact optical performance. This NW layer could then be added onto a new substrate by etching the top of the PDMS along with the base of the wire.

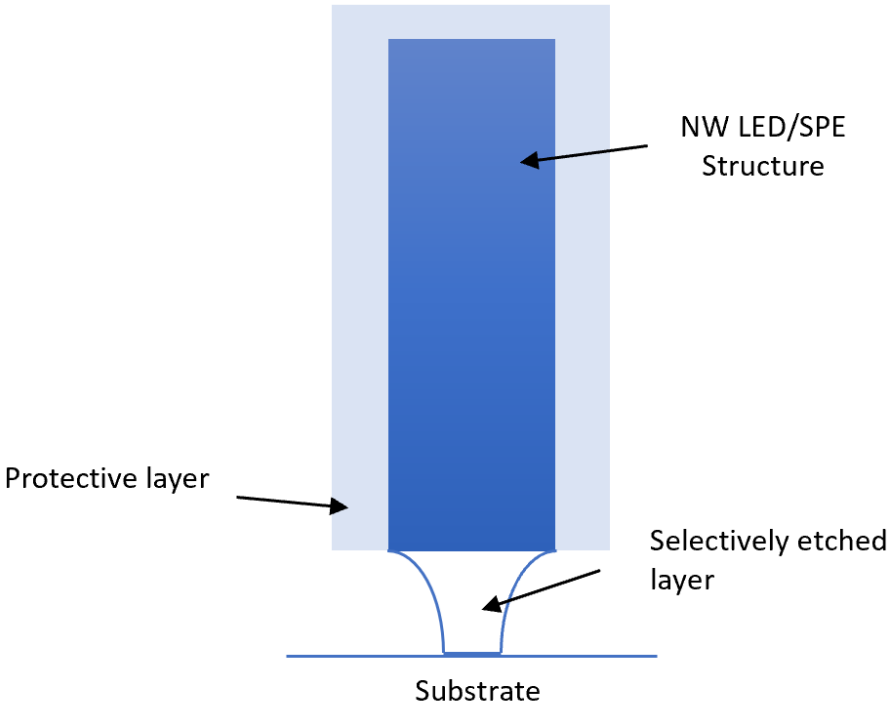

Figure 29: Schematics of an EC etched GaN NW base for lift-off purposes

PDMS embedded GaN NW lift-off has been achieved in the past, but not relying on an EC etch process [68]. This new process could be extended to the SPEs presented in chapter 4 and further extend their potential.

The primary motivation behind pursuing this newer etch was the lift-off method. However, the abilities of this set-up go beyond this application. All the possibilities that may be explored are detailed in section 6.2.

5.1.2 Theoretical principles

Electrochemistry relates to the interaction between electricity and chemical reactions. It generally consists of the creation of an electrical potential by a chemical reaction or the application of an electrical potential to induce a chemical reaction. The latter is frequently used to enhance etching reactions for semiconductor device fabrication, for instance with metal-assisted chemical etching [69]. EC etching of semiconductor was achieved in the past for both Silicon and other III-V semiconductor but recent interest in moving away from sapphire substrates along with the discovery of non-illuminated EC etch has resulted in additional attention for this technique [70] [71] [72].

This section focuses on detailing the series of mechanisms which occur at the interface between the targeted semiconductor and the electrolyte.

An electrolyte is a solution which contains suspended ions. Not unlike in a semiconductor material, the ions possess an energy level, which can be referred to as the electrochemical potential (as a voltage) or redox energy level (as an energy).

Once the electrolyte-semiconductor contact occurs, the Fermi level and the redox energy level will equalize, as dictated by the energy band model of semiconductor materials. This difference in energy results in a band bending at the interface of the semiconductor [73].

In the case of an n-type semiconductor, using an acidic electrolyte will result in an upward bending of the bands in the semiconductor. To determine this change, the fermi level in an n-type semiconductor can be calculated using: [16]

$$E_F \approx E_c + kT\left[\ln\left(\frac{n}{N_c}\right) + 2^{-\frac{3}{2}}\left(\frac{n}{N_c}\right)\right] \tag{5.1}$$

Where E_F is the fermi level, E_c is the energy level of the conduction band, k is the Boltzmann constant, T is the temperature, n is the doping concentration in the n-type semiconductor and N_c

corresponds to the effective density of states in the conduction band. The redox energy level can be calculated using the Nernst equation: [74] [75]

$$E_{red} = E^0_{red} - \frac{RT}{zN_A} \ln\left(\frac{\alpha_{red}}{\alpha_{Ox}}\right) \quad (5.2)$$

Where E_{red} is the redox energy level, E^0_{red} is the standard reduction potential, R is the universal gas constant, T is the temperature, z is the amount of electrons transferred during the reaction, N_A is the Avogadro constant and the α values correspond to the chemical activity of the reducing(electron donor)/oxidizing(electron acceptor) species.

As the equilibrium occurs between the two energy levels, charges are transferred from one side to the other. The excess charges present in the n-type semiconductor accumulate at the interface in a region known as the space charge region and create an electric field.

The concentration of charges at this interface will drive the electron flow towards the bulk of material. Inversely, holes will tend to flow towards the interface.

If enough holes can be redirected to the interface, then a dissolution reaction may occur [76]. The number of holes in an n-type material is low, and no meaningful etching will therefore be observed by submerging a semiconductor in an electrolyte solution.

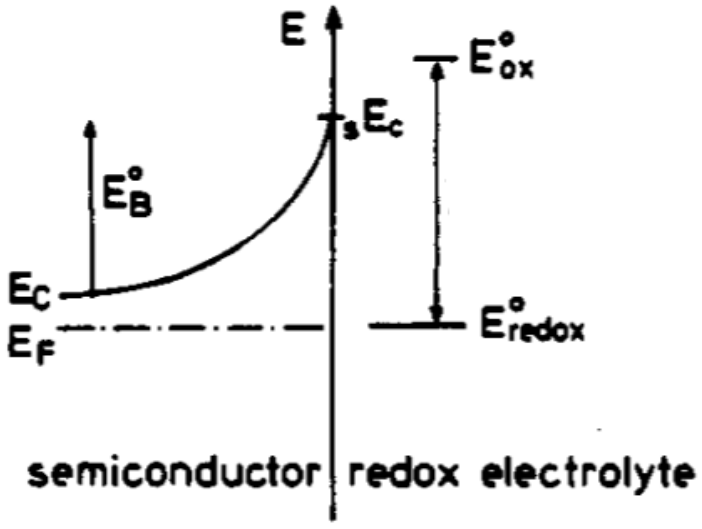

Figure 30: Band diagram of an n-type Semiconductor - electrolyte interface [105]

By applying an additional bias to the system, it is possible to accentuate the band bending that occurs. If a positive bias is applied to the semiconductor, then the conduction band will be raised at the interface. This will cause the top of the valence band to come near the bottom of the conduction band. If the doping density and the voltage are both sufficiently high, the proximity will cause some electrons to tunnel through the bandgap. At a sufficiently high voltage, tunneling may induce an avalanche reaction or an ionization breakdown [77]. As such, the essential mechanism is not just the band bending but rather the band thinning that accompanies the band bending, which allows for optimal accumulation of holes at the interface. The holes may then react with the electrolyte and the semiconductor material to form a soluble material, generally an oxide, which is then removed from the semiconductor. This dissolution results in the targeted removal of materials with a high conductivity or n-type doping concentration.

To enhance this reaction, it is also possible to add optical energy, which will generate additional holes at the interface thanks to the formation of electron-hole pairs. This optically-enhanced process is referred to as photo(enhanced)-electrochemical (PEC) etching and can be used to etch many semiconductor materials, including GaN [78]. Due to the enhancement by illumination facilitating the etch, PEC etching predates the specific EC etching studied here.

In a p-type semiconductor, the band bending would result in a local electric field which drives the holes away from the interface. Holes would not be able to accumulate at the interface, and no chemical reaction would occur. This explains why EC etching of semiconductors is inherently conductivity selective and targets materials with the higher n-type doping concentration [79].

While PEC of GaN had been achieved quite easily in the past, the first instances of conductivity-selective, EC etching of GaN were established recently [80] [81]. The process initially proposed by these references will be the focus of this section.

Like other semiconductor materials, EC etching of GaN yields three main regimes as a function of applied bias. If the voltage is too low, no etching will be observed (insufficient band bending). If the voltage is increased, a porous etch will be observed. Once it reaches a certain threshold, the etch becomes

smooth, resulting in an electropolishing of the sample. Etching regimes for GaN in oxalic acid are summarized in Figure 31. The potential ranges are dependent on aspects such as doping concentration and electrolyte choice.

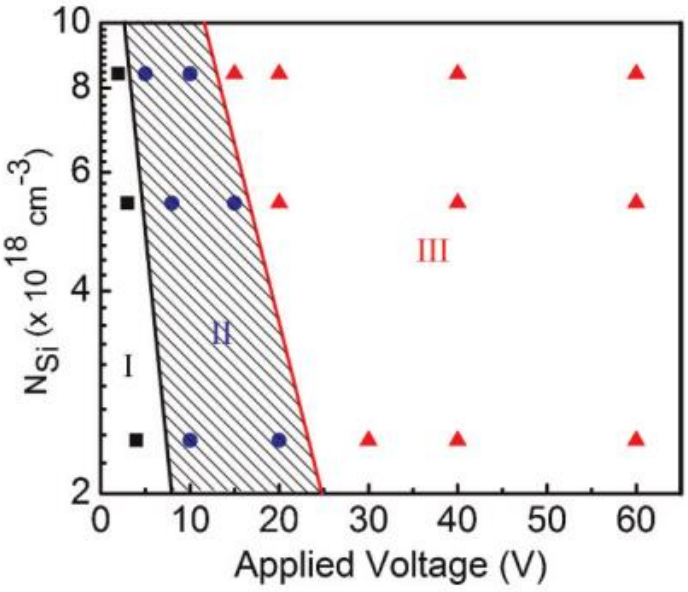

Figure 31: EC etching regimes of GaN in oxalic acid as function of silicon doping concentration and applied bias: no etch (I), porous etch (II), smooth etch (III) [81]

5.1.3 System components

Each component of the system described earlier must be transcribed into a practical application.

The sample, made primarily of GaN, corresponds to the anode. By connecting it to the bias supply, holes are provided to the material allowing for the dissolution reaction to occur.

The second component of the circuit is the opposite electrode, the cathode. It is used to close the contact in the circuit to ensure that the reaction is working as intended. Platinum is the electrode of choice in all GaN EC setup. The choice of electrode is dependent on factors such as the ions created, electrolyte composition, and more. In the original set-ups, Pt was likely picked due to desirable overpotential properties [82].

Connecting the two electrodes requires a conductive medium, here an electrolyte. For most EC etching system, the electrolyte bath provides the liquid in which the targeted material dissolves. As such,

the choice of the chemistry must account for the ability of the system. In this case, it provides the acidic medium required to break down GaN.

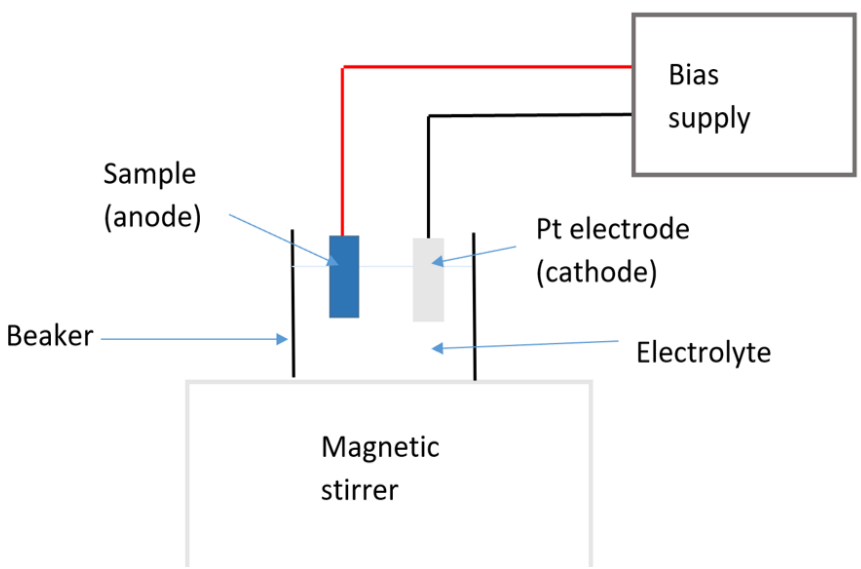

Figure 32: Conventional semiconductor EC etching setup

The first developed EC etching process used oxalic acid, however, other options such as sulfuric acid (H_2SO_4), nitric acid (HNO_3) and hydrofluoric acid (HF) have been shown to work as well [83] [84] [85]. A few of the pioneers of this method eventually replaced oxalic acid with nitric acid, and later settled on the use of HF which seemed more promising to achieve a porous etch. HF appears to yield the best results for a pure porous etching, and it can be mixed with glycerol and ethanol for smoother features [86]. Oxalic acid appears to be responsible for the formation of micro cracks in the films, hence why HF is more appropriate for the creation of pores [75] [87]. There are nonetheless safety concerns associated with HF, due to its ability to deplete calcium from bones. Moreover, reaching the electropolishing regime with HF as an electrolyte requires a higher doping concentration in GaN [88]. Since the main goal of this study is the electropolishing regime, oxalic acid is most appropriate.

Figure 32 shows an example of a conventional etching set-up relying on the components presented in this section.

5.1.4 Chemical reactions

While there have been tests on the electrochemical etching of GaN, the exact dissolution mechanisms of GaN in oxalic acid has not been demonstrated yet [89].

Precedents indicate that III-V materials are etched with a two-step mechanism [90]. The first step consists in breaking the semiconductor compound, sometimes by forming an oxide. The second step consists in the dissolution of the newly formed molecule.

In the presence of HF, one study proposed the following mechanism: [75]

$$GaN + 6h^+ \longrightarrow Ga^{3+} + N^{3+} + 6e^-$$

$$Ga^{3+} + 3F^- \longrightarrow 3GaF$$

In the presence of KOH (not used here as its preference for certain crystal planes would interfere with the final application aim), another study proposed a mechanism triggered by the presence of OH ions: [77]

$$2\,GaN + 6\,OH^- + 6h^+ \longrightarrow Ga_2O_3 + 3H_2O + N_2$$

Followed by:

$$2\,Ga_2O_3 + 6\,OH^- \longrightarrow Ga_2O_3^{3-} + 3H_2O$$

Resulting in the formation of a soluble form of gallium oxide (oxidation state of +3) [91].

Oxalic acid does not contain the fluoride or hydroxide. The final reaction must therefore be adapted. One study used an aqueous solution of sulfuric acid as an electrolyte instead. They proposed the following reactions: [83]

$$2GaN + 6\,H_2O + 6h^+ \longrightarrow 2Ga(OH)_3 + N_2 + 6H^+$$

Since $Ga(OH)_3$ is not stable in sulfuric acid, it is followed by:

$$2Ga(OH)_3 + 6H^+ \longrightarrow 2Ga^{3+} + 6H_2O$$

This reaction relies on the water present in the solution. The oxalic acid in this experiment also contains H_2O, as it is originally in the form of an oxalic acid dihydrate ($C_2H_2O_4$) which is then mixed with water. While the H_2O is presented as responsible for the reaction, the oxalic acid dihydrate is just as essential. It provides the band bending necessary for the accumulation of holes through the presence of a sufficiently high redox energy level. We believe that the combination of H_2O and holes results in the adequate environment for the separation of gallium and nitrogen. From this information, we can hypothesize that the last reaction accurately describes the chemical reactions responsible for the etching of GaN in oxalic acid.

5.2 Experimental setup

To implement the EC etching setup, a set-up similar to the one in the original GaN EC etching references will be used [80] [81].

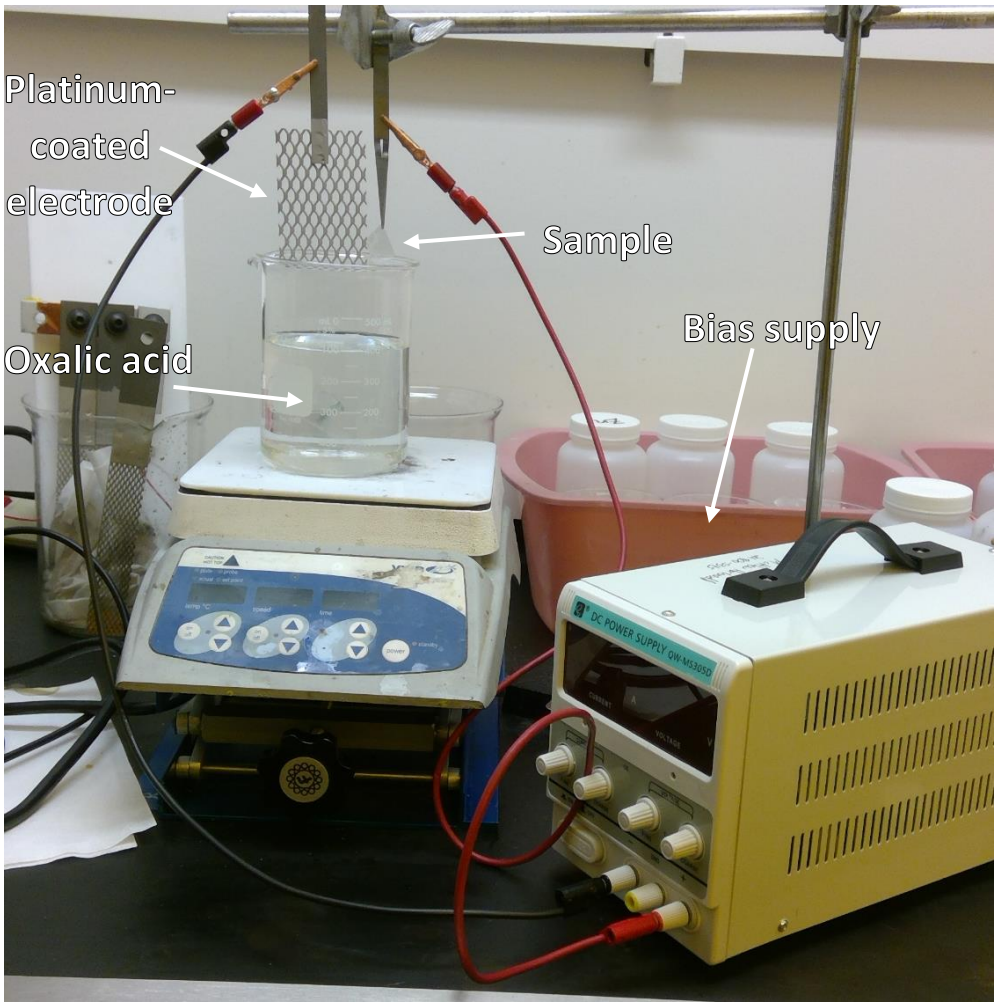

Figure 33: EC Etching setup

The experimental setup used in the context of this work has all the elements presented earlier. The sample (anode) is held using Dumont Biology Grade self-closing tweezers in a bath of oxalic acid (electrolyte). The electrolyte was purchased as Oxalic acid dihydrate (247537 from Sigma-Aldritch) and mixed with water to obtain oxalic acid. It was then diluted to a concentration of 0.3M. A 2" × 3" platinum-coated titanium grid is used for the cathode, purchased from TWL.

A magnetic stirrer is used to ensure that the solution is homogenous, which is crucial to obtain a high quality etch and avoid uneven targeting of the material. The set-up was also placed on a hot plate to gain control over temperature. The samples used for the experiments have an identical structure to the MQW samples presented in chapter 3.

5.3 Results and discussion

The initial goal here is to replicate the results presented in the section 5.1. To achieve this, a first test is conducted to obtain porous GaN. This was achieved by an initial test using the set-up described above. A 20V bias was applied to the sample for 4 minutes at room temperature and with no intentional UV illumination.

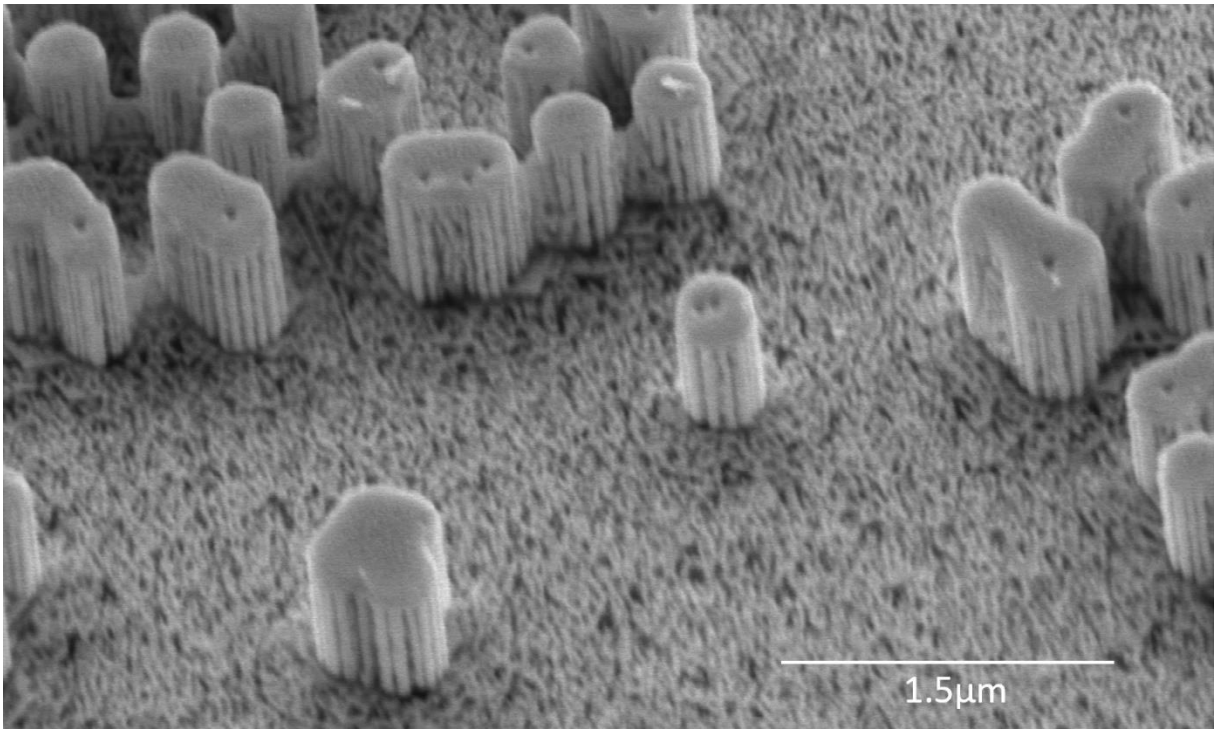

Figure 34: EC etch test of GaN NWs

Results can be seen in Figure 34. This produced a porous etch that only targeted the base of the sample. The top was left intact, which is to be expected as it corresponds to the MQW region, which is not n-doped and does not fulfil the band bending condition for EC etching.

The next step consisted in replicating the electropolishing regime. Initial testing used a higher voltage of 25V. As specified before, the n-GaN layer at the bottom of the sample is doped with Silicon at a concentration of $7\times10^{18}cm^{-3}$. Using Figure 31, it can be inferred that an electrical potential higher than 20V should result in electropolishing. To test this hypothesis, etch times ranging from 2 minutes to 6 hours were used, along with voltages ranging from 25V to 300V. 3 different bias supplies were utilized (Kikushi Model PAB 250-0.25A, QW-MS305D, and a Keithley 2635 System sourcemeter), coupled with an amplifier to reach the higher voltage values. All of these experiments resulted in a porous etching of the surface instead of the expected electropolishing.

Temperature was varied from 20°C to 80°C. The etch was observed to occur faster, but it did not impact the regime. Solution or sample age and NW diameter were not found to result in a successful smooth etch. An HF dip was also attempted but yield identical results to the ones displayed in Figure 34.

While the exact reason for the inability of this setup to achieve electropolishing has yet to be uncovered, a few things can be noted. A drop in the voltage value is observed if the measurement is taken at the electrodes instead of at the source. Attempts to uncover the source of this drop by permutating different components of the system were not successful. Additionally, measuring the current during an etch indicates that current is only flowing while the etch proceeds. After a given time, which was found to depend on factor such as temperature and voltage, the etch stops, leaving a porous surface. Using a current-controlled bias source may help reaching the desired regime instead. However, trying to increase the current input while maintaining a sufficiently high voltage (above 20V) does not produce the intended GaN electropolishing using the system in its current form.

While the desired smooth etch cannot be performed with the present set-up, the introduction of porous etching capabilities is still a very valuable addition, with many potential applications (see section 6.2).

Chapter 6: Conclusion and Future Work

6.1 Nanowires and single photon emitters optimization

With regards to chapter 3 and 4, there is still some work that can be done for the project to reach its full potential.

While the NWs have reached the diameter that was set as a goal, it would be possible to push the top-down approach further and obtain even smaller features. However, this would require great care as the structure will be rendered very fragile. To ensure that NWs are conserved, uniformity could also be improved. This could be achieved by controlling factors such as temperature homogeneity in the chemistry. Nonetheless, the process established in this study has provided a reliable way to fabricate ultra-thin GaN NWs, and most of the future tasks will be dedicated to device applications. If the wire diameter is eventually found to be too large for single photon emission, NWs can still be thinned down by increasing the etch time. Uniformity will also help with this, to ensure that wires do not get entirely removed by over-etching.

As the SPEs fabricated here are at the preliminary stages, there is still plenty of work to be accomplished. The process for SPE fabrication should be repeated on SQW samples, as this will improve reliability of the single photon emission detection. A diagram of the final process flow can be found in Figure 35. To avoid a build-up of metal on the NW sidewalls, the contacts are placed farther away from the base of the wires. After it is achieved, optical and electrical characterizations can be fully pursued. Focus should be given to completing the interferometry experiments with the aim of detecting single photon emission via the HBT set-up that is being developed and achieving optical and/or electrical pumping.

Finally, steps can be taken to optimize the process and obtain a better yield. This would improve potential for manufacturing larger amounts of devices, in line with the intent behind the use of top-down fabrication.

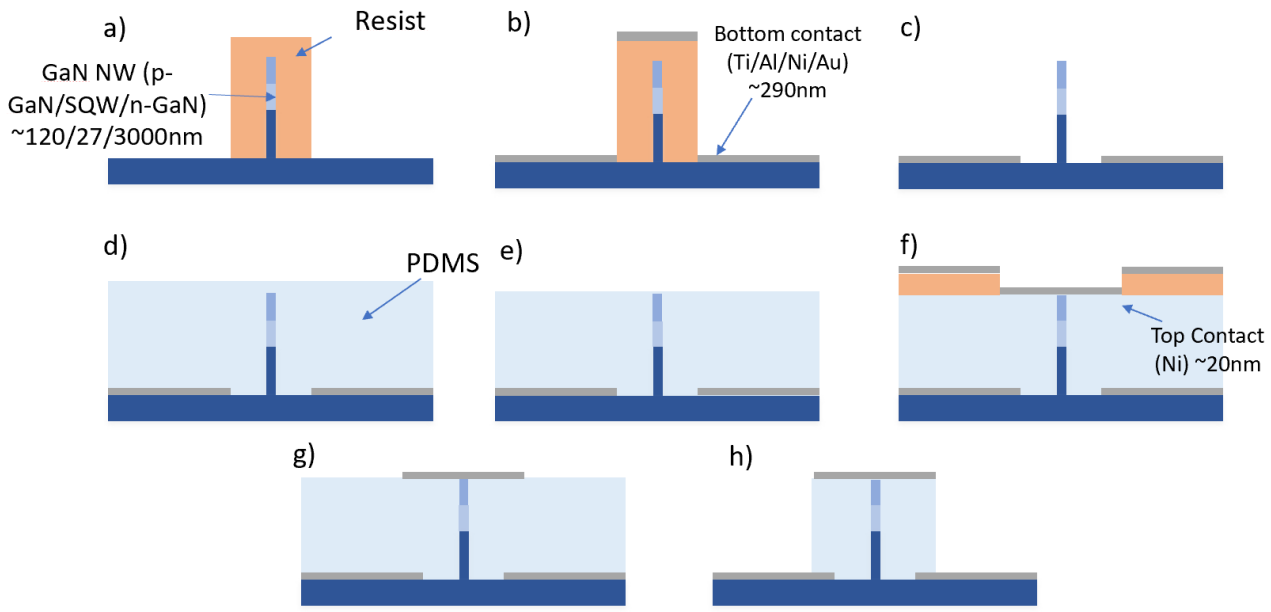

Figure 35: Summary of the future process flow: a) resist deposition, b) bottom contact metal deposition, c) resist lift-off, d) PDMS deposition, e) PDMS etch, f) resist patterning and top metal deposition, g) resist lift-off, h) PDMS etching

6.2 Electrochemical etch possibilities

Upcoming efforts on the EC set-up should be focused on achieving electropolishing, as it will unlock the lift-off process previously detailed.

In addition to the smooth etch and its application detailed in section 5.1, there are many other options that can be explored using the work that was begun in chapter 5.

While lift-off can be performed using the smooth etch presented earlier, a porous etch can also achieve the same effect. After a sample is exposed to the conditions favoring a second regime, its surface will be covered in holes. If exposed to high temperature (for example during regrowth), it has the ability to create a layer of "void" in the structure, which can be used to separate the top half of the device from the substrate/bottom half. The top part of the device can then be transferred to another substrate or an existing structure, and the substrate can be re-used to cut down costs. This process, shown in Figure 36, has already been exploited in several studies, as a proof of concept but also for functional devices [65] [92] [93].

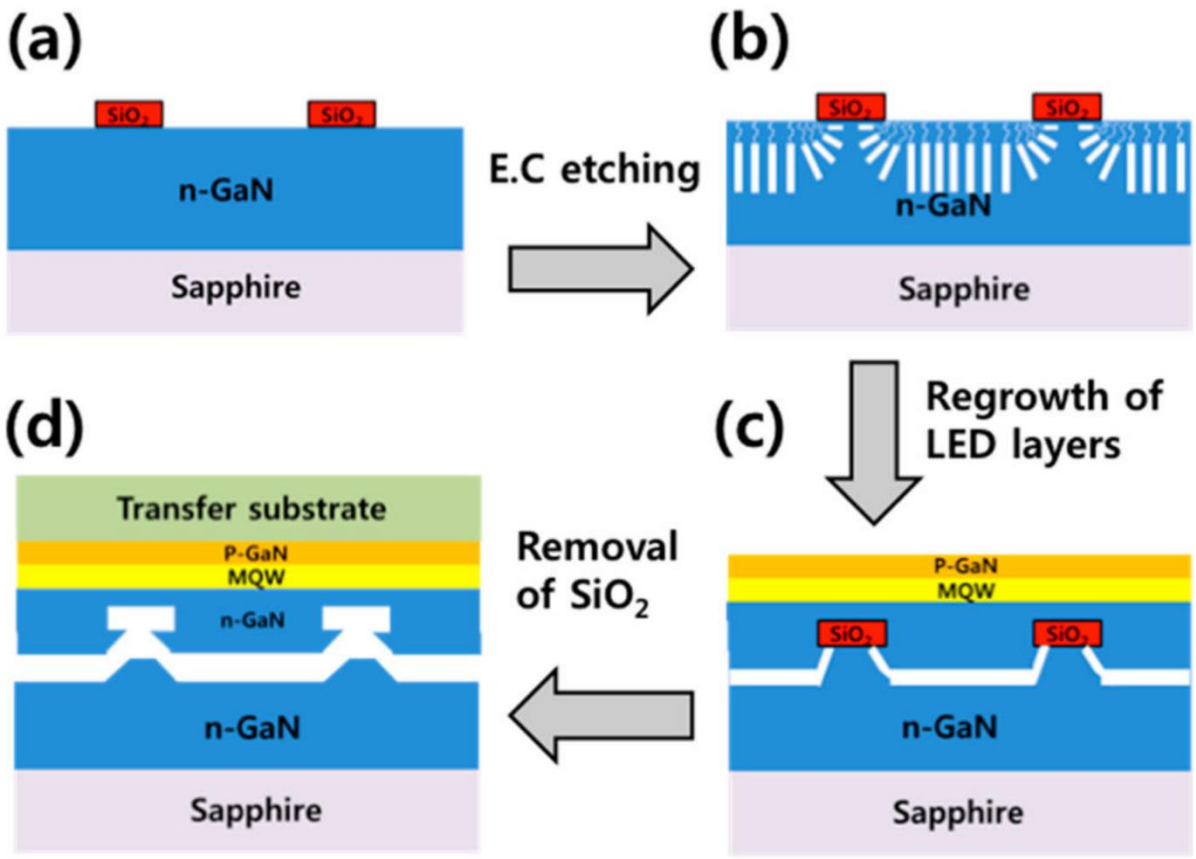

Figure 36: Example of a lift-off process flow [65]

While the lift-off method is extremely useful to make full use of certain structures, the holes created in this regime also have beneficial properties. Porous materials have been shown to exhibit desirable properties. In the case of GaN, nanosized holes can induce a local confinement that is desirable for the improvement of optical properties, useful for many solid-state lighting applications [94] [95]. Lift-off and porous etch can be combined to create membrane layers. Using HF, it is possible to etch a sacrificial layer (n+ GaN) while creating pores in the less doped n-GaN layer. As the n+ layer is etched away (note that this usually requires an additional patterning step to expose the sides), the n layer can be separated and added to another structure. An example is given in Figure 37, and much more work on the details of GaN nanomembranes has been conducted [75] [96].

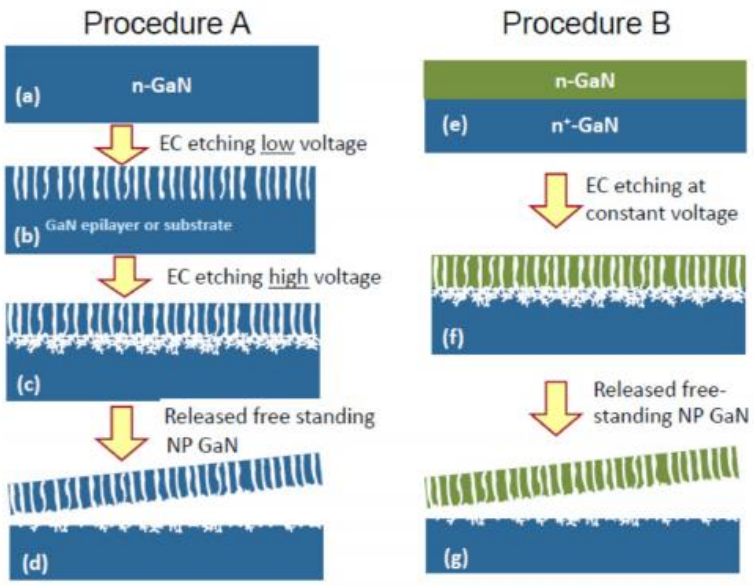

Figure 37: Procedure for GaN membrane layer detachment [96]

Once the GaN membranes are fabricated, they can be used for many optoelectronic devices, such as lasers/LEDs or be used as distributed Bragg reflectors [97] [98] [99]. They have also show potential for piezoelectric applications [100] [101].

Therefore, if the smooth etch results cannot be replicated., there are many possible routes that can be taken to expand on this new EC etching set-up. This broadens the capacities of the group and future work can be undertaken to explore new device applications.

6.3 Final words

In this work, three main tasks have been accomplished. Beginning from work previously undertaken by the group, a process was established for the consistent manufacturing of ultra-thin NWs. By optimizing the etching conditions, GaN NWs with a sub 50nm diameter were eventually obtained.

Next, a process for the manufacturing of GaN NW-based SPEs was laid out. This included work to achieve a sparse repartition of the wires on samples using nanosphere lithography, contact deposition and preliminary testing. The initial tests yielded promising results, showcasing the potential for these GaN NWs to achieve single photon emission in a cheap, mass producible way. Very little has been done with regards to top-down manufacturing of GaN NW-based SPE, this project has therefore a lot of

potential for future device achievements. More work will be pursued to finish the fabrication and testing of functioning SPEs with the aim to obtain a novel fabrication method for these promising devices.

Finally, an EC etching station was set-up and tested. While a smooth etching of GaN was not achieved, the set-up has the capacity to provide a porous etch in high conductivity GaN. This means that a process with the ability to create holes in specific layers was achieved, opening the door for applications ranging from improving lift-off techniques to enhancing optical properties of structures. Future work will be undertaken in order to improve the capacities of this etching set-up within the context of the devices relevant to the group.

Throughout this work, we have optimized existing processes and set-up novel ones that will contribute to improving research and creating future optoelectronic devices.

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Appendix

This appendix contains the recipes used for the fabrication of GaN NWs and SPEs:

Nanosphere Lithography
1 part 500nm sphere solution/27000 part DI Water (50µL to 1.5cL, diluted three times)

O_2 plasma treatment
Step 1:
120 mTorr
0 W
100 sccm (standard cubic centimeters per minute) Oxygen
30 seconds
Step 2:
Identical to Step 1 with a power of 100W instead of 0

SiO_2 spheres spin coating
Step 1:
1700 RPM
20 seconds
3 second ramp
Step 2:
1700 RPM
60 seconds

SiO_2 spheres dry etch
Step 1:
60 mTorr
200W
30 sccm of chlorine
20 sccm of argon
2 sccm chloroform
15 minutes
Step 2:
Step 1 repeated for 2 minutes instead of 1.

NW Wet etch step
Solution of 40% AZ 400K, 60% DI Water (10cL/15cL)
80°C

PDMS Spin Coating
Step 1:
1000 RPM
1 second
Step 2:
4000 RPM
1 second
Step 3:
5000 RPM
120 seconds

PDMS Setting:
11 minutes baking at 90°C

PDMS dry Etch:
Step 1:
100 mTorr
360W
20 sccm of oxygen
40 sccm of tetrafluoromethane
Time was carefully modified as the etch needs to be stopped at the edge of the wire, otherwise the device will be shorted.

Note: samples should always be dried using evaporation as opposed to a nitrogen to avoid damages to the sample.