8-2019

Engineering Source/Channel/Drain Regions for PMOS TFTs in Flash Lamp Annealed Polycrystalline Silicon

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August 2019

A Thesis Submitted
In Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

RIT | Kate Gleason College of Engineering

Department of Electrical and Microelectronic Engineering

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ACKNOWLEDGEMENTS

I would like to extend thanks to all the people who have generously helped and inspired me in some way to complete this research. First, I would like to thank my advisor, Dr. Karl Hirschman, for all his support throughout my research and study at Rochester Institute of Technology. I would also like to thank my committee members, Dr. Robert Pearson, Dr. Parsian Mohseni and Dr. Ivan Puchades for their guidance and Dr. Denis Cormier for his timely help and support with the FLA tool. I would like to thank Glenn Packard for his constant assistance in processing and analysis. I express my deepest gratitude to Team Eagle for their constant support and help in the clean room. I would like to acknowledge the whole SMFL staff; without their support this project would not be possible. I would like to also thank Robert Manley and Corning Inc. for the help in providing material required for the research.

I would like to thank all my friends and family who have motivated and helped me with patience throughout the research.

QUOTE

"He who climbs upon the highest mountains laughs at all tragedies, real or imaginary"

- Friedrich Neitszche

View from the summit of Mount Washington (Feb 12, 2019)

ABSTRACT

The flat panel industry requires high performance semiconductor materials to withstand the growth rate in the standards of display quality due to the inability of amorphous silicon (a-Si) to support the next generation display manufacturing. Upon research of other materials, low temperature polycrystalline silicon (LTPS) has exhibited the maximum potential considering its high charge carrier mobility. Currently, industry has been employing excimer laser annealing (ELA) process for production of polycrystalline silicon from amorphous silicon which is an expensive process and limits its usability to small screen displays. Flash lamp annealing (FLA) is another approach that is cost efficient and can be utilized for large glass panels and presents itself as a potential candidate to replace ELA; however challenges in obtaining uniform morphology over large areas must be addressed.

Previous work on FLA polycrystalline silicon TFTs demonstrated high carrier mobility but exhibited scalability issues due to liquid-phase dopant diffusion. To avoid this issue, dopants were ion implanted post-FLA, then activated through furnace annealing at relatively low temperatures ($T \leq 700$ °C). This procedure resulted in reasonable dopant activation, and p-channel TFT operating characteristics with an effective hole channel mobility of 40 – 50 $cm^2/(Vs)$. However 700 °C annealing was required to promote TFT electrical performance, which is beyond a practical limit for large panel manufacturing. This work presents on strategies which use FLA for both crystallization and dopant activation processes.

An initial study explored low intensity FLA for partial solid-phase crystallization of a-Si to realize microcrystalline material with mixed-phase morphology, with crystallization and dopant activation processes occurring simultaneously. Exceedingly high series resistance rendered the material incapable of demonstrating working TFTs. Efforts were then redirected based on the success of an approach using pre-amorphization of FLA LTPS by Si^+ ion implantation, followed by boron ion implantation and activation through solid-phase crystallization in the source/drain regions. The pre-amorphization process demonstrated improved TFT characteristics on both furnace anneal treatments done at lower temperature (T = 630 °C) and FLA activation treatments. This approach was modified to include a furnace anneal treatment in between the Si+ pre-amorphization and boron ion implant processes, which following FLA activation has yielded the lowest sheet resistance obtained thus far (Rs < 400 Ω/□). This high level of boron activation suggests the lack of extended defects, and thus the potential to realize an improvement in transitions at the source/channel and channel/drain interface regions.

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1. Introduction

1.1 Background

Flat panel displays (FPDs) have been an integral part of our daily lives with about 70 years of manufacturing history. The first flat-panel display, Aiken tube, was developed in the early 1950s and was manufactured in limited numbers in 1958 as a heads-up display in military systems [1]. Particularly, the thin film transistor (TFT) liquid crystal displays (TFT-LCDs) occupy 95% of the market shares across TVs, computer monitors, smartphones etc. Due to the enormous effort in the display industry, the performance of TFT-LCD has surpassed its predecessor cathode ray tube (CRT) and, the cost barrier has been considerably reduced for its mass adoption.

An image consists of a picture element known as pixel. A pixel in a TFT-LCD consists of backlight illumination, polarizers, conductive electrodes, color filters (RGB), liquid crystal and TFT. The transistor acts as a control mechanic for each pixel. The amount of voltage applied to the transistor determines the rotation of the liquid crystal allowing the light to pass through the system to obtain an image on the glass screen. The backlight illumination used previously comprised of compact fluorescent lamps (CFLs) but considering the significant difference in the power consumption, industry has employed use of light emitting diodes (LEDs) for backlight illumination.

In general, an LCD is referred to as a non-emissive display. An organic light emitting diode (OLED) system is referred to as emissive display since it doesn't require a backlight illumination and uses LEDs in place of liquid crystals. In this case, the voltage

applied to the TFT controls the intensity of light produced by the LED. Fig. 1 and 2 represent construction of LCD and OLED units respectively.

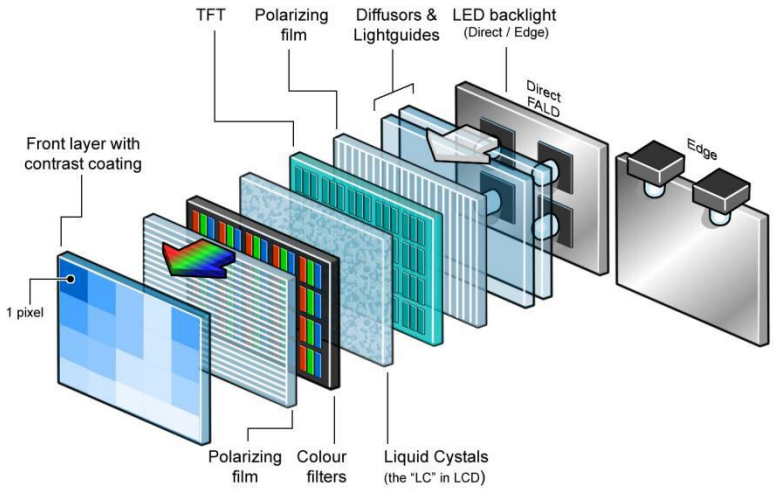

Fig. 1. Construction of LCD panel [2]

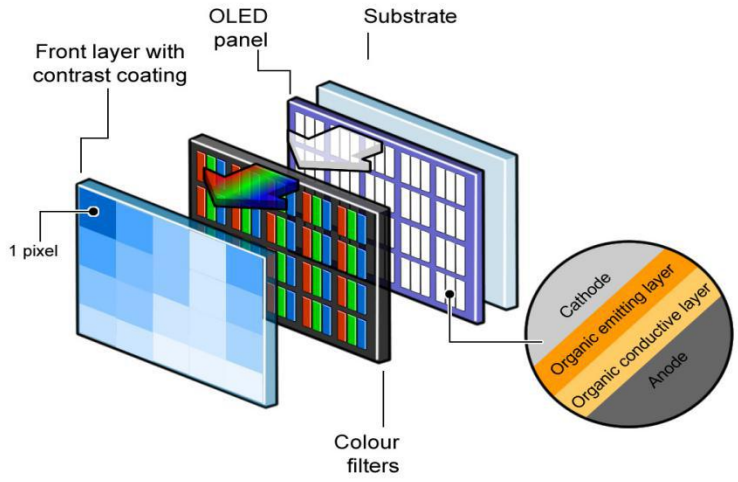

Fig. 2. Construction of OLED panel [2]

1.2 Addressing schemes

During the early production of LCDs, a passive matrix addressing scheme was used that had a row and column arrangement of conductive electrodes to apply voltage to the liquid crystals for selective transmission of light. The problem with this technology

was slow response since each crystal had to be addressed one at a time along with distribution losses that led to deterioration of image quality. Another drawback with the passive matrix addressing scheme is the imprecise voltage control which hinders its ability to control one pixel at a time causing partial transmission through adjacent crystals affecting the contrast output of the display.

With the advent of technology, the FPDs started adopting TFT backplanes which brought out a new technology, commonly known as, active matrix display. This addressing scheme employs a combination of transistor and capacitor with every pixel and all these transistors can be addressed simultaneously thus, increasing the response time. The transistor addressed charges the capacitor to in turn rotate the crystal to transmit light. The capacitor can hold charge until the next refresh cycle thus providing a better black and white contrast. Also, this addressing scheme provides a better gray scale control since individual transistors charge the capacitors to give precise control over crystal rotation to restrict the transmission of light as per requirement. As can be seen from figure 3, the leakage via conducting material in the passive matrix display causes the unselected pixels to light up as well which is not the case in active matrix scheme due to the transistor control.

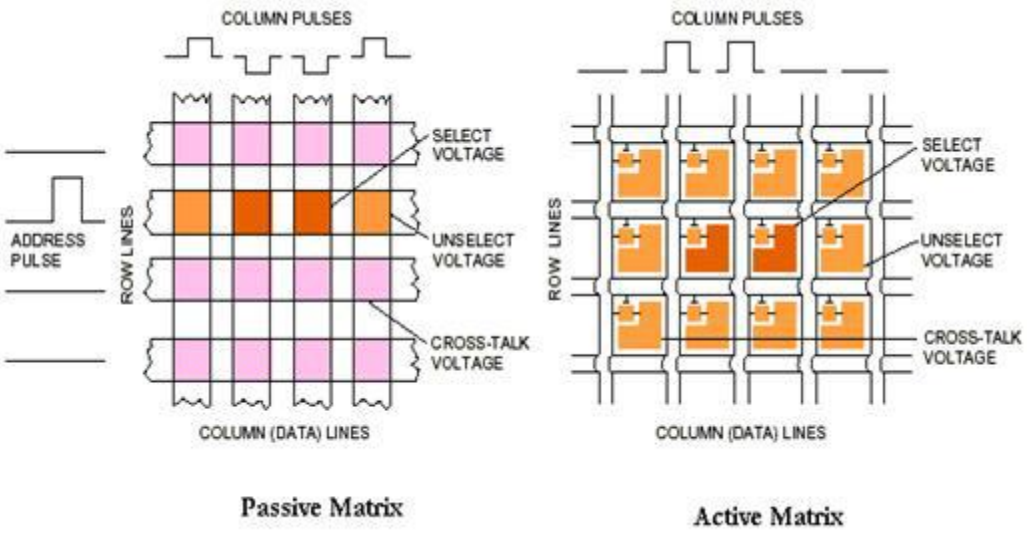

Fig. 3. Various TFT addressing schemes [3]

Unlike LCDs, OLEDs employ active matrix technology in a different manner. The level of current through the transistor dictates the brightness of the LED in the pixel. Therefore, the devices are current-driven and hence, it becomes vital for industry to facilitate research on different materials and techniques to promote fabrication of TFTs with higher current throughput. Fig. 4 gives an account of the electronics display industry with OLED technology slowly increasing its share in past few years.

Fig. 4. Flat panel display market by technology. Increasing percentage of AMOLED displays through the years. [4]

1.3 Semiconducting materials

With the progressing research in the TFT backplane technology regarding LCDs and OLEDs, the semiconductor channel layer has been a vigorous topic of investigation pertaining to the various requirements of the FPD industry. Essentially, the competition being among three candidates; hydrogenated amorphous silicon (a-Si:H), amorphous metal-oxide semiconductors (AOS) and low temperature polycrystalline silicon (LTPS).

1.3.1 Hydrogenated amorphous Silicon

The material that has been most widely regarded suitable for TFT production has been a-Si:H. The primary method of production of a-Si using plasma enhanced chemical vapor deposition (PECVD) provides this material an extra edge considering the high deposition rates and large area uniformity, making it one of the most inexpensive technology for FPD industry.

Amorphous silicon has a tetrahedral structure network of silicon atoms with different bond lengths and bond angles. This presents a threat of formation of dangling bonds that weaken the structural integrity of the silicon films and its interface with other materials which in turn affects the TFT performance. Therefore, incorporation of hydrogen during the PECVD deposition of a-Si had been implemented due to the properties of hydrogen of passivating the dangling bonds. The hydrogen content in a-Si:H layer is generally around 10 percent; higher concentration causes peeling of the thin film during thermal processing.

The devices fabricated using this material exhibit good electrical behavior with low off-state leakage current and acceptable on-state current. The electron mobility is

approximately 1 $cm^2/(Vs)$; hole mobility is only around 0.003 $cm^2/(Vs)$ [5], which is exceedingly low. For a significant time, a-Si:H NMOS technology has been utilized for TFT fabrication in the FPD industry. But, with the introduction of OLEDs and the demand for high resolution displays, the low mobility offered by this material does not meet the needs of advanced display products and has inspired the industries to pursue alternative materials.

1.3.2 Amorphous metal oxide semiconductors

Metal oxide semiconductors have been captivating a lot of interest for the display applications. The fact that these materials can be deposited via processes such a sputtering, make them viable to be used with glass panels for larger displays. Zinc oxide (ZnO) and Indium Gallium Zinc oxide (IGZO) are two such metal oxide semiconductors. The oxygen vacancies present in these materials act as donors making them inherent an n-type semiconductor. Further, these materials have been reported to exhibit electron mobilities as high as 10 $cm^2/(Vs)$, which is significantly greater than a-Si:H.

The TFTs with IGZO channel have good on/off current ratio and low threshold voltage along with low off-state leakage current. Despite the high-performance characteristics, IGZO hasn't been able to completely take over the industry attributing to its compatibility with various processing technologies such as plasma etching etc. Currently, IGZO is being used in large display panels and further research efforts are being made to make it more suitable to the industry.

Fig 5. Sharp Develops IGZO 4K Ultra HD Screen with Stunning Pixel Density of 736ppi [6]

1.3.3 Low temperature polycrystalline silicon

With the initial success of a-Si:H material, polycrystalline silicon became an immediate topic of research. The large grain property of the poly-crystalline silicon promotes an ordered arrangement of the silicon atoms, hence, reducing the number of dangling bonds remarkably. This increases the carrier mobility of the dopants by at least two orders of magnitude when compared to a-Si:H.

Transistor devices fabricated using LTPS exhibit very high current drives and overall current throughput. Further, LTPS has bipolar properties and can be used to fabricate both n-type and p-type TFTs. This presents the opportunity to manufacture CMOS system in the TFT circuit which will provide faster switching speeds and low power consumption which is ideal for high resolution displays in the case of LCDs and OLEDs.

Table 1. Comparison of present generation TFT technologies [9]

	LTPS	a-Si:H	IGZO
Channel mobility	>100 $cm^2/V \cdot s$	1 $cm^2/V \cdot s$	~10 $cm^2/V \cdot s$
TFT type	CMOS	NMOS	NMOS
Bias stress stability	Excellent	Poor	Fair
TFT uniformity	Fair	Good	Good
Pixel Circuit	Complex	Complex	Simple/complex

Currently, Excimer laser annealing (ELA) is being used in the industry to realize LTPS material. This process involves using an excimer laser such as XeCl to melt the a-Si layer and crystallize it forming large grain structures during the process. This material is relatively defect free and high quality due to the transition from melt phase to final crystallization. Though ELA has been known to develop transistors with superior performance, it is a raster scanning process which makes it impractical to be used over large display panels due to the long duration of the process and cost inefficiency. Despite these challenges, the industry has been incorporating ELA process for small display applications such as mobile phones, tablets etc.

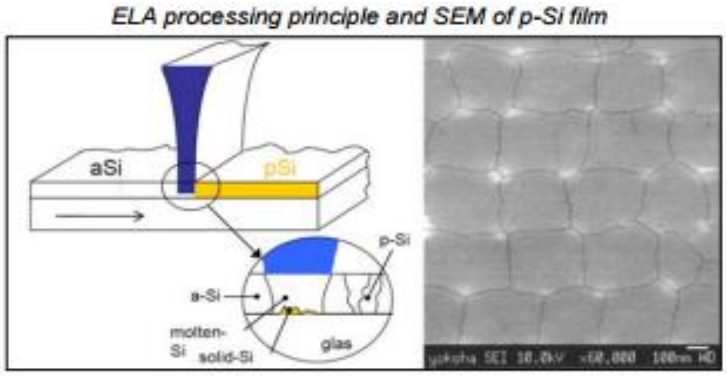

Fig. 6. ELA processing Principle and SEM of polycrystalline silicon film [7].

2. Flash lamp annealing (FLA)

Flash lamp annealing of amorphous silicon is a technique that has been subjected to a lot of research due to its potential to replace ELA. The setup involves short bursts, on a microsecond time scale, of broad-spectrum light from xenon arc lamps for the crystallization of the required material; in this case amorphous silicon. As seen from figures 7 and 8, the wavelength spectrum of light radiated by the FLA system is such that can be easily absorbed by silicon.

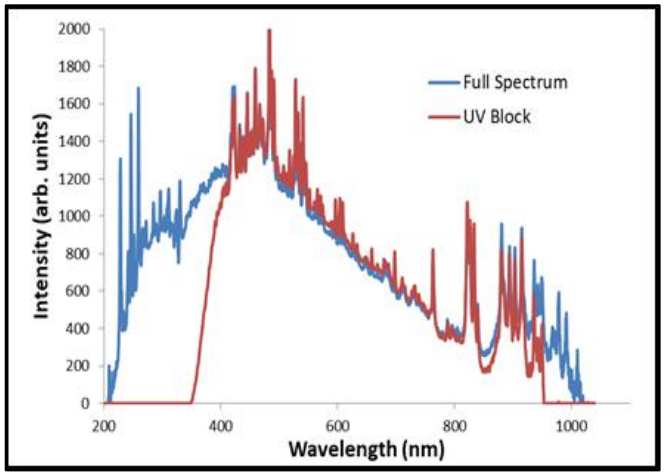

Fig. 7. Spectral data of Xenon flash lamp exposure with and without UV block. [Courtesy Novacentrix]

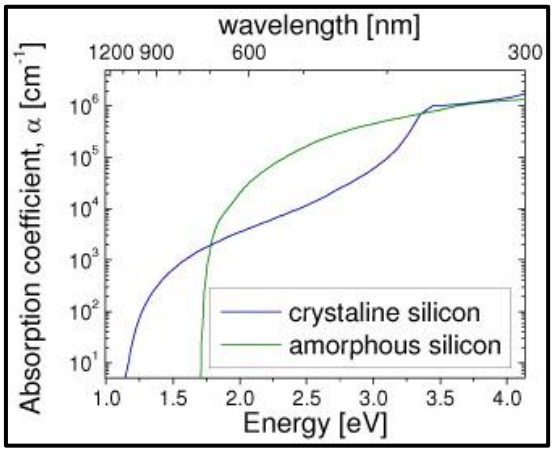

Fig. 8. Absorption coefficient of crystalline and amorphous silicon [8]

FLA has a much larger exposure area when compared to the ELA since it is not limited by a laser spot size and can be scaled up using more arc lamps and some design engineering. This makes FLA suitable for manufacturing of large glass TFT backplanes for FPDs on substrate size even greater than gen 10. The FLA process can simultaneously crystallize large a-Si silicon regions, thus making it cost effective.

Research suggests that FLA process promotes devices with high mobility and high current throughput along with low production cost. All these advantages support its incorporation in the manufacturing of high-performance LCDs and OLED displays. However, it is not all glory for FLA since it has its own demerits primarily being lack of precise control and non-uniformity of crystallization over large area substrates.

2.1 FLA system

For FLA, the NovaCentrix PulseForge 3300 has been used in this research. The PulseForge 3300 is designed to process higher melting point materials, such as silicon, zinc oxide, ITO, ceramics and CIGS, used for printed logic, display, and photovoltaic applications. The tool creates a very high processing temperature required for recrystallization and annealing, but without damaging low–temperature materials like polymeric substrates, glass (including thin flexible glass) or adjacent organic materials [8].

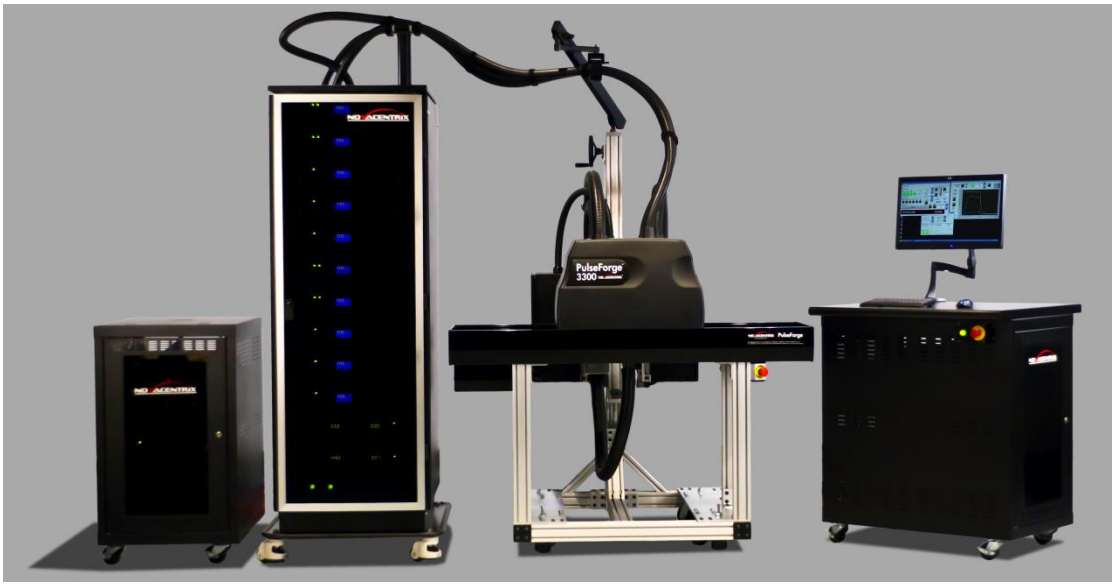

Fig. 9. NovaCentrix PulseForge 3300 FLA system at RIT

The system comprises of two xenon bulbs with an exposure window of 75x150 mm which can provide irradiance greater than 40 kW/cm^2 with the pulse duration being as short as 30 microseconds. A chiller utilizes deionized water to form a cooling mechanism for the bulbs. A capacitor bank consisting 10 drivers acts as a control unit for the flash system with 5 drivers designated to each bulb and can be charged up to 600 V in total. The bulbs are setup in a reflector dome lamp head with a quartz plate fitting the exposure window. Furthermore, the lamp head can be moved vertically to configure the distance between the lamps and target material substrate. The energy density transmitted by the bulbs is determined by the input energy which is proportional to the input voltage and the capacitance discharge from the bank at that voltage.

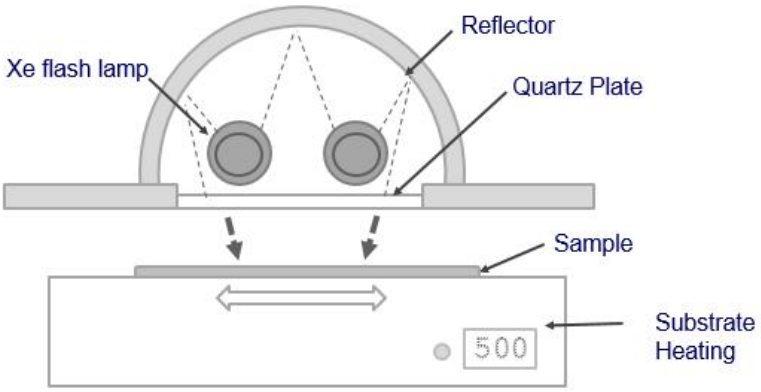

Fig. 10. FLA tool schematic [9]

2.2 Previous work

During the earlier research, large grain polycrystalline silicon channel material had been reported with columnar growth directing from the mesa edges towards the center, as seen in figure 11. However, this material was rendered not reproducible after several efforts and instead a phenomenon of silicon de-wetting was observed. The surface tension at the interface during the high intensity FLA treatment of the material caused the silicon films to ball up and form voids. The material from these voids migrated to the surviving conductive pathways, increase the thickness of the silicon layer.

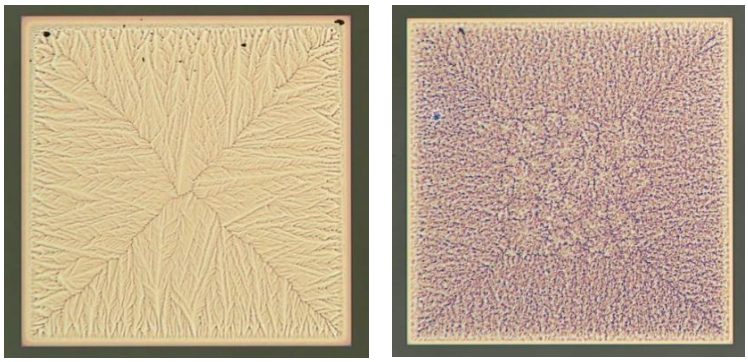

Fig. 11. Large grain Morphology with FLA at 500 V and 620 V respectively. The grains start forming at the edge of the mesas directed towards the center. [9]

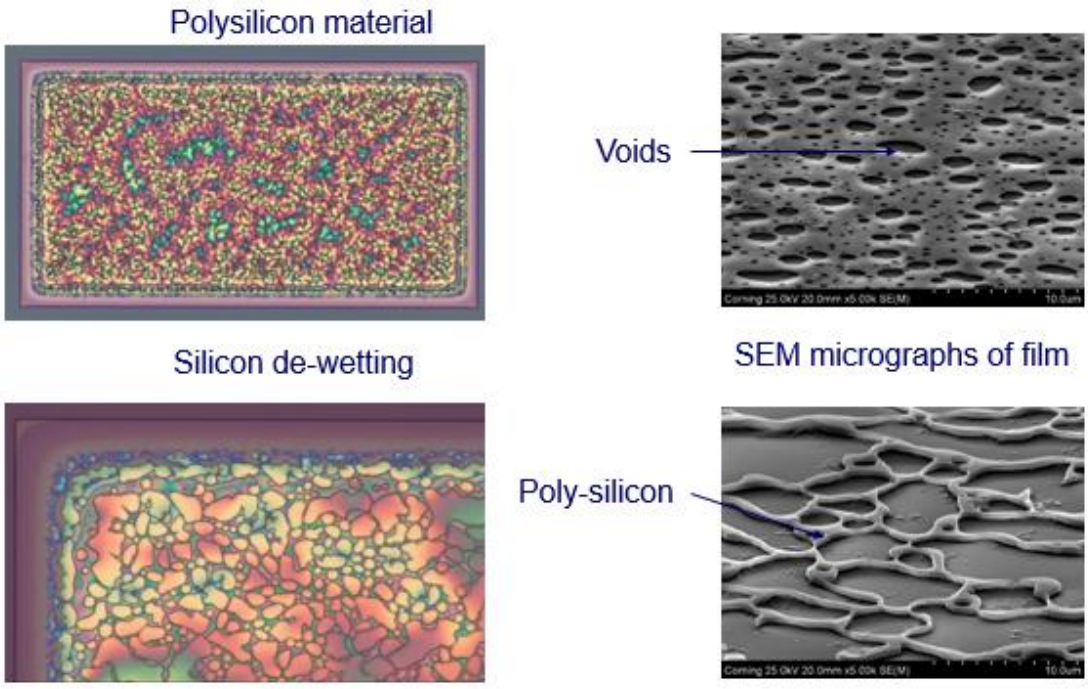

Fig. 12. Channel morphology with SEM micrographs.[9]

Figure 12 shows the SEM micrographs from the polycrystalline silicon films obtained via flash lamp annealing at high intensities. The pictures depict presence of voids in the thin layer with randomized connection of silicon islands. This morphology significantly differs from the large grain structure previously obtained. Due to the inability to replicate the large grain crystal growth, the devices were fabricated using the de-wetted material at the channel layer. The devices were doped with boron and phosphorus ion implantation prior to the FLA treatment in open source/drain regions. This presented the opportunity to use FLA treatment to crystallize the amorphous silicon material and activate the dopants simultaneously. Upon testing, the fabricated devices showed promising results with high carrier mobilities and steep subthreshold slopes as denoted in table 2. However, the transistors demonstrated a significant reduction in the effective channel length predominantly due to lateral dopant diffusion during the FLA

treatment. Thus, the devices with channel lengths smaller than 20 microns were unable to show functionality. Figure 13 shows excellent I-V characteristics for both PMOS and NMOS TFTs.

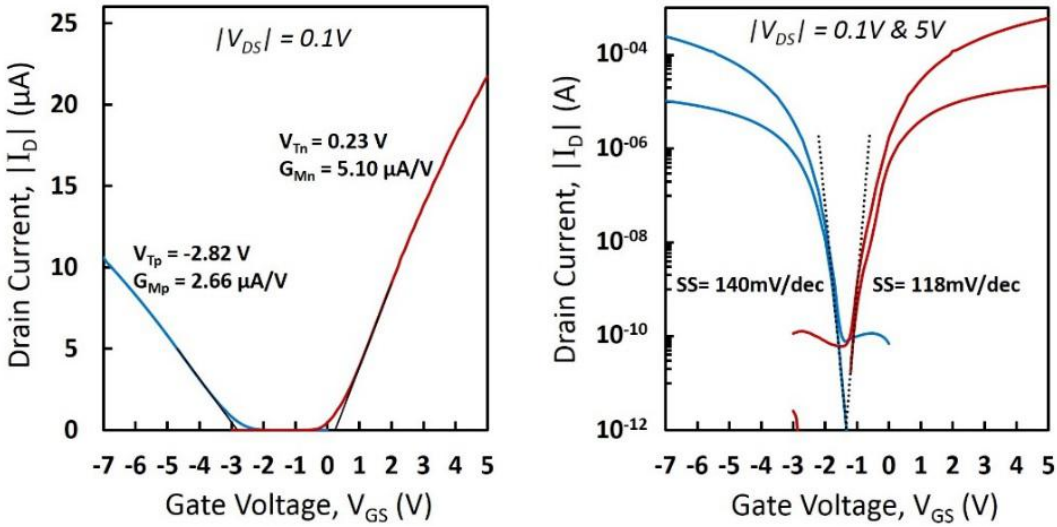

Fig. 13. NMOS and PMOS linear and log scale transfer characteristics for FLAPS TFTs with W/L = 100 µm/32 µm [10]

Table 2. Summary of best case operational parameters for previously realized FLA TFTs [9]

Parameter		NMOS	PMOS
Physical	L_{mask}	32 µm	32 µm
	ΔL	6.3 µm	13.4 µm
	L_{eff}	25.7 µm	18.6 µm
	W	100 µm	100 µm
	W/L_{eff}	3.89	5.38
	C_{ox}'	34.5 nF/cm^2	34.5 nF/cm^2
On-State	V_T	0.23 V	-2.82 V
	$g_{m(max)}$ @ $\lvert V_{DS}\rvert$ = 0.1V	5.10 µA/V	2.66 µA/V
	$\mu_{ch(max)}$	380 cm^2/V·s	143 cm^2/V·s
Off-State	$I_{(leak)}$ @ $\lvert V_{DS}\rvert$ = 5V	~ 1 pA/µm	~ 1 pA/µm
	$SS_{(min)}$	120 mV/dec	140 mV/dec

3. FLA TFT fabrication process basics

Lotus NXT glass substrates are received with 60 nm as deposited hydrogenated amorphous silicon with a 200 nm barrier layer of SiO_2 between the substrate and silicon layer. The wafers are then subjected to furnace heat treatment at 450 °C for 1 hour for a dehydrogenation anneal. The silicon thin film is then patterned into small mesas for devices of different channel lengths and widths and later etched using SF_6 RIE etch. A capping layer of 100 nm TEOS is then deposited over the patterned Si. These wafers are then subjected to flash lamp annealing using PulseForge 3300 Xe halogen lamp system. A hotplate is used for substrate heating and then material is exposed to a wavelength spectrum at certain intensity to crystallize the a-Si layer. After the FLA process, a combination of piranha clean and HPM clean is carried out on the wafers.

The next step is to pattern the source/drain regions into the capping layer and etch using 10:1 BOE mixture. Further, p-type dopants are introduced into the source and drain regions using different techniques. After this step, the capping oxide is etched off completely and a fresh layer of 100 nm TEOS is deposited as the gate oxide. Then the contact cuts are patterned and etched to expose the source/drain regions and 0.75-1 μm thick Al layer is deposited using a cold/hot sputter process. This layer is then patterned to form the source, drain and gate electrodes. Finally, the wafers are sintered in forming gas in a step process to complete the fabrication of TFT. The fabricated devices have a mask length ranging from 1-96 μm and width ranging from 12-96 μm.

4. Microcrystalline Silicon

TFTs have been realized using various materials such as oxide-based materials and semiconducting nanowires etc. and few of them exhibit potentially high-performance characteristics and yet, silicon has been adopted as the industry standard and has been a continual subject of research. Recent developments have presented microcrystalline and nanocrystalline silicon with capability to replace a-Si:H technology and can act as a substitute while efforts are being made to reduce the fabrication cost pertaining to polycrystalline Si TFTs. Microcrystalline silicon material has charge carrier mobility that is significantly high as compared to a-Si:H and comparable uniformity over large substrate areas.

Microcrystalline silicon is comprised of silicon crystallites with a grain size of several nanometers, amorphous phase material and voids. The crystallinity can be controlled via changing certain process parameters which would in turn affect the crystalline volume fraction (X_c) of the material. For example, when depositing microcrystalline silicon via PECVD, the X_c can be controlled by adjusting the source gas composition and the plasma conditions. However, it is difficult to have a very precise control due to unavailability of any real time analysis for the X_c during the deposition process. Figure 14 demonstrates the microstructure of the semiconductor layer with varying X_c ranging from 1 (complete crystallization) to zero (completely amorphous).

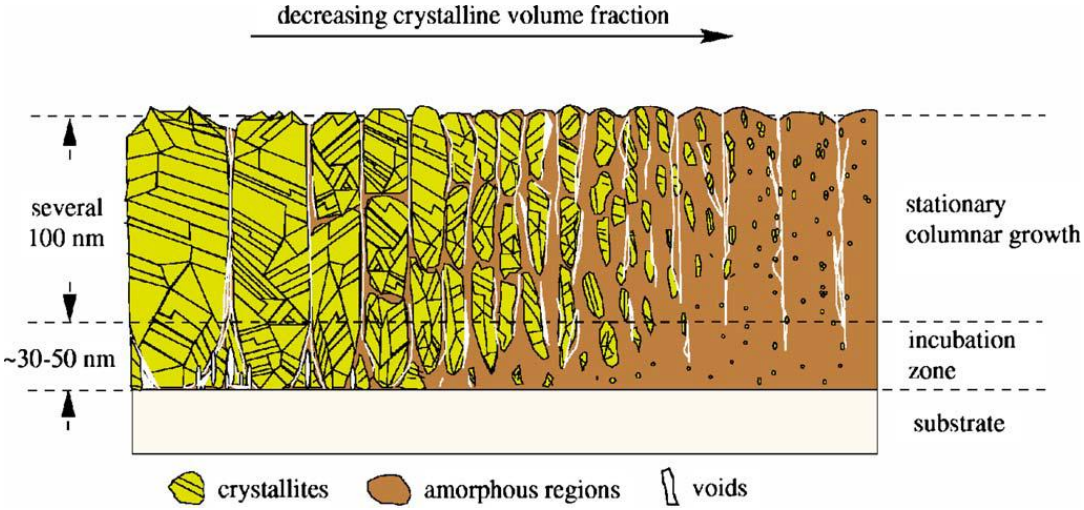

Fig. 14. Structure of microcrystalline silicon as a function of crystalline volume fraction [11]

4.1 Mixed phase morphology

Hydrogen passivation of dangling bonds in a-Si regime has been an established phenomenon used to improve the TFT performance. Interestingly in the case of microcrystalline silicon, the silicon provides self-passivation, thus alleviating trap states. Additionally, research suggests that hydrogen passivation is enhanced if the material has a mixed phase. Upon control of X_c and careful engineering of the material, the amorphous phase material in the microstructure envelopes the microcrystalline phase thus providing better interface for the hydrogen to eliminate the charge traps otherwise present and a better platform for charge conduction through the channel.

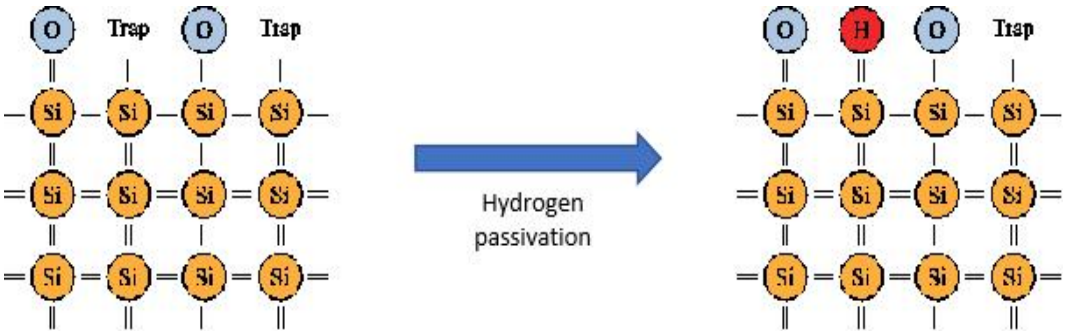

Fig. 15. A schematic of Hydrogen passivation of trap states in amorphous silicon

4.2 Motivation

The research by Chan *et al.*[12] demonstrates the effect of mixed phase morphology on the performance of TFTs by varying the X_c of the material. The crystalline volume fraction was varied by changing the gas flow rate of silane during the PECVD deposition of the material. Devices were fabricated at X_c = 47%, 54% and 66% and tested for charge carrier mobility. The results from figure 16 depict that the devices exhibit the highest charge carrier mobility of 55cm^2/(Vs) and 12 cm^2/(Vs) for electrons and holes respectively, at X_c = 54%. Furthermore, the defect densities of the tested devices were calculated to 4.1 x 10^{16} and 7 x 10^{16} cm^{-3} eV^{-1} which is in agreement with the aforementioned results. The electrical performance characteristics of the devices and other results have been shown below. Figure 17 demonstrates a more uniform and superior grain quality for the microcrystalline silicon film with X_c = 54% as compared to higher crystalline volume fractions. As seen from figure 18, the NMOS performance is much better than PMOS with regards to the current throughput and sub-threshold characteristics. Using FLA for the same concept may yield better transistor characteristics for PMOS TFTs.

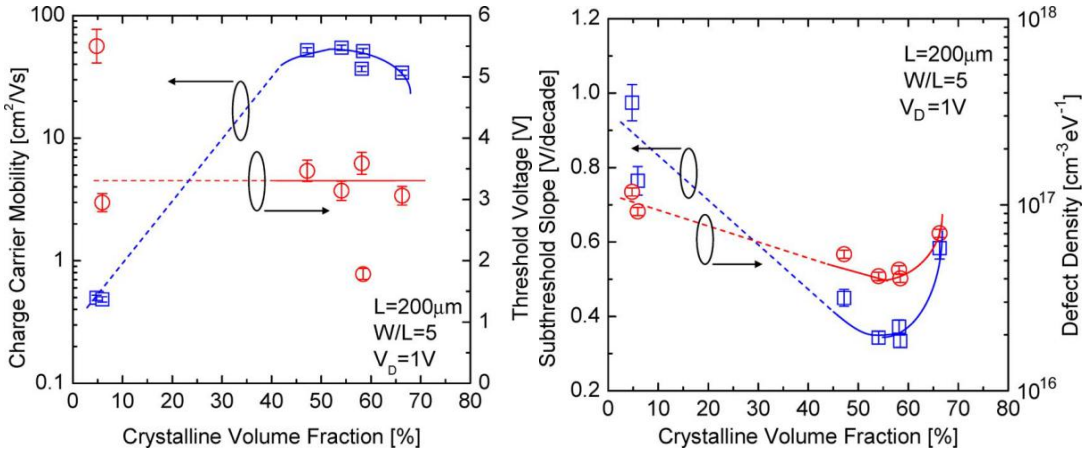

Fig. 16. Device performance parameters as a function of X_c [11]

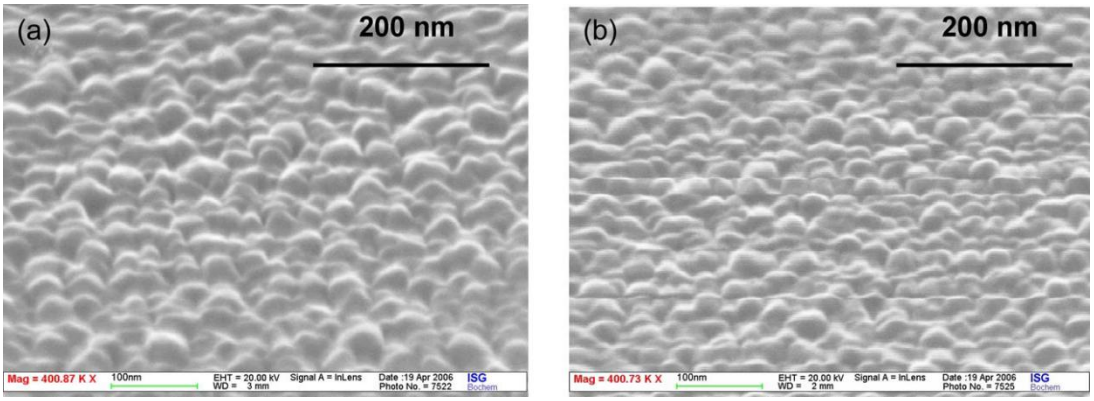

Fig. 17. SEM micrographs for 100nm layer of microcrystalline silicon (a) $X_c = 54\%$ and (b) $X_c = 66\%$ [11]

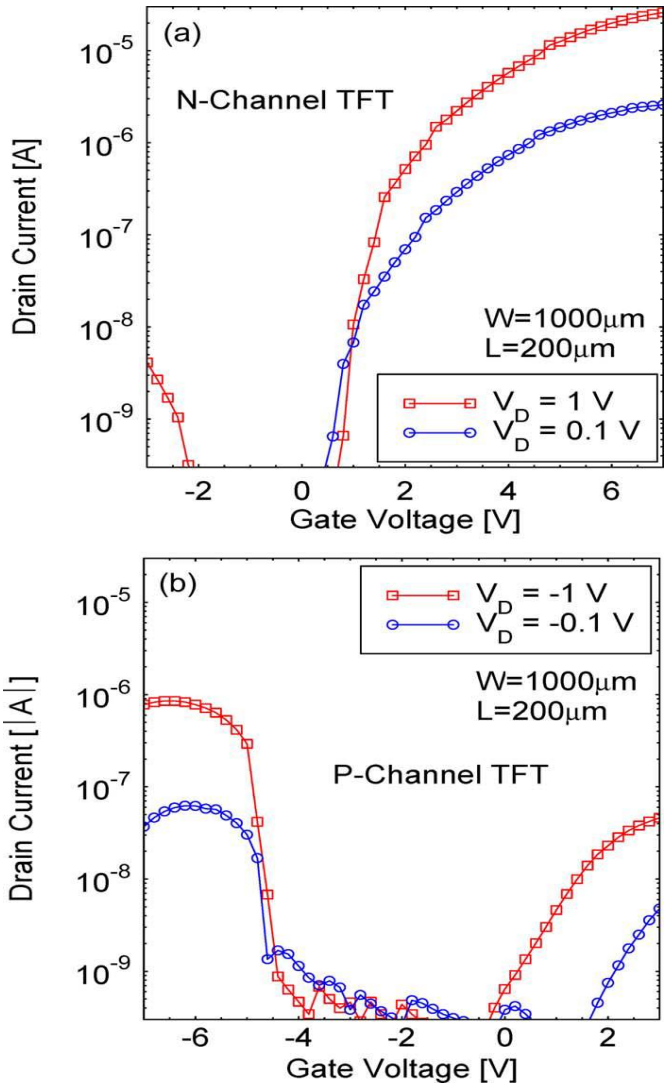

Fig. 18. Id-Vg characteristics of the TFT device [11]

4.3 Fabrication of Microcrystalline p-Channel TFTs

This approach focuses on producing the Si channel morphology with grain size ranging between 300-700 nm. Therefore, the FLA crystallization exposure energies were limited between 3.3-4.2 mJ/cm^2 with the substrate heating at 400 °C. Any thermal process beyond 500 °C will potentially crystallize the channel material completely. Therefore, to preserve the channel material morphology two different source/drain doping techniques were used.

4.3.1 Doping via Aluminum

In this process, the source/drain silicon regions were exposed and 100% pure aluminum was deposited during the metallization. Further, the wafers were subjected to furnace treatment at 450 °C for 2 hours so that the aluminum can encroach into the Si mesa, specifically the source drain regions, to dope it with p-type Al ions. The following table shows the different treatment combinations that were carried out in this experiment lot. The aluminum encroachment into the silicon channel has been carried out using two different methods; through oxide layer via contact cut and through direct contact between S/D metal and the silicon mesa. Additional sinter was done for 2 hours at 450 °C with N_2/H_2 to provide hydrogen passivation.

Table 3. Treatment combinations for Al doped microcrystalline Si channel PFETs

Wafer (Lotus NXT®)	Encroachment via contact cut	FLA crystallization (J/cm²)
W1	Yes	3.3-3.6
W2	No	3.3-3.6
W3	Yes	3.3-3.6
W4	No	3.3-3.6
W5	Yes	3.9-4.2
W6	No	3.9-4.2
W7	Yes	3.9-4.2
W8	No	3.9-4.2

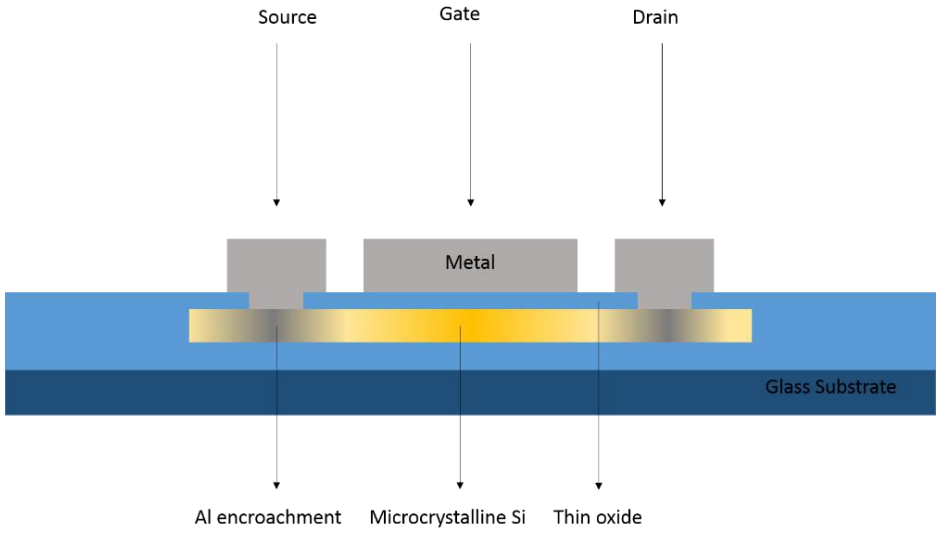

Fig. 19. Cross-sectional view of the final TFT using AST

4.3.2 Aluminum Substitution technology (AST)

Aluminum has been known to exhibit properties of reacting with silicon. The substitution reaction of aluminum for polysilicon has long been explored to fabricate self-aligned aluminum gate MOSFETs. The solid-phase reaction between the two elements depends on various factors like, crystallinity of the polysilicon, doped impurity concentration, Si content in the aluminum and the contact structure between them. Upon annealing treatment at high temperatures, aluminum can encroach into the polysilicon.

Depending on the volume of available polysilicon material and anneal duration, aluminum can extend up to microns in length. Furthermore, aluminum creates a doped region while physically diffusing into the polysilicon material being a p-type dopant. This phenomenon can be further explored for low temperature source drain doping for fabricating p-type TFTs.

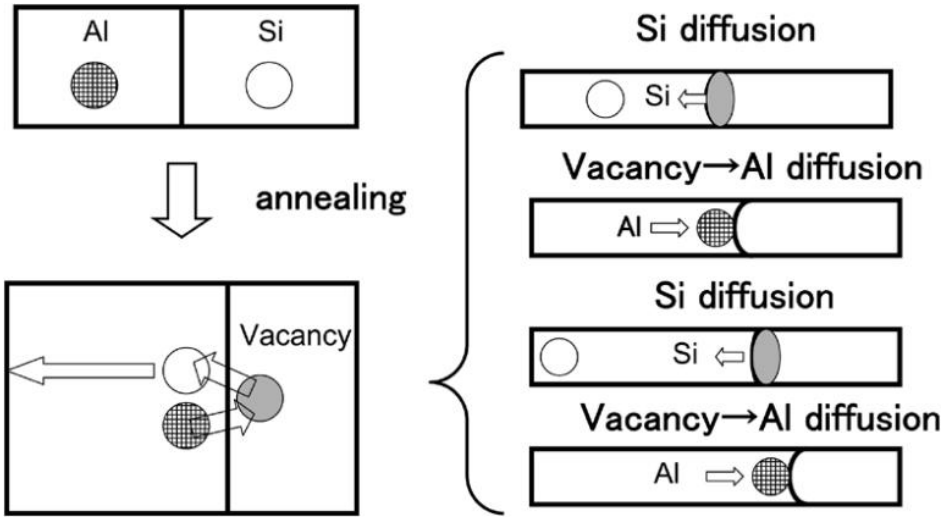

Fig. 20. Schematic diagram of AST mechanism[12]

4.3.3 Preliminary results from material characterizations

Fig. 21. Al encroachment from source/drain regions into silicon channel. As observed, the encroachment via contact cut is much more than the other case where S/D metal is in direct contact with silicon mesa. (L/W = 24/24 and 48/24 respectively)

As can be seen from the figure 21, the aluminum seems to be encroaching into silicon via capillary action. However, the uniformity of this encroachment is very inconsistent and is adversely affected when the channel is smaller in width. Surprisingly, contrary to popular belief, the encroachment through contact cuts into the oxide is significantly greater when compared to the case where aluminum is directly in contact with the silicon mesa in entirety.

4.3.4 Boron implant and FLA activation

This experiment lot incorporated a conventional boron implant with a dose of $2x10^{15}$ cm^{-2} at 35 keV. A single FLA treatment is carried out to simultaneously crystallize the a-Si layer and electrically activate the doped boron. Additionally, one wafer went through furnace activation anneal at 630 °C for 12 hours to compare the sheet resistance.

Table 4. Treatment combinations for boron doped FLA activated microcrystalline Si channel PFETs

Wafer (Lotus NXT®)	a-Si channel	Br Implant	FLA crystallization / activation (J/cm^2)
W1	100 nm	$2x10^{15}cm^{-2}$, 35 keV	3.3-3.6
W2	100 nm	$2x10^{15}cm^{-2}$, 35 keV	3.9-4.2
W3	100 nm	$2x10^{15}cm^{-2}$, 35 keV	3.3-4.2

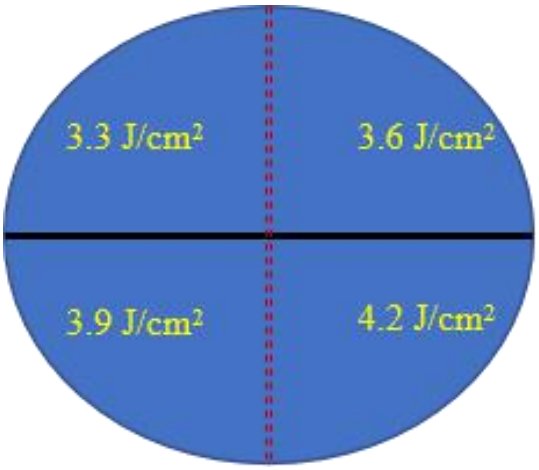

Fig. 22. Schematic of FLA dopant activation treatment on W3

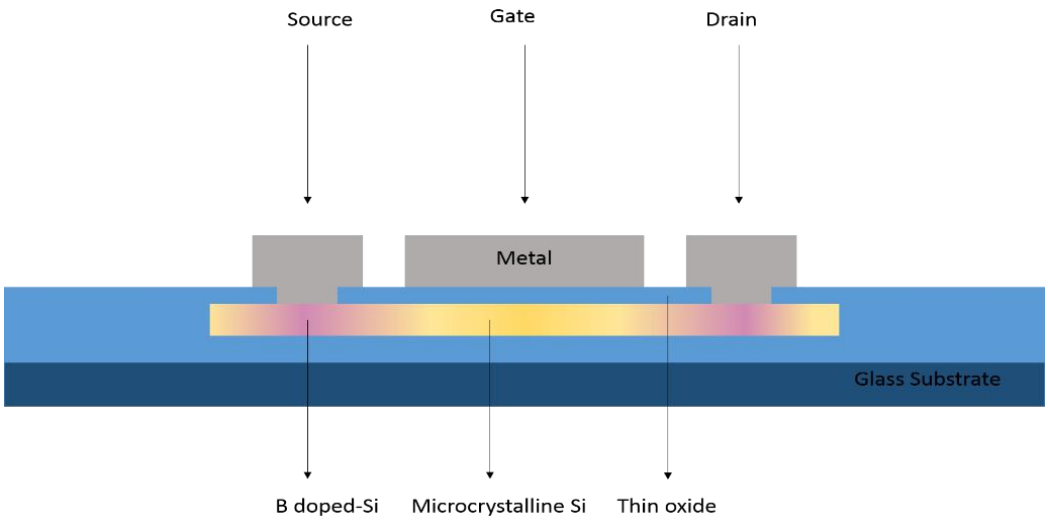

Fig. 23. Cross-sectional view of the finished TFT

4.3.5 Preliminary results from material characterizations

A 60 nm a-Si layer corning NXT glass substrate was capped with a screen oxide of 100 nm TEOS layer and implanted with B^{11} throughout at 35 keV with an ion dose of $1.5x10^{14}$ cm^{-2}. Later, the wafer was subjected to low intensity FLA exposure with energy density ranging between 3.3-4.5 J/cm^2 along with substrate heating. Then, a 4 pt. probe measurement was carried out across the wafer the measure the sheet resistance. From the

figure given below, it can be observed that FLA energies between 3.9-4.2 J/cm^2 show promising sheet resistance data with values around 3.5kΩ/□.

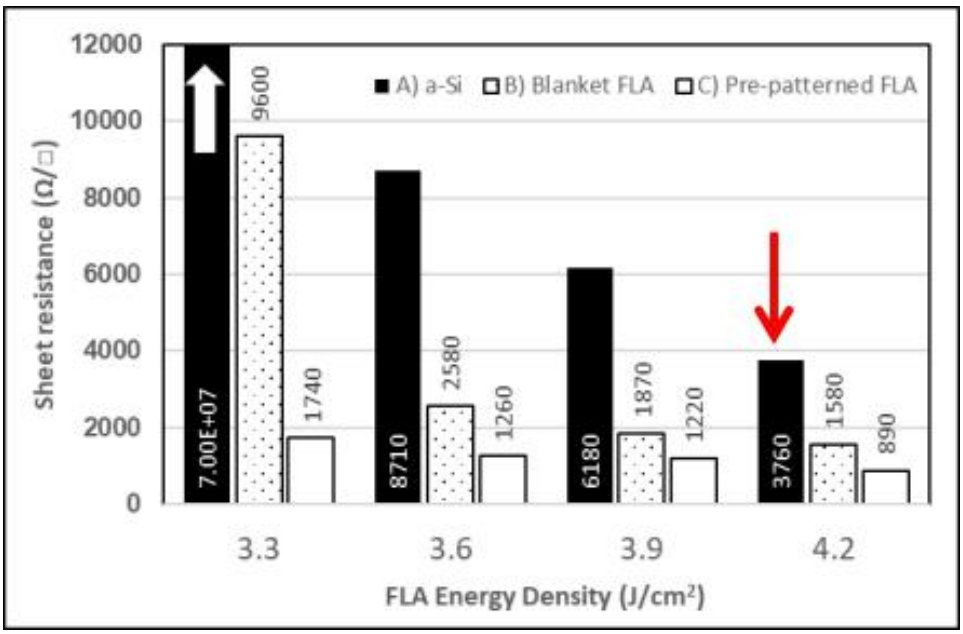

Fig. 24. 4pt. probe measurements for simultaneous crystallization and dopant activation using FLA. Sample A: Implant into a-Si. Sample B: Implant into blanket FLA-LTPS film. Sample C: Implant into patterned FLA-LTPS mesa. Activation FLA energy density as indicated. [17]

4.3.6 Final results for Microcrystalline Silicon morphology

TFT devices were realized for microcrystalline channel mixed phase morphology using both the low temperature doping techniques; AST and ion implantation followed by FLA dopant activation. However, none of the devices demonstrated good conductive behavior and turned out to be either short circuit or open circuit. This could be attributed to certain reasons that have been scrutinized further.

In the case of doping via aluminum encroachment (AST), refer to table 3, the devices has a gate under-lap of 4 microns. This meant that the aluminum was required to encroach 3-4 microns in length from either side and dope the S/D regions. However, W1,

W3, W5 and W7 that had design scheme involving encroachment via contact cut through the oxide produced too much encroachment thereby forming metal conductive pathway throughout the channel, leading to short circuits.

In the other case of W2, W4, W6 and W8, where the encroachment did not occur through the oxide, there was a presence of intrinsic regions within the S/D regions and the channel. This caused the gate to have absolutely no control over the charge conduction through the channel hence, showing open circuit behavior.

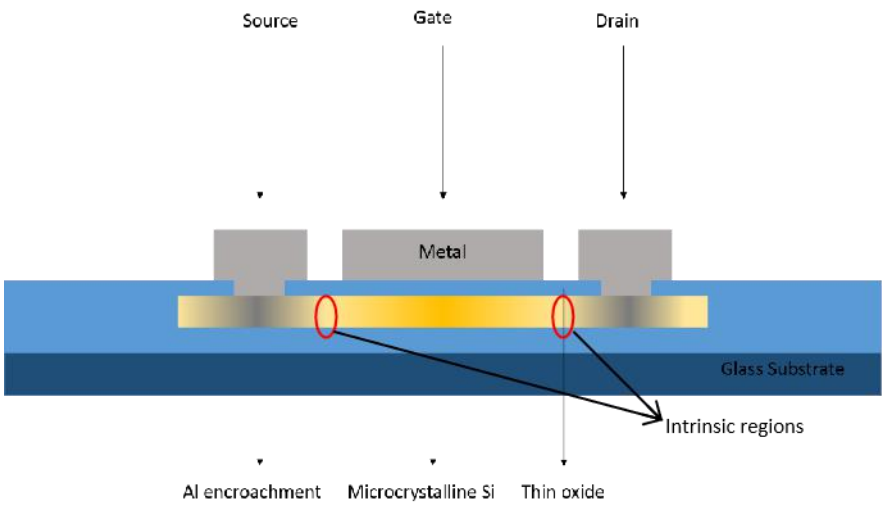

Fig. 25. A schematic diagram depicting the presence of intrinsic undoped regions within the source and drain restricting any charge conduction through the semiconductor channel.

In the other scenario in which ion implantation was used to dope the source and drain regions with boron, processing issues such as over-etch of silicon mesa and insufficient metal step coverage meant that the devices could not be tested properly. Resistors were measured by directly probing the contact regions, with characteristics shown in figure 26.

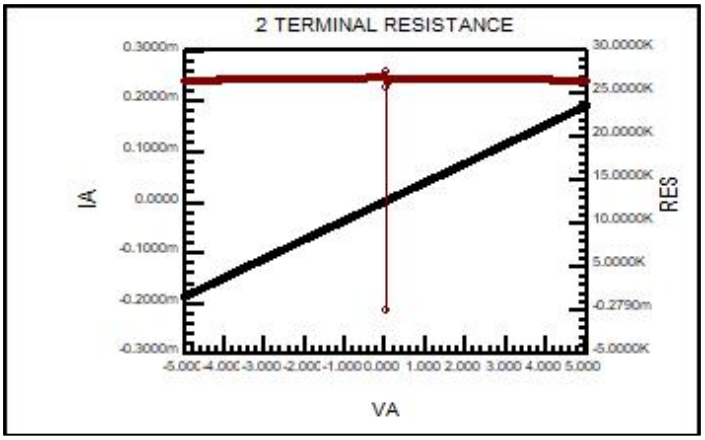

Fig. 26. Best-case resistor from W3 with of length and width of 80 and 96 microns respectively with FLA energy of 4.2 J/cm^2 yielding a sheet resistance Rs ~ 26 kΩ/□.

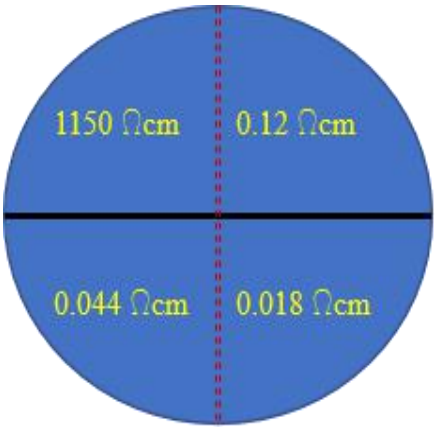

Fig. 27. Average resistivity for 80x96 resistors on W3 for different FLA activation in each quadrant of the wafer respectively.

Figure 27 provides the average material resistivity calculated from measured resistors of length 80 microns and width 96 microns. As it can be observed, the resistivity was too high, even for the highest FLA intensity (0.018 ohm-cm at 4.2 J/cm^2). This value translates to a sheet resistance was calculated as to be around 26 kΩ/□ which is much higher than the expected value of 3760 Ω/□. This result suggested that the channel region may also exhibit similar challenges in electrical quality and inhibit TFT operation, thus this approach was ceased and efforts were redirected to an alternative strategy.

5. Pre-amorphization for enhanced dopant activation

As observed in the previous work with FLA, the dopant activation along with simultaneous a-Si crystallization at high intensity FLA treatments can cause large area melting of the silicon mesa hence giving way to significant dopant diffusion. This process presents with unique scalability issue that need to be resolved for FLA to find its utilization in the FPD industry. One of the solutions in response to the dopant lateral diffusion suggests that dopants be implanted succeeding the FLA crystallization process. Ion implantation is the primary technology used to introduce dopants into silicon, however the dopants require significant thermal energy to place them into substitutional lattice sites. However, with the TFTs being fabricated on a glass substrate pertaining to their use in the display industry, this limits the thermal budget for the semiconductor processing far below the temperatures typically used for furnace or rapid thermal annealing for dopant activation.

Figure 28 shows the results from devices the receive dopant implantation after the FLA crystallization process. While these devices succeeded in demonstrating a process that would eliminate the lateral dopant diffusion in the previous work, they suffered from low dopant activation, shallow subthreshold characteristics and a significant threshold voltage shift. Moreover, the current output of these devices was limited to as high as 1μA/μm.

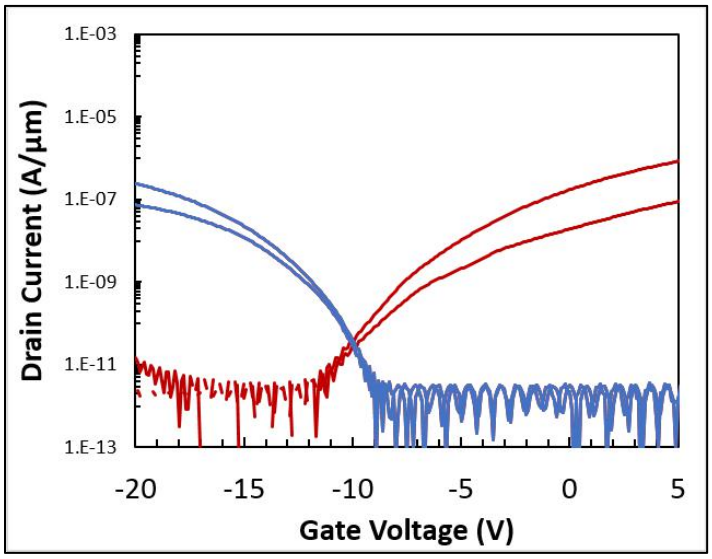

Fig. 28. Drain current vs. gate voltage for typical NMOS and PMOS devices with length of 24 µm and width of 48 µm, with boron and phosphorus dopant introduced into FLA-crystallized material. Drain biases are ± 1 and ± 10 V respectively [13]

Table 5. Device performance parameters

Parameter	NMOS	PMOS
VT	7.5 V	-16.3 V
µCH;Lin	39.1 cm2/(Vs)	12.8 cm2/(Vs)

5.1 Solid phase epitaxial regrowth (SPER)

SPER is one of the techniques used for low temperature activation of dopants. The phenomenon is only demonstrated during ion implantation into crystalline materials. During a high energy implant, the dopant ions physically interact with the crystalline lattice of the material producing damage to the crystalline structure. This may create an

amorphous region in the areas of the ion implant. When subjected to heat treatment during the electrical activation process, the crystalline phase material that is in contact with the amorphous material acts as a seed for the nucleation and promotes crystalline regrowth. The implanted amorphous phase thus reforms into adjacent crystal completing the process.

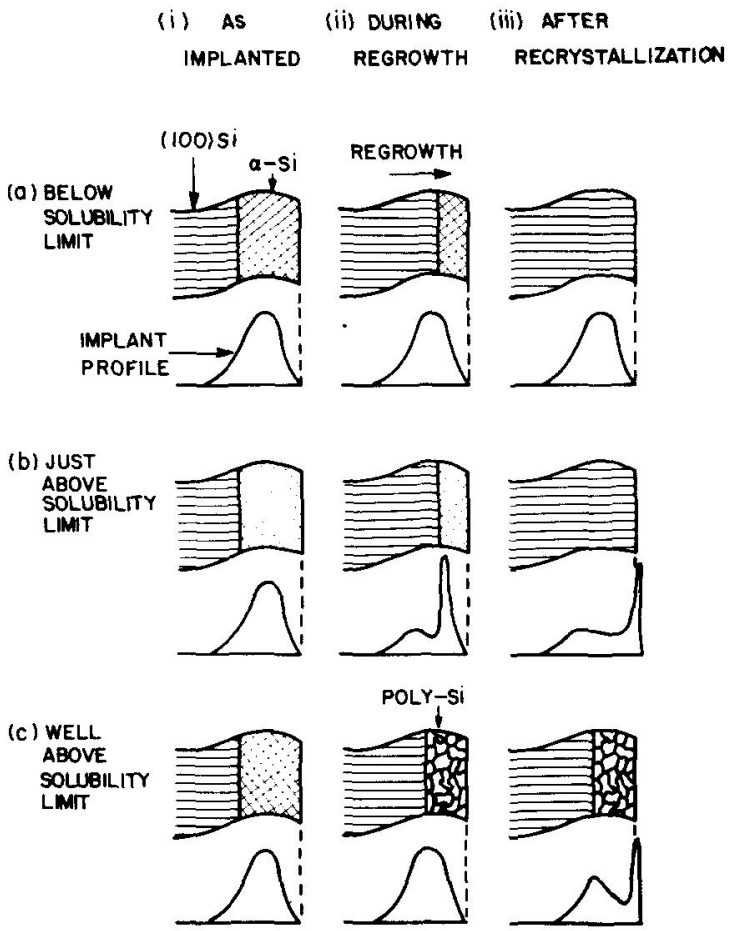

Fig. 29. A schematic of SPER mechanism[14]

It is imperative for the dopants to cause enough lattice damage during implantation to create an amorphous region to promote SPER, which is a challenge for boron due to low atomic mass and nuclear charge. Pre-amorphization has been used to promote the activation of high-dose boron implants in crystalline silicon, in both thin-

film and bulk wafer form, via SPER during 600 °C furnace annealing [15]. The species used for pre-amorphization must avoid interaction with the dopant atom and remain electrically inert. Si^+ is an obvious choice as the implant species for this purpose.

5.2 Pre-amorphization of FLA LTPS

Considering the fact that the silicon thin film layer in FLA LTPS is not crystalline, the pre-amorphization phenomena cannot take full advantage of SPER. A remaining layer of polycrystalline material will promote nucleation and solid phase crystallization (SPC) of the amorphized material during a thermal process. Experiments have been performed to study the activation of boron using Si+ pre-amorphization, with different damage distribution profiles and activation annealing conditions. Results have shown distinct advantages in boron activation levels and TFT electrical characteristics, with improvements realized using both low temperature furnace annealing and FLA activation processes.

5.3 Experiments for pre-amophization and furnace activation

The first experiment revolved around pre-implant amorphization of source drain regions of the TFTs to promote low temperature activation of boron. In this experiment, the a-Si layer is crystallized at high exposure energy equivalent to 5.2 J/cm^2 with the substrate heating at 500 °C. Later, the source/drain regions are defined and a Si pre-amorphization implant is carried out in these regions. By varying the implant energy, two amorphization regimes were established; partial pre-amorphization and total pre-amorphization. The partial pre-amorphization would crystal lattice damage only at the

surface crystal lattice structure of the polycrystalline silicon layer whereas the total pre-amorphization would damage the entire thin film in the source and drain regions. Silicon has been selected as the dopant species for the pre-amorphization implant because the self-implantation of silicon ions into a silicon lattice is guaranteed to have no chemical or electrical effect on the final material. Further, the boron activation anneal and material recrystallization anneal has been varied between 630 ºC and 700 ºC with the higher temperature being near the thermal limit of the glass substrate. The SRIM simulations have been in the following figure.

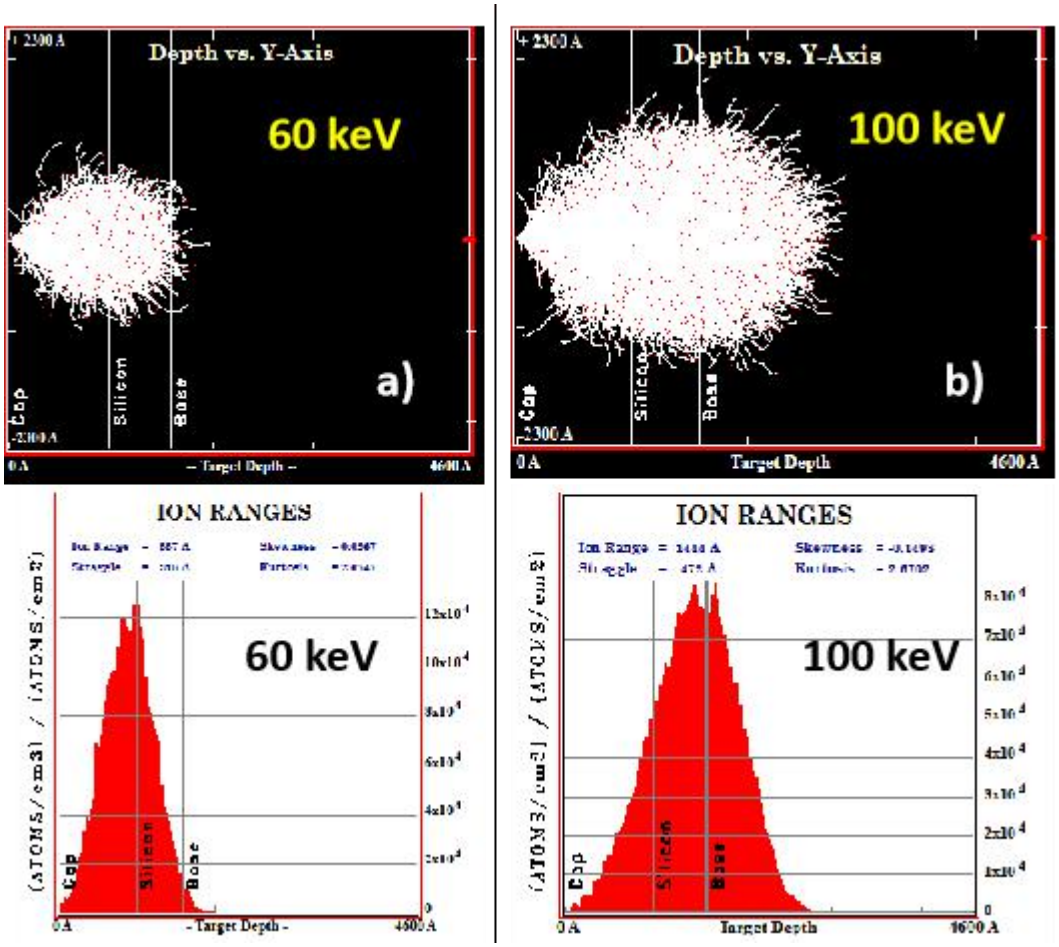

Fig. 30. SRIM simulations for Si implant into the thin film layer stack for partial amorphization at 60 keV and total amorphization at 100 keV [16]

Table 6. Treatment combinations for pre-implant amorphization experiment

Wafer (Lotus NXT ®)	a-Si channel	Silicon Amorphization Implant	B^{11} Implant	Activation Anneal
A	60 nm	$1x10^{15}$ cm^{-2}, 60 keV	$4x10^{15}$ cm^{-2}, 35 keV	N_2 @ 630 °C, 12hr
B	60 nm	$1x10^{15}$ cm^{-2}, 60 keV	$4x10^{15}cm^{-2}$, 35 keV	N_2 @ 700 °C, 12hr
C	60 nm	$3x10^{15}$ cm^{-2}, 100 keV	$4x10^{15}$ cm^{-2}, 35 keV	N_2 @ 630 °C, 12hr
D	60 nm	$3x10^{15}$ cm^{-2}, 100 keV	$4x10^{15}$ cm^{-2}, 35 keV	N_2 @ 700 °C, 12hr

5.4 Final results for amorphization and furnace activation

The TFT devices from the first experiment were tested and a comparison has been among the different treatments each device received. For partial pre-amorphization, TFTs from wafer A and B were tested. It can be seen from the figure 31 below that the devices that were subjected to higher temperature for the dopant activation anneal, sample B, perform better with a high current output of about 10 µA/µm. However, these devices exhibit high gate-induced drain leakage (GIDL) current at high drain bias. Sample A fell short in comparison to sample B due to the lower temperature anneal exhibiting lower current and poor sub-threshold characteristics. This analysis goes along with the fact that higher temperatures promote solid phase crystallization of the amorphous material along with dopant activation.

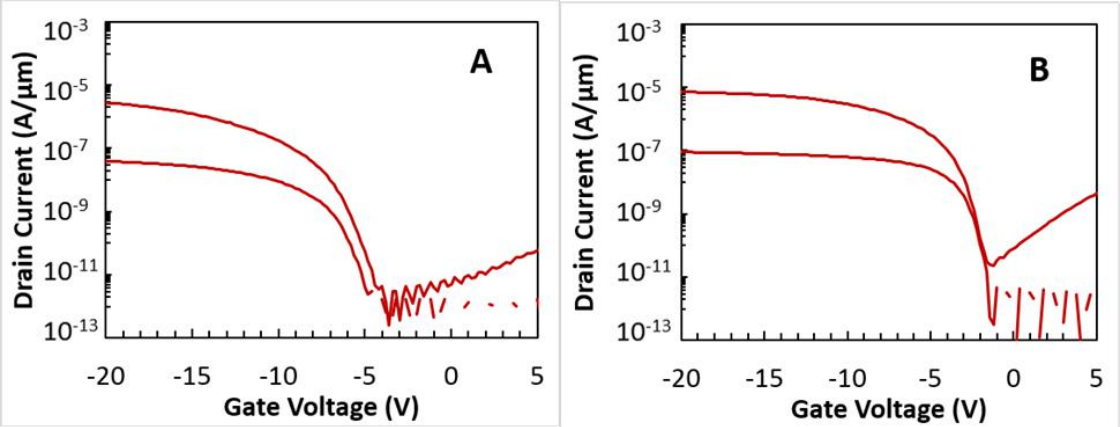

Fig. 31. Id-Vg characteristics of partially amorphized TFT devices with channel length and width of 12 µm and 24 µm respectively. Sample A and B with partial pre-amorphization implant and 630 ºC and 700 ºC furnace anneal for dopant activation respectively. [16]

For total pre-amorphization results, devices from sample C and sample D were tested. As seen in the transfer I-V characteristics below in figure 32, the total pre-amorphization is not very productive procedure. The devices exhibit poor switching behavior at low drain bias with a huge threshold voltage shift. Moreover, the output current is also severely limited as compared to devices from partial pre-amorphization. Further, sample D seems to have some advantage over sample C with higher temperature anneal improving the characteristics by some amount. These results are likely associated with low-quality polysilicon material in the source and drain regions.

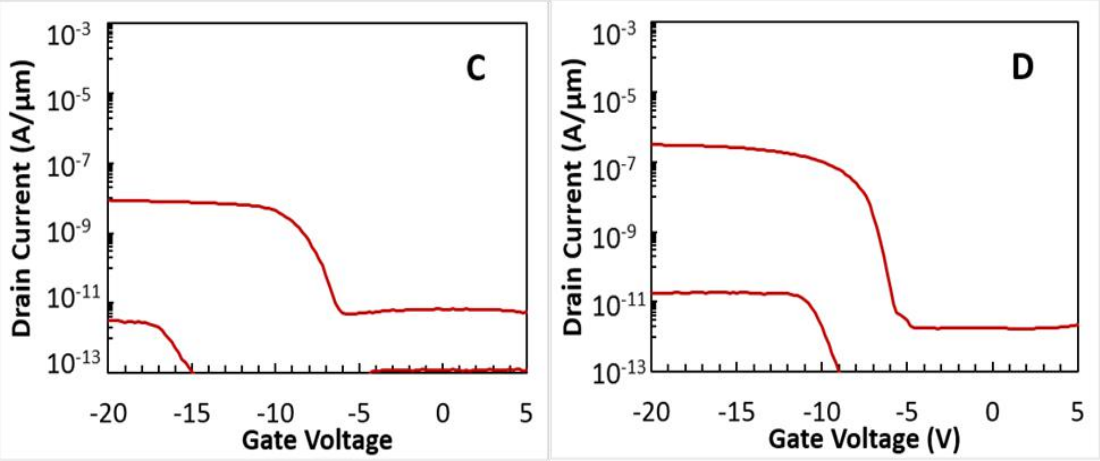

Fig. 32. Id-Vg characteristics of totally pre-amorphized TFT devices with channel length and width of 12 µm and 24 µm respectively. Sample C and D with total pre-amorphization implant and 630 ºC and 700 ºC furnace anneal for dopant activation respectively. [16]

Table 7. An account TFT performance parameters for samples A, B, C and D [16]

	630° C Activation		700° C Activation	
Partial	V_T	-7.6 V	V_T	-2.8 V
	I_{ON} @ -20 V	66.7 µA	I_{ON} @ -20 V	174 µA
	I_{OFF} @ 10 V	8.7*10^{-3} µA	I_{OFF} @ 10 V	1.1 µA
	Max $\mu_{CH;Lin}$	13.5 cm^2/(Vs)	Max $\mu_{CH;Lin}$	44.2 cm^2/(Vs)
	Yield	80%	Yield	88%
Total	V_T	-14.4 V	V_T	-9.9 V
	I_{ON} @ -20 V	0.21 µA	I_{ON} @ -20 V	7.5 µA
	I_{OFF} @ 10 V	7.8*10^{-4} µA	I_{OFF} @ 10 V	4.1*10^{-4} µA
	Max $\mu_{CH;Lin}$	--	**Max $\mu_{CH;Lin}$**	**0.04 cm^2/(Vs)**
	Yield	(Low)	Yield	30%

Implanted boron activation into a-Si is certainly possible, as shown in figure 24 (sample A), however these results show that total pre-amorphization results in significantly inferior device operation, suggesting extended defects at the source/channel and channel/drain transition regions. Partial pre-amorphization benefits from the initial FLA LTPS morphology which promotes SPC, with markedly superior TFT performance.

5.5 Pre-amorphization with FLA dopant activation

Learning from the benefits of the partial pre-amorphization, the study was extended to explore benefits in realizing non-self-aligned devices using FLA treatment for dopant activation instead of furnace treatment in the previous case. The doped boron was activated using 2 different FLA treatments; 5 pulses at 3.3 J/cm^2 and 5 pulses at 4.2 J/cm^2.

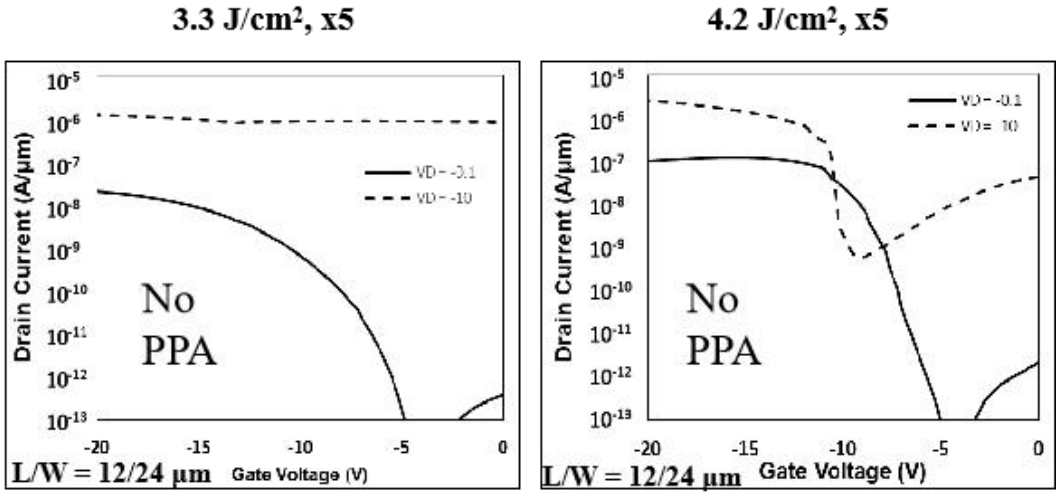

Fig. 33. Id-Vg characteristics of non-self-aligned devices without any partial pre-amorphization with FLA dopant activation. The length and width of the transistors are 12 and 24 microns respectively. [17]

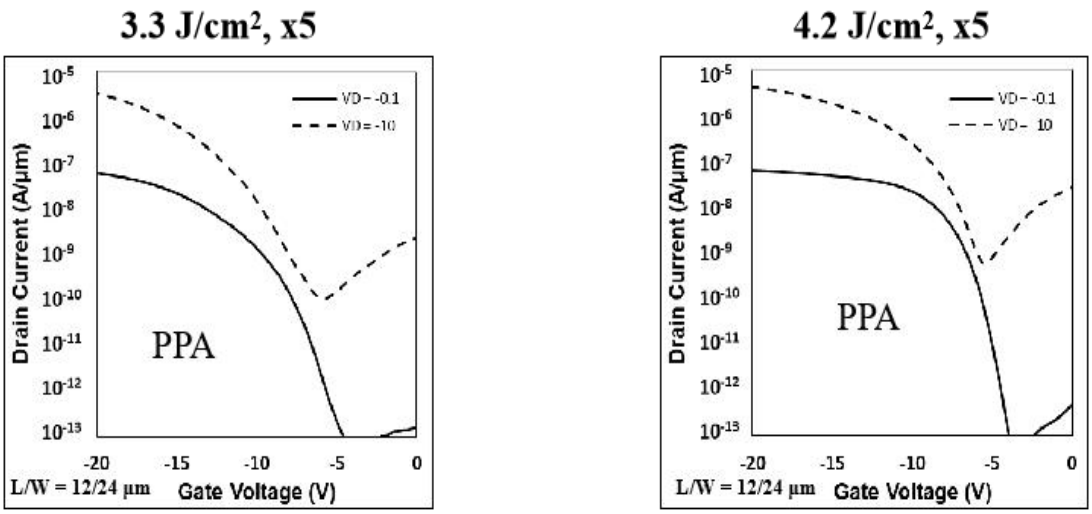

Fig. 34. Id-Vg characteristics of non-self-aligned devices with partial pre-amorphization with FLA dopant activation. The length and width of the transistors are 12 and 24 microns respectively.[17]

The plotted data in figure 33 suggests that without any partial pre-amorphization treatment, the devices suffer from lack of gate control at high drain bias of -10 V and the gate is not able to shut off the transistors. The sub-threshold characteristics of the devices are also very poor along with the significant threshold voltage shift. In the case where the devices received a partial pre-amorphization treatment, as shown in figure 34, the I-V curves demonstrate better gate control and sub-threshold performance. There is significant improvement in the current output for both low drain and high drain bias suggesting higher carrier mobility. However, there isn't any notable improvement in the threshold voltage shift and off-state leakage.

5.6 An alternative amorphization approach

The benefit of partial pre-amorphization in TFT operation was clearly demonstrated, however boron activation levels were not significantly enhanced and challenges in current drive, subthreshold slope and off-state leakage still remain. The

highest level of boron activation achieved thus far in FLA-LTPS was realized using a 12 hour furnace anneal at 630 °C in between the Si+ amorphization and boron implant processes [17]. The implanted boron was electrically activated via additional low energy FLA exposure. Finally, 4pt. probe measurements were carried out across the samples to characterize the sheet resistance values for each morphology.

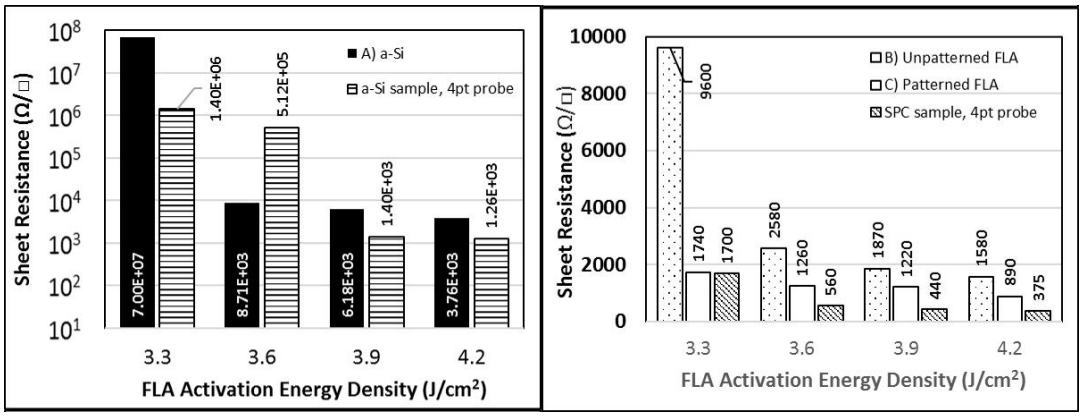

Fig. 35. Comparison of sheet resistance data for different channel morphologies using FLA dopant activation. Sample B: Implant into blanket FLA-LTPS film. Sample C: Implant into patterned FLA-LTPS mesa.Sample D: Implant into SPC polysilicon film. Activation FLA energy density as indicated. The Sample D demonstrates the lowest sheet resistance value of **375 ohm/sq** when activated at 4.2 J/cm^2.[17]

The data in the figure 35 is representative of the lowest sheet resistance values for the SPC Silicon morphology despite the presumed difference in the grain size between the three morphologies with FLA crystallized silicon having the larger grains than the former. An approach which utilizes this benefit in combination with TFT fabrication has the potential for improvements in the source/channel and channel/drain transition regions which are critical to device operation.

6. Reworking Source/Drain Morphology

A different process integration scheme has been researched for the performance improvement of PMOS TFTs. The pre-amorphization implant has remaining challenges in charge injection as indicated by the best-case effective channel mobility $\mu_{ch} \sim 40$ cm^2/(Vs) from the 700 °C furnace anneal treatment (see Table 7) in comparison to the melt-phase activation results shown in Table 2, where $\mu_{ch} > 100$ cm^2/(Vs). In addition the off-state shows pronounced GIDL, presumably due to remaining defect states that facilitate band-to-band tunneling.

Lateral end-of-range defects, caused by the heavy ions during the implant, interact with boron causing dopant segregation at the grain boundaries in the source/channel and channel/drain interface regions. An additional furnace anneal prior to dopant implant has the potential to mitigate these defects by crystallizing the newly formed amorphous S/D regions, post-amorphization implant, and convert it into a “nano-grain” region. This will minimize any boron segregation at the grain boundaries thus, providing a high quality interface between source/channel and channel/drain regions for improve charge transport.

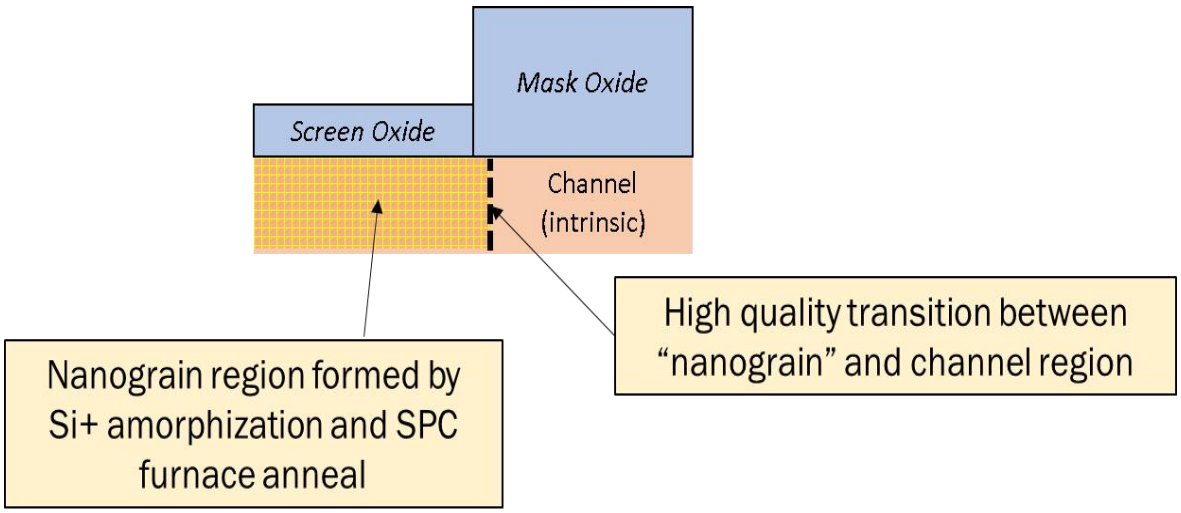

Fig. 36. A schematic of new process integration scheme highlighting the nanograin S/D region and its high quality interface with the channel region suppressing the lateral end-of-range defects.

6.1 Design of experiments and results

In this experiment, the pre-implant amorphization has been succeeded by a furnace treatment at 630 °C for 12 hours for solid phase crystallization of the source/drain silicon material. Later, boron is implanted into the source and drain at 35 keV and ion dose of $2x10^{15}$ cm^{-2}. Due to RIT implanter not being available at the time, the wafers were sent out for the Si amorphizaton. To avoid any budget implications, the amorphization implant was carried out in a different manner to compensate for partial and total amorphization of the silicon in the source and drain regions. Instead of varying the implant energy, the thickness of the TEOS capping layer was varied, while having the implant energy constant at 80 keV, to have a similar effect. A final low intensity FLA treatment is performed to electrically activate the implanted boron. The treatment combinations for this experiment have been listed in table 7. Figures 38 and 39 provide an account for the SRIM simulation carried for partial and total amorphization in silicon material in the source and drain regions.

Table 8. Treatment combinations for pre-implant amorphization and furnace crystallization experiment

Wafer (Lotus NXT®)	FLA crystallization (J/cm^2)	Amorphizaton implant (S/D)	FLA dopant activation (J/cm^2)
W1	5.0	Ar, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2
W2	5.0	Si, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2
W3	5.0	Si, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2
W4	5.2	Ar, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2
W5	5.2	Si, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2
W6	5.2	Si, $2x10^{15}cm^{-2}$, 80keV	3.6/4.2

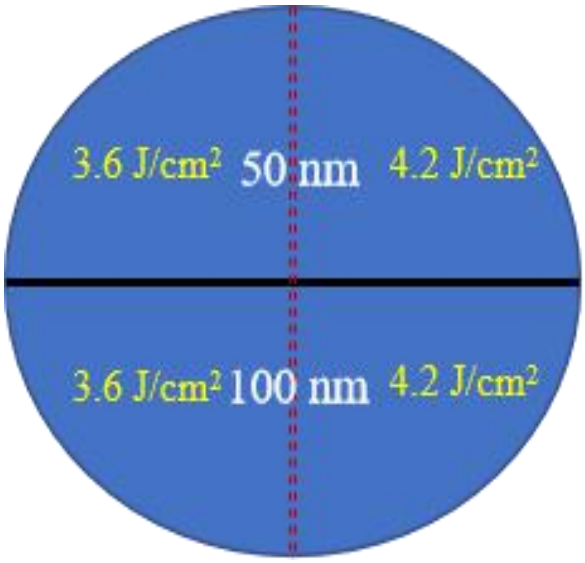

Fig. 37. A schematic of glass wafer subjected to different TEOS thickness and FLA dopant activation intensity

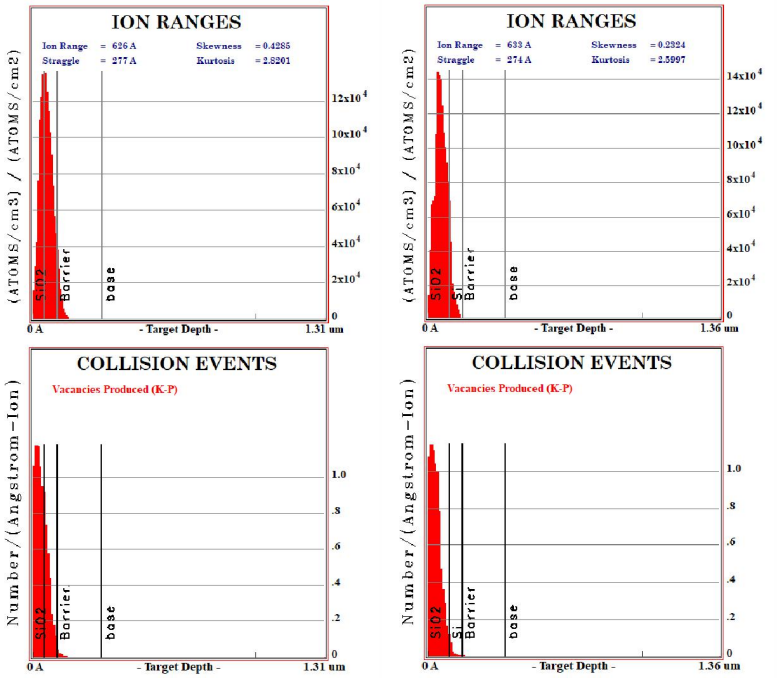

Fig. 38. SRIM simulations of Ar amorphization implant at 80 keV for (a) 50 nm SiO_2 total amorphization (b) 100 nm SiO_2 partial amorphization

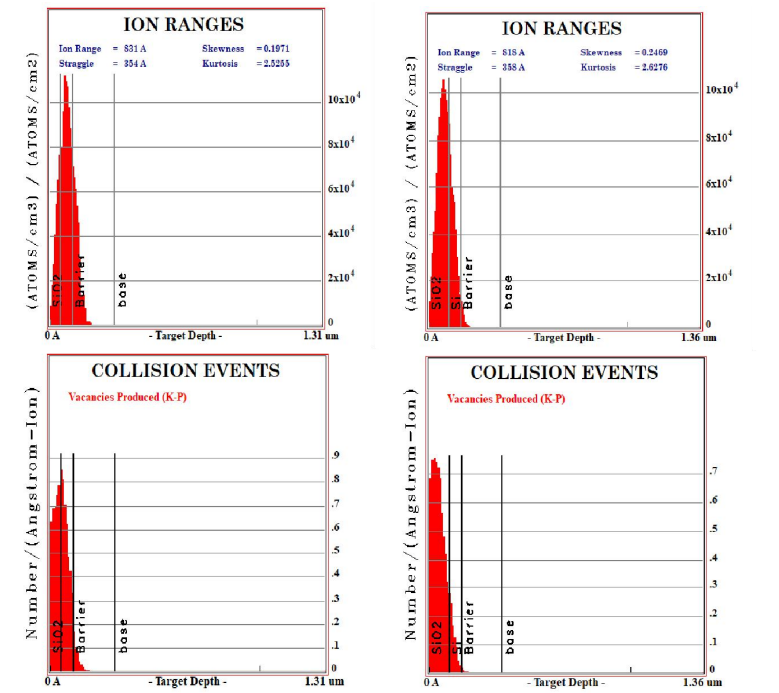

Fig. 39. SRIM simulations of Si amorphization implant at 80 keV for (a) 50 nm SiO_2 total amorphization (b) 100 nm SiO_2 partial amorphization

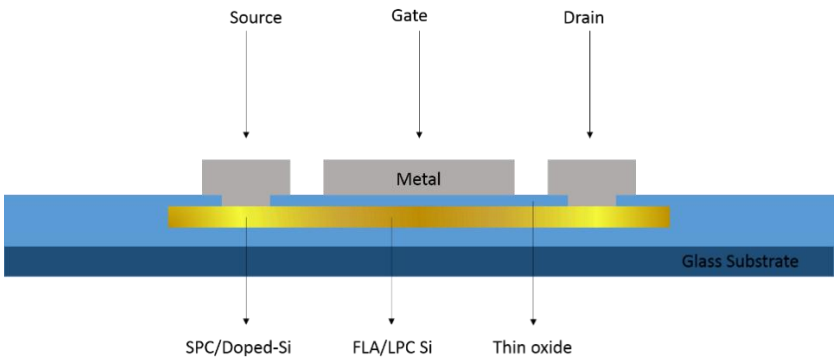

Fig. 40. Cross-sectional view of the completed TFT

The experiment was hindered by some processing issues such as silicon flaking due to implant over etch and also step coverage issues during metal deposition. W1-4 broke during different stages of processing due to compromise in the structural integrity of the glass substrate. Further, BOE over-etching undercut the mesa and caused complete delamination on almost 100% of devices. Wafer fracturing and process integration issues resulted in the inability to obtain measurable results. Figure 41 shows the state of silicon mesas prior to the metal deposition which suggests that the implanted S/D regions do not have any silicon layer remaining for any conduction whatsoever.

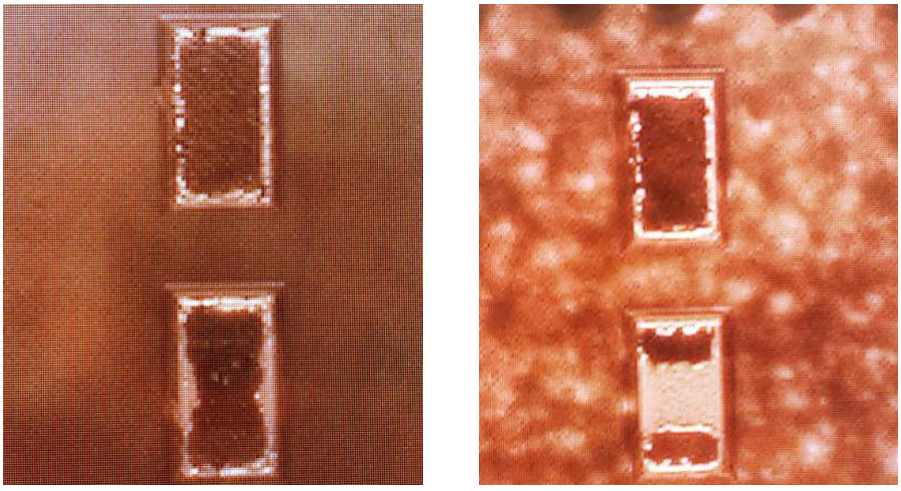

Fig. 41. Images of TFT silicon mesa prior to metal deposition. Silicon has flaked off in the implanted regions.

7. Conclusion

Two methods for implementation of FLA for both crystallization and dopant activation processes have been investigated. The first method involved a simultaneous crystallization/activation processes within the same FLA exposure using an irradiance level that maintained solid-phase material. This was in the attempt to create a mixed-phase microcrystalline/amorphous composite for the active channel region, which would potentially take advantage of self-passivating properties and improve the electrical quality of the channel region [11]. The ability to activate implanted boron using FLA below the melt threshold was verified on control samples, however the doped regions that were fabricated using the full TFT process demonstrated exceedingly high resistivity. As a result the p-channel TFTs lacked the ability to modulate charge injection, rendering them inoperable.

Efforts were then redirected towards an alternative strategy that builds on the success of previous work using Si+ pre-amorphization as a means to promote boron activation and TFT performance [16]. The application of SPC of a-Si using a 12 hour furnace anneal at 630 °C has been shown to support the lowest resistivity achieved in p+ regions doped by boron implantation FLA activation. High-intensity FLA was used to melt and crystallize a-Si, which was then re-amorphized via Si+ implant in selective source/drain regions. Samples were then furnace annealed for SPC, followed by a high-dose boron source/drain implant and FLA activation. The concept combined techniques which have separately demonstrated best-case results in achieving low p+ resistivity and good TFT performance, with the hypothesis that the low resistivity is associated with lower defect levels that may promote improved transitions between the source/drain and

channel regions, offering improved source charge injection and reduced off-state leakage. Unfortunately operational TFTs using this concept were not realized due to compromise of the semiconductor regions during fabrication. Alternative process integration schemes must be implemented for further investigation on this approach.

7.1 Future Work

To recap, the proposed strategy which remains to be demonstrated uses the following process sequence: FLA crystallization, Si+ amorphization, furnace anneal SPC, boron implantation, and finally FLA activation. Improved process integration schemes which support this strategy will be implemented in experiments which are currently in progress. Additional adjustments in factors that would be expected to have a significant impact include FLA, furnace, and PECVD process parameters; these will be studied further using a design of experiments approach.

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