A DIAGNOSTIC TEST CHIP FOR NMOS PROCESSING

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ABSTRACT

Novel test chip structures isolating process problems in certain device regions were designed in area ratios of 1x,4x, and 16x in order to investigate sizing trends. The upper three levels of an NMOS process (poly, dielectric, and metal) were fabricated. Metal line integrity structures were tested on a pass or fail basis. Results show that problems did occur in the metal patterning steps causing shorts between adjacent lines. The actual processing steps (photolithography or etching) that were responsible could not be determined without much further testing.

INTRODUCTION

Over the last few years, several diagnostic patterns have been developed by chip designers to aid in the analysis of the fabrication process. These test patterns provide feedback in areas such as alignment, level to level contacts, resistivity, breakdown voltage, leakage current, oxide reliability, and defect densities. In order to find the particular level on which problems occur (metal, poly, etc.), structures must be made to isolate and test each level. Since most devices are more concerned with interlayer problems, structures should isolate particular regions of a device. Each region of a device (i.e. source, drain, gate, and connections) has various sub-regions of which it is comprised. Thus, test structures are needed for each and every device region in order to avoid omissions in structures designed to explore electrical faults in the substrate [1].

Structures are designed with area sizings of 1x, 4x, and 16x to provide an extra dimension to validate the integrity of the results [2]. Each sizing will have different ratios of perimeter, area, and number of contacts. These ratios are made to maximize the features of the particular structure that they represent while keeping the other parameters to a minimum. Linear relationships between measured values and these ratios will indicate that the particular structure has some part in causing the device to fail. Statistical comparison of these relationships for all of the structures will narrow the problems with processing to the steps used to create a particular region or sub-region. These steps can then be monitored and altered to improve device performance.

One NMOS process at RIT has 6 masking levels and 54 different processing steps, any one of which could be a possible cause of faults. To find the step or group of steps that is causing the failure, the device regions associated with these steps must be identified. Initial runs of this 6 level NMOS process has identified six main regions of concern: metal-poly dielectric, metal line integrity, junction leakage, gate dielectric, source-drain isolation, and transistor isolation. These regions are shown in Figure 1.

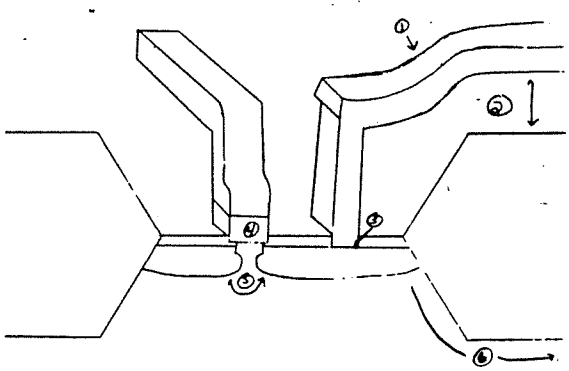

Figure 1: 6 Level NMOS Regions of Concern: 1) metal 2) dielectric 3) junction 4) gate oxide 5) source/drain 6) field oxide

Each of these regions can be sub-divided into a number of distinct sub-regions. The metal-poly dielectric has metal area over poly area, poly lines, and poly corners. Thus it needs three test structures. The junction region has four distinct subdivisions: metal-diffusion contact, area beneath the contact, field oxide edge, and gate oxide edge. The gate dielectric is composed of three sections: gate area over the channel, the gate edge along the channel, and the gate edge along the field oxide. The body of the channel and the edge along the channel are two regions of source-drain leakage. Transistor leakage can occur between source/drain regions or between inversion layers, thus two structures are again needed.

An example of sub-region breakdown is the gate dielectric regions shown in Figure 2. The processing steps responsible for leakage current will vary depending upon the sub-region that fails. The test structures maximizing the features of these regions will have cross sections similar to those shown in Figure 3A. The actual structures are shown in Figure 3B.

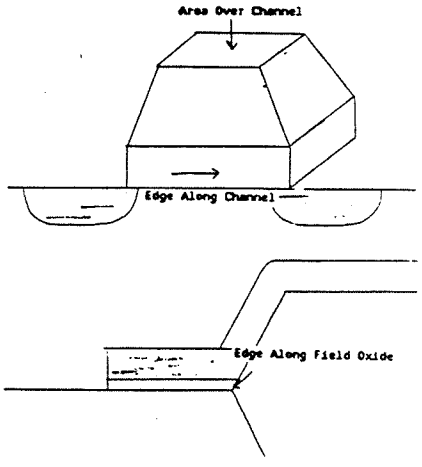

Figure 2. Gate sub-regions

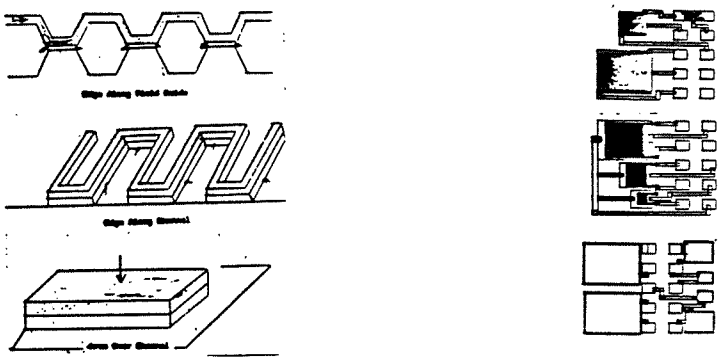

Figure 3 a) Cross section of gate structures
b) Gate sub-region structures

In this project, the following structures were designed and placed onto a testchip: electrical alignment, resistance, contact, combs, serpentines and leakage devices. The electrical alignment structures are used to measure the x,y alignment of contacts to a conducting structure (diffusion, poly) by forcing current through a resistive path and reading the voltage values at designated areas [3]. Van der Pauw structures are used to determine the sheet resistance by measuring the voltage difference due to a forced current across a square region. The contact structures consist of via chains of interwoven layers. Combining these with various combs and serpentines results in a matrix of structures that can be analyzed to pin-point the causes of shorts and opens inter- and intra- level. All of these structures provide information on the integrity of the leakage structures. For example, failing contact vias would imply that the leakage structures requiring contacts may be invalid due to bad connections. This feedback, along with the leakage structure data, is then used to find the particular processing steps that are causing the device failures.

EXPERIMENT

Test structures that modelled each sub-region were designed using ICE, an RIT graphics layout program. All three sizings of each structure were placed in a 1mm by 1mm cell so that it can be easily transferred to other layouts. A reticle set of the upper layers (Poly, CC, Metal) was made from the ICE mann files. 10 wafers (including dummies) had 5000 A of poly-Si deposited upon them. The poly was imaged using the appropriate mask with the GCA4800 wafer stepper. The poly was dry etched with SF6/02. A phosphosilicate glass was then spun on each wafer and the glass was flowed at 1000 deg C. Contact cuts were made through the glass using buffered HF. Metal was then evaporated onto the wafers using the CVC evaporator. The metal was patterned on the GCA wafer stepper, and then etched in Aluminum etchant. The metal integrity structures were then tested for leakage using a +5 volt supply. The pass/fail current was arbitrarily chosen to be 1 uA.

RESULTS

Table 1 lists the parameters associated with the test structures. A layout of the test chip is in Appendix A.

Table 1
Chip Layout Parameters

Structure		Diff Area *Metal (sq.um)	#CC(Area) +to Poly (sq.um)	Perimeter (um)	Other (Poly) (sq.um)	
GATE REGION						
1. Gate Edge	a	25.6	2 (200)	1,100	5.5	
	b	57.6	2 (200)	4,020	20.1	
	c	160	2 (200)	10,660	53.3	
2. Field Edge	a	10	2 (200)	760	3.6	
	b	40	2 (200)	3,510	17.1	
	c	160	2 (200)	14,220	70.2	
3. Area	a	10	1 (100)	400	14.4	
	b	40	1 (100)	800	48.4	
	c	160	1 (100)	1,600	176.4	
JUNCTION						
4. Area	a	10	1 (16)	400	-	
	b	40	1 (16)	800	-	
	c	160	1 (16)	1,600	-	
5. Under Contacts	a	10	54 (864)	400	-	
	b	40	171 (2736)	800	-	
	c	160	256 (4096)	1,600	-	
6. Field Edge	a	10	2 (200)	760	3.6	
	b	40	2 (200)	3,510	17.1	
	c	160	2 (200)	14,220	70.2	
SOURCE/DRAIN						
7. Edge	a	0.24	3 (300)	120	6 gates	
	b	0.96	5 (500)	480	24 gates	
	c	3.52	7 (700)	1,760	88 gates	
METAL-POLY DIELECTRIC						
8. Area	a	10*	1 (100)	400	14.4	
	b	40*	1 (100)	800	48.4	
	c	160*	1 (100)	1,600	176.4	
9. Edges	a	2.5*	2 (200)+	200	1.0	
	b	10*	2 (200)+	800	4.0	
	c	40*	2 (200)+	3,200	16.0	
10.Corners	a	10*	1 (100)+	720	3.6	32a
	b	40*	1 (100)+	3,040	15.2	144a
	c	160*	1 (100)+	13,860	69.3	684a

METAL INTEGRITY	Area (sq.um)	Overlap Area (sq.um) Serpentine	Combs
11. Lines	10K	240	192
	40K	864	768
	160K 3,672	3,456	
12. Uneven Lines	10K	600	480
	40K	1,728	1,536
	160K	4,896	4,608
13. Uneven Thick	10K	720	576
	40K	2,160	1,920
	160K	8,568	8,064
14. Over Grid	10K	216	-
	40K	1,440	-
	160K	8,640	-

a- number of corners in structure
NOTE: Structures used for more than 1 test.
#1 Source/Drain Body and Junction Edge
#2 Inversion Layer Isolation
#6 Transistor Isolation

Table 2: Testing Results

Structure	Size	Percent Passing Serpentine	Comb
11. Met-Poly Lines	S	100	67
	M	100	0
	L	100	0
12. Met-Poly Uneven Lines	S	100	100
	L	100	20
13. Met-Poly Uneven Thickness	S	100	50
	M	100	33
	L	100	0
14. Met-Poly Grid	S	100	-
	M	100	-
	L	100	-

These results tend to indicate that there are problems with adjacent lines in the metal lithography and etching steps. The percent failing increases with structure size due to the higher probability of a short in the larger area. To differentiate between the actual cause (photolithography or etching), more structures would have to be tested.

ACKNOWLEDGMENTS

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REFERENCES

[1] W. Lukaszek et al., Solid State Technol., vol. 29, no. 3, pp.87-93,Fall 1986.

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[3] M. G. Buehler, Solid State Technol., vol.22, no.10, pp 89-94,Oct. 1979.

APPENDIX A

TESTCHIP