Rochester Institute of Technology
RIT Digital Institutional Repository

Theses

12-20-2018

On the Reversible Effects of Bias-Stress Applied to Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors

Anish Suresh Bharadwaj
asb4349@rit.edu

Follow this and additional works at: https://repository.rit.edu/theses

Recommended Citation

Suresh Bharadwaj, Anish, "On the Reversible Effects of Bias-Stress Applied to Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors" (2018). Thesis. Rochester Institute of Technology. Accessed from

This Thesis is brought to you for free and open access by the RIT Libraries. For more information, please contact repository@rit.edu.

On the Reversible Effects of Bias-Stress Applied to Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors

Anish Suresh Bharadwaj

On the Reversible effects of Bias-Stress Applied to Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors

Anish Suresh Bharadwaj

December 20th, 2018

A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

R.I.T | KGCOE

Department of Electrical and Microelectronic Engineering

On the Reversible effects of Bias-Stress Applied to Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors

Anish Suresh Bharadwaj

Committee Approval:

____

Dr. Karl Hirschman Date
Advisor
Micron Professor, Microelectronic Engineering

____

Dr. Michael Jackson Date
Associate Professor, Microelectronic Engineering

____

Dr. Robert Pearson Date
Program Director, Microelectronic Engineering

Acknowledgments

I would like to thank everyone whose guidance and support helped me complete this project successfully. To begin with, I would like to thank Dr. Karl Hirschman, my thesis advisor who provided me with the opportunity to work on this project. None of this would have been possible without his continuous guidance and support. Secondly I would like to acknowledge my thesis committee members Dr. Michael Jackson and Dr. Robert Pearson for the guidance and feedback they provided. I would like to thank Tarun Mudgal, our group's Ph.D mentor for tutoring me, Nicholas Edwards and Prashant Ganesh for working as a team from the beginning. I owe team eagle research group my acknowledgements for all support throughout this project. I would specially like to thank the SMFL staff including Patricia Meller and Sean O'Brien for helping me getting certified on all relevant tools in the fab, John Nash, Bruce Tolleson, Rich Battaglia, Scott Blondell and Tom Grimsley for their timely assistance during issues. Finally I would like to thank all of RIT's faculty and staff for without their support this project would not have been possible.

Abstract

The role of amorphous IGZO (Indium Gallium Zinc Oxide) in Thin Film Transistors (TFT) has found its application in emerging display technologies such as active matrix liquid crystal display (LCD) and active matrix organic light-emitting diode (AMOLED) due to factors such as high mobility 10-20 $cm^2/(V.s)$, low subthreshold swing (~120mV/dec), overall material stability and ease of fabrication. However, prolonged application of gate bias on the TFT results in deterioration of I-V characteristics such as sub-threshold distortion and a distinct shift in threshold voltage. Both positive-bias and negative-bias affects have been investigated. In most cases positive-stress was found to have negligible influence on device characteristics, however a stress induced trap state was evident in certain cases. Negative stress demonstrated a pronounced influence by donor like interface traps, with significant transfer characteristics shift that was reversible over a period of time at room temperature. It was also found that the reversible mechanism to pre-stress conditions was accelerated when samples were subjected to cryogenic temperature (77 K). To improve device performance BG devices were subjected to extended anneals and encapsulated with ALD alumina. These devices were found to have excellent resistance to bias stress. Double gate devices that were subjected to extended anneals and alumina capping revealed similar results with better electrostatics compared to BG devices. The cause and effect of bias stress and its reversible mechanisms on IGZO TFTs has been studied and explained with supporting models.

Table of Contents

Signature Sheet i

Acknowledgments ii

Abstract iii

Table of Contents iv

List of Figures vi

List of Tables x

List of Symbols xi

1 Introduction to Thin Film Transistors 1

1.1 Historical Overview of Thin Film Transistors 1

1.2 Liquid Crystal Displays 2

1.3 Organic Light Emitting Diode (OLED). 4

1.4 Next Generation Displays. 5

1.5 Hydrogenated Amorphous Silicon. 6

1.6 Candidates to Replace a-Si:H. 9

2 Overview of Amorphous Indium Gallium Zinc Oxide (IGZO) 12

2.1 Amorphous Oxide Semiconductors. 12

2.1.1 Conduction mechanism in Amorphous Oxide Semiconductors. 13

2.2 Prospective of Zinc Oxide Thin Film Transistors. 14

2.3 Development of IGZO TFTs. 15

2.4 Motivation for the Study of IGZO TFT Instabilities: Bias Stress. 19

3 Bias Stress Instability of IGZO TFTs 20

3.1 Preliminary Research 20

3.1.1 Positive Bias Stress. 20

3.1.2 Negative Bias Stress. 21

3.2 Initial Experimentation. 22

4 TFT Fabrication 24

4.1 Staggered Bottom-Gate TFT. 24

4.2 SiO2 Passivated TFTs. 26

4.3 Dual Gate TFTs 27

5 Results and Discussions 29

5.1 Effect of Bias Stress on BG TFTs. 29

5.1.1 Response to Positive Bias Stress. 29

5.1.2 Response to Negative Bias Stress. 32

5.2 Reversible Stress Response in BG TFTs. 34

5.2.1 Relaxation at Room Temperature 34

5.2.2 Proposed model for bias stress and relaxation. 36

5.2.3 Trap Associated Barrier Lowering (TABL). 39

5.2.4 Relaxation at Cryogenic Temperature. 40

5.3 Improved Passivation Anneal and Alumina encapsulation. 42

5.3.1 Alumina encapsulated BG TFTs. 42

5.3.2 Response to DG devices. 43

6 Conclusion 46

6.1 Future Work. 48

References 49

List of Figures

1.1 History of TFT and IC development. 1

1.2 Cross section of an LCD. 3

1.3 Schematic of an active-matrix LCD circuit. 3

1.4 Cross section of an OLED active-matrix. 4

1.5 Summary of required carrier mobility for future displays. .6

1.6 First a-Si:H transfer characteristics. 7

1.7 H atoms tie up the dangling bonds inherent to a-Si. 7

2.1 Indication of oxide TFTs depicting a steady growth in manufacturing. 12

2.2 Shell level representation of covalent and ionic semiconductors in. 13
(a) crystalline and (b) amorphous structures

2.3 Current-voltage characteristics and differential mobility extraction of the. 14
PE-ALD deposited ZnO TFT

2.4 Structure of crystalline IGZO 16

2.5 Defect state concentration integrated over energy near E_C for IGZO TFTs. 17

2.6 Current-voltage characteristics of un-passivated IGZO TFT fabricated at RIT. . . .19

3.1 Transfer characteristics of a TFT for positive gate bias stress test. 21

3.2 Transfer characteristics of a TFT for negative gate bias illumination stress test. . .22

3.3 Transfer characteristics of a TFT fabricated at RIT depicting a negative shift in . . 23
V_T under the influence of NBS

4.1 Top-down (left) and cross-sectional illustration (right) of un-passivated BG TFT. . 25

4.2 Current-voltage characteristics of BG un-passivated device with L/W=24/100 µm. 25

4.3 Cross-section of a passivated BG TFT. 26

4.4 I-V characteristics (left) for a passivated device showing shallow sub-threshold. . . 27
swing and family of curves, I_{DS}-V_{DS} depiction the same device

4.5 Schematic of a dual/double gate TFT. 28

4.6 Current-voltage characteristics of a L/W=24/100 µm device and (b) family of. . . . 28
curves, I_{DS}-V_{DS} depiction the same device

5.1 BG device under the influence of PBS showing no effect on device 30
characteristics. Shallow sub-threshold swing for typical passivated device is
as shown in figure 4.4.

5.2 ATLAS simulation showing electron concentration of BG TFTs in un-biased 30
state (left) and in positive-stress (right)

5.3 (left) PBS for 2000s causing distorted characteristics with a slight left shift 31
due to the presence of remaining interface traps. The distortion appears to
manifest itself as a 'hump' that is associated to a trap state that is induced
during PBS. (right) TCAD simulation depicting hump-like behavior in PBS
with reduced Vo energy state.

5.4 (left) Schematic representing ionized oxygen vacancies as fixed positive 32
charges at the back-channel interface. (right) I-V characteristics of
L/W=24/100 µm device showing a significant left shift in V_T under NBS

5.5 BG device under the influence of NBS at -15V for 2000s. 33

5.6 Electron concentration of BG device in negative-stress. 33

5.7 Depiction of a BG TFT exhibiting auto relation after subjected to 2000s NBS. . . 35

5.8 Time resolution of the auto-recovery process for a device subjected to 2ks NBS. .35

5.9 IGZO energy band diagram, showing single-donor (V_O^+) and double-donor. 36
(V_O^{2+}) oxygen vacancy defect states within the bandgap. The Fermi Energy
(E_F) is approximated at flatband and NBS conditions. Using the indicated
energy differences referenced to E_V, the energy levels for the V_O^+ and V_O^{2+}
states are calculated to be 70 meV and 500 meV below E_C, respectively.
Figure adapted from Chowdhury et al

5.10 Representative response to NBIS, shown previously in chapter 3. 37

5.11 Proposed Configuration coordinate diagram by Chowdhury et al. for the. 38
creation and relaxation of NBIS defects; NBS instability presumed to be of
similar origin. State definitions are described in the corresponding narrative.
The zoomed-in region identifies the state transitions and associated activation
energies, both forward and reverse, between a "weak bond" neutral defect
(WB) and the double-donor V_O^{2+} defect created during NBS which is not in
thermal equilibrium once NBS is removed

5.12 A BG device where application of negative-stress makes TABL disappear. 39

5.13 TCAD model of TABL (right), where high-trap regions at the back-channel. . . . 40
are separated by well passivated gaps. The contours identify the probability of
occupancy of trap states which is dependent on the gate bias. The simulated
I_D-V_{GS} transfer characteristics (left) show three scenarios: Large passivation
gaps which are desirable (green); smaller passivation gaps (0.2 μm) which
result in TABL (blue); no passivation gaps (red) which shows significant
left-shift and distortion

5.14 Depiction of a BG TFT exhibiting accelerated recovery under the influence. 41
of LN2.

5.15 Schematic representation of BG TFT capped with ALD Al_2O_3. 41

5.16 BG passivated L/W=24/100 μm TFT with extended 8 hour anneal and ALD. . . 43
Al_2O_3 encapsulation showing very good resistance to NBS

5.17 ATLAS simulation showing electron concentration in DG devices under (left) . . 44
un-biased state (middle) negative-stress and (right) positive-stress

5.18 DG device with increased 8 hr anneal with capped ALD alumina under the. 45
influence of PBS (left) and NBS (right)

List of Tables

1.0 Comparison between a-Si:H, LTPS and a-IGZO material properties. 9

2.0 Parameters used in TCAD simulations to extract the density of states for. 18
IGZO TFTs

3.0 Bias stress conditions incorporated in our study. 22

List of Symbols

Term	Description	Units/value
C'_{ox}	Oxide capacitance per unit area	F/cm^2
E_g	Band gap energy	eV
E_{OV}	Energy of oxygen vacancies	eV
g_m	Transconductance	S
I_D	Drain current	A
L	Channel length	µm
N_{GD}	Donor-like states defining Gaussian distribution	$/cm^3/eV$
E_{GD}	Mean energy defining Gaussian distribution for donor-like) states	eV
W_{GD}	Standard deviation of Gaussian distribution for donor-like states	eV
W	Channel width	µm
N_{TA}	Density of acceptor-like states in the tail distribution at the conduction band	$/cm^3/eV$
W_{TA}	Decay energy of conduction band-tail states	eV
V_O	Neutral oxygen vacancy defects	eV
V_O^+	singly charged oxygen vacancy defects	eV
V_O^{2+}	doubly charged oxygen vacancy defects	eV
V_{TH}	Threshold voltage	V
H_f^0	Neutral vacancy formation energy	eV
H_f^{2+}	Formation energy of double ionized vacancy	eV
V_{DS}	Drain-Source voltage	V
V_{GS}	Gate voltage	V
E_F	Fermi energy	eV
$\varepsilon(+/0)$	Transition energy from singly ionized to neutral state	eV
$\varepsilon(2+/+)$	Transition energy from doubly to singly ionized state	eV

Chapter 1

Introduction to Thin Film Transistors

1.1 Historical Overview of Thin Film Transistors

Since the realization of first integrated circuits by Jack Kilby in 1958, engineering smaller devices has been constantly pursued to incorporate more functionality on a single chip. Moore's law being the governing principle has resulted in fabrication of transistors down to a 7nm technology node that is currently being ramped up for production. Technological advancements in the IC industry has created demand in display technology in parallel [1]. Thin Film transistors (TFTs), which have similar structure and operation as field effect transistors (FET) were potential candidates to control switching of pixels that were to be used in flat panel displays (FPD).

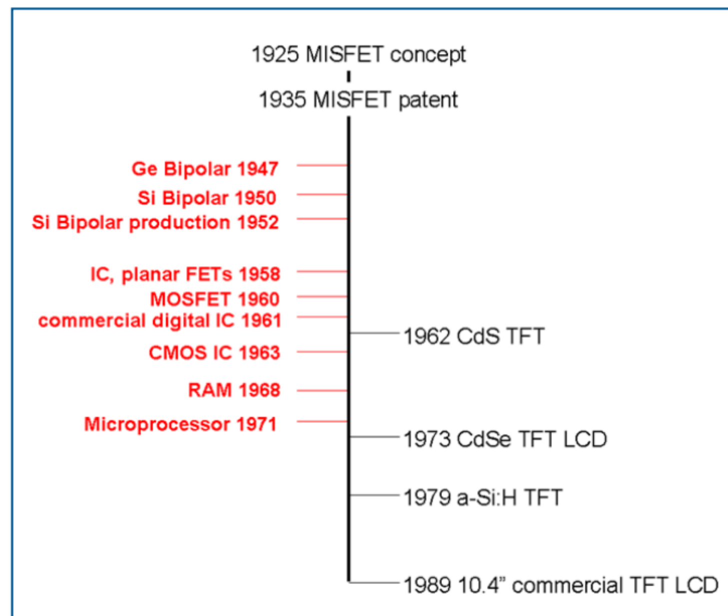

Figure 1.1. History of TFT and IC development[1].

To be precise, a TFT can be considered as a special type of FET that is fabricated by placing thin films of dielectric and semiconductor layers with metallic contacts onto a supporting substrate [2]. It can be operated either in enhancement mode or depletion mode depending on the application of gate bias to induce conduction in the channel. Dating as early as 1960s, TFTs with compound semiconductors such as CdS or CdSe were developed [3]. 1979 saw a breakthrough in display technology where the first functional TFT made from hydrogenated amorphous silicon (a-Si:H) with a silicon nitride gate dielectric layer was reported. Since display circuits require a transparent substrate, different substrate materials such as glass or plastic had to be incorporated. A lower melting point was a characteristic property of such substrates which required low temperature processing of these TFTs. These were few key reasons responsible for the difference in cost of production that varies significantly when compared to conventional integrated circuits where the substrate is crystalline silicon.

1.2 Liquid Crystal Displays

Recent display technologies are dominated by a variety of FPDs such as liquid crystal display (LCD), organic light emitting diodes (OLED), plasma display panels (PDP) and field emission displays (FED). LCDs, precisely active-matrix LCDs (AM-LCDs), and OLEDs among these are predominantly used in today's technology. The advantage of active-matrix LCDs over passive-matrix or direct pixel addressing LCDs are the use of transistors that eliminate the issue of presence of a leakage path as observed in a passive-matrix LCD that would in turn allow adjacent pixels to be partially turned on. AM-LCDs, as depicted in figure.1.2, consists of a backplane source such as LEDs or cold cathode fluorescent lamps (CCFL). A diffuser and polarizer is placed in front of the light source. The glass substrate on which the TFTs are fabricated are bonded to the polarizer. A common transparent electrode, color filter and a

polarizer are adhered onto the second half of the display. The liquid crystal is sandwiched between the first and second layers of glass substrates

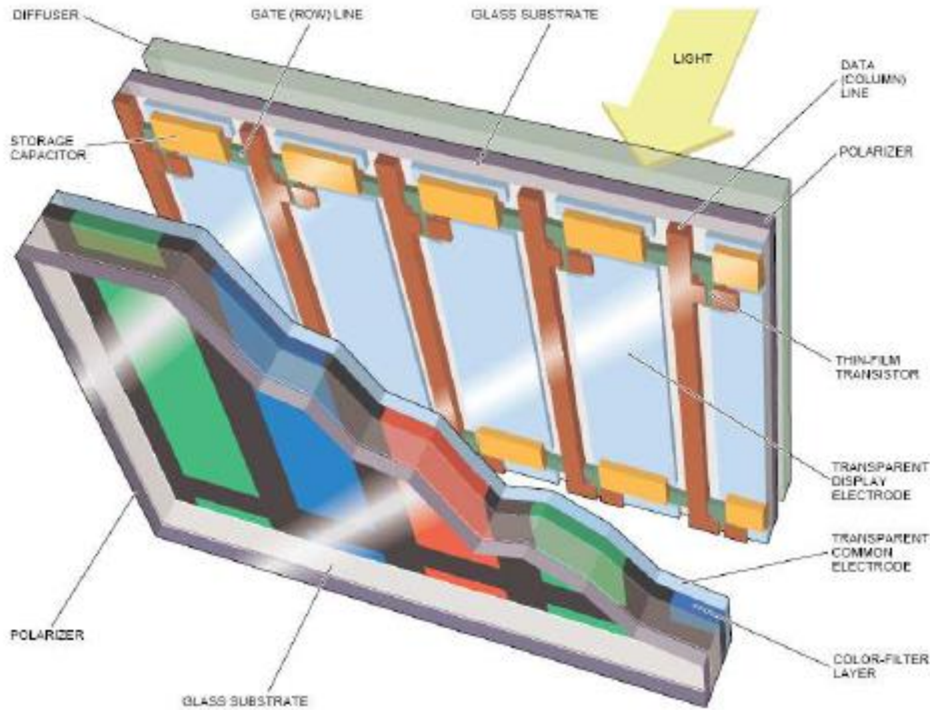

Figure 1.2. Cross section of an LCD [4].

through which a voltage maybe developed. The basic functionality of an active-matrix circuit is as shown in figure.1.3 which consists of a switching TFT, a storage capacitor and a liquid crystal.

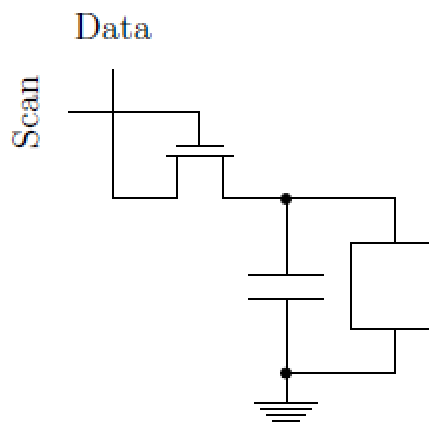

Figure 1.3. Schematic of an active-matrix LCD circuit.

The pixel is set to turn on under three conditions. The liquid crystal must be uncoiled by applying a bias to it; there must be an appropriate voltage applied to the pixel through the data line; and the pixel must be addressed via the scan line. As long as the storage capacitor is charged, the pixel will be addressed after which the TFT is turned off by discontinuing biasing the scan line. Until the pixel is addressed again, bias across the liquid-crystal is maintained by the storage capacitor. High contrast ratios can be achieved by precisely controlling the bias applied to the liquid crystal by controlling the amount of light that passes through it.

1.3 Organic Light Emitting Diode (OLED)

To obtain higher resolution the requirement for increased number of pixel density became evident. As display technology advanced to generation 10 (Gen 10) which used a 3m×3m substrate, large area uniformity became a concern. Even though OLED displays demand more stringent electrical uniformity requirements when compared to LCDs, the ability to control the brightness of

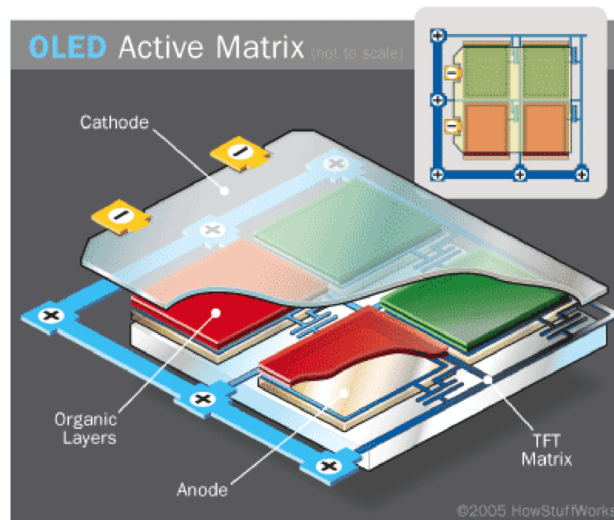

Figure 1.4. Cross section of an OLED active-matrix. Picture courtesy: AMAT

individual pixels facilitates a display with enhanced resolution. Unlike the LCD which consists of a back lit source, OLEDS are designed to produce light by themselves when a voltage is applied across the cathode and anode. As shown in figure.1.4, the display uses an array of electroluminescent OLED pixel controlled by TFTs. The organic layers consists of an emissive layer and a conductive layer. Once there is a potential difference across the electrodes, the cathode receives electrons from the source simultaneously making the anode rich in holes. This makes the emissive layer negatively charged while the conductive layer is positively charged. Since the mobility of holes are higher than electrons, they cross the boundary from the conductive layer to the emissive layer and recombine to emit photons which act as the light source for individual pixels. A typical OLED pixel unit would consist of TFTs and storage capacitors similar to the LCD circuit, but only in a complex network that would allow individual pixels to behave as an emissive unit. The superiority of OLED lies in their size that they are around 0.2-0.3mm or eight thousandths of an inch compared to LCDs. Since they are self-emissive they consume much lesser energy than LCDs, respond up to 200 times faster and are potential candidates in the design of flexible displays.

1.4 Next Generation Displays

With the increase in demand for next generation displays with higher resolution, several challenges emerge that become evident in high density pixel displays and in applications involving fast switching speeds.

Figure.1.5 clearly summarizes the requirement of transistors with higher mobility in order to overcome the above mentioned challenges. A 50-inch active matrix LCD with copper bus lines was used to estimate the mobility requirements depicted in the figure above. If a 70-inch LCD was considered, the values roughly double due to increase in delay times [5].

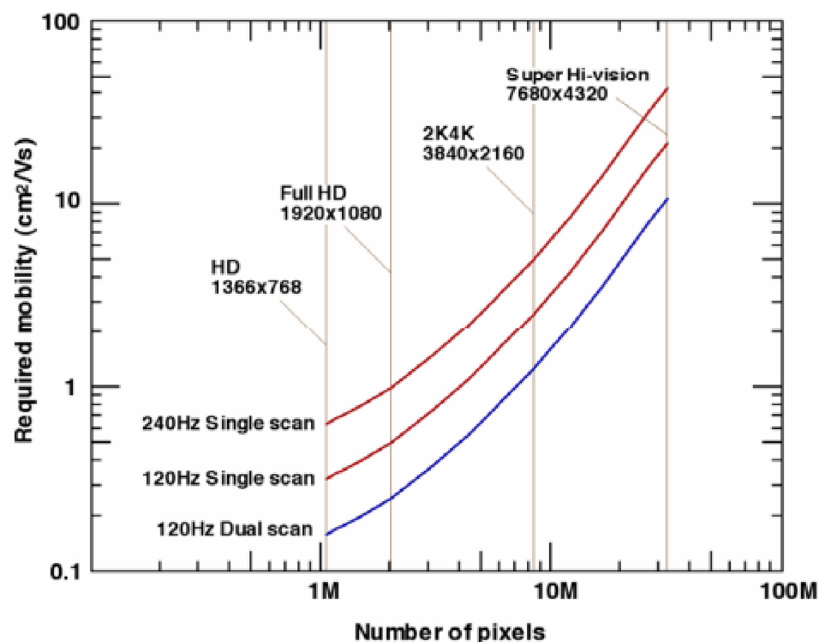

Figure 1.5. Summary of required carrier mobility for future displays [5].

It is here that compound semiconductors begin to play a role and fare better when compared to a-Si:H that has been dominating the display industry over the past three decades.

1.5 Hydrogenated Amorphous Silicon

Crystalline silicon has been the undisputed leading technology in the semiconductor industry. Favorable economics in terms of availability, manufacturing cost and the potential to grow a high quality oxide thus reducing the oxide-semiconductor interface defect states has made silicon an apparent choice in fabricating semiconductor devices. Silicon was hence the most understood material which led to the advancement of its technology in the display industry. 1979 marked the year when the first functional TFT made from Hydrogenated Amorphous Silicon (a-Si:H) was realized. Until this day a-Si:H is used as the TFT's channel material in various display applications due to its compatibility with low temperature processing and good large area uniformity.

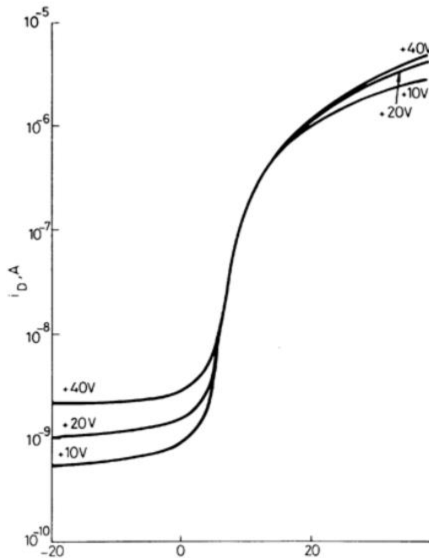

Figure 1.6. First a-Si:H transfer characteristics [1].

The TFTs fabricated using a-Si:H used silicon nitride as the dielectric material. The composing films were deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) below 350 °C that enabled low-temperature processing on glass substrates with high throughput. The resulting devices were stable at room temperature under atmospheric conditions. However, due to a high density of dangling bonds in a-Si, hydrogenation is required to passivate these dangling bonds which would otherwise make it electrically inactive.

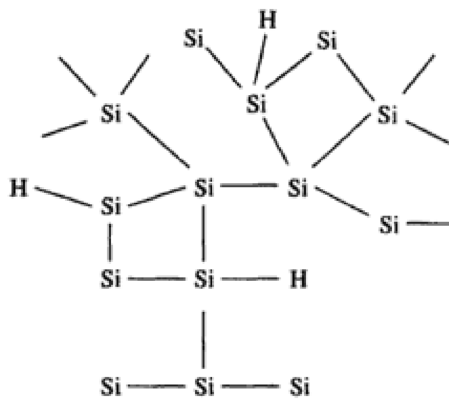

Figure 1.7. H atoms tie up the dangling bonds inherent to a-Si [6].

Conduction in a-Si:H occurs primarily through three means. They are the band tail states, deep level defect states and extended conduction and valence band states. Band tail states originate due to the difference in bond angles and bond lengths in the amorphous material which causes disorder in the energy of bonding and anti-bonding states. These are localized states in the energy band which extends into the band gap and decreases exponentially. Deep level states are created due to the high density of dangling bonds and their conduction mechanism depends on temperature position of the Fermi level. Typically at low temperatures, an electron at a localized dangling bond defect site just below the Fermi could tunnel into the Fermi level which is in close proximity to the initial state on the application of an electric field. The conduction and valence band states originate from the tetrahedral silicon network where the carriers are not bounded to local defect states but move through the periodic potential of the tetrahedral network. The conduction in these states occurs at elevated temperatures of above 500 K.

Although a-Si:H possesses electrical properties good enough for LCD applications with lower frame rates (120Hz or less), there are a few drawbacks in a TFT that uses a-Si:H as channel material. a-Si:H fails to keep up to the expectations of modern technologies requiring higher carrier mobility to obtain better resolutions. A relatively shallow sub-threshold profile when compared to other oxide semiconductors result in low-performance TFTs. a-Si:H is also deterrent in applications using flexible displays due to complexities involved in fabrication. Finally, even though the device's response to bias stress is acceptable for LCD applications, the tolerance limit for threshold voltage shift observed due to bias stress for OLED devices are very low. These were the factors which paved the way to explore other candidates. Table.1 summarizes the electrical properties of a-Si:H in comparison with other potential candidates that have replaced a-Si:H, thus catering to the requirements of today's leading display technologies.

Table.1 Comparison between a-Si:H, LTPS and a-IGZO material properties

TFT channel material	a-Si:H	Low temperature poly silicon (LTPS)	a-IGZO
Field effect mobility ($cm^2V^{-1}s^{-1}$)	~1	~100	> 10
TFT uniformity	Good	Poor	Good
Fabrication cost	Low	High	Low
Yield	High	Low	High
Processing temperature	~250° C	> 250° C	Room temperature (RT) ~ 360° C
Electrical stability	Poor	Good	Good in dark
Optical stability	Poor	Poor	Good
On-off current ratio	< 10^{-7} A	< 10^{-7} A	10^{-8} A
Visible transparency	Poor	Poor	~ 80 %
Number of mask	4-5	5-12	5-6
Pixel circuit	1T + 1C	5T + 2C	2T + 1C
Pixel TFT	nMOS	CMOS	nMOS
Generation	8G	4G	8G

1.6 Candidates to Replace a-Si:H

Low Temperature Polycrystalline Silicon (LTPS) provides a promising carrier mobility that fulfills the requirements of today's display technology. Unlike a-Si:H, the partially crystallized polycrystalline material offers carrier mobility greater than almost one orders of magnitude in comparison to its amorphous counterpart.

Formation of polysilicon films can be achieved by two techniques involving either direct deposition of polycrystalline material, or by crystallization of an a-Si precursor layer. Low-Pressure Chemical Vapor Deposition (LPCVD), with temperature T > 580 °C or Plasma-Enhanced CVD with lower temperatures can be used to deposit the polysilicon film. Even though LPCVD yields in uniform film thickness and low defect density, low deposition rates have been known to pose a significant impact on production throughput. Although PECVD is relatively faster, the major set-backs are uniformity and films with grain boundary defects. In contrast, crystallization of a-Si has a practical significance in the formation of polysilicon film.

Crystallization of a-Si can be realized using liquid-phase or solid-phase techniques. Liquid-phase crystallization (LPC) involves melting of the a-Si material and letting it cool and solidify to form polycrystalline layer. Excimer Laser Annealing (ELA) is one of the most prominent LPC techniques used to achieve polysilicon film with demonstrated advantages of high electron mobility and cleaner films. Nevertheless, limited scaling capacity and high cost of equipment have limited the capabilities of ELA. Solid-Phase Crystallization (SPC) is another technique to realize polycrystalline silicon that produces films with high uniformity, low defect density and higher carrier mobility. But factors such as high temperature processing, high cost and complex processing for the fabrication of large quartz substrate were the major drawbacks. Flash lamp Annealing (FLA) which involves exposure of a-Si film with a high energy xenon flash lamp is another novice technique enabling polycrystalline silicon films with grain size larger than ELA by at least one order of magnitude [7].

As mentioned earlier, the major benefit of using LTPS as the TFT's channel material is due to its high mobility. Unlike a-Si:H and amorphous oxide materials, it is also possible to fabricate both nMOS and pMOS TFTs with LTPS that results in the transistor behaving like a CMOS. However, LTPS poses drawbacks in terms of complex processing that result in high cost and process scaling limitations. Large scale electrical uniformity due to the presence of grain boundaries is another significant challenge that LTPS faces.

Amorphous oxide materials, upon extensive research, gained importance since they showed high mobility compared to a-Si:H, lower density of tail-states in the conduction band making them less sensitive to bias stress than a-Si:H. Also their low temperature compatibility and better electrical uniformity than LTPS, due to their amorphous structure made them emerge as one of the most promising candidates to replace a-Si:H.

Chapter 2 describes the properties of one such material, Indium Gallium Zinc Oxide (IGZO) that has proven to be a potential candidate in replacing a-Si:H to realize displays with higher resolutions and better frame rates.

Chapter 2

Overview of Amorphous Indium Gallium Zinc Oxide (IGZO)

2.1 Amorphous Oxide Semiconductors

Amorphous Oxide Semiconductors (AOS) are promising channel materials for TFT backplanes in FPDs because of the features summarized in Table.1. They are compatible with the current FPD industry, which uses large cost-effective glass substrates since they are fabricated at low temperatures below 400 °C. Although a-Si:H is also compatible with low temperature processing, it has been reported that a-Si:H cannot drive larger LCDs (55 inches) operating at high frame rates above 120 Hz, as depicted in figure.1.5. Recently, three-dimensional displays which have appeared in the market with large panel sizes require higher frame rates of e.g. 480 Hz in order to improve the quality of the picture because a 3D display must project two or more picture frames alternately for the left and right eyes. These are the reasons that led to extensive research in AOS materials because they comply with all the above requirements [8-10]. Since then, AOS has been catching up with LTPS technology and are eventually bound to make a-Si:H TFTs an obsolete technology

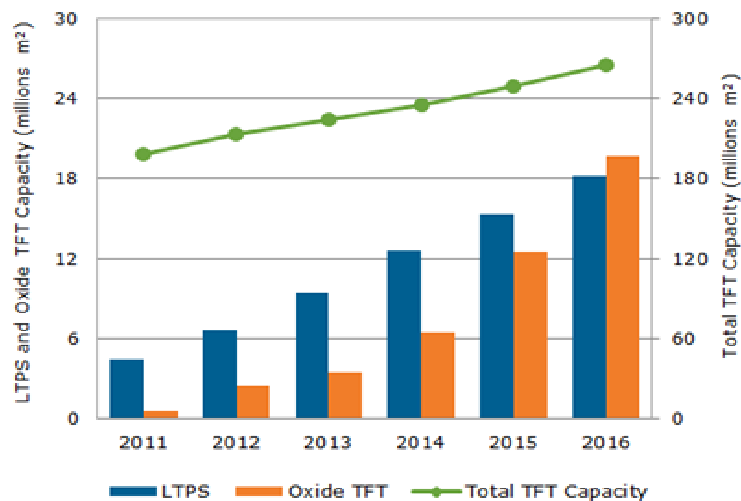

Figure.2.1. Indication of oxide TFTs depicting a steady growth in manufacturing.

2.1.1 Conduction mechanism in Amorphous Oxide Semiconductors

Figure.2.2 illustrates shells of covalent and ionic bonded semiconductors in crystalline and amorphous structures.

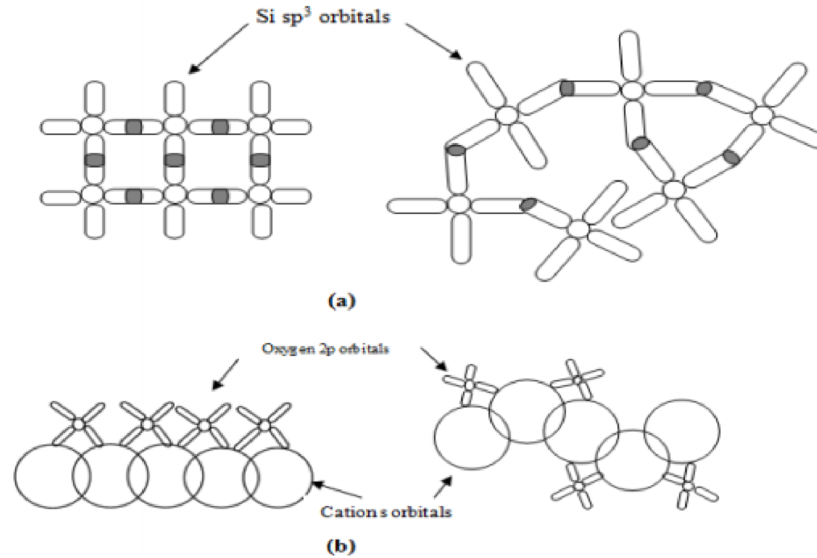

Figure 2.2. Shell level representation of covalent and ionic semiconductors in (a) crystalline and (b) amorphous structures.

Hosono *et al.* in 1996 proposed a theory to determine a wide band gap amorphous oxide semiconductor which would have mobility values comparable to covalent semiconductors such as silicon [11]. Silicon sp^3 orbitals form the conduction path for covalently bonded semiconductors. Mobility of these semiconductors directly depends on the amount of overlap that exists between the sp^3 orbitals of neighboring atoms. However, conduction path in oxide semiconductors such as AOS comprises of valence shell of heavy-metal cations. If a suitable metal cation is chosen, a larger spherical *s*-orbital could be obtained that results in a faster conduction mechanism. From figure 2.2 it is apparent that for covalent semiconductors such as silicon, mobility takes a toll in the amorphous state compared to crystalline state. This is because of the minimal overlap between the sp^3 orbitals causing electrons to transport through a hopping mechanism thus affecting overall mobility. In contrast, large isotropic spherical orbitals in AOS provide sufficient overlap between neighboring atoms regardless of bonding angles that yield

similar mobility for both amorphous and crystalline states. Hosono *et al.* proposed using metal cations that have an electronic configuration of $(n-1)d^{10}\ ns^{0}$ where $4 \le n \le 6$.

2.2 Prospective of Zinc Oxide Thin Film Transistors

Following the proposal of CdS TFTs, single crystal zinc oxide (ZnO) TFT was published in 1968. ZnO was an interesting and promising material to replace a-Si:H mainly due to its high carrier mobility and feasibility of low temperature processing below 300 °C. Similar to most binary metal-oxides ZnO is easily crystallized into polycrystalline-ZnO (poly-ZnO) which resulted in high mobility, making it a potential replacement to a-Si:H as the TFT's active layer. D.A. Mourey *et al* demonstrated that Plasma Enhanced – Atomic Layer Deposition (PE-ALD) ZnO passivated with alumina resulted in high performance TFTs with threshold voltage of 4.5 V, mobility ranging between 20-30 $cm^2/(V.s)$ and a sub-threshold swing of 200mV/dec [12]. Current-voltage characteristics of the device is depicted in figure.2.3.

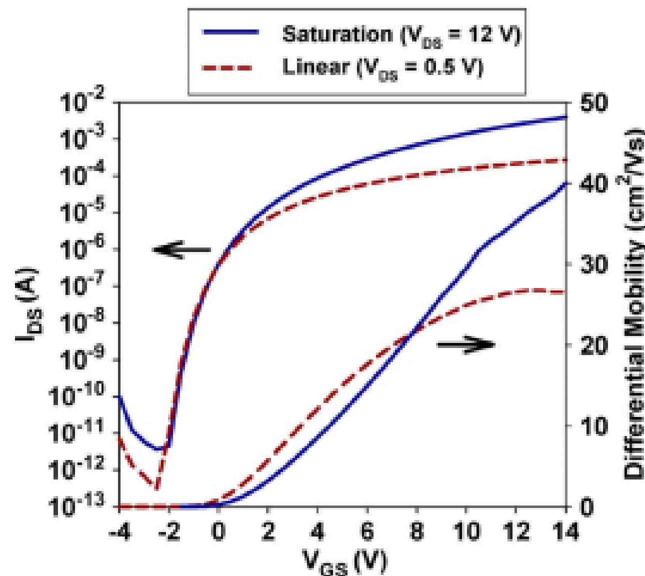

Figure 2.3. Current-voltage characteristics and differential mobility extraction of the PE-ALD deposited ZnO TFT [12].

Hydrogen free precursors such as CO_2 and N_2O were used in the process since hydrogen incorporation increases the concentration of free electrons by bonding with oxygen giving rise to OH^- bonds which behave as additional donors in the channel.

Even though ZnO TFTs hold an upper hand with regards to high carrier mobility, transparency and flexibility than a-Si:H they suffer in terms of instability and non-uniformity due to grain boundaries. Also adsorption and desorption of trace amounts of oxygen and water alters the electrical properties of the material significantly. The high concentration of residual free electrons which is greater than $10^{17}/cm^3$ due to native zinc interstitials and oxygen vacancy defect states is another cause of concern in ZnO.

2.3 Development of IGZO TFTs

Although binary metal oxides such as poly-ZnO can provide high mobility due to their larger spherical *s* orbit of the cation facilitating increased mobility irrespective of the bonding angles, issues with grain boundaries led to continued research in the field of AOS. It was desired that the ideal material would need to form a stable and uniform amorphous phase with good carrier mobility and must be compatible with low temperature processing. In addition, a controllable carrier concentration ($< 10^{15}$ cm^{-3}), electrical stability in terms of threshold voltage shifts and large area uniformity were desired. To meet these requirements in AOS, it was necessary to form a dispersed conduction band minimum which could be realized by incorporating unoccupied metal ns orbital with large principal quantum number (n>4) [13]. To suppress the formation of excess oxygen vacancies, metals with stronger metal oxygen bonds such as Gallium, Aluminum were used to create Ga-O and Al-O bonds that in turn led to realization of Indium Gallium Zinc Oxide [14].

In 2004 Nomura *et al*. first introduced amorphous IGZO as the channel material for TFTs. IGZO is an n-type semiconductor consisting of In_2O_3, Ga_2O_3, and ZnO, which are known n-type semiconductors. IGZO is inherently n-type due to its native point defects. Upon extensive research it has come to light that the origin of these defects could be explained with respect to either hydrogen molecules or oxygen vacancies which act as donors thus making the material n-type. Upon further study and various tests such as bias stress, illumination stress, thermal analysis, it has become apparent that oxygen vacancies are indeed the predominant defect states that is responsible for IGZO's inherent n-type behavior. Tauc plots, which are used to determine the band gap values for AOSs reveals an energy band gap of 3.2eV for high quality IGZO films with In:Ga:Zn in the ratio of 1:1:1. For deteriorating films, the band gap reduces to ~3.0eV for poor-quality films. The electron mobility of IGZO is reported to be greater than around 10 $cm^2/(V\cdot s)$. This value is almost ten times higher than that of a-Si:H making IGZO a potential replacement for a-Si:H. Current-voltage characteristic comparison Study on coordination structures and electronic structures using x-Ray Absorption Fine Structure (XAFS) reveal that the structure of a-IGZO is similar to crystalline IGZO films which is depicted in figure 2.4.

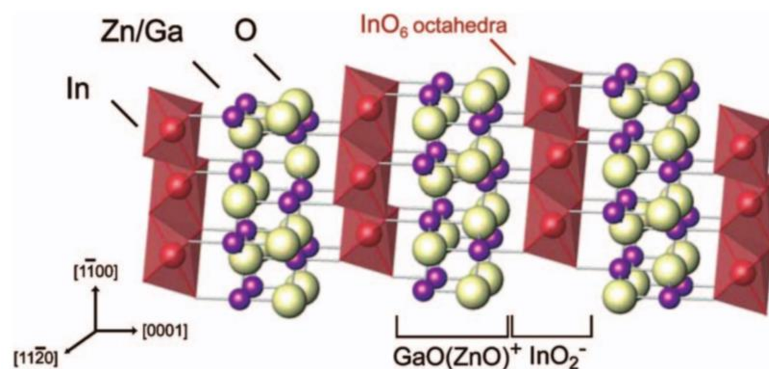

Figure 2.4. Structure of crystalline IGZO [15].

Since it is not feasible to fabricate crystalline IGZO to make TFTs, amorphous IGZO was the chosen candidate to dominate display industry due to its similar structure to crystalline IGZO and

its ease of fabrication. Unlike silicon which utilizes doping to make the channel conductive, IGZO relies on its oxygen vacancies which act as donors. The lack of hole-states to facilitate valence band transport makes IGZO dearth in free hole carriers thus leading to excellent low off-state currents and at the same time impossible to obtain p-type characteristics. Electrical performance of IGZO is governed by its defect states. The mid-gap region of IGZO's energy band diagram comprises of a distribution of density of defect states that represent acceptor/donor-like band-tail states and oxygen vacancy donor states [16]. They are defined as exponential and Gaussian distributions respectively as shown in figure.2.5. The oxygen vacancy distribution coupled with the acceptor tail-state defect distribution near the conduction band are found to predominantly affect electrical properties of the material, verified by TCAD simulations.

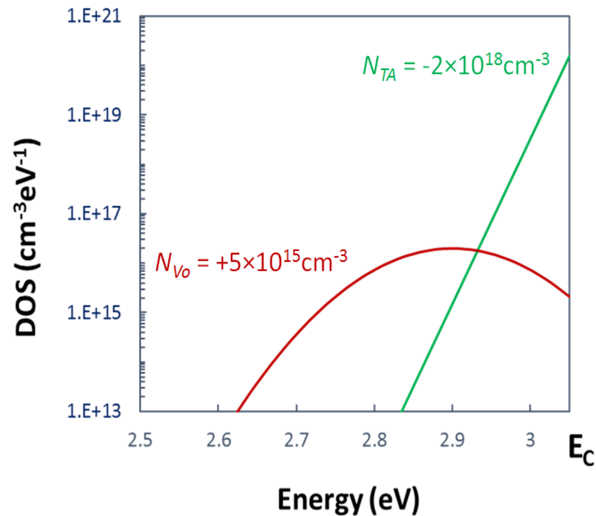

Figure 2.5. Defect state concentration integrated over energy near E_C for IGZO TFTs.

Parameters used to simulate the density of states are listed in Table.2. Defect states at the valence band are ignored since they have no effect on the device's electrical characteristics.

Table.2. Parameters used in TCAD simulations to extract the density of states for IGZO TFTs with modified values*

Symbol	Value
Band gap	3.05 eV
Electron affinity	4.16 eV
Relative permittivity	10
Electron mobility	12.7 $cm^2/(V.s)$*
NGD	2×10^{16} $/cm^3/eV$*
EGD	2.9 eV
WGD	0.1 eV
NTA	1.55×10^{20} $/cm^3/eV$
WTA	0.013 eV

A comparative study between the three prominent TFT channel materials is summarized in Table.1 depicted in section.1.5. It is evident that IGZO is definitely a promising candidate as it neither suffers from a low mobility as in a-Si:H, nor lacks in formation of less uniform films due to grain boundary issues as in LTPS.

Typical I-V characteristics for an un-passivated IGZO TFT fabricated in RIT is as shown in figure.2.6. The device measured is a L/W=24/100 µm TFT after undergoing N_2 anneal at 400 °C and ramp down in an oxidizing ambient. The characteristics obtained are one of the best to be reported and a stable process has been developed to reproduce similar devices. The plot shows impressive I_{ON}:I_{OFF} ratios, threshold voltage V_T~0V, a steep sub-threshold slope of ~150mV/dec and a saturation mobility of ~12$cm^2/(V.s)$.

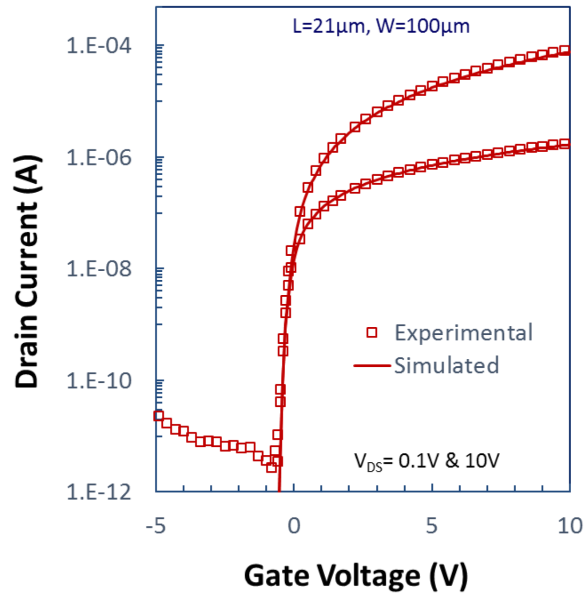

Figure.2.6. Current-voltage characteristics of an un-passivated IGZO TFT fabricated at RIT.

2.4 Motivation for the Study of IGZO TFT Instabilities: Bias Stress

With the advancement in the field of display technology IGZO has proven to be a potential replacement to a-Si:H as the TFT's channel material. The year 2012 was the first year that marked mass production of IGZO TFTs. However, TFTs fabricated using IGZO has been known to have issues related to bias stress. Large V_T variations (>2V) of the transfer characteristics are observed when the device is subjected to bias stress.

The application of bias stress can be detrimental to a TFT's performance in terms of its electrical properties. Hence, the effect of bias stress on the operation of IGZO TFT becomes a vital study to achieve a comprehensive understanding on the device's instability. The outline of this document is to understand and study the application of bias stress on IGZO TFTs, the resulting response due to the applied stress conditions and recovery following bias stress testing.

Chapter 3

Bias Stress Instability of IGZO TFTs

3.1 Preliminary Research

Application of voltage for a prolonged period of time to one or more of the TFTs terminals has resulted in significant variations in the TFT's transfer characteristics. These variations manifest themselves as a shift in threshold voltage, degradation in sub-threshold swing or deteriorate the overall performance of the transistor. One of the major drawbacks of not proceeding with a-Si:H as the TFT's channel layer in OLED displays is its instability with respect to bias stress conditions. A TFT's V_T shifted by 0.1 V can result in a 20% change is brightness [17]. Having said this, the importance of bias stress study on the TFT's performance is paramount.

3.1.1 Positive Bias Stress

Positive Bias Stress (PBS) is the application of a positive voltage to the transistor's gate for a specific period of time. In our study, two variations of PBS have been deployed based on the application of stress either to the gate only or the gate and drain simultaneously. The latter was considered since the transistor is said to be 'truly ON' when both its gate and drain terminals are biased in the TFT pixel circuit. Under PBS, the transistor functions as an accumulation mode device. Literature reveals that most of the research groups observe a lateral positive shift (right shift) under PBS as depicted in figure.3.1. There have been reports of sub-threshold variation post stress in few cases as well. The shift in V_T is attributed to either electron traps at the interface and/or generation of acceptor-like states in the bulk or at the interface. Creation of additional defect states in the bulk is believed to cause variations in the sub-threshold characteristics of the device [18]. Since a lateral shift is what is observed in most cases, the phenomenon of this positive shift in threshold voltage under PBS is said to arise from negative charge being trapped at the channel/dielectric interface or getting injected into the dielectric.

The positive shift is then justified by the negative charge screening the applied gate voltage. The lower effective gate bias results in a smaller current flowing through the channel, thus requiring a larger positive voltage to turn the device ON and reach saturation [19].

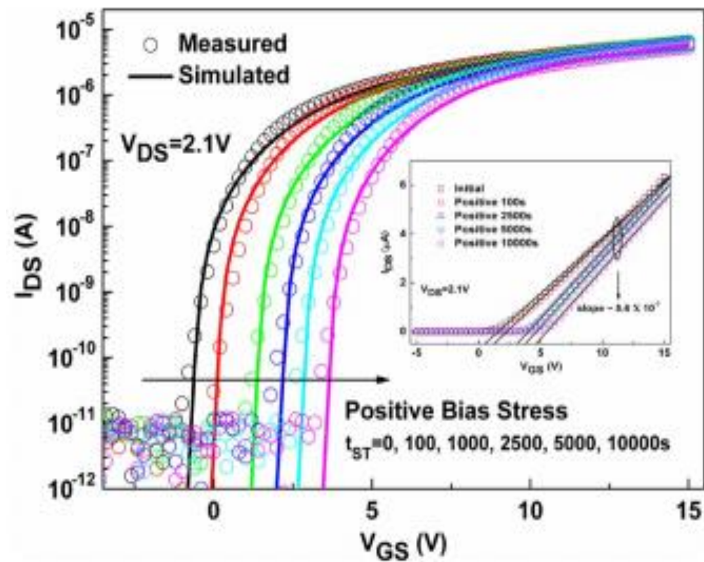

Figure 3.1. Transfer characteristics of a TFT for positive gate bias stress test. The inset shows [linear (I_{DS})-V_{GS}] characteristics [18].

3.1.2 Negative Bias Stress

The application of a negative voltage to a TFT's gate and holding it for a specific amount of time is referred to as Negative Bias Stress or commonly NBS. Similar to PBS, NBS can be detrimental to a TFT's performance. The device under NBS operates in depletion mode. Negative Bias under Illumination Stress (NBIS) is applied by holding the gate at a negative potential while simultaneously irradiating the device with near or above bandgap light. Large negative shifts in transfer characteristics have been reported when the devices were subjected to NBIS as shown in figure.3.2. However, literature [20] suggests that negligible or no shift in characteristics were noticed for devices that were subjected to only NBS since the transistor channel is said to be depleted at the channel/dielectric interface and the unavailability of mobile

charges for charge trapping and tunneling process resulted in this kind of behavior. But under illumination, photo-induced ionization is assumed to play a vital role in explaining a change in device characteristics. Charge trapped in the gate dielectric or at the interface and/or creation of ionized oxygen vacancies were the most likely explanations to justify the degradation mechanism.

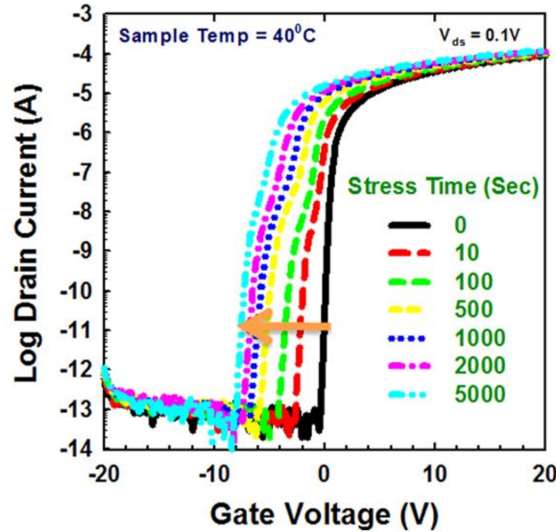

Figure 3.2. Transfer characteristics of a TFT for negative gate bias illumination stress test [20].

3.2 Initial Experimentation

The above results were intriguing, which led to the motivation of understanding the phenomenon of bias stress induced instabilities in the TFTs fabricated here at RIT. The type of stress incorporated in this study and the nomenclature used henceforth is summarized in Table.3. All voltages are set to either +/-10 V unless and until specified otherwise.

Table.3 Bias stress conditions incorporated in our study

Terminal/Stress	PBS (volts)	NBS (volts)
V_{GS}	+10	-10
V_{DS}	0	0

Figure.3.3 depicts transfer characteristics of a device fabricated at RIT. On the contrary to what was published in literature about NBS instability, transfer characteristics show a significant left shift when the device was subjected to NBS1 at -10V.

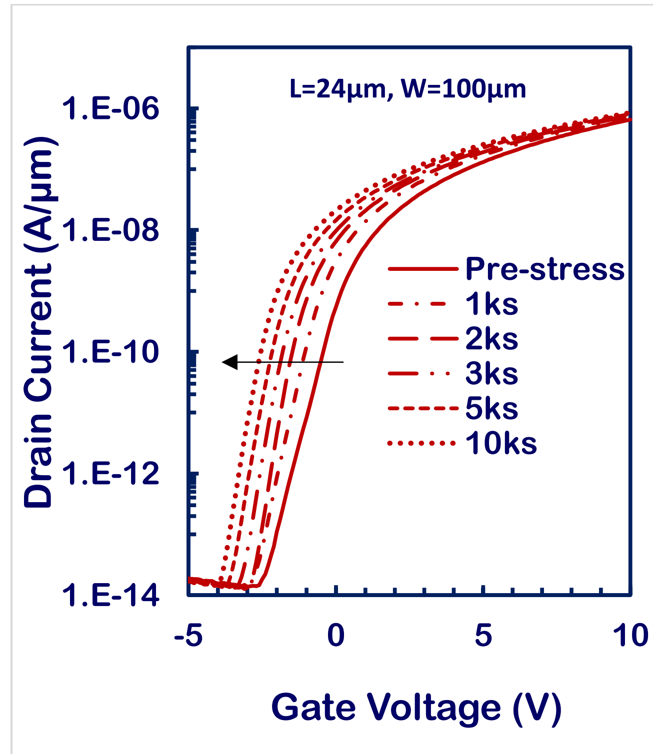

Figure 3.3. Transfer characteristics of a TFT fabricated at RIT depicting a negative shift in V_T under the influence of NBS.

On the other hand, the effect of PBS was also found to differ when compared to what was explained in literature. The reason supporting this degradation mechanism is detailed in Chapter.5. The fabrication procedure incorporated to realize TFTs with different gate electrode configurations to study this degradation mechanism is discussed in the following chapter.

Chapter 4

TFT Fabrication

This chapter provides an overview of TFTs fabricated at RIT's Semiconductor and Microsystems Fabrication Laboratory (SMFL). Fabrication steps incorporated to realize TFTs with different gate electrode configurations will be discussed. The chapter initially covers fabrication of the standard base-line process flow to realize a staggered Bottom-Gate TFT (BG TFT). Next, the advantages of adding a secondary gate to the BG TFT, making it a Dual-Gate TFT (DG TFT) are discussed. The motivation is to ultimately understand the response of these TFTs with different gate electrode configuration to the application of bias stress testing.

4.1 Staggered Bottom-Gate TFT

To begin, 6 inch RCA cleaned Si wafers were used as substrates to fabricate TFTs. 650 nm of oxide was thermally grown to emulate a glass substrate. 50nm of Mo gate is sputter deposited at a chamber pressure of 2.8m Torr with 20sccm of Ar flow at 1000W for 300 seconds. It is patterned by a subtractive wet etch process. 100nm of SiO_2 gate dielectric is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) using Tetra Ethyl Ortho Silicate (TEOS) as the precursor. After densifying the dielectric for 2 hours at 600 °C in N_2 ambient, IGZO is RF sputtered on to the gate dielectric using the Applied Materials Centura system with a 12.8" target consisting of In:Ga:Zn:O in the ratio of 1:1:1:4 and 7% O_2 in an Ar ambient. The IGZO mesa is patterned using 6:1 H_2O:HCl mixture to form the channel region. Gate contact cut lithography is done next to open contact to the gate pads by etching the oxide in 10:1 buffered HF. The source/drain metal is defined by lift-off process following a Mo/Al bi-layer sputter. The bi-layer stack is chosen in order to prevent Mo from oxidizing in further anneal steps. Unpassivated devices are annealed in the furnace with N_2 ambient for 30 minutes followed by an air ramp down. Un-annealed devices show high conductivity initially and this anneal helps in

incorporating optimal concentration of oxygen into the channel making it semi-conductive from a conductive state. Figure.4.1 depicts a top-down micrograph and cross-sectional illustration of the fabricated TFT structure. The device is said to have a staggered configuration since the gate and the source/drain are on the opposite sides of IGZO.

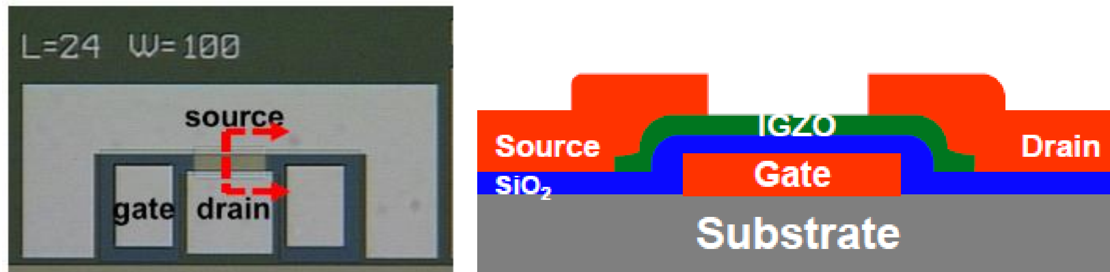

Figure 4.1. Top-down (left) and cross-sectional illustration (right) of unpassivated BG TFTs.

The resulting transfer characteristics of an unpassivated BG device is shown in figure.4.2. The annealed devices are tested using the HP-4156 parameter analyzer with a matlab script. Extracted values of V_T, sub-threshold swing and mobility are -0.25 V, 124mV/dec and 11.19 $cm^2/(V.s)$ respectively.

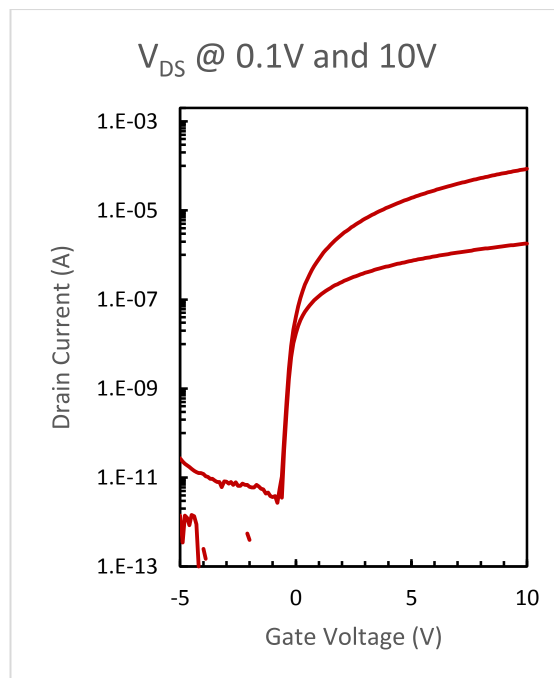

Figure 4.2. Current-voltage characteristics of a BG un-passivated device with L/W=24/100 µm.

4.2 SiO_2 Passivated TFTs

Previously various passivation materials such as TEOS SiO_2, Low Temperature oxide (LTO) SiO_2, evaporated alumina, etc. were investigated [21] and it was determined that a dielectric and passivation stack of TEOS SiO_2 for both resulted in devices with minimal degradation. A 100 nm of PECVD TEOS SiO_2 was deposited and annealed at 400°C in oxygen ambient for 4 hours followed by an oxidizing ramp-down on un-passivated devices. Contact cuts and source/drain metals are later defined as described for un-passivated devices.

Passivation plays an important role since it ensures the device is protected from ambient environment and prevents degradation over the period of time. However, devices passivated immediately show distortion in transfer characteristics due to the presence of interface charges induced. Figure.4.3 shows a cross-section of a passivated device and figure.4.4 depicts transfer characteristics and the family of curves for a 24 μm TEOS SiO_2 passivated TFT.

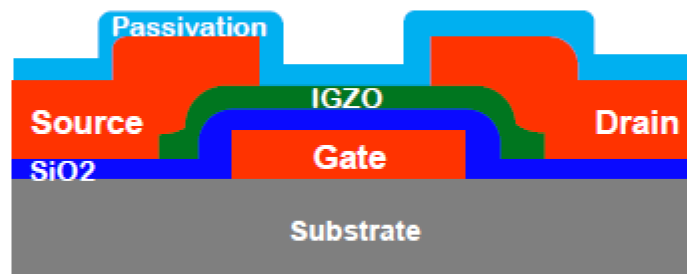

Figure 4.3. Cross-section of a passivated BG TFT.

Distortion in transfer characteristics for a passivated device can be clearly observed in figure.4.4. A shallower sub-threshold swing in the order of ~ 250 mV/dec, a Drain Induced Barrier Lowering (DIBL)-like separation between the low drain and high drain bias and decreased mobility were few of the prominent trade-offs observed after passivating the devices. Upon performing bias stress measurements on passivated bottom gate devices, the responses obtained proved to be worthy of carrying out further investigations in the domain. The behavior of bottom

gate passivated TFTs under bias stress testing, as detailed in Chapter.5, provides a valuable insight in understanding defect states in the IGZO material.

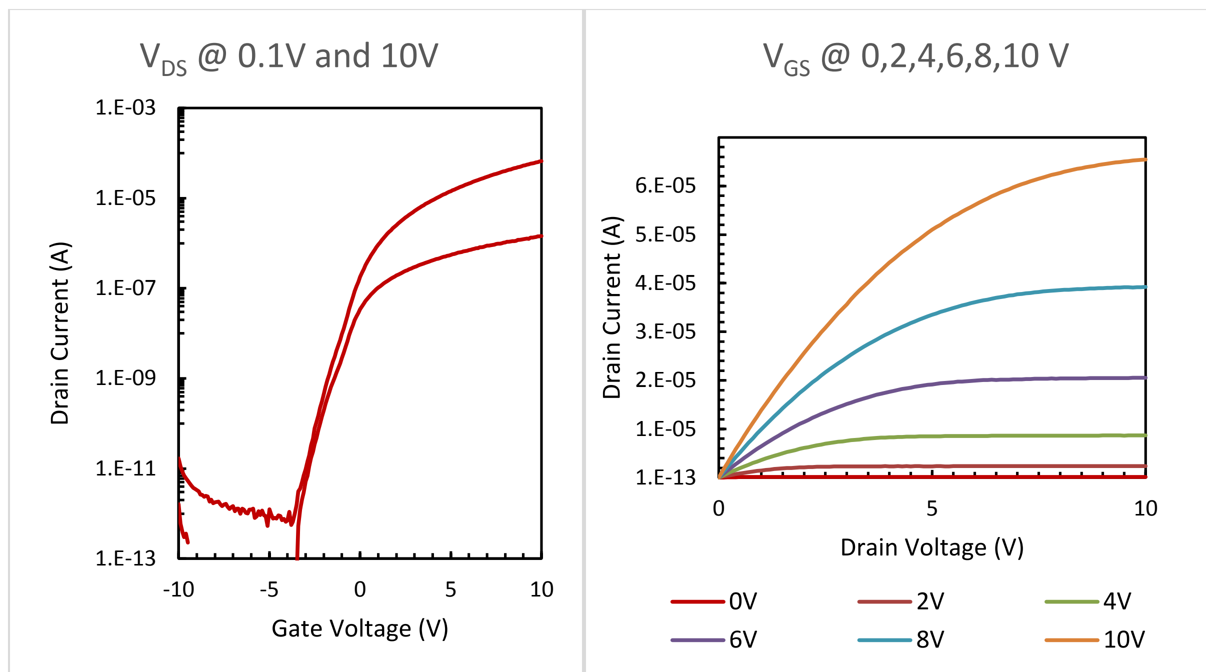

Figure 4.4. I-V characteristics (left) for a passivated device showing shallow sub-threshold swing and family of curves, I_{DS}-V_{DS} depiction the same device (right).

In order to improve the performance of passivated devices, several investigations were explored which led to the ideology of incorporating a secondary gate on top of the passivation material, which would now act as the dielectric for the second gate. Dual Gate or Double Gate (DG) TFTs were thus realized by making minor modifications to the process flow.

4.3 Dual Gate TFTs

Dual gate structure was fabricated by incorporating an additional gate over SiO_2 passivated devices. After defining contact cuts for the source/drain metal by etching in10:1 buffered HF, the top gate metal is defined by lift-off process and Al film of 250 nm is evaporated. The schematic representation of a dual gate TFT is depicted in figure.4.5.

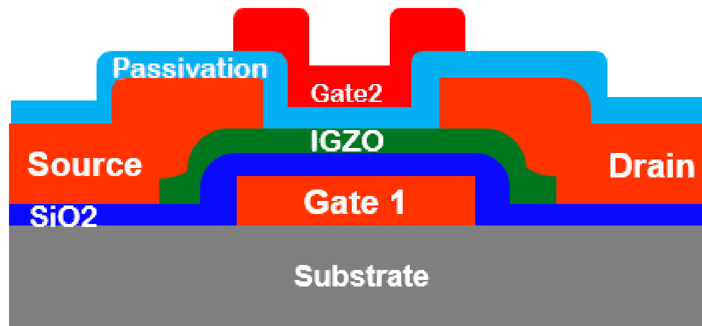

Figure 4.5. Schematic of a dual/double gate TFT.

As seen in figure.4.6, transfer characteristics for the DG TFT shows significant improvement with clear benefits in both on-state and off-state operation due to good control over the channel due to the gate on either sides.

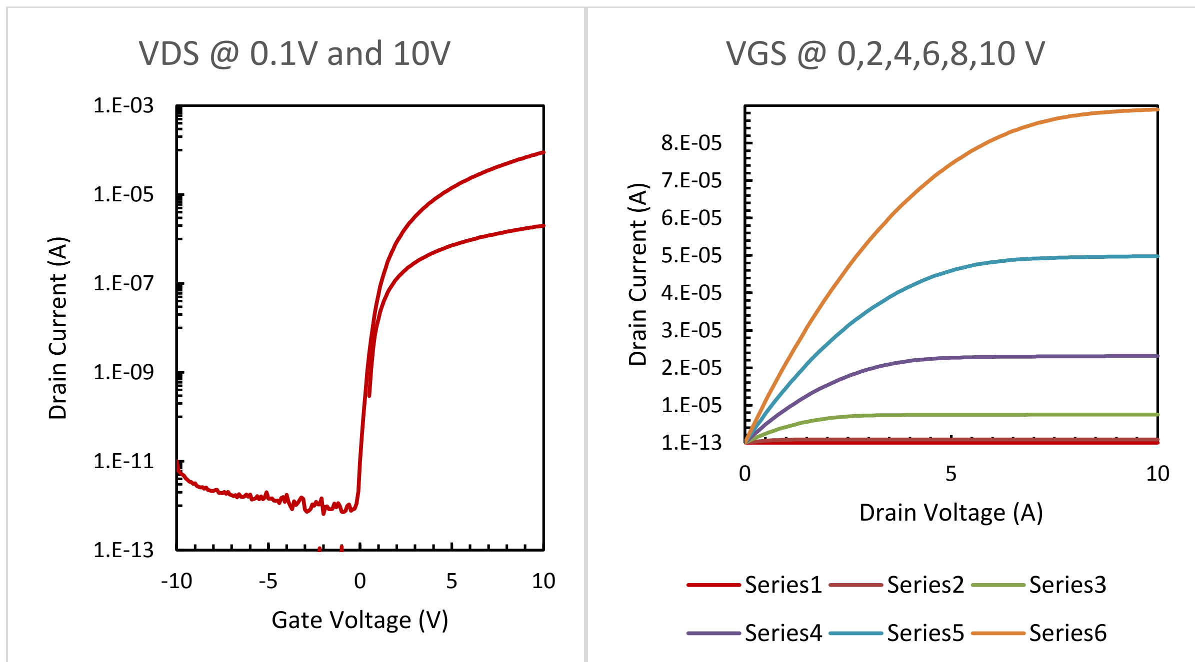

Figure 4.6. Current-voltage characteristics of a L/W=24/100 µm device and (b) family of curves, I_{DS}-V_{DS} depiction the same device.

The DG device demonstrates steep subthreshold that is right shifted from the BG device and added current drive.

Chapter 5

Bias Stress Results and Discussion

5.1 Effect of Bias Stress on BG TFTs

The response to bias stress was investigated for each device configuration. Reiterating, positive bias stress (PBS) and negative bias stress (NBS) tests involved setting the gate voltage to +10 V and -10 V, respectively, with source & drain at reference ground. Measurements were taken at various intervals over an accumulated time of 10,000 seconds or as mentioned otherwise. Channel length of devices are at L/W=24/100 µm or as mentioned otherwise. A characteristic shift in response to bias stress can be attributed to defect state changes either in the dielectric region, the IGZO/SiO2 interfaces, or the bulk IGZO material. Charge trapped in a dielectric or interface region that remains fixed would induce a lateral characteristic shift, whereas changes in interface traps would tend to cause differences in characteristic distortion and spreading. Results discussed in this section are consistent with TCAD simulations for density of states as presented in chapter.2 and has allowed us to further discuss the effect of bias stress on IGZO TFTs.

5.1.1 Response to Positive Bias Stress

BG devices show little or no response to PBS as seen in figure.5.1. Although most devices in literature [19] depict a positive shift in threshold voltage for PBS, it is important to note that devices fabricated at RIT did not show any significant shift. Figure.5.2 shows ATLAS simulations of electron concentration in IGZO TFTs. The device was simulated to be in PBS (right) compared to un-biased state (left). The TFT is in accumulation mode under positive-stress and the voltage drop occurs in the oxide where we see minimal back-channel effect. Interaction with the front-channel is said to have no effect on our devices since this behavior is attributed to

the high quality of our gate oxide that significantly minimizes the effect of front-channel interface defects on device performance.

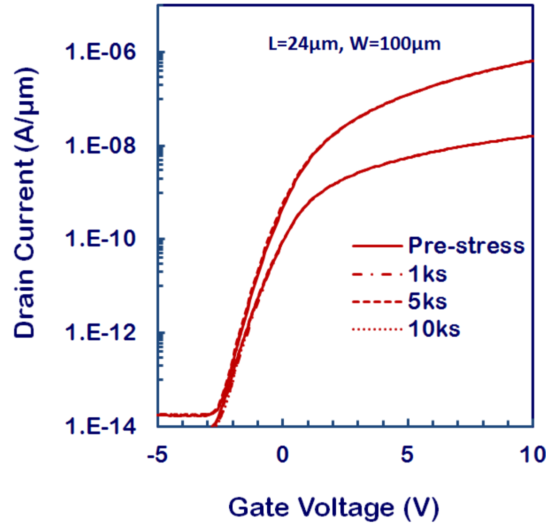

Figure 5.1. BG device under the influence of PBS showing no effect on device characteristics. Shallow sub-threshold swing for typical passivated device is seen here as shown in figure.4.4.

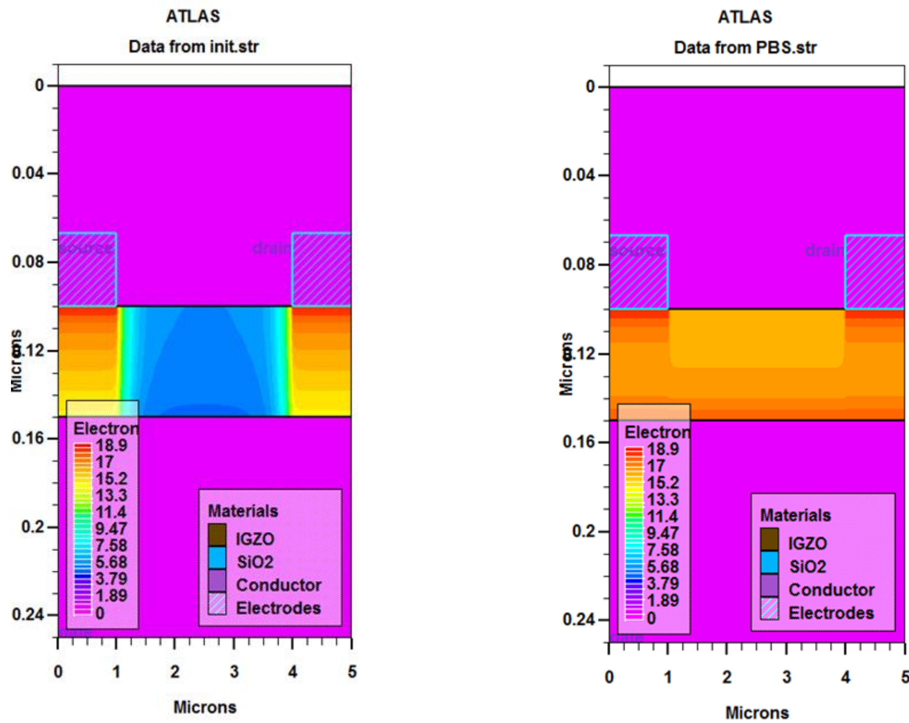

Figure 5.2. ATLAS simulation showing electron concentration of BG TFTs in un-biased state (left) and in positive-stress (right).

However, in some cases PBS was found to cause distortion in device characteristics as seen in Figure.5.3 (left). Post-stress characteristics show a slight left shift accompanied by a hump-like signature. The manifestation of the hump is identified as a distinct distortion with a specific energy state (trap state) that is said to be induced during the application of stress.

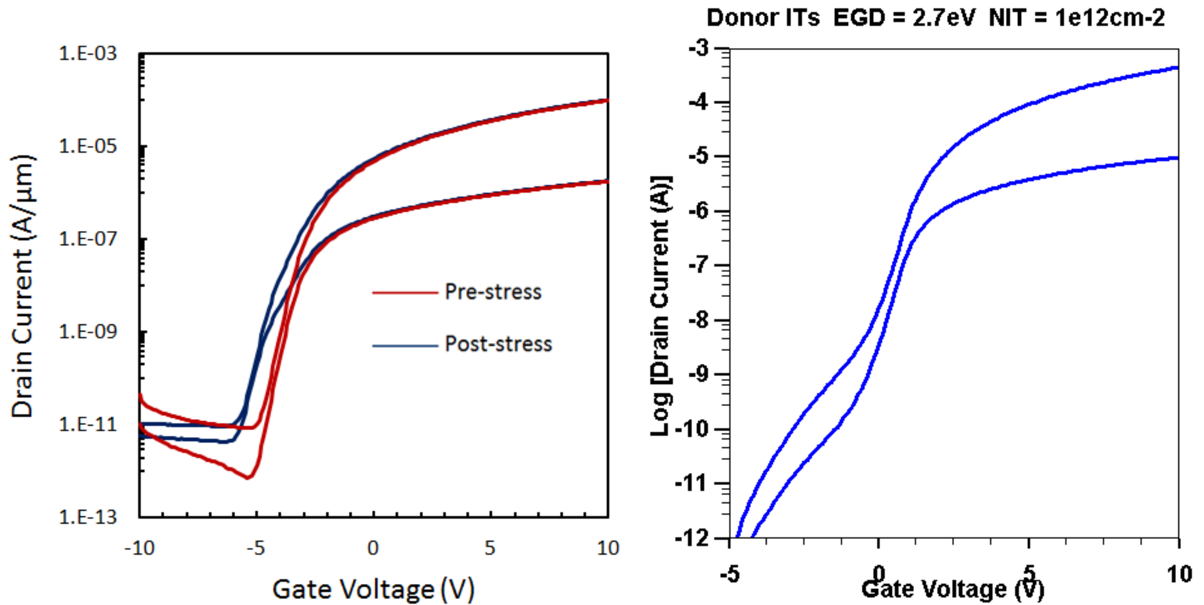

Figure 5.3. (left) PBS for 2000s causing distorted characteristics with a slight left shift due to the presence of remaining interface traps. The distortion appears to manifest itself as a 'hump' that is associated to a trap state that is induced during PBS. (right) TCAD simulation depicting hump-like behavior in PBS with reduced Vo energy state.

TCAD simulations were done to model this distortion. Figure.5.3 (right) shows simulated transfer characteristics where the effect of hump-like distortion is pronounced. Since the devices are passivated these distortions suggest they are not water related. Electrically, a change in the energy state of oxygen vacancies from 2.9 eV to 2.7 eV is said to give rise to the 'hump' [24].

5.1.2 Response to Negative Bias Stress

NBS resulted in significant left-shifting (shift ~ -1.5 V) and subthreshold steepening as shown in Figure.5.4 (right). The starting characteristic has a shallow subthreshold slope, indicating poor gate control over interface traps. Time under NBS appears to convert some of these donor-like traps into positive charge that remains fixed during transfer characteristic measurements [22]. This attracts a negative charge in the channel making it abundant in electrons because of which the transistor doesn't need as much gate voltage to turn on, thus explaining the left shift. A schematic representation of this phenomenon is shown in figure 5.1d (left) along with respective I-V characteristics on the effect of NBS on a BG device.

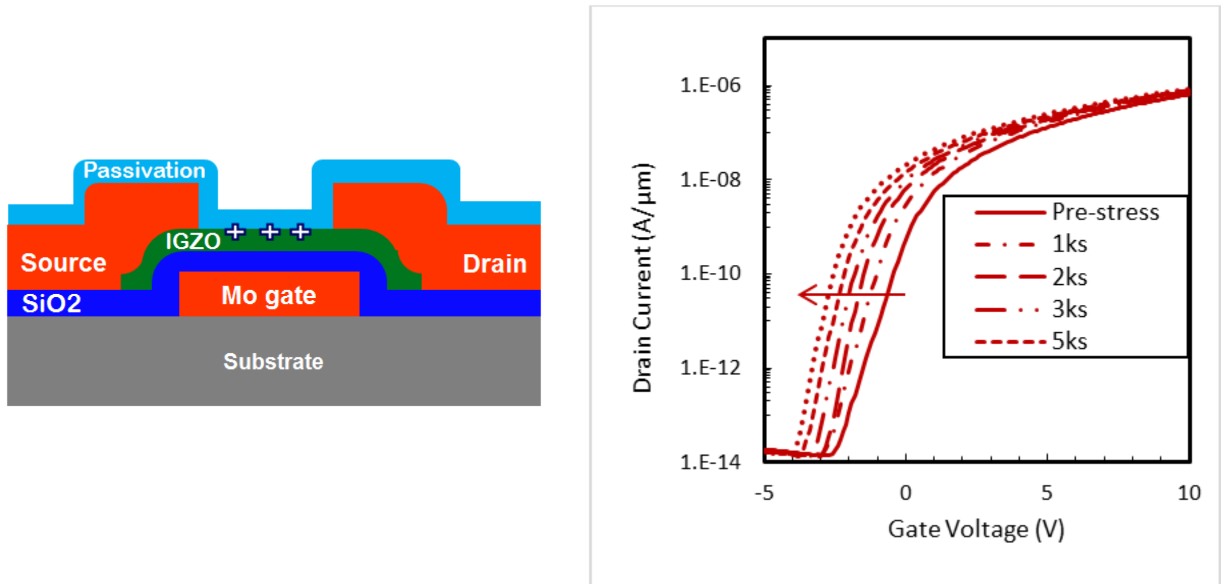

Figure 5.4. (left) Schematic representing ionized oxygen vacancies as fixed positive charges at the back-channel interface. (right) I-V characteristics of L/W=24/100 µm device showing a significant left shift in V_T under NBS [22].

Application of higher gate bias resulted in the threshold voltage shifting more to the left supporting the phenomenon explained above. As seen in Figure 5.5 higher the bias, more shift in the threshold voltage was observed.

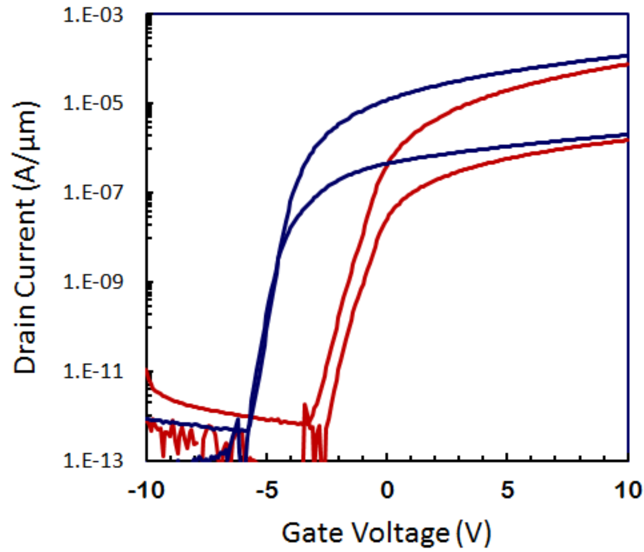

Figure 5.5. BG device under the influence of NBS at -15V for 2000s.

ATLAS simulations of NBS depicted in figure.5.6. shows the channel completely depleted of electrons when there is application of -10V on the gate. The mechanism for negative-stress as explained earlier is consistent with the device working in depletion mode.

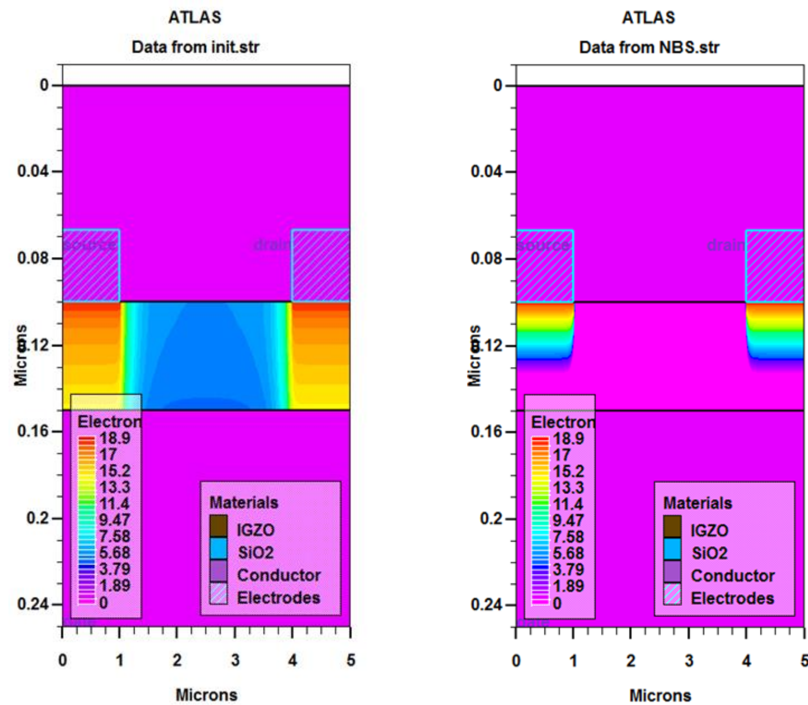

Figure 5.6. Electron concentration of BG device in negative-stress.

In addition to the lateral shift in threshold voltage, we see short-channel like behavior similar to DIBL (drain induced barrier lowering) disappearing with the effect of NBS as seen in figure.5.5. Since the device's channel is L/W=24/100 μm, it does not qualify for a short-channel device and hence the phenomenon of DIBL is not practical for such large devices.

5.2 Reversible Stress Response in BG TFTs

Upon investigating TFTs that were bias stressed, the devices exhibited relaxation or recovery back to their original profiles. Not all devices that were stress tested showed recovery, however bottom gate devices in particular were identified to show a complete recovery when subjected to NBS. As discussed earlier PBS has an insignificant effect on the threshold voltage shift of bottom gate TFTs and hence the corresponding recovery mechanism was not apparent in this case.

5.2.1 Relaxation at Room Temperature

The transfer characteristics for BG TFTs were found to return back to their original "pre-stress" profiles without subjecting the device to any treatment in room temperature. The right shifting "relaxation" phenomenon in these devices began as soon as the application of stress was withdrawn. The mechanism automatically begins and continues to recover until the original profile is met. The recovery period depends on the amount of stress applied. As shown in figure.5.7 the time taken by the BG TFT to completely recover after the application of a 2000s NBS was around five hours. Conversion of ionized donor states back to neutral oxygen vacancies is said to cause the relaxation mechanism.

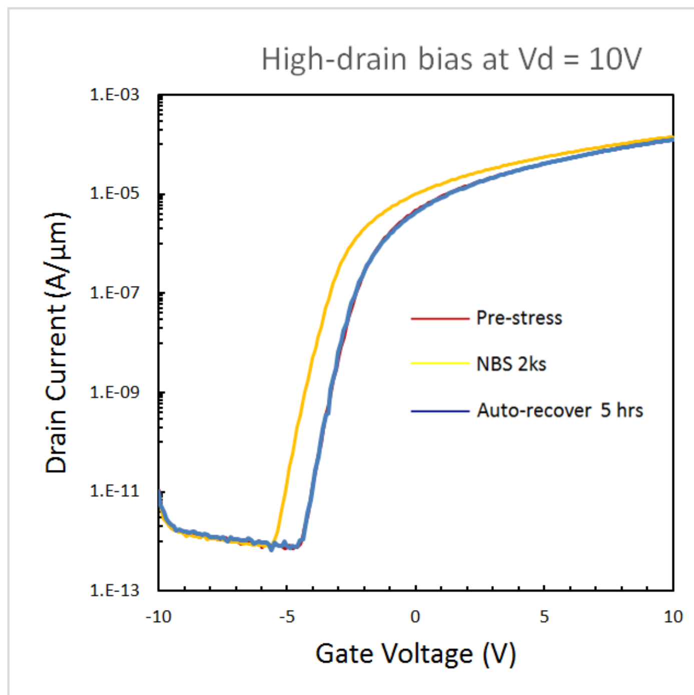

Figure 5.7. Depiction of a BG TFT exhibiting auto relation after subjected to 2000s NBS.

The process of auto-relaxation was found to be accelerated in the first few seconds after which it appeared to reach steady state gradually while recovering to its original characteristics. This behavior can be seen in figure.5.8.

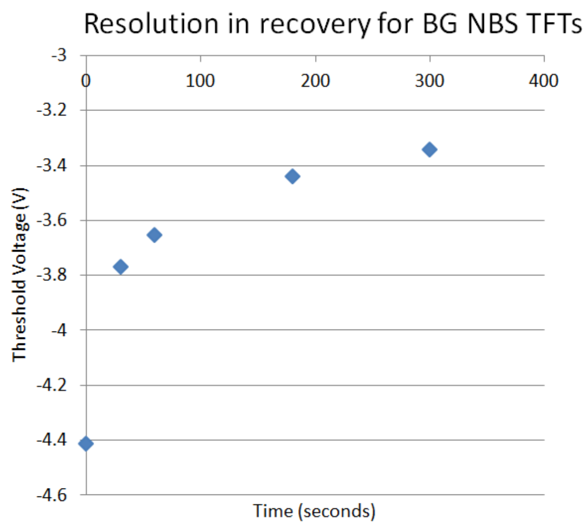

Figure 5.8. Time resolution of the auto-recovery process for a device subjected to 2ks NBS.

As discussed, most devices were resistant to the influence of PBS, with certain devices exhibiting a response that was somewhat characteristic of NBS (i.e. distortion and/or left shift) rather than a right shift as might be expected. Hence, the following proposed model focusses only on the influence of NBS on BG devices during applied bias stress and relaxation.

5.2.2 Proposed Model for Bias Stress and Relaxation

Analogous to dopant atoms in semiconductor materials, oxygen vacancy defects in IGZO behave as donors which when ionized provide free electron carriers. However these defects may exist in various charge states, specifically in a neutral V_O, singly ionized, V_O^+, and doubly ionized, V_O^{2+}, state. Under NBS the channel region is completely void of free electrons, and the Fermi Energy (E_F) drops below the energy of the double-donor V_O^{2+} state, as portrayed in figure.5.9, thus supporting ionization.

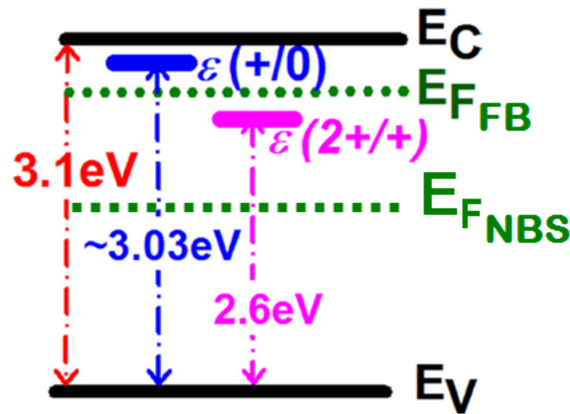

Figure 5.9. IGZO energy band diagram, showing single-donor (V_O^+) and double-donor (V_O^{2+}) oxygen vacancy defect states within the bandgap. The Fermi Energy (E_F) is approximated at flatband and NBS conditions. Using the indicated energy differences referenced to E_V, the energy levels for the V_O^+ and V_O^{2+} states are calculated to be 70 meV and 500 meV below E_C, respectively. Figure adapted from Chowdhury et al. [20]

A model proposed to explain the temperature dependence of NBS under illumination (NBIS) and relaxation has been presented by Chowdhury et al. [20] and has been the primary reference towards the interpretation of NBS results in this investigation without illumination. NBIS using a UV light source (λ = 365nm) resulted in the creation of V_O^{2+} donor states that left-shifted the I_D-V_{GS} transfer characteristic (see figure.5.10) with a forward activation energy of 1.06 eV. The relaxation process resulted in neutralization of the donor states and a characteristic right-shift with an activation energy of 1.25 eV.

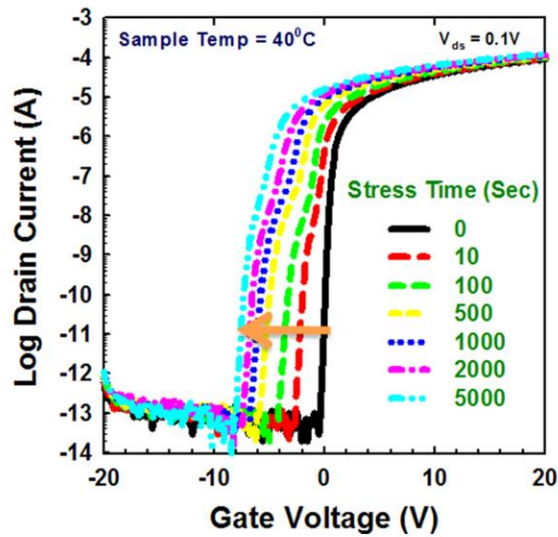

Figure 5.10. Representative response to NBIS [20], shown previously in chapter 3.

Note that the characteristic left-shift is consistent with a certain level of V_O^{2+} existing in quasi steady-state, appearing like fixed charge. However the distinct hump formation is likely due to back-channel interface traps also related to oxygen vacancy defects (see figure 5.3). The stated activation energies are shown in the following potential energy – configuration coordinate diagram in figure.5.11 that represents the formation and relaxation of the operative V_O^{2+} defect state.

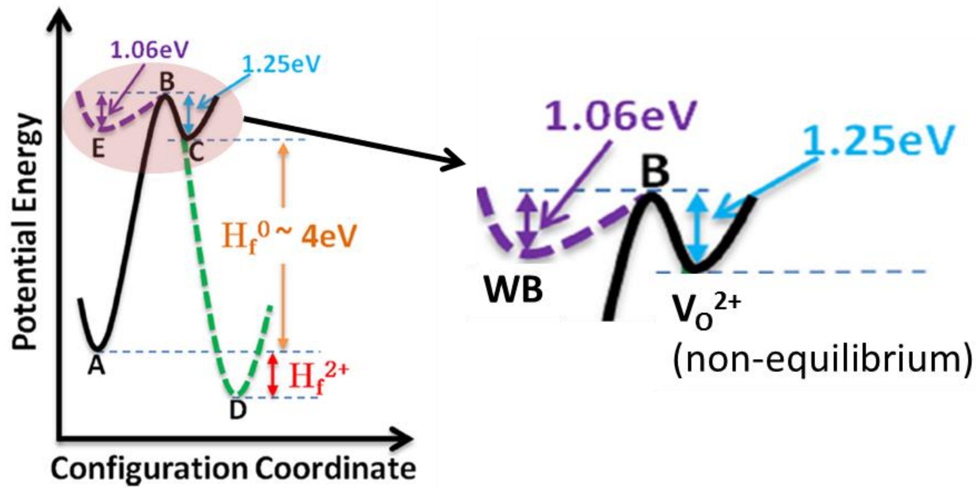

Figure 5.11. Proposed Configuration coordinate diagram by Chowdhury et al. [20] for the creation and relaxation of NBIS defects; NBS instability presumed to be of similar origin. State definitions are described in the corresponding narrative. The zoomed-in region identifies the state transitions and associated activation energies, both forward and reverse, between a "weak bond" neutral defect (WB) and the double-donor V_O^{2+} defect created during NBS which is not in thermal equilibrium once NBS is removed.

The states in figure.5.11 are defined as follows: "A" is a reference ground state (no defect); "B" is a saddle point (i.e. energy barrier); "C" is a neutral oxygen vacancy state; "D" is a double-ionized oxygen vacancy state; "E" is a weak bond state. A detailed discussion can be found by Chowdhury et al.[20] Application of NBS, along with thermal energy and time, will enable a transition from "E" (or WB) to another state over the barrier represented by "B". As E_F is below the double-ionized donor state energy during NBS (see figure.5.9), the neutral oxygen vacancy defect state "C" is not favorable. This results in the creation of a V_O^{2+} defect state "D" which is in thermal equilibrium only during NBS. Once NBS is removed the double-donor defect is no longer in thermal equilibrium, and should recapture electrons and relax back to the neutral V_O state "C", however experimental results show that the energy barrier for the forward transition is

immediately reestablished. Thus the relaxation process involves a transition from the non-equilibrium V_O^{2+} state to WB, with a barrier appearing as if it were returning from state "C". Overcoming the relaxation energy barrier and the recapture of electrons can be considered simultaneous events.

5.2.3 Trap Associated Barrier Lowering (TABL)

Another observation associated with the characteristic left-shift during NBS was a reduction or elimination of behavior similar to drain-induced barrier lowering (DIBL), as well as subthreshold slope steepening and/or reduction of distortion (see figure.5.12). This "DIBL-like" behavior is referred to as trap-associated barrier lowering (TABL) and is related to inhomogeneity of interface charge traps at the back-channel [22]. This results in a series/parallel network of channel regions to complete the electron pathway from source to drain. Figure.5.13 shows a TCAD model of this concept, where high trap density interface regions are separated from each other by narrow gap regions without interface traps.

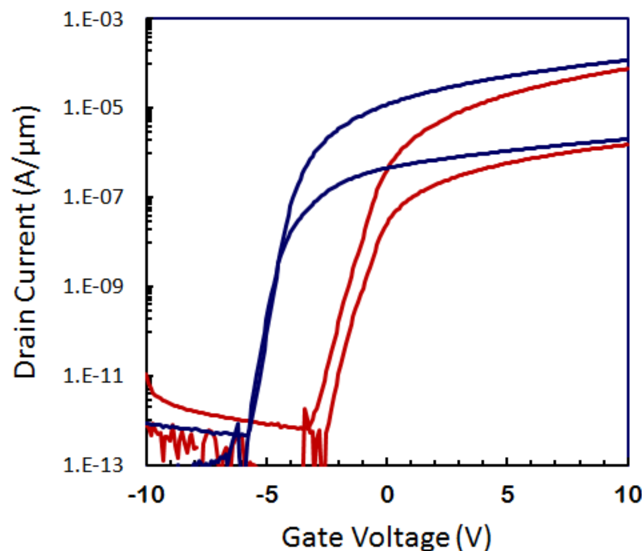

Figure 5.12. A BG device where application of NBS suppresses TABL and steepens the subthreshold region.

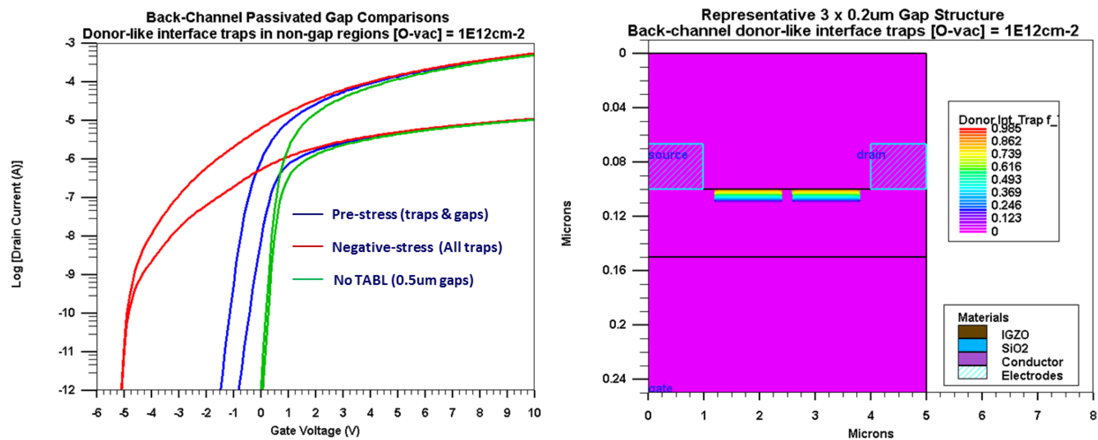

Figure 5.13. TCAD model of TABL (right), where high-trap regions at the back-channel are separated by well passivated gaps. The contours identify the probability of occupancy of trap states which is dependent on the gate bias. The simulated I_D-V_{GS} transfer characteristics (left) show three scenarios: Large passivation gaps which are desirable (green); smaller passivation gaps (0.2 μm) which result in TABL (blue); no passivation gaps (red) which shows significant left-shift and distortion.

The TCAD simulation of the "all trap" scenario (red curves) is somewhat representative of the condition following NBS, however the simulated traps operate in thermal equilibrium and result in significant distortion. The actual behavior would be better characterized by applying a uniform density of positive fixed charge at the back-channel interface. This would be representative of the "temporary" non-equilibrium V_O^{2+} defects which would both left-shift the characteristic and eliminate the subthreshold separation.

5.2.4 Relaxation at Cryogenic Temperature

Under the influence of Liquid Nitrogen (LN2), BG TFTs show an accelerated recovery mechanism. The BG device shown in figure.5.14 was stress tested for NBS at 2000s.

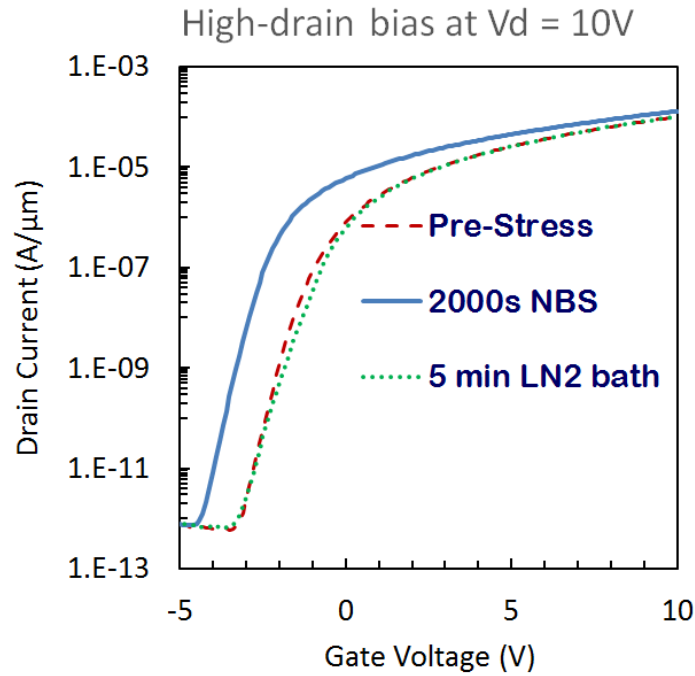

Figure 5.14. Depiction of a BG TFT exhibiting accelerated recovery under the influence of LN2.

Post application of stress, the device was dipped in LN2 bath for 5 minutes. The resulting I-V characteristics showed a complete recovery, suggesting that cryogenic treatment by-passes the pathway for oxygen vacancies to transition from an ionized state to neutral state. In other words, the mechanism dictating the transition of ionized donor states back to neutral vacancy state appeared to be short-circuited under the treatment on LN2. The same relaxation mechanism which took 5 hours to auto-recover was now achievable in 5 minutes. This behavior suggests that when subjecting the device to LN2 temperature, induced stress facilitates the state transition from V_O^{2+} to WB.

5.3 Improved Passivation Anneal and Alumina encapsulation

5.3.1 Alumina Encapsulated BG TFTs

Water molecules at the back-channel interface are reported to act as carrier trap centers which increases instability under bias stress [25]. To eliminate the effect of water on device performance, passivated BG devices were annealed at 400 °C for 8 hours. Following this, a 15nm ALD alumina was deposited immediately post thermal anneal followed by contact opening with 10:1 BOE. The cross-section of an ALD encapsulated device is shown in figure.5.15.

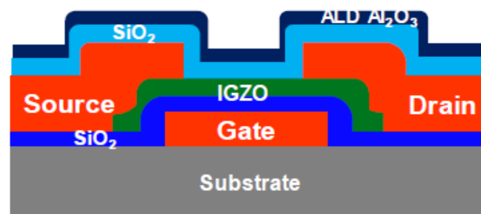

Figure 5.15. Schematic representation of BG TFT capped with ALD Al_2O_3.

Transfer characteristics for alumina capped BG TFTs is shown in figure.5.16. With the encapsulation layer, the devices showed no response to negative-stress, which is in agreement to our discussion involving the removal of interaction of water with the back-channel interface.

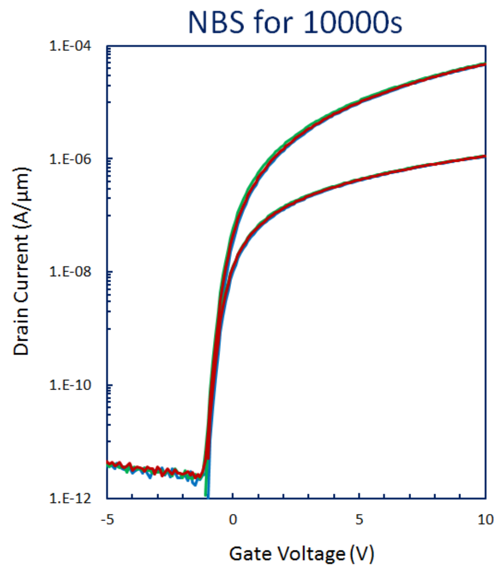

Figure 5.16. BG passivated L/W=24/100 µm TFT with extended 8 hour anneal and ALD Al_2O_3 encapsulation showing very good resistance to NBS.

5.3.2 Response to DG devices

DG devices that were subjected to increased 8 hour anneal with capped ALD alumina also showed excellent resistance under the application of either positive or negative stress. Atlas simulation of electron concentration in DG IGZO TFTs under various stress conditions are shown in figure.5.17.

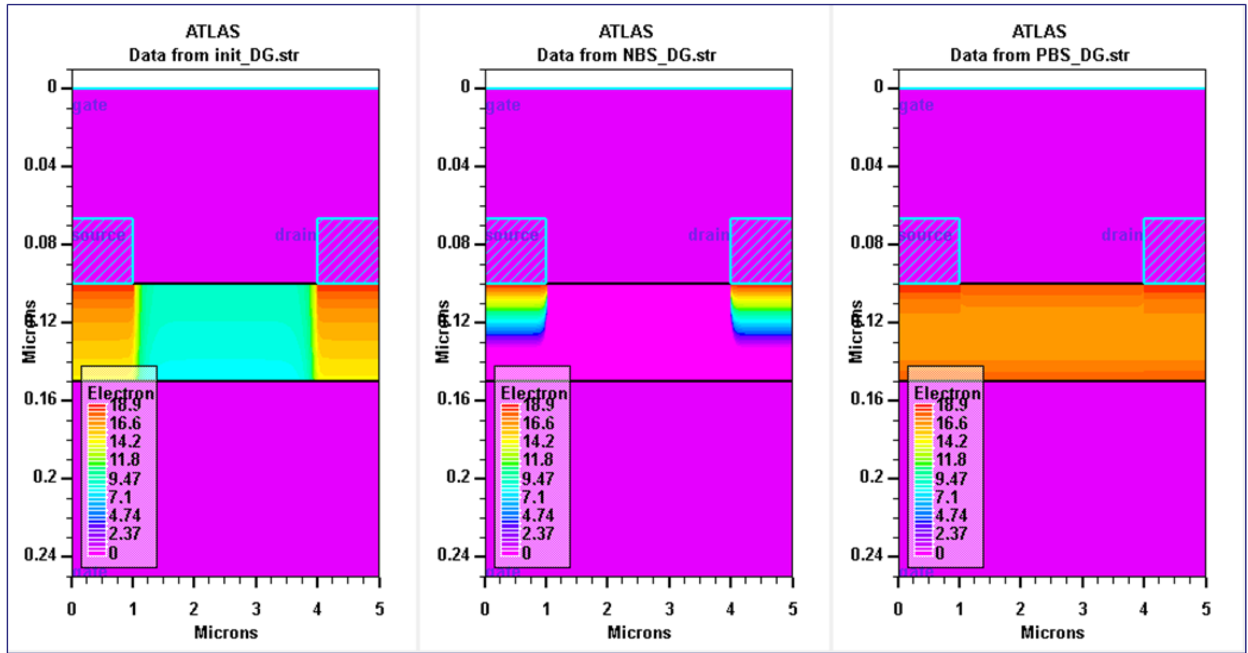

Figure 5.17. ATLAS simulation showing electron concentration in DG devices under (left) un-biased state (middle) negative-stress and (right) positive-stress.

Simulations revealed a device in DG configuration works in depletion mode during NBS and accumulation mode during PBS similar to BG devices. An increased accumulation of electrons at the back-channel is seen.

However with +10V on the gate that is now dictating the transistor's behavior from both sides of the channel, the devices exhibited very good control over defect states explaining such a robust behavior for DG devices. This is apparent in figure.5.18 where PBS shows very good resistance in DG configuration with capped ALD alumina. NBS also seems to have no significant effect on device transfer characteristics. An increased current drive compared to BG devices with extended anneal and capped ALD alumina (see figure.5.16) is apparent.

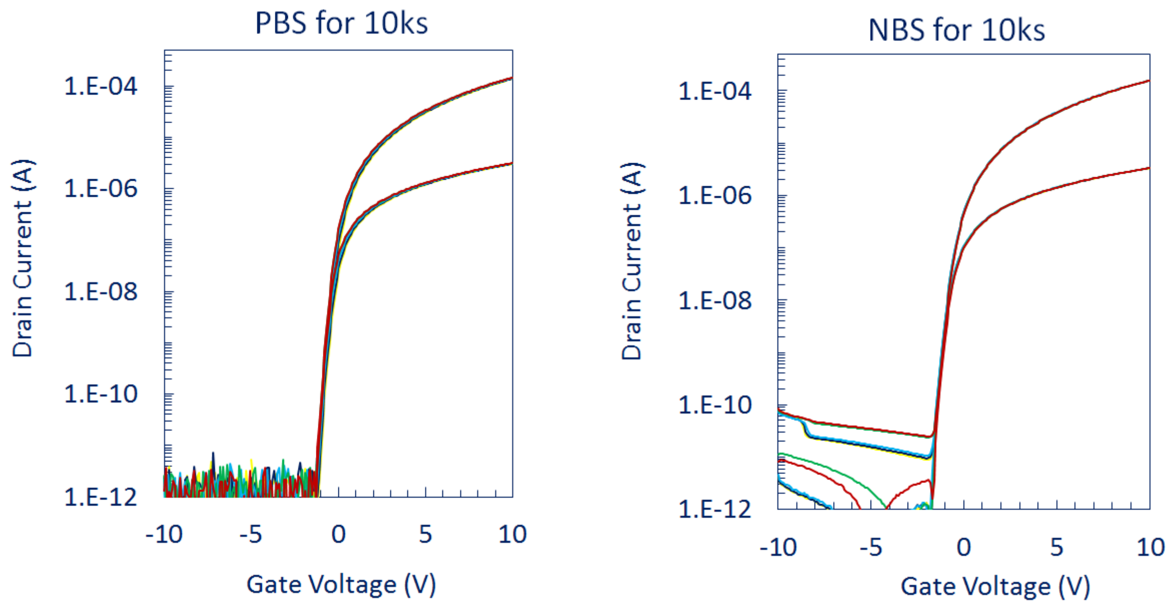

Figure 5.18. DG device with increased 8 hr anneal with capped ALD alumina under the influence of PBS (left) and NBS (right) [23]

Although few devices whose top-gate oxide was known to be compromised showed distinct shifts in threshold voltage [22], there were no changes in transfer characteristics for devices with good dielectric quality.

Chapter 6

Conclusion

Amorphous-IGZO has proved to be a worthy candidate that caters today's display requirements meeting industry standards. With mobility of 10 $cm^2/(V.s)$ and very good sub-threshold characteristics it is now being used in large scale manufacturing of small scale display applications replacing a-Si. Despite being the best candidate to replace a-Si bias stress induced instabilities, which is known to cause degradation in device performance over a period of time has been investigated in detail. Literature review further supports the cause to explore bias stress for IGZO TFTs. IGZO with bottom gate and dual gate configurations were fabricated at RIT to study the response of bias stress for each device configuration. Positive bias stress (PBS) and negative bias stress (NBS) tests involved setting the gate voltage to +10 V and -10 V, respectively, with source & drain at reference ground. Measurements were taken at various intervals over an accumulated time of 10,000 seconds. A characteristic shift in response to bias stress can be attributed to defect state changes either in the dielectric region, the IGZO/SiO_2 interfaces, or the bulk IGZO material.

Passivated BG devices showed slightly degraded transfer characteristics due to interface traps that originated during passivation. BG devices under PBS were found to be fairly stable with few devices showing a slight left shift along with a hump-like distortion in I-V characteristics. This stability is due to the high quality of front-channel SiO_2-IGZO interface. The dielectric goes through densification for 2 hours at 600 °C in N_2 ambient. This was followed by furnace anneal at 400 °C with N_2 ambient for 30 minutes ramped down in air ambient. However, the distortions mentioned are said to arise from minimal back-channel effects as corroborated by TCAD simulations. The device works in accumulation mode during PBS and ATLAS simulations

depicting electron concentrations revealed minimal back-channel effects at the interface. The manifestation of hump-like characteristics has been identified as a distinct distortion with a specific energy state (trap state) that is said to be induced during the application of stress. Change in oxygen vacancy energy state is also suggested to cause such distortions as validated by simulations.

BG devices under NBS showed a significant left shift in I-V characteristics leading to a ~2V shift in V_T. The starting characteristic has a shallow subthreshold slope, indicating poor gate control over interface traps. Time under NBS appears to convert some of these donor-like traps into positive charge that remains fixed during transfer characteristic measurements [22]. This attracts a negative charge in the channel making it abundant in electrons because of which the transistor doesn't need as much gate voltage to turn on, thus explaining the left shift.

The transfer characteristics for BG TFTs were found to return back to their original "pre-stress" profiles without subjecting the device to any treatment in room temperature. The right shifting "relaxation" phenomenon in these devices began as soon as the application of stress was withdrawn. The mechanism of relaxation has been studied using a suitable model involving a barrier for relaxation which the oxygen vacancies must cross to achieve recovery. Cryogenic testing involving liquid nitrogen bath for 5 mins demonstrated an accelerated recovery.

The phenomenon of TABL was investigated in detail since this effect was pronounced in most of our BG devices. Hypothesized as a back-channel effect, TABL is interpreted as inhomogeneity in the back-channel. Time under NBS appears to make TABL disappear, thus homogenizing back-channel charge. Upon withdrawing stress, it was noticed that TABL re-appears. This effect was supported by TCAD simulation scenarios.

BG devices demonstrated weak control over back-channel interface traps with a relatively shallow subthreshold swing and TABL between low and high drain curves. To combat this,

increased back-channel dielectric anneal time up to 8 hours along with ALD alumina encapsulation proved to be an excellent combination to minimize the effect of bias stress on BG devices. A 15nm ALD alumina film deposited over passivated BG devices showed very good resistance to both PBS and NBS. Interaction of water molecules with the back-channel was nullified by ALD capping, thus minimizing the effect of bias stress on IGZO TFTs. Dual gate TFTs exhibited increased current drive and steeper sub-threshold swings compared to BG devices. Upon the application of ALD alumina encapsulation on DG TFTs, the devices showed excellent resistance to bias stress.

6.1 Future Work

Investigating experimental parameters which offer similar benefits in stability with a reduction in anneal time is a potential area that requires to be explored. This involves re-visiting the IGZO and back-channel dielectric thickness since the anneal time required depends on oxygen diffusion through these layers. In addition, alternative ALD encapsulation processes may provide improved suppression to water while enhancing device stability. TFTs will be characterized for bias stress stability as well as the addition of illumination, which has particular importance in display devices. The thermal response of bias stress and relaxation requires further investigation, including both elevated temperature and cryogenic test conditions.

References

[1] Y. Kuo, “Thin Film Transistor Technology—Past, Present, and Future,” Electrochem. Soc. Interface, vol. 22, no. 1, pp. 55–61, Jan. 2013.

[2] A. Sharma, C. Madhu, and J. Singh, Performance Evaluation of Thin Film Transistors: History, Technology Development and Comparison: A Review.

[3] H. Hosono, “Current status and future challenge of oxide semiconductors,” in 2012 19th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD), 2012, pp. 1–4

[4] S. W. Depp and W. E. Howard, Scientific American, 266(3), 90 (1993)

[5] Matsueda Y. Required Characteristics of TFTs for Next Generation Flat Panel Display Backplanes. In The Proceedings of the 6th International Thin-Film Transistor Conference 314–317 (2010)

[6] Singh, Jasprit & Bauer, Siegfried. (2006). Smart Electronic Materials: Fundamentals and Applications. Physics Today - PHYS TODAY. 59. 10.1063/1.2387090.

[7] S. Saxena and J. Jang, "Protrusions of Super Grains Formed by Ultrashort Xe Flash-Lamp Annealing of Amorphous Silicon and Its Effect on the Performances of Thin-Film Transistors," in IEEE Transactions on Electron Devices, vol. 58, no. 8, pp. 2638-2643, Aug. 2011.

[8] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Nature 432, 288 (2004).

[9] E.M.C. Fortunato et al., “Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature,” Appl. Phys. Lett., vol. 85, no. 13, pp. 2541–2543, Sep. 2004.

[10] E.M.C. Fortunato et al., “Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature,” Advanced Materials, vol. 17, no. 5, pp. 590–594, 2005.

[11] H. Hosono, M. Yasukawa, and H. Kawazoe, “Novel oxide amorphous semiconductors: transparent conducting amorphous oxides,” Journal of Non-Crystalline Solids, vol. 203, pp. 334–344, Aug. 1996.

[12] D. A. Mourey, D. A. Zhao, J. Sun, and T. N. Jackson, “Fast PEALD ZnO Thin-Film Transistor Circuits,” IEEE Transactions on Electron Devices, vol. 57, pp. 530–534, 2010

[13] T. Kamiya, K. Nomura, and H. Hosono, “Present status of amorphous In–Ga–Zn–O thin-film transistors: Science and Technology of Advanced Materials: Vol 11, No 4.”, 2010

[14] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” Nature, vol. 432, no. 7016, pp. 488–492, Nov. 2004

[15] K. Nomura et al., “Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment and ab initio calculations,” Phys. Rev. B, 75, 035212, 2007.

[16] T. Mudgal, N. Walsh, N. Edwards, R. G. Manley, and K. D. Hirschman, “Interpretation of Defect States in Sputtered IGZO Devices Using I-V and C-V Analysis,” ECS Trans., vol. 64, no. 10, pp. 93–100, Aug. 2014.

[17] J. K. Jeong, “The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays,” Semicond. Sci. Technol., vol. 26, no. 3, p. 034008, 2011.

[18] E. N.Cho, J. H. Kang, C. E. Kim, P. Moon, and I. Yun, “Analysis of Bias Stress Instability in Amorphous InGaZnO Thin-Film Transistors,” IEEE Transactions on Device and Materials Reliability, vol. 11, no. 1, pp. 112–117, Mar. 2011.

[19] A. Suresh and J. F. Muth, “Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors,” Applied Physics Letters, vol. 92, no. 3, p. 033502, 2008.

[20] M. D. Hossain Chowdhury, P. Migliorato, and J. Jang, “Temperature dependence of negative bias under illumination stress and recovery in amorphous indium gallium zinc oxide thin film transistors,” Applied Physics Letters, vol. 102, no. 14, p. 143506, 2013.

[21] N. Edwards, “Engineering SiO2 Passivated Indium-Gallium-Zinc-Oxide TFTs for Improvement in Channel Control,” Theses, Aug. 2016.

[22] T. Mudgal et al., “Investigation on the Gate Electrode Configuration of IGZO TFTs for Improved Channel Control and Suppression of Bias-Stress Induced Instability,” ECS Transactions, vol. 75, no. 10, pp. 189–197, 2016

[23] Mudgal, “Interpretation and Regulation of Electronic Defects in IGZO TFTs Through Materials & Processes,” Theses, Aug. 2017.

[24] J. Yang et al., “Investigation of an anomalous hump phenomenon in via-type amorphous In-Ga-Zn-O thin-film transistors under positive bias temperature stress,” Applied Physics Letters, vol. 110, no. 14, p. 143508, Apr. 2017

[25] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, et al., “The Effect of Moisture on the Photon-Enhanced Negative Bias Thermal Instability in Ga-In-Zn-O Thin Film Transistors,” Applied Physics Letters, vol. 95, no. 23, p. 232106, 2009.