

PLASMA DAMAGE TO NMOS CAPACITORS

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ABSTRACT

High frequency C-V curves were taken of NMOS capacitors to determine the effect that a RF oxygen plasma has on the underlying thin gate oxide. This plasma was used to remove a positive photoresist. The C-V curves show a threshold voltage shift of 3.75 volts with respect to the undamaged capacitors. The C-V curves also show that the thinner were more affected than the thicker oxides.

INTRODUCTION

In today's semiconductor industry the use of plasma etching is wide spread. Thus, it is important to understand its effects on the electrical properties on thermally grown gate oxides. The plasma etching process exposes the thin gate oxides to high stress electric fields and energetic electrons and ions. These energetic particles damage the gate oxide. This damage introduces energy levels in the forbidden band gap. These levels provide more generation and recombination sites. When these sites are exposed to a high energy stress, such as a plasma, they become charged [1-5]. It is important to understand the plasma's affect on gate oxides, since performance of the devices are affected.

In any thermally grown oxide there are electrically active traps at the Si-SiO₂ interface. These interface traps result from dangling bonds. These dangling bonds are caused by the abrupt ending of a silicon lattice or impurities in the oxide [4,5]. Figure 1 illustrates the physical model of a dangling bond.

These traps introduce energy levels in the forbidden band gap that act as centers for generation and recombination site. When these sites are exposed to a high energy stress, such as a plasma, they become charged. This charge trapping is a major reason for degradation and instability in the operation of MOS devices [1-5].

This research project will reexamine Patricia Ostling's senior project, done in 1988, on how plasma damage affects gate oxides [1]. The major difference will be the use of n-type wafers instead of p-type wafers. How the plasma

damages the oxide will be determined by examining the high frequency C-V curves of NMOS capacitors. The first step in the project is the fabrication of these NMOS capacitors. From the C-V curves, the flatband and the threshold voltages will be examined for shifts, as well as general slope vs theory curves. Figure 2 shows an ideal C-V curve vs a plasma damaged C-V curve. This experiment will attempt to match these curves.

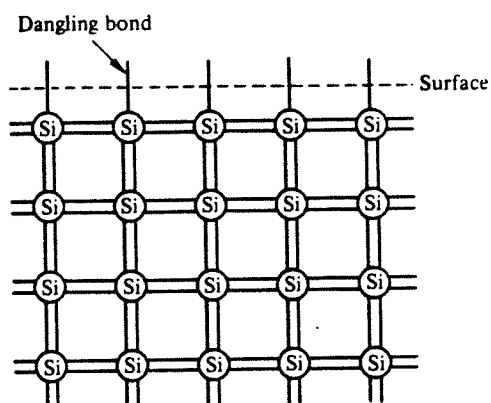


Figure 1 Physical model for the interfacial traps caused by the abrupt termination of the Si lattice. [5]

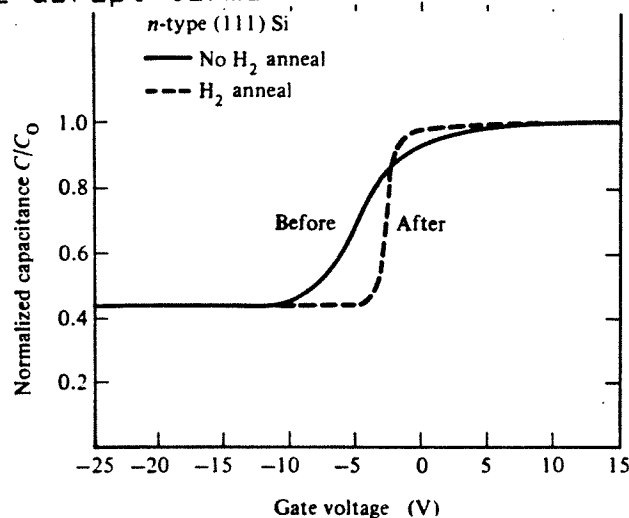


Figure 2 Ideal C-V curves vs plasma damaged C-V curves.

[5]

EXPERIMENT

Eight 3 ohm-cm silicon wafers <111> orientation were used. The wafers were cleaned in $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$, $\text{HF}/\text{H}_2\text{O}$, and $\text{HCL}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$, in preparation for the gate oxide growth. The wafers were divided into two lots, wafers one through four had 600Å of oxide grown on them, and wafers five through eight had 450Å. Half of each of these lots of were coated with KTI-B20 photoresist and ashed. The plasma ash was done for twenty minutes at a forward power of three

hundred watts. All of the wafers then were then cleaned using the standard RCA clean. A film of 2500 angstroms of aluminum was then evaporated on all eight wafers and then patterned into the capacitors. Since N-type wafers were used the back side of the wafer was abraded using a sand blast. This was done to get an ohmic contact on the back side of the wafer [6]. After the silicon lattice was damaged aluminum was evaporated on the back side of all eight wafers. All eight wafers were then sintered at four hundred and fifty degrees in forming gas.

At this point testing was then done using the PNP model 410 high frequency C-V set up in the testing area.

RESULTS/DISCUSSION

Figure 3 and Figure 4 are typical C-V plots. These C-V plots have both the damaged and undamaged capacitors shown. As can be seen the oxides that saw the plasma suffer degradation. The C-V plots show a shift in both the threshold and the flatband voltage as well as a change in slope. The gradual slope of the damaged oxides indicates more interfaces sites than the undamaged oxides. The thinner oxide shows the greater shift in the C-V curves.

Tables 1 and 2 show the summary of the C_{ox} , C_{min} and $V_{flatband}$ values for the capacitors.

Summary of Results
Oxide Thickness of 450A
TABLE 1

Capacitor size	Cox (pf)		Cmin (pf)		Vfb(volt)	
	Plasma	No Plasma	Plasma	No Plasma	Plasma	No Plasma
.0061cm ²	400	390	40	140	-2.0	-.45
		10		100		-1.57
.0046cm ²	238	240	30	90	-1.67	-.25
		02		060		-1.42
.0023cm ²	110	148	25	60	-1.40	-.25
		38		035		-1.44
.0006cm ²	023	034	09	22	-2.0	-.30
		11		013		-1.58

For an oxide of 450A the delta V_t shift was found to be -1.50 volts with a deviation of 1.16.

Figure 3: Capacitance Voltage Curves with and without Plasma for the 450A oxide.

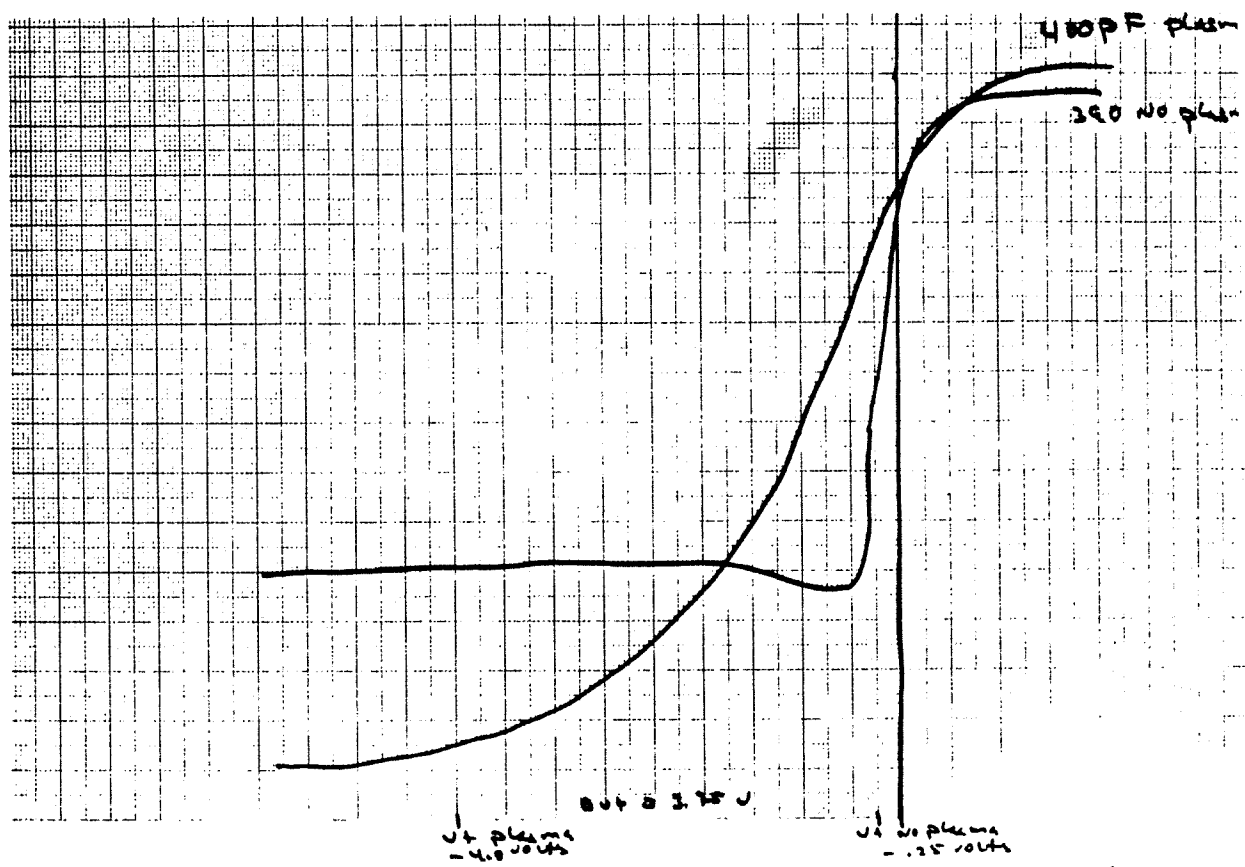
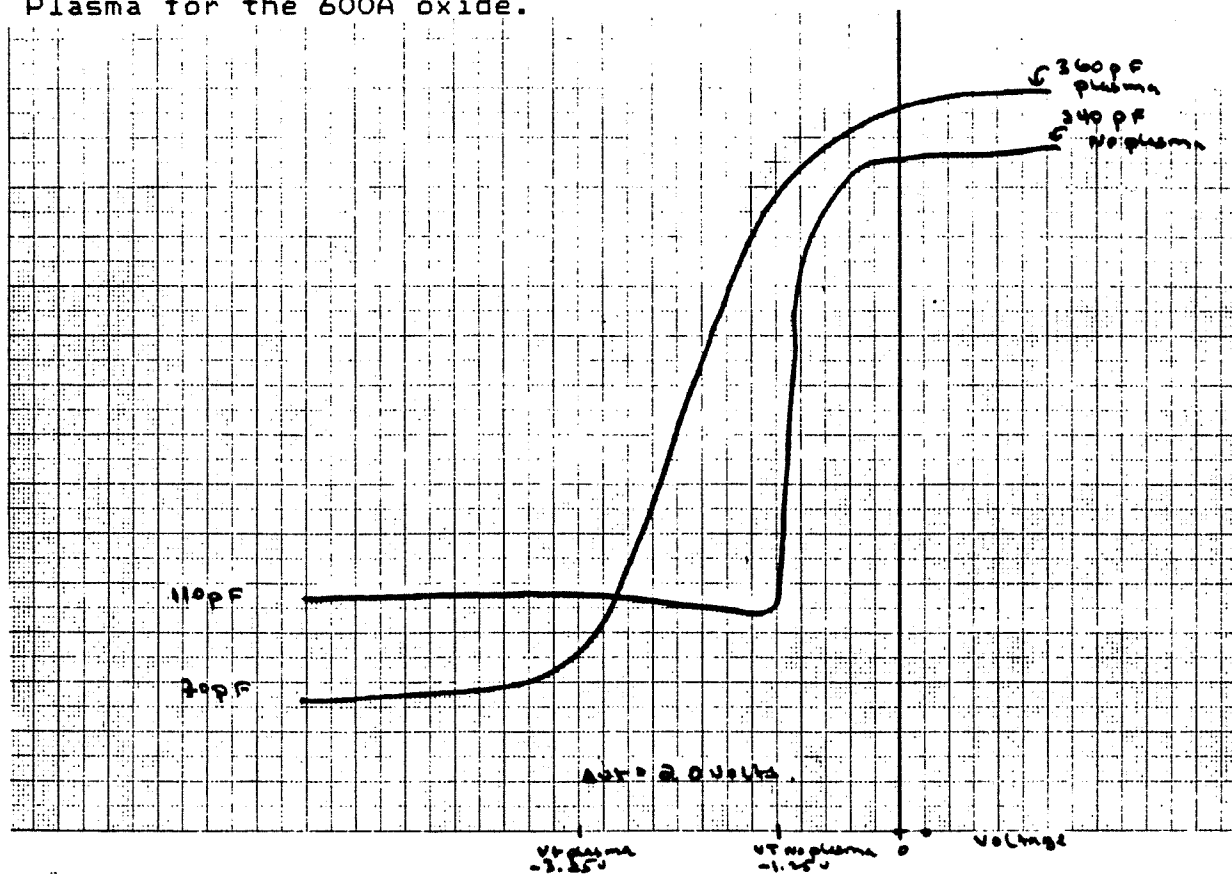


Figure 4: Capacitance Voltage Curves with and without Plasma for the 600A oxide.



Summary of Results
Oxide Thickness of 600A
TABLE 2

Capacitor size	Cox (pf)		Cmin (pf)		Vt(volt)	
	Plasma	No Plasma	Plasma	No Plasma	Plasma	No Plasma
.0061cm ²	342	340	160	113	-1.50	-.20
		02		047		-1.11
.0046cm ²	267	250	60	75	-1.45	-.05
		17		015		-1.06
.0023cm ²	145	130	27	60	-1.45	-.12
		15		033		-1.03
.0006cm ²	049	041	11	22	-1.56	-.10
		08		011		-1.16

For an oxide of 600A the delta Vfb shift was found to be - 1.10V with a deviation of 0.35.

From the table the thinner oxide was more noticeably affected by the plasma damage. The thinner oxides flatband voltage was shifted by -2.17V, whereas the thicker oxides flatband voltage was shifted by only -1.68V. The tables indicate that Cox and Cmin were also affected. The Cmin of the plasma damaged capacitors were less capacitive. The Cox however became more capacitive in the plasma damaged cases. The thinner oxide showed the greater affects of the plasma damage.

CONCLUSIONS

This experiment confirms Patricia Ostling's experiment from last year, except with N-type wafers. It shows that plasma process's effect MOS devices. Significant voltage shifts occurred in both of my oxides. The thinner oxide was more affected. The thinner oxide showed a shift of -1.58V were as the thicker oxide showed a shift of -1.10V.

ACKNOWLEDGEMENTS

I would like to thank Mike Jackson for getting me started on this project. I would also like to thank Gary Runkle for helping me with the sand blasting equipment.

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