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Design, Fault Modeling and Testing Of a Fully Integrated Low Noise Amplifier (LNA) in 45 nm CMOS Technology for Inter and Intra-Chip Wireless Interconnects

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Design, Fault Modeling and Testing Of a Fully Integrated Low Noise Amplifier (LNA) in 45 nm CMOS Technology for Inter and Intra-Chip Wireless Interconnects

by

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To my beloved parents and my mentors without whom, my dreams of obtaining my Master's degree would not have came into a reality

Abstract

Research in recent years has demonstrated that intra and inter-chip wireless interconnects are capable of establishing energy-efficient data communications within as well as between multiple chips. This thesis introduces a circuit level design of a source degenerated two stage common source low noise amplifier suitable for such wireless interconnects in 45-nm CMOS process. The design consists of a simple two-stage common source structure based Low Noise Amplifier (LNA) to boost the degraded received signal. Operating at 60GHz, the proposed low noise amplifier consumes only 4.88 mW active power from a 1V supply while providing 17.2 dB of maximum gain at 60 GHz operating frequency at very low noise figure of 2.8 dB, which translates to a figure of merit of 16.1 GHz and IIP3 as -14.38 dBm.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

While intra-chip communication architecture is shifting from bus-based systems to Network-on-Chip (NoC) architectures [1], inter-chip communication is also advancing at a fast pace to take into account expanding data transfer capacity requests within strict power restrictions. Recent trends according to the International Technology Roadmap for Semiconductors (ITRS) predict that the pitch of the I/O interconnects in ICs is not scaling as fast as the gate lengths or pitch of on-chip interconnects [2]. This implies a gap in density and performance of traditional I/O systems relative to on-chip interconnections. The wiring complexity of both intra and inter-chip interconnects intensifies the issue by posing design challenges, crosstalk and signal integrity issues. This issues are leading towards interconnect technologies like photonic interconnect [3] and wireless interconnects [4] as an energy efficient and speed requirements solution for inter and intra-chip data communication.

Long-range wireless transceiver operating in the millimeter-wave (mm-wave) frequencies [5] do not require physical interconnects for communication. Moreover, such mm-wave antennas fabricated using top layer metals are CMOS process compatible making them suitable for near-term solutions to the wired interconnect problem [6].

Research has demonstrated that on-chip and off-chip wireless transceivers are capable of establishing RF communication links within a chip as well as between multiple chips. Typically, the antennas are embedded in a layer of silicon dioxide (SiO_2), which facilitates the wireless transmission within the chip as well as outside chips [4]. Using such fully integrated on-chip antennas, wireless multi-chip interconnection systems and wireless NoC (WiNoC) architectures have evolved [4][5]. These architectures are shown to improve energy efficiency and bandwidth of inter and intra-chip data communications [4].

The primary empowering innovation for such inter and intra-chip wireless interconnection is the physical layer design comprising of the transceiver circuits and antennas. To compete with state-of-the-art technologies the power consumption of the transceiver circuits should be a minimum while providing the maximum possible bandwidth. Trends indicate a target link energy efficiency of <1pJ/bit at data rates of >10Gbps [7][8].

In this work, I have introduce a low noise amplifier implementation tailored for the requirements of the intra and inter-chip wireless interconnect. The receiver consists of a Low Noise Amplifier (LNA) to boost the degraded received signal.

1.2 Thesis Contribution

- The following points summarize contributions made during the work of this thesis:
- Design and implementation of fully integrated low noise amplifier (LNA) in 45 nm CMOS technology node for the WiNoC interconnection system
- Integrating the proposed low noise amplifier (LNA) with the OOK non-coherent receiver
- Performing schematic-level simulations for characterization of proposed low noise amplifier (LNA)
- Present a system performance comparison between the different receiver designs and proposed design

1.3 Organization of the Thesis

This thesis is organized in five chapters. A brief information about each chapter is mentioned below:

- **Chapter 1. Introduction**: introduces the motivation behind the work that has been performed toward completing this thesis. Then, it states the thesis organization.
- **Chapter 2. Background and Related Work**: explains the trend from single chip to multiple cores systems and evolution of Network on-Chip as an interconnection

fabric. Then it describes the need of Wireless Network-on-Chip (WiNoC) interconnection system and importance of low noise amplifier (LNA) in it.

- **Chapter 3. LNA Design Approach:** describes the different parameters needs to consider while process of low noise amplifier (LNA) design. It includes specification definition, different design topologies, noise sources in electronics, stability and linearity considerations and, effective design approach.

- **Chapter 4. Two Stage CS inductive source degenerated LNA implementation in 45nm CMOS Technology:** explains actual application specific low noise amplifier (LNA) design implemented in 45nm CMOS technology node. It includes working of each component which has been used to design low noise amplifier (LNA) and its effect on performance of the design.

- **Chapter 5. LNA Characterization:** presented obtained simulations results with different setup and analysis performed over designed low noise amplifier (LNA).

- **Chapter 6. Fault Modeling and Testing:** explains an approach of transistor and passive component fault modeling and fault detection model for proposed low noise amplifier (LNA).

- **Chapter 7. Conclusion and Future Work:** mentions a brief summary about the work of this thesis and the obtained results. It also point out the future work.

Chapter 2

Background

2.1 Wireless Network-on-Chip (WiNoC)

Among, these alternatives, wireless interconnect operating in millimeter wave (mm-wave) band is nearer term solution due to its CMOS compatible integration of the underlying enabling technology of miniature antennas and transceivers [19]. However, utilizing the full potential of the novel mm-wave interconnect technology in a wireless NoC (WiNoC) requires overcoming two critical design challenges: i) design of efficient, simple and fair medium access control (MAC) mechanism and ii) managing the wireless bandwidth effectively.

In any wireless network, a MAC mechanism is responsible for ensuring contention free communication among the wireless nodes over the shared wireless channel. However, unlike macro networks, the MAC for WiNoC requires to be simple to minimize area and power overheads [20]. In mm-wave WiNoC architecture, designing multiple non-overlapping channels for Frequency Division Multiple Access (FDMA) is non-trivial from the perspective of transceiver design and is not easily scalable into more than a few concurrent channels. Hence, a single wireless channel is shared among the wireless interfaces (WIs). To divide this shared channel into multiple orthogonal code channels, enabling concurrent communication, a Code Division Multiple Access (CDMA) mechanism has been proposed in [21]. However, such scheme requires power hungry coherent transceiver circuits. On the other hand, due to the distributed and low-overhead

implementation, and fairness in channel access, Time Division Multiple Access (TDMA) is used in many WiNoC architectures [22], [23].

2.2 Related Work

Various mm-wave OOK demodulators have been proposed in literature [7][8][9]. In order to realize high gain, existing 60-GHz LNAs utilize three or more gain stages [10]-[12]. However, increasing the number of stages increases the power consumption and worsens the noise characteristics due to higher number of components. The single-ended EDs implemented in [13] can demodulate up to 10.7Gbps of data rate. However, this design technique utilizes an additional notch filter to attenuate the strong input RF signal due to its single-ended nature resulting in additional area overhead. Differential EDs with connected drain/collector nodes introduced in [14] attained higher data rate of 11.5Gbps compared to single-ended topologies. However, due to the connected drains/collectors, this design yields larger parasitic capacitance at the output restraining the output bandwidth. Moreover, it requires a 5-stage limiting amplifier at the baseband (BB) and a high RF input power, which results in an excessive power consumption. The designed envelope detector in [8] achieves a data rate of 18.7Gbps, however, it requires the use of a gm-boosted cascoded structure that increases the overall power consumption.

None of the above implementations meets all the desirable specifications of the wireless interconnects i.e. high multi-gigabit data rate and high energy efficiency [7] [8]. Hence, in this thesis, we proposes an efficient 60-GHz LNA implementation tailored for the requirements of the on-chip and off-chip wireless interconnect.

2.3 Low Noise Amplifier (LNA)

The Low Noise Amplifier (LNA) is one of the most important block in wireless receiver design. The block diagram of a radio frequency (RF) receiver architecture is as shown [1]:

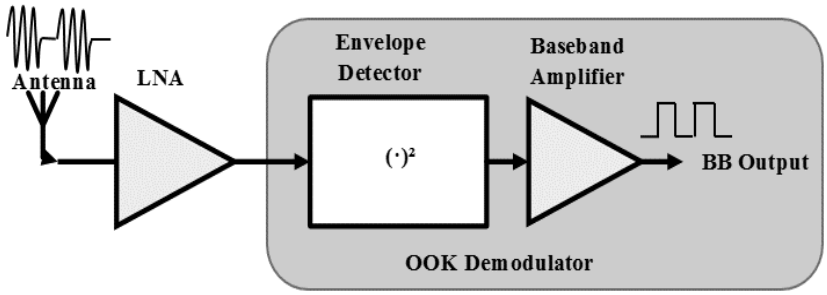


Figure 2.1. Receiver block diagram

The LNA is the first stage of the receiver. This block is used to amplify received signal with minimal noise generated from itself. The signal at LNA input is normally very weak signal, the LNA should provide good gain and noise performance. In LNA Noise Figure (NF) is the critical parameter needs to consider while designing. This can be illustrated using Frii's formula [24] as follows:

$$NFtot = 1 + (NF1 - 1) + \frac{NF2-1}{G1} + \ldots\ldots\ldots + \frac{NFm-1}{G1\ldots\ldots G(m-1)} \quad (2.1)$$

Where $NF_{1...m}$ is the noise figure of the respective stages, NF_{tot} is the total noise figure and $G_{1..(m-1)}$ is the gain of the respective stages. It is evident from the above equation (2.1) that the noise contributed by each stage decreases when the gain of the preceding stage increases. Hence the noise figure of the first few stages in a cascade is very critical.

The significant characteristics of the LNA is to have lesser Noise, optimum Gain across the required Bandwidth and optimum Linearity. Each of these three characteristics along with the LNA design approach have been explained in the following sections.

Chapter 3

LNA Design Approach

This chapter discusses the design procedure of a fully integrated wideband CMOS LNA. The specification definition is discussed first, topology selection and impedance matching is also discussed in this chapter. The derivations and formulas used in design procedure are then provided with detailed design considerations. The comparison of design with existing designs, trade-offs in the design are also discussed in following chapter. The performance and response of the LNA is depend on quality of inductors used. The on-chip inductor design is considered while design process since the LNA design is fully integrated.

3.1 Specifications

Basic requirements for LNA are to provide good gain with low noise production, linearity, impedance matching and low power design. The proposed LNA design is specific to inter and intra-chip communication. Hence it is essential to understand inter and intra-chip communication requirements.

The technology node used for the design of proposed LNA is the Generic 45 nm CMOS process. The considerations and specifications for proposed LNA are as follows. The requirements for low noise amplifier (LNA) design is taken from transmitter design paper [25] and WiNOC papers [26].

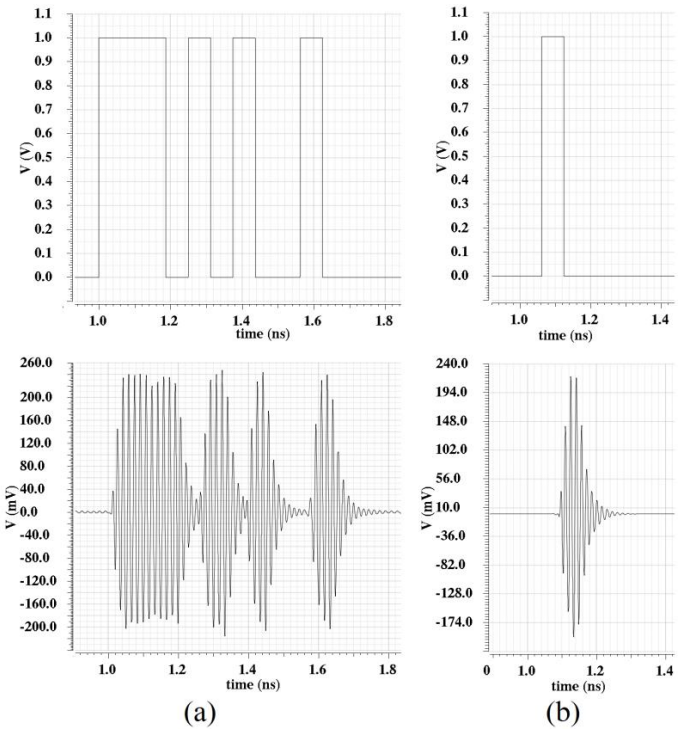


Figure 3.1. BB signal and PA output for (a) pseudo-random sequence and (b) lone pulse analysis.

In [26] the path loss for a 20mm intra-chip link is shown to be around 26dB. In [4] it is shown that the longest distance for an inter-chip link is 59mm resulting in a path loss of about 35dB. Here, we evaluate the BER corresponding to typical intra and inter-chip communication distances. The received signal power is

$$P_R = P_T - PL. \quad (3.1)$$

Here, P_R and P_T are the received and transmitted power respectively and PL is the path loss. We assume a non-coherent OOK receiver as these are most power efficient. LNAs used in typical non-coherent OOK receivers have a noise figure, NF of 10dB or less [27]. The overall Noise Floor, N_{Floor} of such a receiver is given by,

$$N_{Floor} = 10\log(kT) + 10\log(BW) + NF\ . \quad (3.2)$$

Where, k is the Boltzmann constant, T is the absolute temperature and BW is the bandwidth. Therefore, from equation (3.2) the N_{Floor} of the receiver is -67.8dBm at 300K for a *BW* of 16GHz. However, in addition to thermal AWGN, Inter-symbol Interference (ISI) due to bandwidth limitation of the transmitter can add interference noise. As can be seen from the lone-pulse analysis in Figure 3.1. (b) the transmitter [25] output is 450mVpp and 67mVpp when it is transmitting a '1' and a '0' respectively when measured at the center of the pulses. Therefore, the on-off ratio of overall OOK transmitter, R_{OOK} is 16.54dB. The value of ISI noise, N_{ISI} is dependent on path loss and is given by,

$$N_{ISI} = P_T - R_{OOK} - PL. \quad (3.3)$$

The received Signal to Interference and Noise Ratio (SINR) is,

$$SINR = P_R - N_{Floor} - N_{ISI}. \quad (3.4)$$

For non-coherent OOK demodulation, the BER is given by,

$$BER_{OOK} = \frac{1}{2}\exp\left(-\frac{1}{2}SINR\right) + \frac{1}{4}erfc\left(\sqrt{\frac{1}{2}SINR}\right). \quad (3.5)$$

Where, *erfc*(.) is the complimentary error function. For a path loss of 35dB corresponding to a 59mm inter-chip link [4], the BER is dominated by the ISI and is around 10^{-10}.

In [13] the path loss for a 20mm intra-chip link is shown to be around 26dB. The received signal power is given by equation 3.1. In [25], transmitted power is achieved as follows, P_T = -3 dBm *and* P_L = 26 dB. Then the received power is given as, P_R = -29 dB.

For the calculation of the gain output power requirements are calculated first. The LNA output is connect to input of envelope detector (ED) [36]. The minimum power

requirement at the input of ED is -12 dBm. By comparing input and output power of the LNA the gain required to make receiver block functional is around 17 dB.

In many intra and inter-chip wireless communication fabrics, multi-gigabit channels are desirable [28][29]. In our work we target a 16 Gbps wireless receiver for inter and intra-chip data transfer. Therefore, the LNA needs a minimum 16 GHz 3-dB bandwidth at 60 GHz center frequency. We adopt design techniques to achieve extremely low power consumption in the proposed receiver for energy efficiency in the wireless links.

3.2 LNA Topology

The LNA design started with input impedance matching and proper topology selection to perform it. There are several methods to achieve stable input impedance of 50 Ohms. Some of commonly used impedance matching topologies are mentioned below

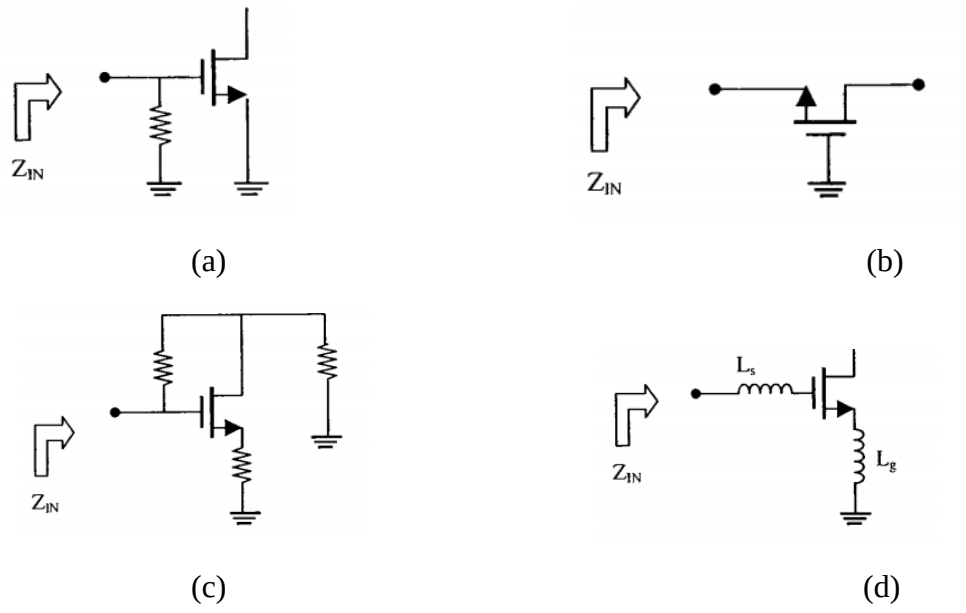


Figure 3.2. Different topologies for input impedance matching.

In above figure different types of input impedance matching topologies are given Figure 3.2. (a) is uses resistive termination but use of resistors is detrimental to the amplifier's noise figure. In Figure 3.2. (b) Another approach for input impedance matching is shown. The common gate input stage to match impedance but gate current degrades noise figure at high frequencies. The third topology shown in Figure 3.2. (c) Uses resistive shunt and series feedback which results in higher power consumption.

3.3 Two stage approach

To achieve low noise, high gain, large bandwidth, high output power and, high linearity using single stage LNA design is very difficult, due to the conflicting operating conditions of the active devices. One can achieve this requirements by implementing two stage design [30]. In the two stage LNA design approach first stage targets low noise and high gain whereas second stage aims for high linearity and high output power requirements.

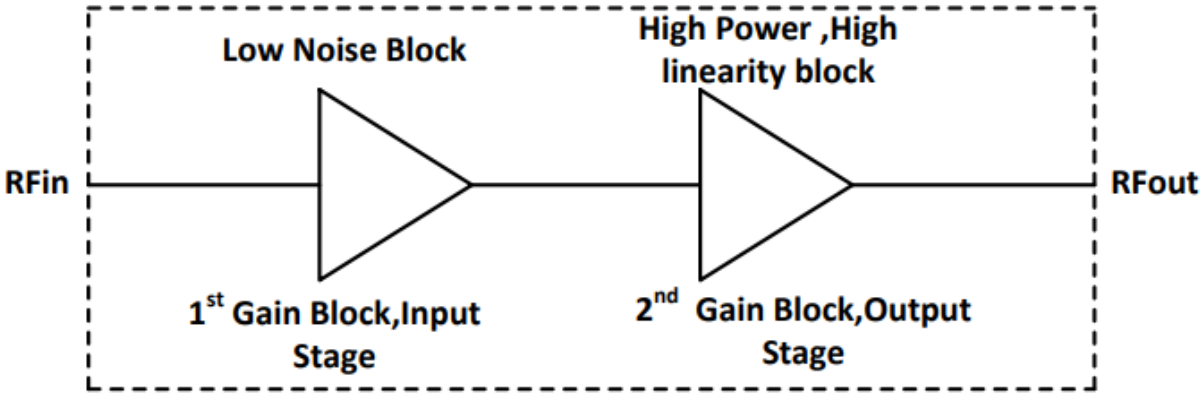


Figure 3.3. Two stage approach

The block diagram of the two stage LNA design approach is shown in Figure 3.3. The first stage provides high gain to reduce the noise in second stage. The high gain of the first stage makes linearity requirements of the second stage very high.

3.4 Noise in cascade system

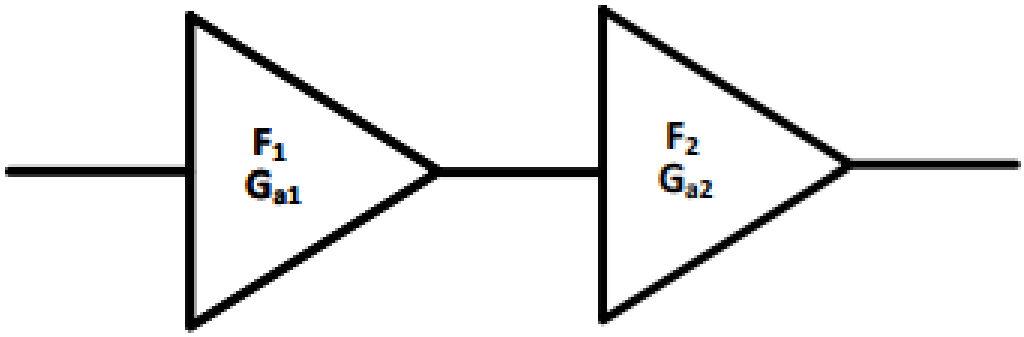


Figure 3.4. Noise figure of cascade two stage approach

The two stage cascade LNA design approach shown in Figure 3.4. where, Ga1 and Ga2 are gain of the stages and F1 and F2 are noise figures of both stages. The noise figure of the overall two stage LNA design approach is given by,

$$F = F1 + \frac{F2-1}{Ga1} \quad (3.6)$$

Here we can say that by improving gain of the first stage we can able to reduce noise figure of the second stage but noise figure of the first stage will be dominant while calculating accumulative noise figure.

3.5 Inductor Degeneration

The topology chosen for input impedance matching of proposed LNA is that of CS amplifier with inductive source degeneration and series gate inductance as shown in Figure 3.2. (d). CS and CG are two widely used transistor configuration in CMOS LNA design. CS LNA has high gain and good noise performance [31]. The placement of inductor in source of CS configuration is known for inductive source degeneration. This inductor affects gain and noise performance of an amplifier. CS configuration can be used in wideband application with the help of special feedback or matching circuits.

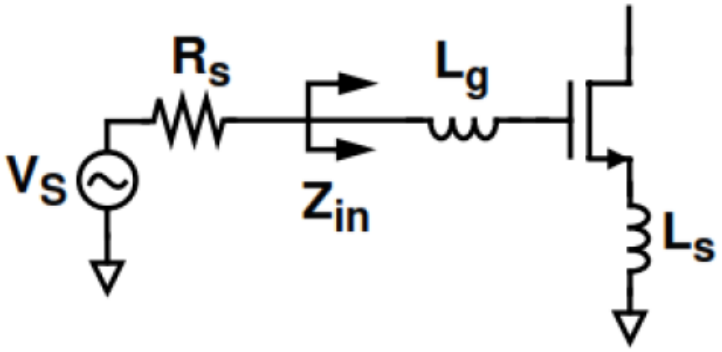


Figure 3.5. Inductor degeneration

If we apply KVL on input side of small signal model shown in Figure 3.6. then we will get.

$$V_{in}(s) = I_{in}(sLg) + I_{in}\left(\frac{1}{sCgs}\right) + \left(I_{in} + g_m I_{in}\left(\frac{1}{sCgs}\right)\right) sL_s \qquad (3.7)$$

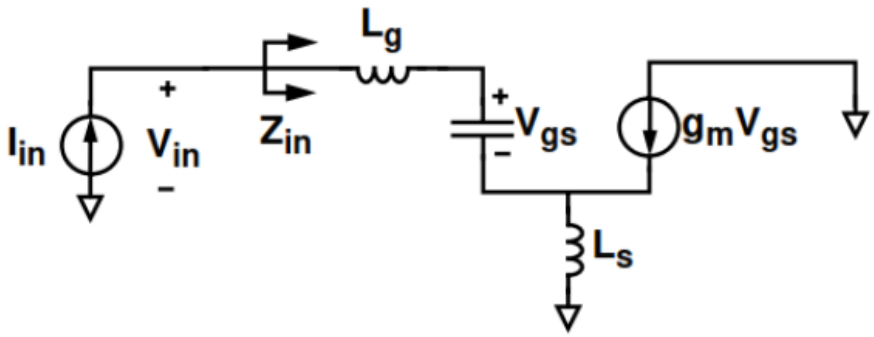


Figure 3.6. Small signal model

Then we can express Zin as follows,

$$Z_{in}(s) = \frac{Vin}{Iin} = \left(\frac{1}{sCgs} + sL_g + sL_s + g_m\frac{LS}{Cgs}\right) \quad (3.8)$$

From equation (3.8) we can say that the matching criteria for input impedance matching is,

$$C_{gs} = \frac{1}{Ls+Lg} \quad \text{and} \quad g_m\frac{Ls}{Cgs} = R_s$$

$$w_0 = \frac{1}{\sqrt{(Lg+Ls)Cgs}} \quad , \quad R_s = \frac{gm}{Cgs}L_s \quad (3.9)$$

3.6 Noise

The degradation of power in the transmitted signal on wireless medium is directly proportional to the distance from the receiver. It is obvious that the signal received at the Receiver is degraded in its strength and the work of the first stage should be to increase this signal strength and itself contributing lesser noise to the actual signal. The received signal strength is given by equation (3.10).

$$P_L = P_T - P_R \quad (3.10)$$

Where:

P_L is the Path Loss suffered by the signal from the Transmitter to the Receiver.

P_T is the Transmitted Power from the OOK Transmitter.

P_R is the Received Power by the OOK Receiver.

The worst-case path loss in intra and inter-chip wireless interconnect systems is found to be around 35dB [1].

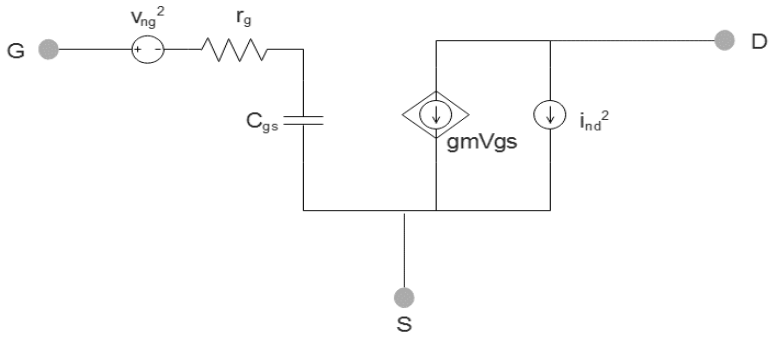


Figure 3.7. Noise model for the MOS transistor.

The basic Noise Model for the MOS is shown in Figure 3.7. Here V_{ng}^2 corresponds to the Gate Thermal Noise. I_{nd}^2 corresponds to the Drain Thermal Noise.

3.6.1 Thermal Noise:

There are two factors contributing to the Thermal Noise namely the Drain Thermal Noise and the Gate Thermal Noise.

- Drain Thermal Noise:

This noise is because of the channel present between the drain and the source region of the MOS. It can be modelled as a voltage controlled resistor as expressed in equation (3.11).

$$ind^2 = 4kT.\gamma.gd0.\Delta f \tag{3.11}$$

Where,

I_{nd}^2 is the Drain Current Noise.

k is the Boltzmann constant.

T is the Temperature (in Kelvin).

γ is a constant equal to 2/3 for long channel MOS and ~ 1 for Short Channel MOS.

gd0 is the output conductance at zero VDS.

Δf is the Bandwidth of Interest.

Equation (3.11) is the approximation of the Drain Thermal Noise in the saturation region without considering the noise from the epi-substrate.

A model can be defined considering the Physical principles and observations. There can be various models for various things. The main purpose is that it needs to emulate a behavior and should aim to be as accurate as possible. For expressing the Noise behavior, there are various standard models that emulate the noise behavior. The SPICE2 noise model is given by equation (3.12) and equation (3.13).

$$|Idnt(f)|^2 = \frac{2}{3}4kT(gm + gmb + gds)\left(\frac{3}{2} - \frac{\frac{Vds}{2}}{Vdsat}\right)\Delta f \quad if\ Vds < Vdsat \qquad (3.12)$$

Where,

gm is the trans-conductance of the MOS.

gds is the output conductance of the MOS.

gmb is the substrate conductance of the MOS.

Vds is the Drain to Source voltage.

Vdsat is the Minimum Overdrive needed for the transistor to be in saturation.

$$|Idnt(f)|^2 = \frac{2}{3}4kT(gm + gmb + gds)\Delta f \quad if \quad Vds > Vdsat \tag{3.13}$$

The BSIM3V3 noise model is given by equation (3.14).

$$|Idnt(f)|^2 = \frac{4kT}{RDS + Leff^2/(\mu eff|Qinv)}\Delta f \tag{3.14}$$

Where,

R_{DS} is the Drain to Source Resistance.

L_{eff} is the Effective length of the MOS.

μeff is the effective mobility.

Q_{inv} is the inverse Charge Density of the MOS.

The Q_{inv} is the inverse Charge Density of the MOSFET which is given by equation (3.15)

$$Qinv = -Weff * Leff * Cox * Vgseff\left(1 - \frac{Abulk}{2(Vgseff + 2vt}Vdseff\right) \tag{3.15}$$

Where

W_{eff} and L_{eff} is the Effective aspect ratio of the MOS

V_{gseff} is the effective Gate to source Voltage

A_{bulk} is the area of the Bulk

V_T is the Threshold Voltage

V_{dseff} is the effective Drain to Source Voltage.

The important takeaway from the equations is that the thermal noise mainly depends on the trans-conductance and the signal Bandwidth.

- Gate Thermal Noise:

There is an unwanted capacitive coupling between the channel and the gate terminal leading to the gate noise. It is modelled as shown in Figure 3.8.

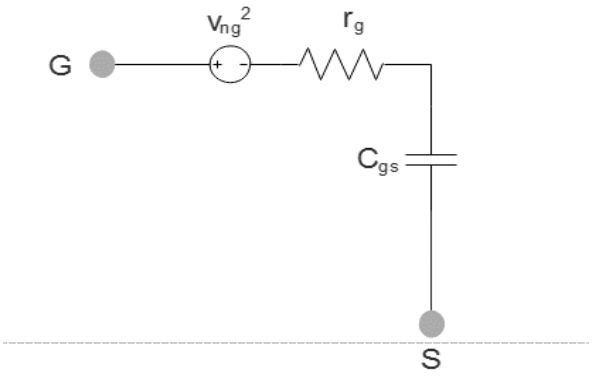


Figure 3.8. Noise Model for Gate Thermal Noise.

Here,

$$vng^2 = 4kT\delta rg\Delta f \tag{3.16}$$

Where

δ is the gate noise coefficient ~4/3 for long channel devices.

rg is the gate resistance contributing to the noise.

The relation of the gate noise with the thermal noise is as given in equations (3.17a-3.17c).

$$ind^2 = 4kT\gamma gd0\Delta f \tag{3.17a}$$

$$ing^2 = 4kT\delta gg\Delta f \tag{3.17b}$$

$$gg = \frac{\omega^2 Cgs^2}{5gd0} \tag{3.17c}$$

The Gate Noise is generally referred to as the Blue noise and has a Power Spectral Density (PSD) that keeps increasing with the frequency as seen in the equation (3.17c).

3.6.2 1/f Noise

As the name suggests, this noise increases with reduction in the frequency. The equation for the same in its generalized form for a MOS is given in equation (3.18)

$$in^2 = \frac{K}{f}\frac{gm^2}{WLCox^2}\Delta f \tag{3.18}$$

Where,

K is an empirical parameter that is device specific

WL is the gate area

Cox is the Gate Capacitance.

For MOS, the flicker noise is due to the defects and impurities in the crystal that trap and release charge. The distribution of this behavior leads to a 1/f noise like distribution for MOS.

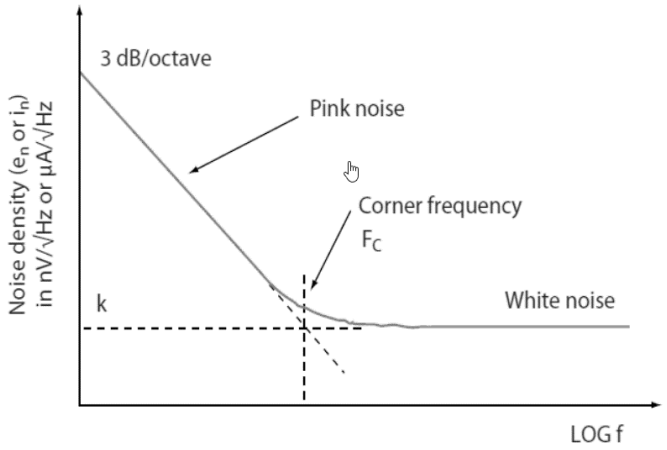


Figure 3.9. Behavior of 1/f Noise with respect to frequency.

It is also called as pink noise. The important takeaway is that the 1/f noise is inversely proportional to the MOS area. Thus, for a given gm, if the device is large, it leads to lesser 1/f noise.

We can now model the noise in the form of system perspective. Noise Factor is one of the important parameter for the LNA which is given in equation (3.19)

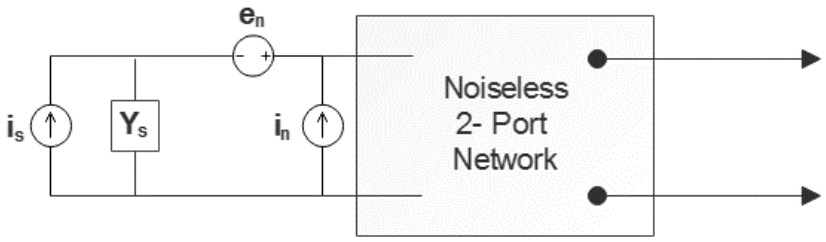


Figure 3.10. Noise Model from the system Perspective.

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise due to input source}} \tag{3.19}$$

The mathematical expression for the Noise Factor is given by equation 11.

$$F = \frac{is^2+|in+Ys.en|^2}{is^2} \quad (3.20)$$

Where

is is the equivalent Shunt Noise Current of the Source.

Ys is the equivalent admittance of the Source.

en and in are the noise generators of the 2-port network.

Considering the correlation (i_c) and the un-correlation (i_u) components affecting the en and in, we can express them as in equation (3.21).

$$in = ic + iu \quad (3.21)$$

Substituting i_n in equation (3.22), we get

$$F = 1 + \frac{iu^2+|Yc+Ys|^2.en^2}{is^2} \quad (3.22)$$

Further, equation (3.22) can be expressed in terms of impedances and admittances

$$F = 1 + \frac{Gu+|Yc+Ys|^2.Rn}{Gs} \quad (3.23)$$

Where,

$$Rn = \frac{en^2}{4kT\Delta f} \quad (3.24)$$

$$Gu = \frac{iu^2}{4kT\Delta f} \quad (3.25)$$

$$Gs = \frac{is^2}{4kT\Delta f} \quad (3.26)$$

Here, the *Rn, Gu* and *Gs* terms correspond to the 3 independent noise sources that are the thermal noise sources produced by an equivalent Resistance or Conductance.

Thus, these equations serve as a purpose in characterizing any two port network as a function of impedances and admittances thereby forming a basis to minimize the noise factor.

3.7 Noise Figure

The MOSFET noise properties depends on the parameters α, γ, δ and, C. These parameters are process dependent which varries with the technology node which we are using for design purposes. The minimu noise for MOSFET amplifier is given by,

$$F_{min} = 1 + 2\left(\frac{w}{wT}\right)\sqrt{gmRg\left(\frac{\gamma}{a}\right)} \qquad (3.27)$$

- Noise Figure for Inductive Degeneration

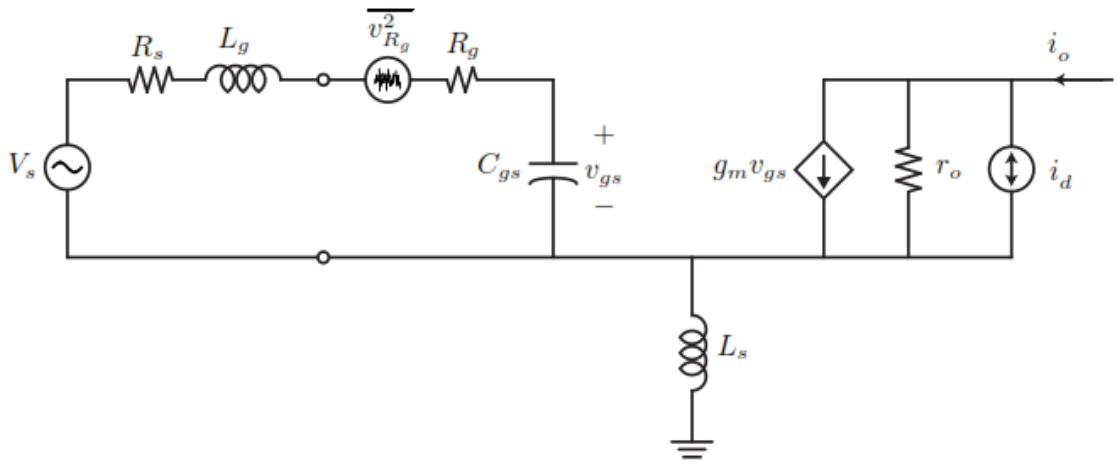


Figure 3.11. Noise figure for inductive source degeneration

The noise figure of the inductive source degeneration CS amplifier is given by following expression,

$$F = 1 + \frac{Rg}{Rs} + (\frac{\gamma}{\alpha})\, g_m R_s\, (\frac{w}{wt})^2 \qquad (3.28)$$

The noise figure is same as CS amplifier which is shown in eq. . The inductive degeneration did not raise the noise so the minimum noise figure Fmin is the same in CS and inductive degenerated CS amplifier topology. The advantage of inductive degeneration is that the input impedance is now real and programmable ($w_T L_s$) without introducing contribution to the noise figure. And by proper sizing, its possible to obtain a noise and power match.

3.8 LNA Stability

Two factors are typically used to evaluate stability of the LNA. The first one is the Rollett stability factor K. Accroding to Rollett stability criteria Rollette stability factor K should be greater than or equal to 1 for unconditional stability.

$$S_{11} = \frac{Zin - Rs}{Zin + Rs} \quad , \quad S_{22} = \frac{Zo - RL}{Zo + RL}$$

$$S_{21} = A_p = \frac{Po}{Pin} \quad , \quad S_{12} = \frac{Pin}{Po}$$

$$D = S_{11} S_{22} - S_{21} S_{12} \quad < \quad 1$$

$$K = \frac{1 + |D||D| - |S11||S11| - |S22||S22|}{2|S21||S12|} \quad > \quad 1$$

The second stability criteria is mu and mu'. This stability measurments gives the distance from the center of the smith chart to the nearest output load stability circle. This stability factor is experessed as,

$$mu = \frac{1 - |S11||S11|}{|S22 - conj\ (S11) * Delta| + |S12\ S21|} \quad (3.29)$$

Where, Delta is the determinant of the S-parameter matrix. There is only one nessasery and sufficuent condition for undition stability of the 2-port network.

That stability condition is expressed as,

$$mu > 1$$

Chapter 4

Two Stage CS inductive source degenerated LNA implementation in 45nm CMOS Technology

4.1 LNA Circuit Design Approach

Previously we discussed about the noise model for a 2 port network. One can use the equations and design the two port circuit to minimize the noise factor derived for this network. The only mentioned drawback for this model is that it is not power constrained. For an optimum design, one should go for a power constrained minimal noise approach as discussed in [32].

The following approach can be used as a starting point in design.

- The width referring to [32] can be given as in equation (4.1).

  $$W = \frac{1}{3\omega LCoxRs} \quad (4.1)$$

  Fixing the length (L) of the transistor and getting the Cox for the process, the width can be found out for the desired center frequency ω and source resistance *Rs*.

- Depending upon the power constraint, bias the device with the needed current.

This involves choosing the V_{gs} for the current required. The V_{th} of the device also plays a role in determining this. Gm/Id design methodologies [gm/id sizing design] can be used to bias the device in weak, moderate or strong inversion.

- The source inductance L_s and gate inductance L_g is then chosen for the input impedance match of 50 ohm to resonate at 60 GHz.

- There are some sacrifices made when considering gain, noise, power and input match. If the gain is not what is needed after employing the first stage, a second stage is cascaded to improve the gain. This also provides an opportunity to increase the bandwidth as the first stage might give a narrowband response.

- Relationship Chart:

  It is a must to have before designing as it gives a clear idea of how one parameter affects another and the best combination to approach a goal.

  The relationship chart used for the LNA design is as shown in Figure 4.1.

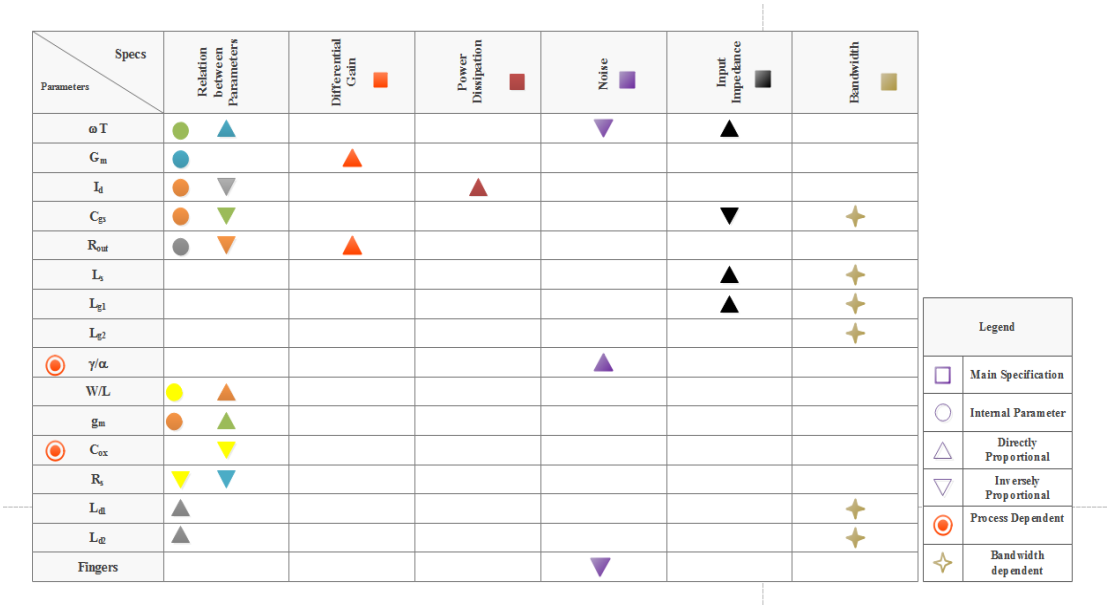
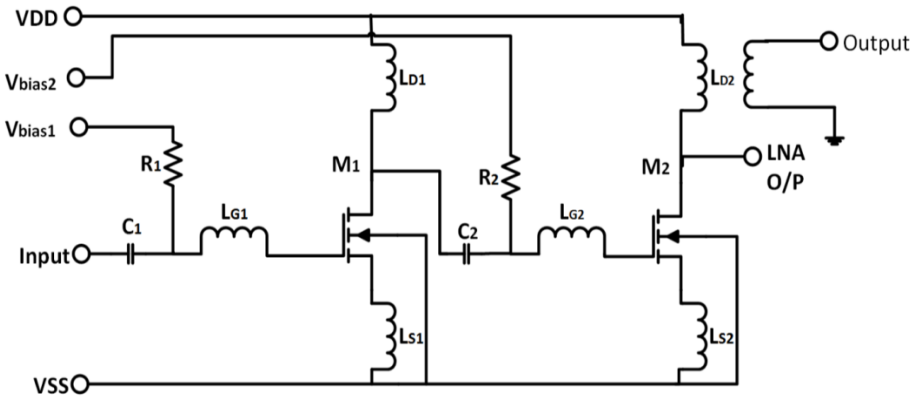


Figure 4.1. Relationship Chart for the LNA Design.



Components	Values
R1	3.2K
R2	3.2K
C1	1pF
C2	18fF
LG1	100pH
LS1	120pH
LD1	400pH
LG2	120pH
LS2	200pH
LD2	750pH
M1	W=24um L=45nm
M2	W=14um L=45nm

Figure 4.2. The schematic of the proposed LNA

The LNA is the first active stage in the most of the receivers. After receiving a weak RF signal degraded by the path loss at its input, the LNA is expected to provide high gain and low noise at its output. On the other hand, LNA designs present a trade-off between the gain and the noise characteristics. Since, the sensitivity of the overall receiver depends on the gain and noise characteristics of the LNA, its design is a critical part of the circuit. Figure

4.2 shows the circuit topology of the proposed low-power LNA based on a two stage Common Source (CS) design. Both LNA stages are chosen to be inductive source degeneration to obtain better thermal noise performance [15]. We specifically choose a two-stage CS configuration as both the Common Gate (CG) and Resistive feedback based topologies suffer from noise figure degradation due to the occurrence of noisy resistances in the signal path. Moreover, cascode structures, which are used commonly in low-frequency design for their high gains, are not suitable for the high frequency application. This is because the parasitic capacitances in the cascode transistors become dominant at higher frequencies, which reduces the inter stage impedance and hence, overall gain.

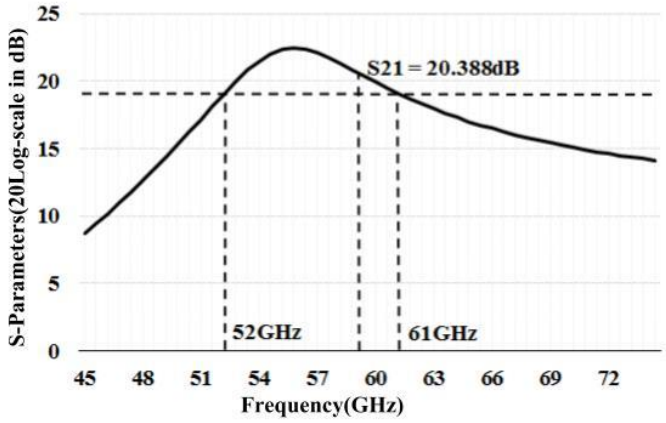


Figure 4.3. The frequency response of LNA without inductor L_{g2}

We have assumed the receiving antenna to have a standard 50-Ohm impedance [16]. Therefore, the input of the LNA is matched to the 50 Ohm impedance of the antenna to achieve optimum gain, power, and minimum noise figure using L-network impedance matching. The equivalent small signal model of the LNA is shown in the Figure 4.3. As can be seen in the figure, L_{g1} is used in the first stage while L_{g2} is used for inter-stage matching. The inductors L_{s1}, L_{g1} and the capacitance C_{gs1} form a series resonant circuit that resonate at

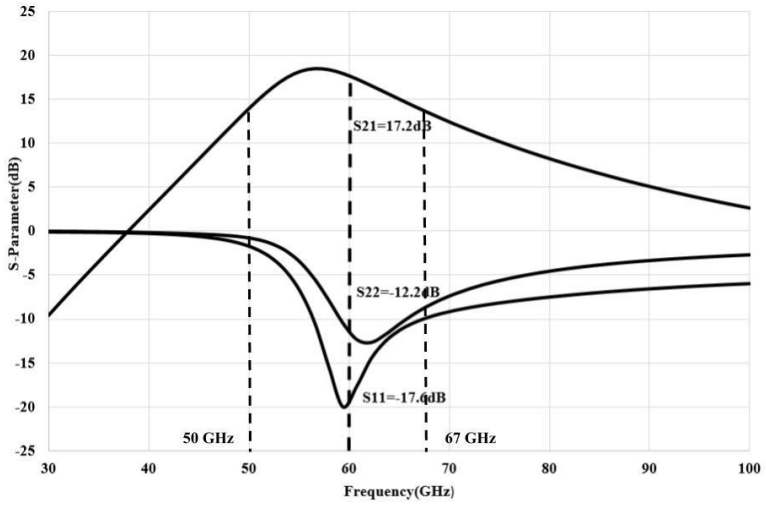


Figure 4.4. The frequency response of LNA with inductor L_{g2}

(Bridged shunt-series peaking)

60 GHz , allowing only the signals having the frequency range centered around 60 GHz. The inductances L_{d1} and L_{g2} form a bridged shunt-series peaking structure that is used for bandwidth extension [14]. In addition, the inductor L_{d2} adds a zero in the overall transfer function further improving overall frequency response. The inductor L_{g2} is inserted to separate the total capacitance into two constituent components. The separation of C_{gs2} and C_2 creates another pole which increases bandwidth. The L_{g2} delays current flow through the rest of the network. This reduces risetime at the drain and increases bandwidth. The Figure 4.3 shows the frequency response without inductor L_{g2}. The bandwidth of 9 GHz is achieved without bridged shunt-series peaking structure. Whereas in Figure 4.4 the frequency response of the proposed LNA is given. The inductor L_{g2} is used to split capacitances C_{gs2} and C_2 which crates bandwidth extension effect and the bandwidth of 17 GHz is achieved. The overall gain or the transfer function of the LNA is expressed as:

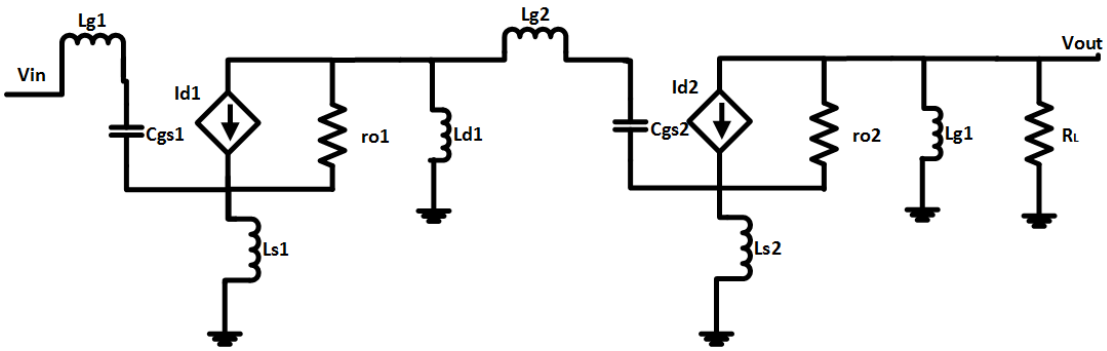


Figure 4.5. Small signal model of the two-stage CS LNA with inductive source degeneration

$$H(s) = H_{stage1}(s) \cdot H_{stage2}(s)\ . \tag{4.2}$$

Where,

$H_{stage1}(s) = g_{m1}(sL_{d1} \,||\, r_{O1}\,(1 + g_{m1} \cdot sL_{s1}))$ and

$$H_{stage2}(s) = g_{m2}(sL_{d2} \,||\, r_{O2}\,(1 + g_{m2} \cdot sL_{s2})). \tag{4.3}$$

From equation (4.2), it can be seen that the gain depends on the output inductive reactance sL_{d1} and sL_{d2}. Hence, selection of these two parameters is important to obtain adequate gain. In order to ensure that the LNA has high bandwidth, the poles of the two CS stages are designed around the 60GHz carrier frequency by tuning the inductors L_{g1}, L_{s1}, L_{g2}, and L_{s2}.

Since the LNA is at the front end of the receiver and sets the system noise floor and sensitivity, Noise Figure (NF) is one of the important specifications that needs to be considered when designing an LNA. With a sufficiently large g_m, the *NF* of a MOSFET at high frequencies can be reduced, and to optimize it, fingered NMOS is used in the circuit

implementation of first stage transistor M_1. By choosing the appropriate number of fingers, the noise figure can be considerably reduced. Besides the number of fingers, the relative placement of the devices also governs the noise figure which must be considered during layout which is outside the scope of this work. Note that diffusion capacitance is also reduced due to the sharing of diffusion regions. A PMOS voltage divider is used for biasing the LNA. The characteristics of the LNA are discussed in chapter 5. The output of the LNA is then fed into the OOK demodulator.

Chapter 5

LNA Characterization

The characterization of the LNA is done using the Cadence Virtuoso Suite. Spectre simulator is used for simulation purposes in the ADEL environment. The transistor model used is the BSIM3 model.

5.1 Noise Figure and Frequency Response

The received signal will have suffered considerable loss in its signal strength due to path loss. Therefore, the noise contributed by the LNA should be minimal, otherwise it will further increase the Bit-Error Rate (BER). This noise is characterized by the noise figure (NF). For the measurement of NF we use the second setup where a port is connected at the input of the LNA that models an antenna with a characteristics impedance of 50 Ohms. A capacitive load is connected at the output port. The same frequency range is used for the measurement of NF as was used for the frequency response.

This is as shown in Figure 5.1. The frequency range used for the measurement of NF is between 45 and 75 Ghz. On simulating, using the Noise Analysis Setup, it is found that a NF of 2.8 dB is achieved as shown in Figure 5.2.

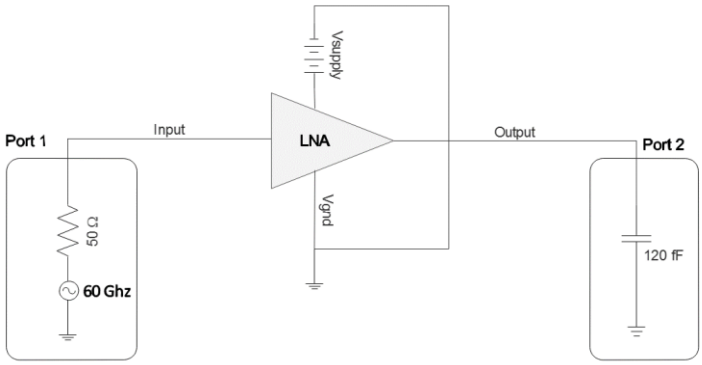


Figure 5.1. Test Bench Setup for Noise Figure Extraction of the LNA.

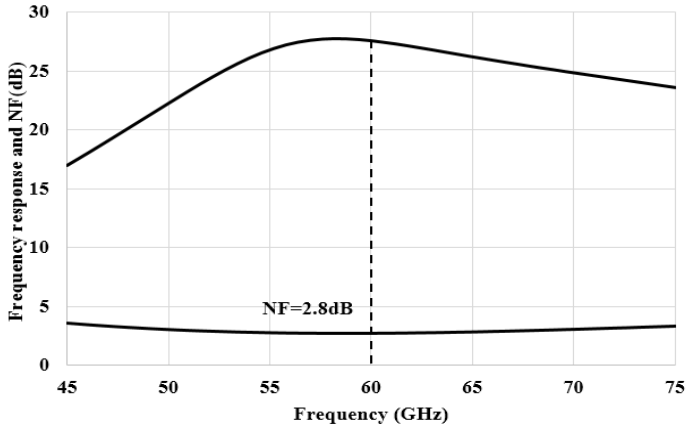


Figure 5.2. The Plot for Frequency Response and Noise figure of the LNA.

5.2 S-parameter Extraction

At high frequencies i.e. 60 GHz, it is important to consider the S-parameters of the circuit as it describes the input output relationship between different terminals of the circuit. A two-port network is setup for the S-parameter extraction. Both the input and

output ports are matched to 50 Ohm impedance to extract the S-parameters. The test bench setup is as shown in Figure 5.3.

It is necessary to define the S-parameters first before moving forward. The S11 is the ratio of reflected power to the incident power in the input port and is known as reflection coefficient or return loss. In our circuit the S11 is -17.6dB at 60 GHz, which signifies the input is matched well with the 50 Ohm impedance of the antenna. This implies negligible reflections from the input at 60GHz. The S22 is the ratio of reflected power to the incident power on the output port and it is found to be -12.2dB at 60 GHz. S21 is the ratio of output power to the input power and represents the power gain for a well-matched LNA. As can be seen the S21 is found to be 17.2dB.

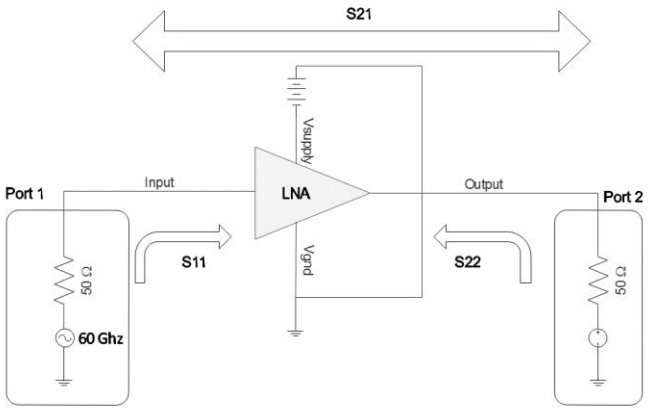


Figure 5.3. Test Bench Setup for S parameter Extraction of the LNA

The S parameters extracted for the LNA receiver model is as shown in Figure 5.4.

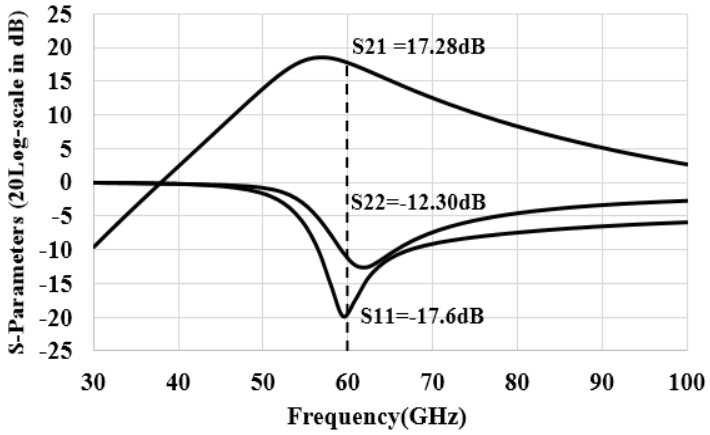


Figure 5.4. The Plot for S-parameter of the LNA.

5.3 IIP3 Linearity measure

As discussed in section 3.3, the significance of Linearity, it is a necessity to measure the IIPR and the 1 dB compression point for the LNA. Though, the test bench schematic is the same as that of the S-parameter extraction, the setup used is quite different. Since IIP3 is related with the harmonics, an hb (Harmonic Balance) Analyses is used for the Linearity measure.

The center frequency and the interference frequency is used in the setup. It can be seen that the IIP3 of the proposed LNA is found to be -14.23dBm at 60 GHz as shown in Figure 5.6.

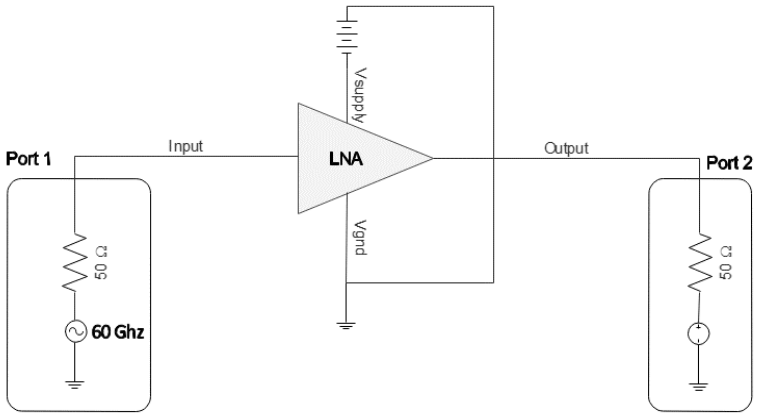


Figure 5.5. Test Bench Setup for IIP3 extraction for the LNA.

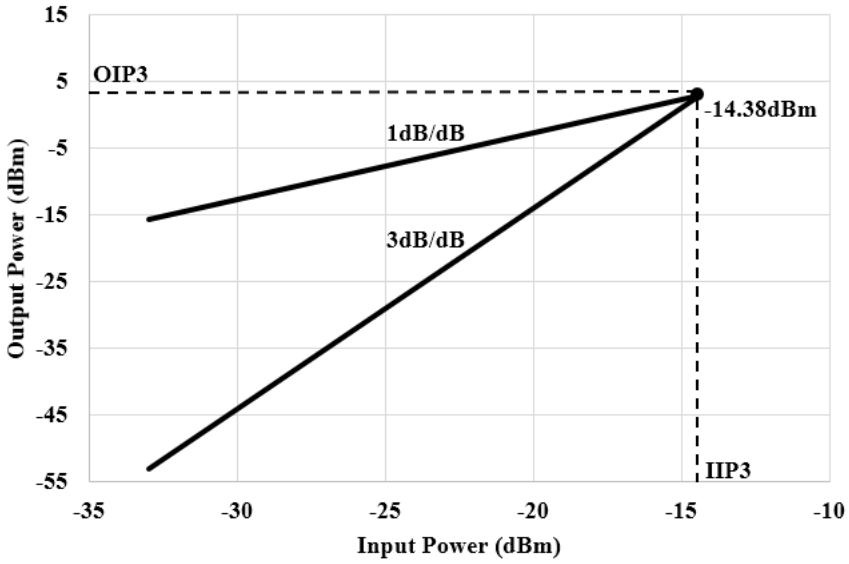


Figure 5.6. The Plot for Linearity Characterization of the LNA

A performance comparison of our LNA with recently published LNAs is summarized in Table 5.1. The power consumption of our LNA is only 4.88mW, which is significantly less as compared to that achieved in the similar works [10][11][12][15]. For a more holistic comparison, we used a metric, Figure-of-Merit (FoM) defined in ITRS, which can be expressed as:

Table 5.1. Summary and comparison of the proposed LNA with prior publications

Ref	***Process***	***Gain Stages***	***Freq. (GHz)***	***3dB BW (GHz)***	***Max. Gain (dB)***	***NF (dB)***	***Supply (V)***	***Pdc (mW)***	***IIP3 (dBm)***	***FoM (GHz)***
[10]	65nm	3 CS	58	8	25	4	1.25	8	~-16.5	22.2
[11]	90nm	1 CS + 2 cascode	60	5	15	3.7	1.5	13.5	-13	25.4
[12]	65nm	2 CS, differential	61	23	10	3.8	1.2	35	4	7.15
[15]	65nm	1 CS + 1 cascode	62	9.2	17.7	3.6	1	9.4	NA	6.66*
This work	**45nm**	**2 CS**	**60**	**17**	**17.2**	**2.8**	**1**	**4.88**	**-14.38**	**16.1**

**without considering harmonic performance*

$$FoM = \frac{G_{max}[abs] \times IIP3[mW] \times f[GHz]}{(NF-1)[abs] \times P_{DC}[mW]}. \quad (5.1)$$

Where, IIP3 is the third order input intercept point, PDC is the power consumption of the LNA, and f is the operating frequency. From Table 5.1, it can be seen that our design consumes the lowest power and achieves the lowest NF for a relatively high gain and FoM. This makes it very suitable for energy-efficient on-chip wireless receivers.

Chapter 6

Fault Modeling and Testing

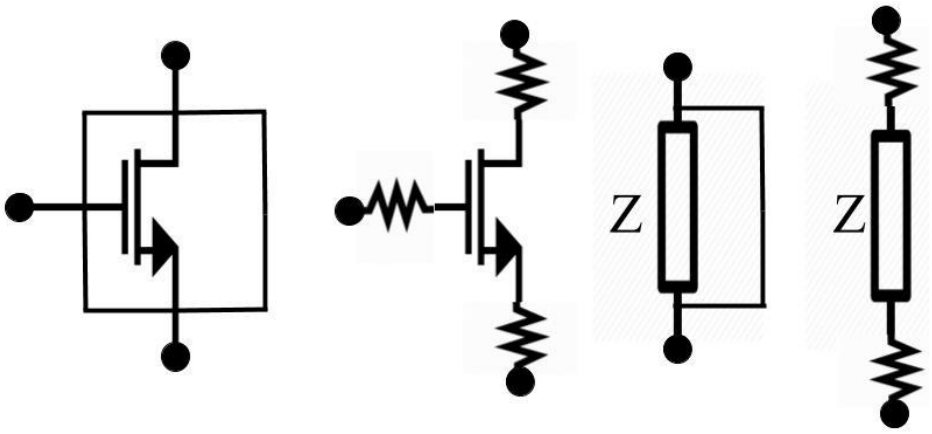
In the development of RF design techniques and CMOS process technologies have brought several new type of process oriented faults which effect on performance of design, quality factor of the passive components on the chip either by coupling different blocks with extra parasitics which ultimately effect on tolerance of the passives. All these issues makes testing of RFIC circuits more challenging and difficult.

Automatic Test Equipment (ATE) is the traditional way of testing analog circuits but, it suffers from the drawback of requirement of test time and expensive testing resources. It is estimated that the testing can account for up to 40% of the manufacturing cost [33][34][35].

Therefore, we came up with cost effective and low-cost alternative test procedure. In previous research different methodologies have been proposed to address the testing issues of RF/ Analog circuits, in particular that of LNAs. In order to reduce testing costs, unique approach is proposed in this thesis by making use of internal circuitry of the receiver block especially envelope detector (ENV) [36] to generate output response over frequency signals of interest in time domain. The obtained time domain response is used to predict fault in the low noise amplifier (LNA) circuit. For comparison with standard fault less and faulty signals both catastrophic (short and open defect) and parametric (process variation or tolerance in parasitics) faults were considered for CMOS low noise amplifier (LNA).

6.1 Catastrophic Faults and Parametric Faults

The catastrophic faults can cause because of low resistance or high resistance between two nodes which is also known as short circuit or open circuit. The catastrophic faults can cause in fabrication process. In this approach we have modeled different catastrophic faults to study behavior of the low noise amplifier (LNA) over chirp signal. There are several different components have been used in low noise amplifier (LNA) circuit such as CMOS, inductor, capacitors etc. The fault models for those components are given below.



(a) (b) (c) (d)

Figure 6.1. Resistive fault models for testing (a) CMOS short (b) CMOS terminal open (c) L/C short (d) L/C terminal open

The parametric faults may introduce due to process variations and change in component value such as inductance, capacitance, resistance, L and W of the transistor.

The Figure 6.1 shows different resistive open and short fault models for CMOS and passive components in the low noise amplifier (LNA) circuit. The possible faults are mentioned below for low noise amplifier (LNA).

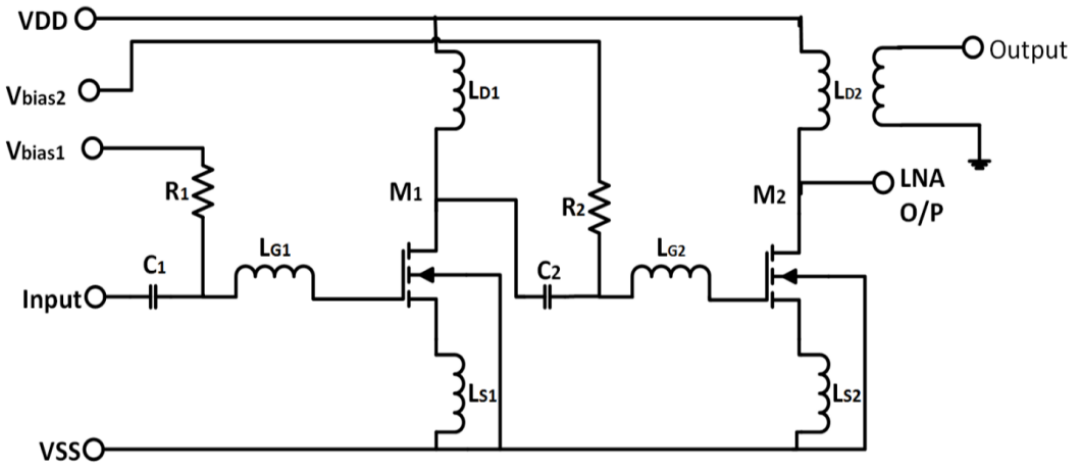


Figure 6.2. The schematic of the proposed LNA

Table 6.1. Catastrophic faults for proposed LNA

Fault placement	**Type of fault**
CMOS	
Gate - Drain (M1)	Short
Gate - Source (M1)	Short
Drain - Source (M1)	Short
Gate - Drain (M2)	Short
Gate - Source (M2)	Short
Drain - Source (M2)	Short
Gate (M1)	Open
Source (M1)	Open
Drain (M1)	Open
Gate (M2)	Open
Source (M2)	Open
Drain (M2)	Open

Passive Components	
LG1	Short
LG2	Short
LS1	Short
LS2	Short
LD1	Short
LD2 - Primary	Short
LD2 - Secondary	Short
LG1	Open
LG2	Open
LS1	Open
LS2	Open
LD1	Open
LD2 - Primary	Open
LD2 - Secondary	Open

Table 6.1. States possible catastrophic faults for proposed low noise amplifier (LNA).

6.2 LNA Test Setup

In Figure 6.3 Practical setup for LNA fault testing is given. It consist of source block which is capable of generating chirp signal.

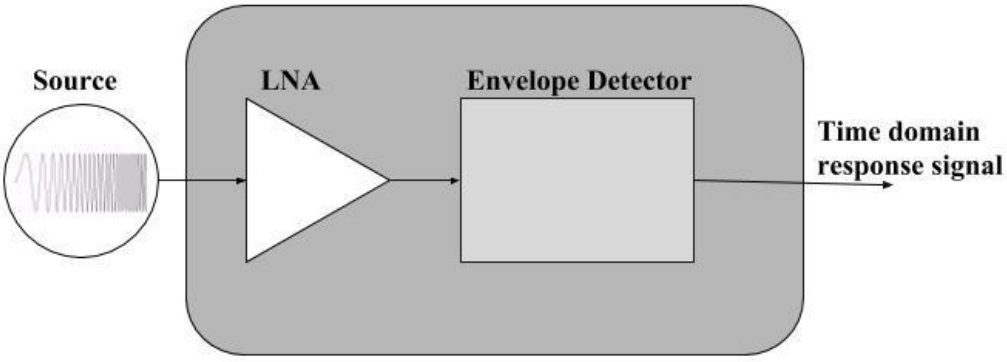


Figure 6.3. The proposed test setup for LNA

6.2.1 Chirp Signal

The chirp signal is a signal in which the frequency of signal changes with respect to time. The frequency can change towards up or down which is also called as up-chirp or down-chirp respectively.

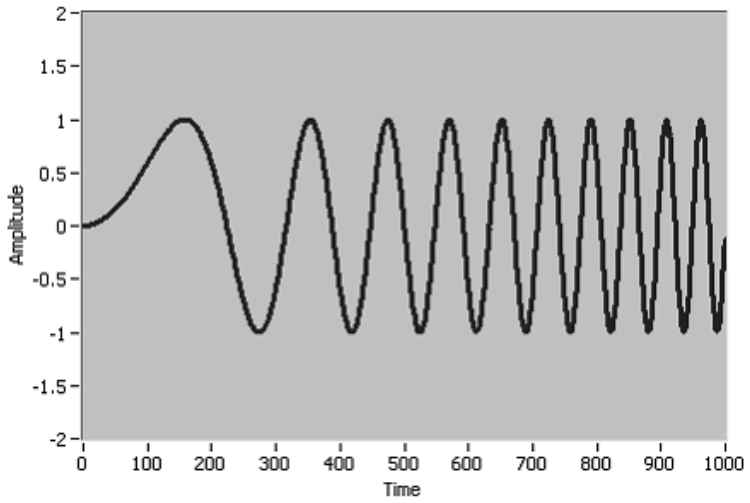


Figure 6.4. Chirp signal

The Figure 6.4 shows chirp signal. The amplitude of the signal is constant over the time but frequency is changing with respect to time.

The chirp signal includes different frequency sinewave signal with same amplitude all over the frequency band. The frequency band which we are considering for testing of proposed LNA is given by bandwidth of the LNA. The frequency band of 55 GHz to 65 GHz we have considered for test analysis. The chirp signal mathematically expressed as [37],

$$A_x \sin \{ 2\pi [f_{min} + (f_{max} - f_{min}) (\frac{t}{2tduration})] t \} \quad (6.1)$$

Where,

t extending from 0 to $t_{duration.}$

A_x is the amplitude of chirp signal

f_{min} and f_{max} are respectively the smallest and largest frequencies of interest

$t_{duration}$ is the duration of the chirp

For Chirp signal implementation in Cadence Virtuoso functional VCO block is used. The chirp signal is obtained from functional VCO block by providing ramp signal to the voltage control pin (V_{ctrl}) of the VCO. The gain of the VCO is calculated by taking ratio of the maximum and minimum frequencies. The gain of the functional VCO is given by following formula,

$$Gain\ of\ the\ VCO = \frac{fmax}{fmin} \quad (6.2)$$

Where,

f_{min} and f_{max} are respectively the smallest and largest frequencies of interest

The alternate way to implement Chirp signal in Cadence Virtuoso is by making use of different multiplexer blocks form Functional library. To obtain chirp signal the frequency range from 55 GHz to 72 GHz is considered and 18 different sinewave sources with 24 mVpp ac magnitude have been used. The ac magnitude is selected to satisfy specific requirements of the components in test measurement setup.

The next block is low noise amplifier (LNA) is under test. At the output of the low noise amplifier (LNA) the observed RF signal has different amplitude with respect to frequency as LNA amplifies particular frequency more than other. The amplitude of the achieved RF signal depend upon bandwidth of the LNA. By introducing above faults all responses were achieved. The obtained responses are difficult to compare because of multiple frequency components and very challenging to predict the fault just by observation. To understand faulty responses more clearly one more block is used in test setup. The envelope detector is used to detect envelope of the RF signal obtained from LNA.

6.2.2 Envelope Detector

The purpose of the OOK demodulator is to recover the digital information embedded in the amplitude of the carrier wave input signal. Since this information is modulated with a high frequency carrier signal, the OOK demodulator will exhibit a Low Pass Filter characteristic, removing the carrier wave and recovering the baseband digital signal.

The referred OOK demodulator [36] consists of a source degenerated ED at the input stage and a two-stage BB amplifier at the output. The schematic of referred source degenerated differential ED is shown in Figure 6.5. Most common ED architectures in literature employ the heterodyne receiver principle wherein the high frequency RF signal is first down-converted to an Intermediate Frequency (IF) and then detected [14]. Such architectures require the use of a local oscillator and a mixer that consume significant

power. Moreover, the design needs to take care of the unwanted image frequencies that leads to additional tuning requirement in the LNA.

The ED referred from paper eliminates these power hungry blocks and directly detects the transmitted OOK high frequency signal without the need of an additional gain boosting mechanism as mentioned in the prior work related to direct conversion receivers [4]. Moreover, the differential pair with inductive source degeneration improves the common mode noise rejection and linearity. A center-tapped transformer is used to split the single ended LNA output to two sinusoidal signals with opposite phases.

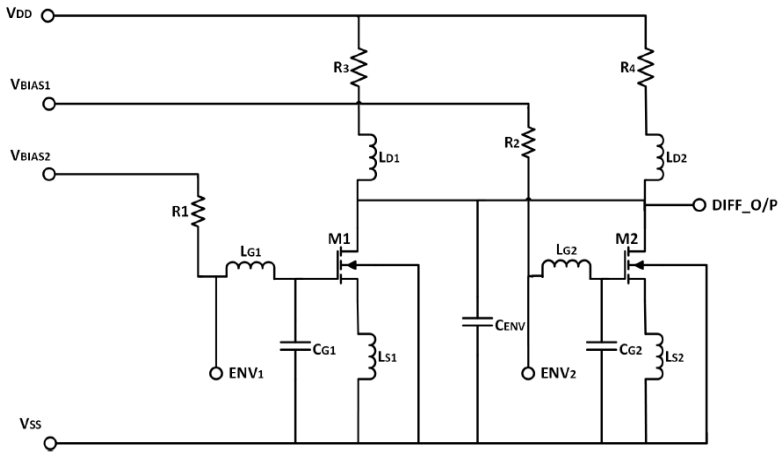


Figure 6.5. Circuit diagram of the Envelope Detector circuit model.

The obtained impedance and the small signal gain with small signal model is as shown in Figure 6.6, also shows the resistance and the capacitance equivalent of the ED. This allows to visualize the components responsible for the Low Pass Characteristic for the ED.

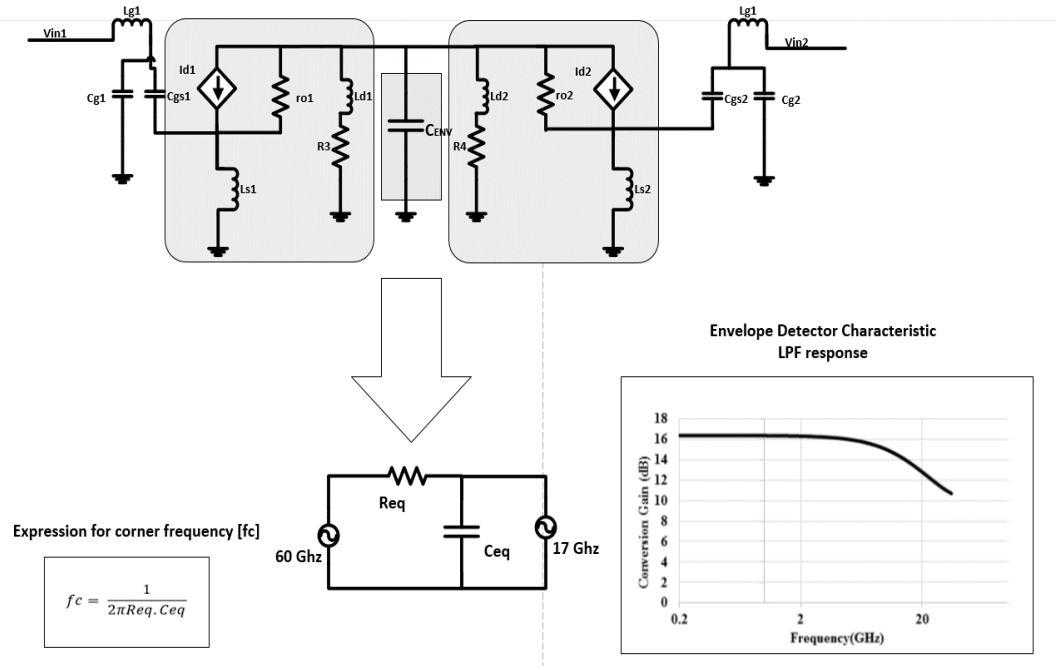


Figure 6.6. Small Signal Equivalent model of the Envelope Detector.

Figure 6.6. shows the conversion gain of the envelope detector. It can be seen that the referred ED achieves a gain of 16 dB with a 3 dB bandwidth of 17 GHz. The referred ED has maximum data rate of 17 Gbps. While doing testing need to make sure that the change in amplitude of RF test signal should be less than 17 Gbps to get undistorted response signal at the output of ED.

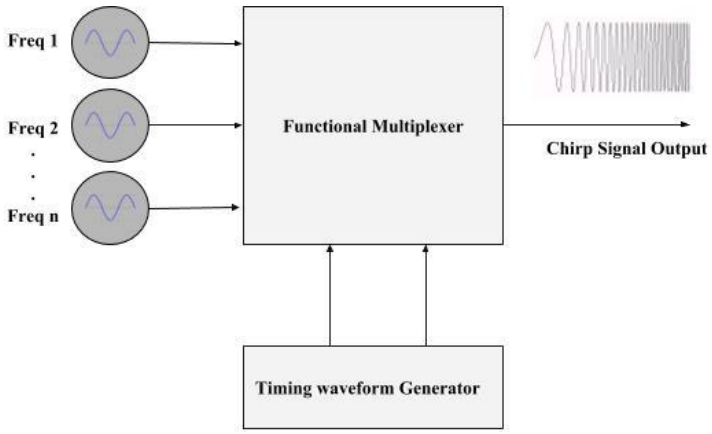


Figure 6.7. The alternet logical approach to generate chirp signal

6.2.3 Simulation Experiments to Differentiate Faults

The LNA faults, simulating the possible manufacturing effects have been introduced using short faults and open faults as discussed in section 6.1. The Figure 6.3 Shows the proposed test setup for LNA. The same test setup is used to introduce faults and simulate it using Cadence Virtuoso to find fault free and faulty responses. By making observation at the output of envelope detector simulation results were recorded. The transient and ac analysis is performed with the help of ADE XL.

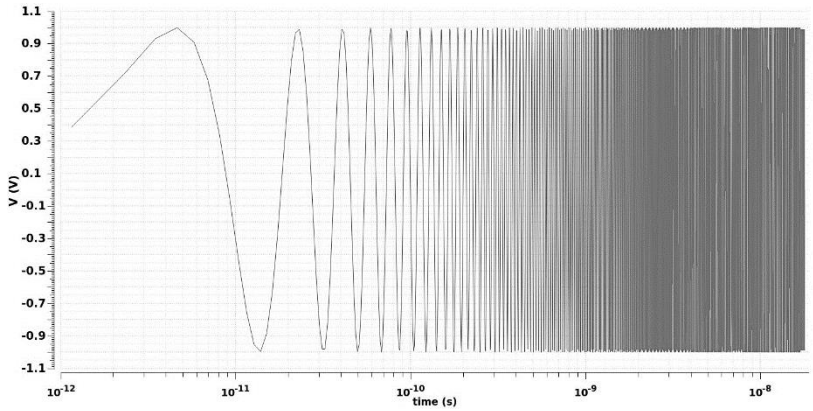


Figure 6.8. The obtained chirp signal

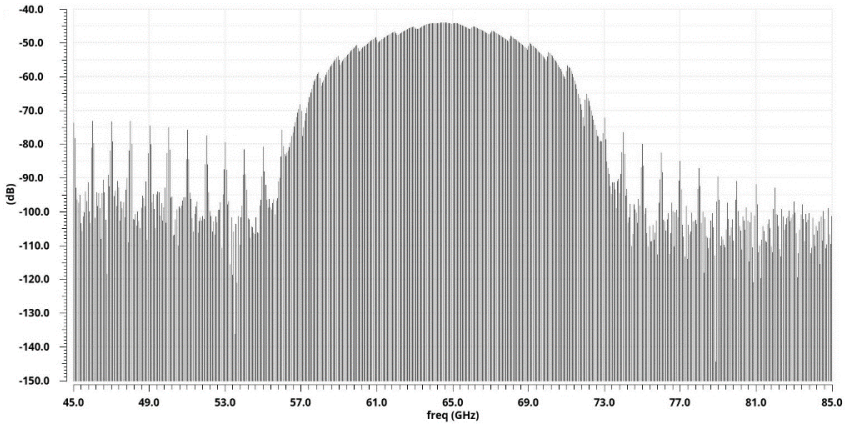


Figure 6.9. The frequency spectrum at the output of LNA for fault free case

For Chirp signal implementation in Cadence Virtuoso different multiplexer blocks form Functional library were used. To obtain chirp signal the frequency range from 55 GHz to 72 GHz is considered and 18 different sinewave sources with 24 mVpp ac magnitude have been used. The ac magnitude is selected to satisfy specific requirements of the components in test measurement setup. The logical implementation of chirp signal generator is shown in Figure 6.7 and Figure 6.8 shows generated chirp signal. The obtained chirp signal represents frequency components from 55 GHz to 72 GHz each for 1 nsec of time period.

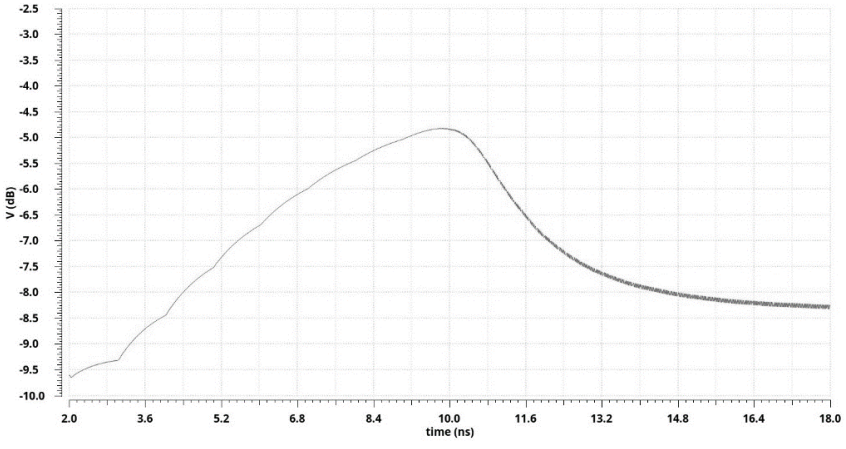


Figure 6.10. The transient signal at the output of ED for fault free case

The test input stimulus of 12 mVp chirp signal with f_{min} of 55 GHz and f_{max} of 72 GHz is applied to the LNA. Thus, in the fault free case, the output of the LNA is a sinusoidal signal of given amplitude that is determined by the performance characteristic of the LNA discussed in Chapter 5: LNA Characterization section 5.1 as it is shown in Figure 6.9 The Discrete Fourier Transform (DFT) has been performed on obtained transient signal to get frequency spectrum of the signal. Simultaneously, the transient output signal at the output of ED is shown in Figure 6.10 for fault free case. Let us consider the faulty cases, wither catastrophic or parametric, which affects the amplitude of LNA output signal due to change in frequency response of the S21 gain of the LNA.

The Figure 6.11 shows faulty signal at the output of ED due to Gate and Source short of M1. The Gate and Source short fault of the transistor effects on Gate to Source capacitance Cgs. The Gate to Source capacitance plays important role in input impedance matching of LNA with source impedance of the antenna typically 50 Ohms. According to matching criteria for input impedance matching,

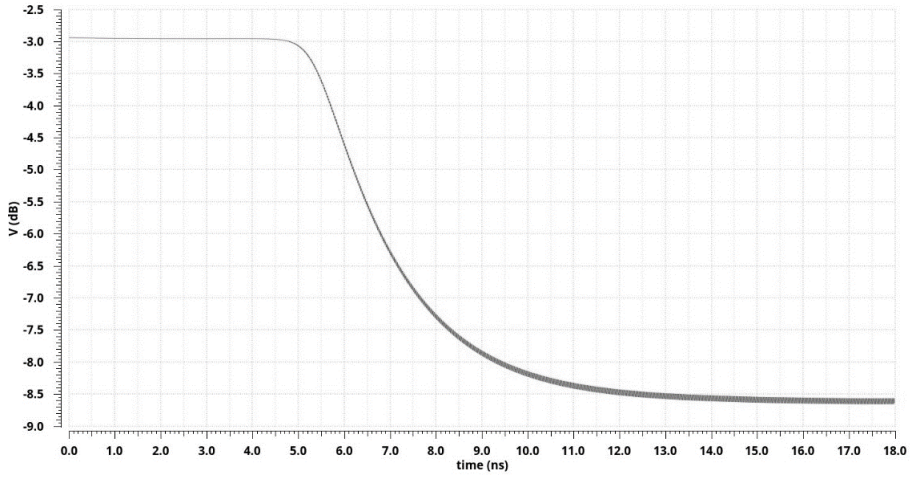


Figure 6.11. The transient signal at the output of ED for faulty case (Gate and Source short for transistor M1)

$$gm\frac{Ls}{Cgs} = Rs \tag{6.3}$$

The impedance mismatch may cause change in frequency response of LNA. The Figure 6.11 shows the affected response at the output of ED. The simulations to perform fault analysis of other components is also performed. The fault modeling and simulation results makes easy to predict fault in the fabricated LNA. The simulated case signals for few other faults are presented below.

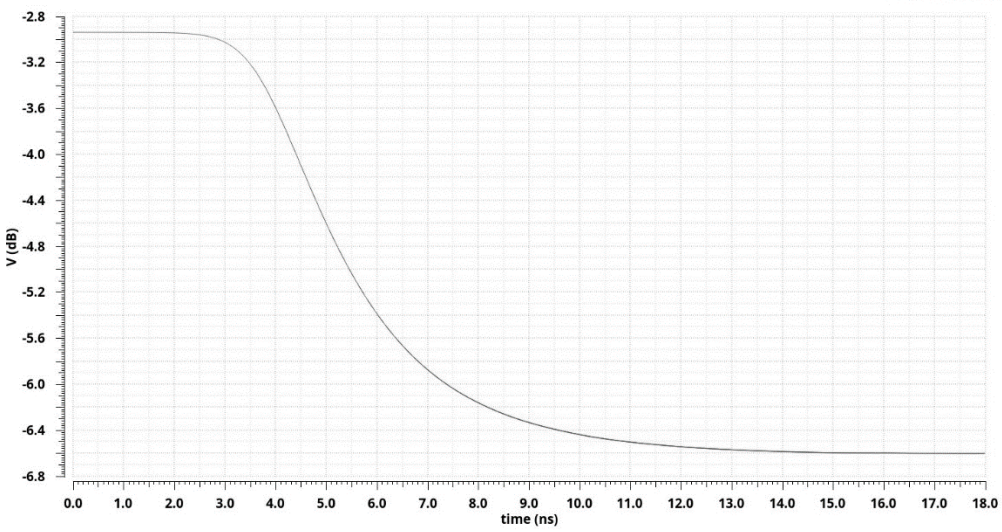


Figure 6.12. The transient signal at the output of ED for faulty case (Drain terminal open for transistor M1)

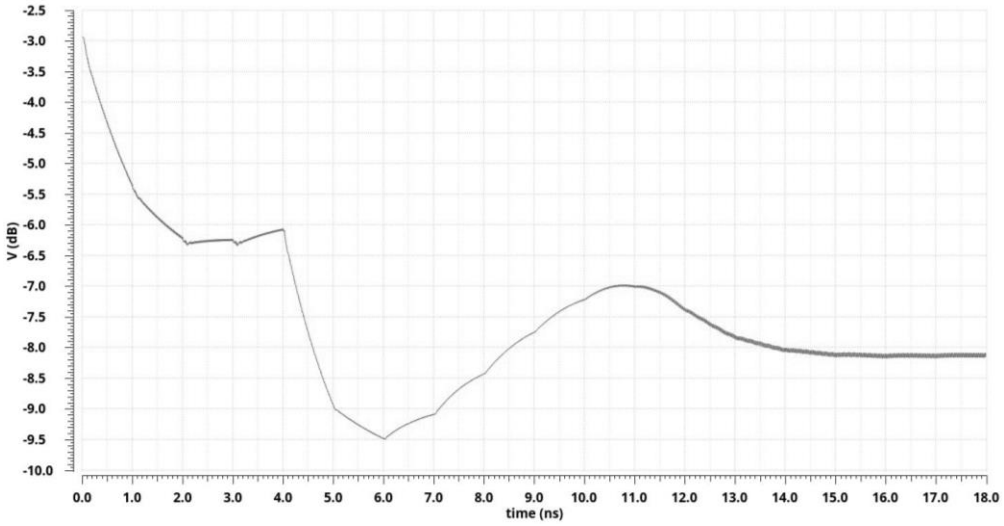


Figure 6.13. The transient signal at the output of ED for faulty case (Source Inductance L_{s1} is open circuit)

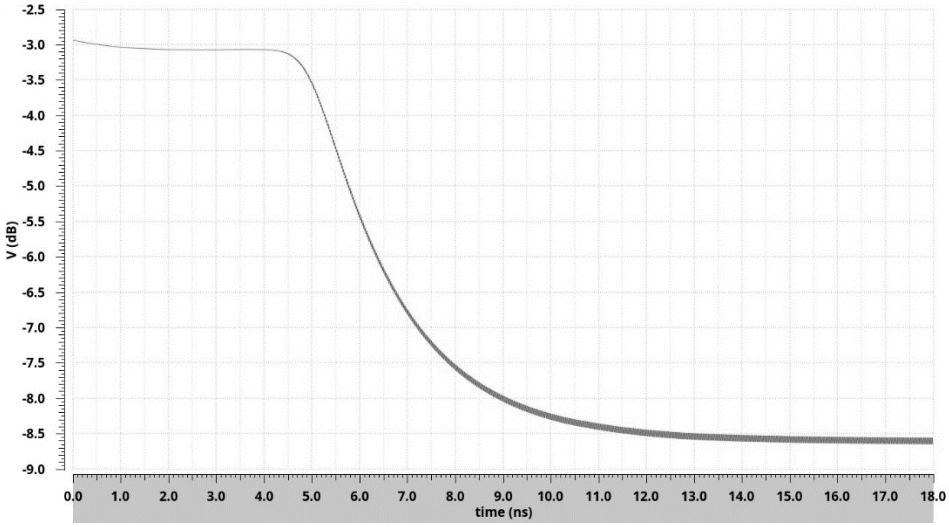


Figure 6.14. The transient signal at the output of ED for faulty case (Source terminal open for M1 transistor)

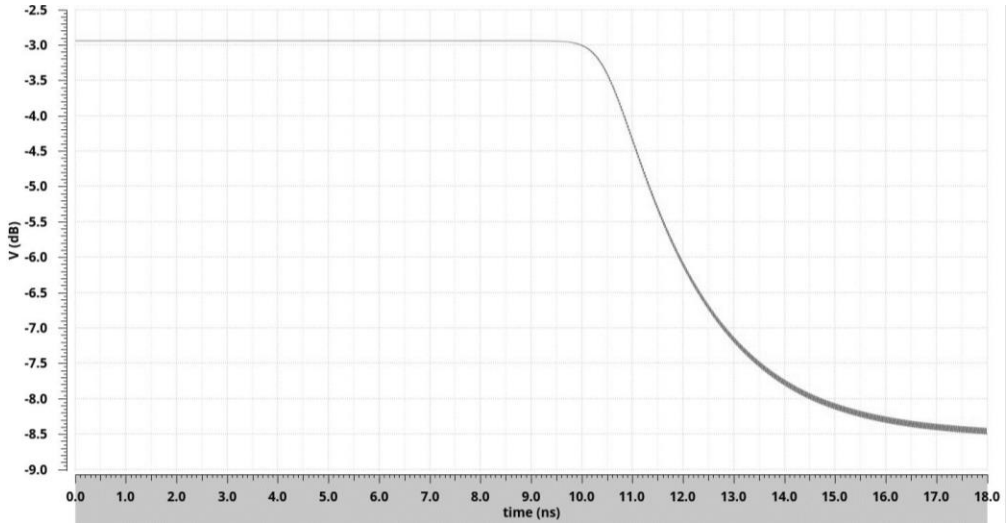


Figure 6.15. The transient signal at the output of ED for faulty case (Primary winding of output transformer is short)

Chapter 7

Conclusion and Future Work

The important takeaways with the thesis, current status of the project and the future work of testing and fabrication is mentioned in this chapter.

The intra and inter-chip communication has certain requirements such as high bandwidth and low power transceiver design to establish energy-efficient data communications within as well as between multiple chips. The main goal of this thesis to design a Low Noise Amplifier (LNA) to enable such high bandwidth and power efficient communication. The two stage common source inductive source degenerated design is implemented and characterized to obtain parameters such as high LNA gain, low Noise Figure, S-parameters and IIP3 linearity measure. To achieve bandwidth requirement of wireless interconnect the bridged shunt-series peaking structure is adopted and bandwidth extension is achieved to support higher data rate of 17Gbps. The frequency and noise analysis is performed and gain of 17.2 dB is obtained at 60 GHz operating frequency at very low noise figure of 2.8 dB. The Harmonic Balance (HB) analysis is performed to obtained linearity (IIP3) of the proposed LNA which is found as -14.38 dBm. The -3 dB bandwidth of 17 GHz is obtained with bandwidth extension technique at the loss of 4.88 mW active power from a 1V supply. This energy –efficient and wideband design makes the low noise amplifier suitable for wireless interconnects and making use of such LNA in wireless interconnects makes it competitive with many emerging and novel intra-chip and inter-chip interconnect technologies.

The thesis also discusses about the design approach to be taken while implementing the high frequency test setup and the different types of faults should be considered while designing fault model. Catastrophic and parametric faults are introduced in the LNA and tested over simulation to obtain faulty responses at the output of envelope detector. This testing methodology makes identification of faulty component or variation in value of specific component on chip easy.

Currently, the characterization of the proposed LNA is carried out over nominal case with the help of 45 nm generic technology node. The schematic needs to be further tested against PVT and the Monte Carlo Corner Cases. Once the results are ready for corner cases, further changes may be need to do in component values to meet the specifications. Once the schematic is finalized according to specification, the components from the Process Design Kit (PDK) provided can be used in the place of 45 nm generic technology node components. Then with the actual extraction of the parasitics simulations can be done for the new schematic modifications can be made to bring the new circuit close to the required specification. Once the schematic meets actual specification at satisfactory level, the physical design of the finalized schematic can be realized. The physical design is significant and critical process at such high frequencies. The parasitics play an important role in physical design process. These parasitics can be extracted from the layout and hence different layout techniques can then be implemented to reduce these parasitics. The different mathematical testing models can be made to predict the response of the circuit over faults with analysis of the circuit models.

Bibliography

[1] Benini, L. and Micheli, G. De, "Networks on chips: a new SoC paradigm," in Computer, vol. 35, no. 1, pp. 70-78, Jan 2002.

[2] International Technology Roadmap for semiconductors (ITRS) 2012 Update. Assembly and Packaging.

[3] X. Wu et al., "UNION: A Unified Inter/Intrachip Optical Network for Chip Multiprocessors," in Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.22, no.5, pp.1082-1095, May 2014.

[4] M.S.Shamim, et al, "A Wireless Interconnection Framework for Seamless Inter and Intra-Chip Communication in Multichip Systems," in IEEE Transactions on Computers, vol. 66, no. 3, pp. 389-402, March 1 2017.

[5] Deb, S., Ganguly, A., Pande, P.P., Belzer, B., and Heo, D., "Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 2, no. 2, pp. 228-239, June 2012.

[6] J. Lin et al.., "Communication Using Antennas Fabricated in Silicon Integrated Circuits," Solid-State Circuits, IEEE Journal of , vol.42, no.8, pp.1678,1687, Aug. 2007.

[7] S. Laha, et al, "A New Frontier in Ultralow Power Wireless Links: Network-on-Chip and Chip-to-Chip Interconnects," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 2, pp. 186-198, Feb. 2015.

[8] X. Yu, H. Rashtian, S. Mirabbasi, P. P. Pande and D. Heo, "An 18.7-Gb/s 60-GHz OOK Demodulator in 65-nm CMOS for Wireless Network-on-Chip," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 3, pp. 799-806, March 2015.

[9] K. Kang et al., "A 60-GHz OOK Receiver With an On-Chip Antenna in 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 9, pp. 1720-1731, Sept. 2010.

[10] E. Cohen, O. Degani, and D. Ritter, “A wideband gain-boosting 8mW LNA with 23dB gain and 4dB NF in 65nm CMOS process for 60 GHz applications,” in Proc. IEEE RFIC 2012, pp. 207-210, June 2012.

[11] H. C. Kuo and H. R. Chuang, "A 60-GHz high-gain, low-power, 3.7-dB noise-figure low-noise amplifier in 90-nm CMOS," 2013 European Microwave Conference, Nuremberg, 2013, pp. 1555-1558.

[12] P. Sakian, E. Janssen, A. H. M. van Roermund, and R. Mahmoudi, “Analysis and Design of a 60 GHz Wideband Voltage-Voltage Transformer Feedback LNA,” IEEE Trans. Microw. Theory Techn., vol. 60, no. 3, pp. 702-713, March 2012.

[13] C. W. Byeon, C. H. Yoon, and C. S. Park, “A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short-range wireless communications,” IEEE Trans. Microw. Theory Tech., vol. 61, no. 9, pp. 3391–3401, Sep. 2013.

[14] S. Shekhar, J. S. Walling and D. J. Allstot, "Bandwidth Extension Techniques for CMOS Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 41, no. 11, pp. 2424-2439, Nov. 2006.

[15] Xinmin Yu, Deukhyoun Heo, Partha Pratim Pande and Shahriar Mirabbasi "A 60-GHz LNA with Feed-Forward Bandwidth Extension Technique for Wireless NoC Application" Proceedings of the 44th European Microwave Conference, 978-2-87487-035-4 © 2014 EuMA.

[16] Pozar, David M. Microwave engineering. John Wiley & Sons, 2009.

[17] B. Razavi, "A Millimeter-Wave CMOS Heterodyne Receiver With On-Chip LO and Divider," in IEEE Journal of Solid-State Circuits, vol. 43, no. 2, pp. 477-485, Feb. 2008.

[18] A. Oncu and M. Fujishima, “49 mW 5 Gbit/s CMOS receiver for 60GHz impulse radio,” Electron. Lett., vol. 45, no. 17, pp. 889–890, Aug. 2009.

[19] S. Deb, K. Chang, X. Yu, S. P. Sah, M. Cosic, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, “Design of an energy-efficient cmos-compatible noc architecture with millimeter-wave wireless interconnects,” IEEE Transactions on Computers, vol. 62, no. 12, pp. 2382–2396, 2013.

[20] V. Vijayakumaran, M. P. Yuvaraj, N. Mansoor, N. Nerurkar, A. Ganguly, and A. Kwasinski, “Cdma enabled wireless network-on-chip,” ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 10, no. 4, p. 28, 2014.

[21] N. Mansoor, P. J. S. Iruthayaraj, and A. Ganguly, “Design methodology for a robust and energy-efficient millimeter-wave wireless network-on-chip,” IEEE Transactions on Multi-Scale Computing Systems, vol. 1, no. 1, pp. 33–45, 2015.

[22] S. Deb, K. Chang, X. Yu, S. P. Sah, M. Cosic, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, “Design of an energy-efficient cmos-compatible noc architecture with millimeter-wave wireless interconnects,” IEEE Transactions on Computers, vol. 62, no. 12, pp. 2382–2396, 2013.

[23] ——, “Design of an energy-efficient cmos-compatible noc architecture with millimeter-wave wireless interconnects,” IEEE Transactions on Computers, vol. 62, no. 12, pp. 2382–2396, Dec 2013.

[24] Friis formulas for noise. (2018, April 03). Retrieved from https://en.wikipedia.org/wiki/Friis_formulas_for_noise

[25] T. Shinde, S. Subhramaniam, P. Deshmukh, M. Ahmed, M. Indovina, and A. Ganguly, “A 0.24pJ/bit, 16Gbps OOK Transmitter Circuit in 45-nm CMOS for Inter and Intra-Chip Wireless Interconnects, ” GLSVLSI '18 Proceedings of the 2018 on Great Lakes Symposium on VLSI, Pages 69-74, ISBN: 978-1-4503-5724-1, May 2018.

[26] C. W. Byeon, C. H. Yoon and C. S. Park. 2013. A 67-mW 10.7-Gb/s 60-GHz OOK CMOS transceiver for short-range wireless communications. IEEE Trans. Microwave Theory Techniques, (September 2013). vol. 61, no. 9, pp. 3391–3401.

[27] X. Yu, et al. 2014. A 1.2-pJ/bit 16-Gb/s 60-GHz OOK Transmitter in 65-nm CMOS for Wireless Network-On-Chip. IEEE Transactions on Microwave Theory and Techniques, (2014). vol. 62, no. 10, pp. 2357-2369.

[28] K. Kawasaki et al. 2010. A millimeter-wave intra-connect solution. IEEE J. SolidState Circuits, (December 2010). vol. 45, no. 12, pp. 2655–2666.

[29] E. Juntunen et al. 2010. A 60-GHz 38-pJ/b 3.5-Gb/s 90 nm CMOS OOK digital radio. IEEE Trans. Microw. Theory Techn., (February 2010). vol. 58, no. 2, pp. 348–355.

[30] S. B. Patil, “An Ultra-Linear LNA for Basestations” MASTER OF SCIENCE THESIS, Delft University of Technology, November 2013.

[31] Sudip Shekhar, Jeffery S. Walling, Sankaran Aniruddhan and David J. Allstot, “CMOS VCO and LNA using tuned-input tuned-output circuits,” IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp.1177- 1186, may 2008.

[32] Thomas H Lee,”The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition”, Cambridge University Press.

[33] Q. Wang and M. Soma, RF front-end system gain and linearity Build-in Test, proceedings of the 24th IEEE VLSI Test Symposium (VTS’06), 2006.

[34] D. Mateo, J. Altet and E. Aldrete-Vidrio, Electrical characterization of analogue and RF integrated circuits by thermal measurements, microelectronics journal, vol.38, pp.151-156, 2007.

[35] J. Youl Ryu, and B.C. Kimb, Low-cost test technique using a new RF BIST circuit for 4.5-5.5 GHz low noise amplifiers, Microelectronics Journal, Vol.36, pp.770-777, 2005.

[36] S. Subhramaniam, T. Shinde, P. Deshmukh, M. Ahmed, M. Indovina, and A. Ganguly, “A 0.36pJ/bit, 17Gbps OOK receiver in 45-nm CMOS for inter and intra-chip wireless interconnects, ” 30th IEEE International System-on-Chip Conference (SOCC), DOI: 10.1109/SOCC.2017.8225977, September 2017.

[37] A. Mishra, M. Soma, “A Time-Domain Method for Pseudo-Spectral Characterization” VLSI Test Symposium, 2008. VTS 2008. 26th IEEE.