nMOS STANDARD CELL LIBRARY

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ABSTRACT

A set of standard nMOS cells was designed following the MOSIS lambda-based design rules, with a lambda of 2.0 microns. The nMOS process was modeled using SUPREM II, and each of the cells was simulated in SPICE. The cells, an inverter, two, three, and four input NANDs and NORs, NAND and NOR RS flip-flops, a 2-bit Multiplexer, and a 2-bit Demultiplexer/Decoder, were designed with ICE, an in house CAD tool.

INTRODUCTION

The fabrication of pMOS devices dominated the 1960's, due to the simplicity of processing, and the fact that the MOS non-idealities did not severely impact their operation. However, pMOS has the inconvenience of negative source voltages and slow operation. In the 1970's nMOS became the dominant process due to it's positive source voltages and it's ability to output voltages, with depletion loaded inverter stages, equal to the supply voltage. nMOS devices are also faster, because of the higher mobility of electrons versus holes. The drawback for nMOS devices comes in its fabrication sequence. In order to counteract the non-idealities of MOS devices, we need to use ion implantation to adjust the substrate threshold voltage. For the same purpose, polysilicon gates were used, since they have a reduced workfunction difference. Furthermore, implants are needed for an n-type channel if we are to build depletion mode devices.

The design process for any circuit will be very slow if it is started at the transistor level, as it would require optimizations in the gate sizes and transistor gains. If a set of pre-designed, optimized, and operational standard logic cells is created, the design could be done at the logic gate level, much more easily and quickly. The purpose of this project is to provide designers with such a library of working standard cells for faster design of circuits in nMOS.

The operation of nMOS devices with depletion loads is as follows. Take, for example the most basic cell, the Inverter, seen in figure 1. The Driver, or pull-down transistor, is an enhancement mode device with a threshold voltage of at least one volt. The load transistor is a Depletion mode device, and has a threshold voltage of less than zero.

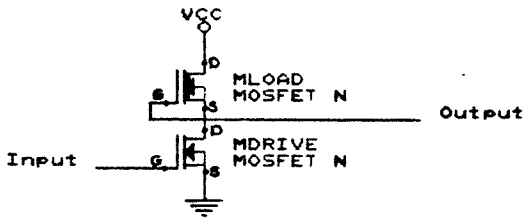

Figure 1. The Inverter.

Since the load's gate is connected to a voltage that is at least ground, it will always be turned on. When the voltage on the driver's gate is high (positive voltage for nMOS) the driver transistor will be turned on, and the output will be driven to ground, or pulled down. Inversely, when the input voltage is low, the driver transistor will be turned off, cutting off the current through it, and causing the output voltage to be driven up to the supply voltage, since the load transistor is always on. Summarizing, the output voltage will always be driven towards the inverse of the input voltage, from this the name Inverter. If more than one driver gate was connected in series, they would all have to be turned on in order for the output voltage to be low, thus making a NAND gate. If the drivers were connected in parallel, we will have made a NOR gate. By connecting these gates together it will be possible to make more intricate gates and circuits.

This project was concerned mainly with the full characterization of the standard cell library. Each different area of the devices will be simulated, namely: the Enhancement and Depletion gate areas, the Source and Drain areas, and the field areas. The gate area simulations will yield the MOS threshold voltage for each device for a given number of surface states, and the gate oxide thickness. The Source and Drain simulations will output the sheet resistance of such areas, and their junction depth. The field areas are also important, since SUPREM will calculate their threshold voltage, to check for possible parasitic type transistors. This will dictate the appropriate Threshold adjustment implant at the beginning of the process. The calculation of the appropriate implant dose is described in Appendix 1.

CELL DESIGN

The cells are all to be designed following the self-aligned nMOS process, and the inverter stages must have enhancement mode drivers, and depletion mode loads. This configuration requires ion implantation over depletion mode gates, polysilicon gates, and the use of buried contacts at the source of the load devices. The necessary ion implantation, and CVD polysilicon process steps have recently been made available at RIT, making it possible to design integrated circuits using this technology. The process can be modeled using the simulation software package SUPREM II, which will yield oxide thicknesses, impurity concentration profiles, and will also compute threshold voltages for a given

number of surface states. Enhancement mode devices require a threshold voltage of about 1.0 volt, and depletion mode devices are preferred to have about -4.0 volts for threshold. These thresholds can be obtained from the SUPREM simulation of the gate areas of the devices. Refer to Appendix 2 for the nMOS process description in the SUPREM simulations.

The MOSIS lambda-based design rules were followed for the layout of the cells in the in house CAD tool ICE (Integrated Circuit Editor). All cells are 150 microns high, and the width is in increments of 12 microns. As an example, the Inverter cell is shown in Figure 2. Supply voltage and ground lines run at the top and bottom of each cell, and all inputs and outputs to and from the cell were placed at the top and bottom, in polysilicon.

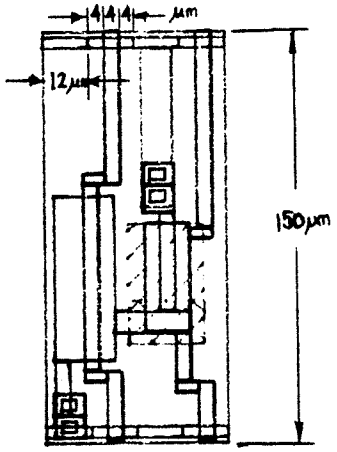

Figure 2. The Inverter cell layout.

The design was done in a six layer process: Diffusion, Implant, Buried Contact, Poly, Contact cuts, and Metal. In order to fabricate the devices a mask set for each level can be obtained from the ICE designs.

Each cell will be electrically simulated using SPICE. SPICE has the advantage of being able to simulate devices following very specific electrical parameters. These parameters form the nMOSFET model card in SPICE, and can be calculated from the SUPREM output values for oxide thickness and sheet resistance, among others. Figure 3 illustrates the role each parameter plays in the nMOSFET electrical model.

Some model parameters can be calculated, but others will have to be given assumed values. This is necessary since they are only extractable from test results on fabricated devices, and this type of process has not been completed at RIT. In the SPICE simulation we will also have to choose the appropriate gate sizes for the desired gate gains. This gain was chosen to be 10.0 at first, but it was found from SPICE that a gain of 7.0 would give much better output characteristics. A gain of at least 5 will be satisfactory for our purposes, should the finished devices not function properly and yield a gain lower than desired. Note that

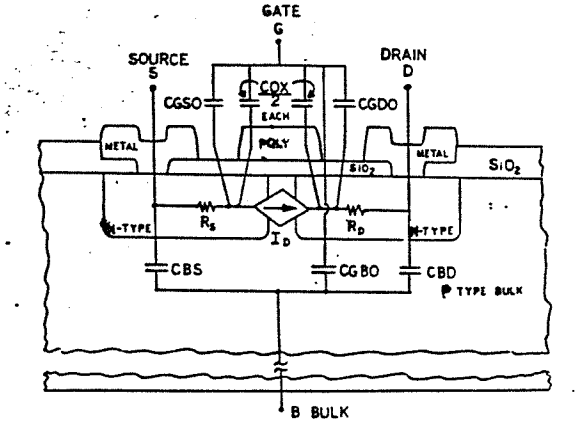

Figure 3. The nMOSFET model parameters.

the gain selection was done at the layout level, since it was then when the gate sizes were decided upon. If the SPICE simulation was not satisfactory, design changes were done on the layout.

The parameters extracted directly from the SUPREM output are RSH (source and drain sheet resistance), VTO (zero bias threshold voltage), TOX (gate oxide thickness), NSUB (substrate doping), TPG (type of gate material, which is polysilicon), and XJ (junction depths). Other calculated SPICE nMOSFET model parameters are the Junction capacitance, CJ, and the Gate to Source and Drain overlap capacitances, CGSO and CGDO. Also, the bulk capacitances of the Source and Drain, CBS and CBD, and the Source and Drain series resistance, RS and RD. Other parameters such as NSS (number of surface states), and LAMBDA (channel length modulation) were given assumed values.

Upon completion of the fabrication and test of the devices, the assumed values entered into the SPICE nMOSFET model can be amended. From the process results we can also obtain more accurate values for the SUPREM parameters (TOX, RSH, etc). More accurate nMOSFET parameters will yield a more reliable and realistic simulation, and will help in determining if any further design adjustments should be made.

RESULTS/DISCUSSION

The calculated nMOSFET model parameters that were used are shown on Table 1.

The optimum sizes were researched in order to achieve the desired gain of 10.0. Gate sizes of (l/w, in microns) 4.0/60.0 for the driver, and 28.0/4.0 for the load transistors were attempted, and the results were dissappointing. The simulated hold, propagation, and fall times were in the picosecond rage, while the rise time was of about 1.4 nanoseconds. Note that all the values obtained from fabricated devices are not likely to be as good as the simulated ones. The high gain was supposed to make up for any problems and malfunctions due to processing.

However, it was found that a gain of seven yielded much better results in terms of pull up times, and output voltages reached, with gate sizes 4.0/60.0 for the driver and 16.0/4.0 for the load.

Parameter	Enhancement	Depletion
LEVEL	1	1
VTO	1.52 v	-4.19 v
NSUB	5.0 E14	5.0 E14
TOX	601 Angs	601 Angs
TPG	1.0 (n+)	1.0 (n+)
XJ	2.41 microns	2.41 microns
LAMBDA	0.01	0.01
RD	100 ohms	100 ohms
RS	100 ohms	100 ohms
CJ	2.59 nF	2.59 nF
CGSO	13.8 pF	13.8 pF
CGDO	13.8 pF	13.8 pF

Table 1. nMOSFET model parameters.

The cells designed are an Inverter, two, three, and four input NAND gates, two three, and four input NOR gates, a Multiplexer, a Demultiplexer/ Decoder, a NAND RS flip flop, a NOR RS flip flop, and an XOR gate. Each cell, as it appears in the library, comprehends an electrical circuit layout, a plot of the ICE layout, the logical truth table, and a SPICE deck that characterizes it.

CONCLUSIONS

There now exists at RIT the possibility to design in nMOS at the logic level, using a set of standard cells. Future designers at RIT will be able to call these cells from within ICE, and build circuits, simply by connecting the cells to one another. It is then possible to produce designs at the logic gate level, not having to worry about the gate's electrical behavior.

ACKNOWLEDGEMENTS

I would like to thank Robert Pearson for his extensive help in the parameter calculation techniques, that helped develop this library.

REFERENCES

[1] James C. Taylor, pMOS Standard Cell Library, (Provided by R. Pearson).

[2] SPICE Simulation of PMOS Digital Structures. (Provided by R. Pearson).