FABRICATION OF A SINGLE LEVEL METAL CCD SHIFT REGISTER

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ABSTRACT

Using a "shadow mask" technique, a single level metal 3-phase CCD shift register was fabricated with electrode separations of 2.5 microns. Testing is pending at this time.

INTRODUCTION

A Charge Coupled Device, or CCD, is essentially a linear array of closely spaced MOS capacitors. Major applications of CCD's have been in the fields of photo-sensor arrays, signal processing components such as variable delay lines, transversal filters and also in the area of large storage memory [1].

A three phase CCD shift register can be fabricated by terminating the array of capacitors with a diode at each end (to inject minority carriers), and connecting every third gate to a common conductor. A cross section of such a three phase CCD shift register is shown in Figure 1.

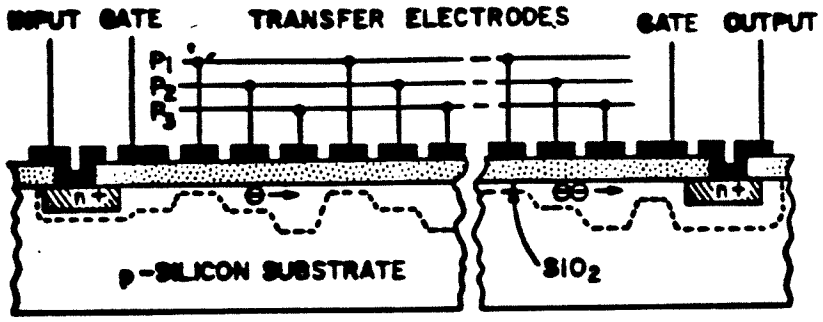


Figure 1: Cross section of three phase CCD shift register[2].

Consider such a device fabricated on a P-type silicon substrate. When a large positive voltage is applied to the first electrode in the array, a depletion region is formed in the underlying silicon, temporarily creating a potential well for electrons, as shown in Figure 2a. Electrons injected from the input diode accumulate in the potential well formed under the electrode. If a positive voltage is then simultaneously applied to an adjacent electrode, the potential wells will overlap and any charge stored under the first electrode will then be shared with the second electrode, as shown in figure 2b (hence the name

"charge coupled"). It then follows that when the bias is removed from the first electrode, the charge is transferred completely to the second, as shown in Figures 2c and 2d. A similar transfer process moves the packet of charge under the third electrode. When the electrodes are pulsed with overlapping clock pulses, as shown in Figure 2e, a moving array of potential wells is established. In this fashion, packets of electrons supplied from the input diode are shifted sequentially through the device, to be detected at the output diode. A CCD is a dynamic device, in which charge may be stored for times shorter than the thermal relaxation time of the capacitors. This time varies from one second to several minutes, depending on the processing [3].

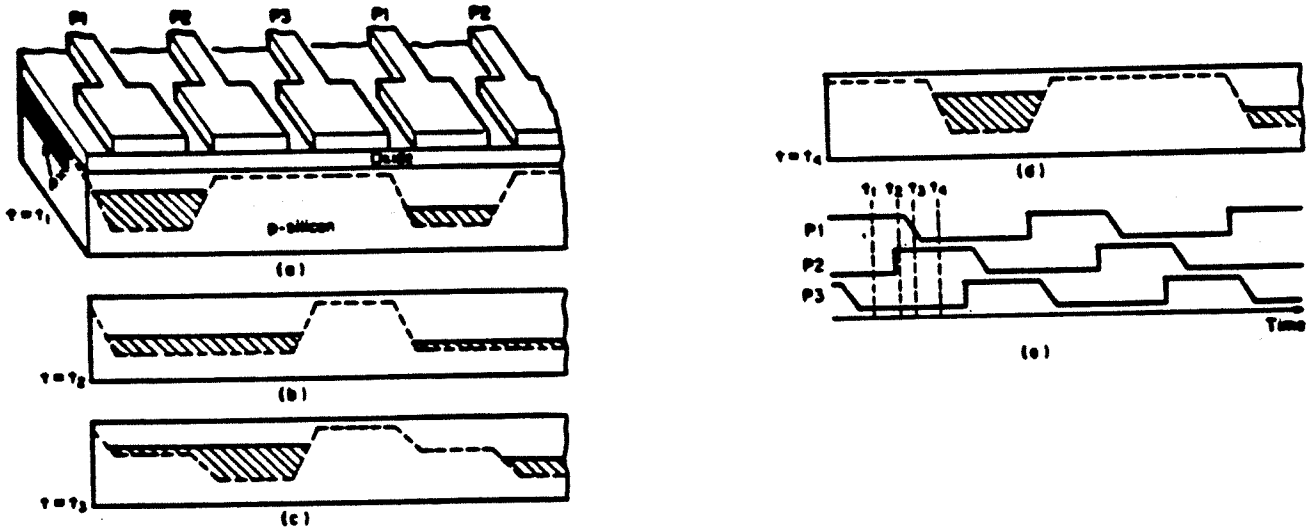
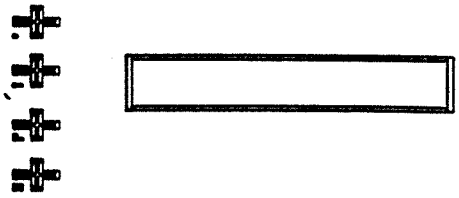


Figure 2: Operation of three-phase CCD[2].

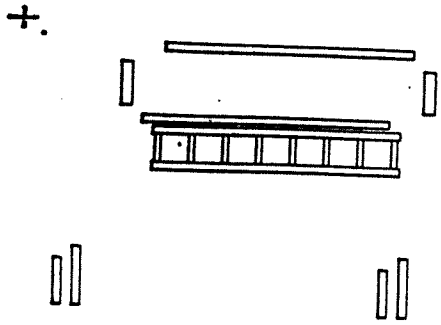
Critical to the operation of the device is spacing the transfer electrodes close enough so that their depletion regions overlap. If they do not overlap no charge-coupling takes place and the device fails. The fraction of charge transferred from one well to the next is defined as the charge-transfer efficiency. Factors which affect the charge-transfer efficiency include incomplete charge transfer, surface states, leakage currents and charge loss. Charge transfer efficiency is the most important performance parameter because it defines how many transfers can be made before the input signal seriously distorts and/or becomes delayed [4]. For transfer efficiencies compatible with today's technology this spacing must be less than three microns [4].

EXPERIMENT

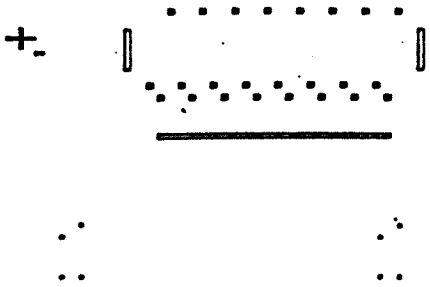
The device fabricated was a three phase CCD, and therefore has 24 transfer electrodes, plus 4 electrodes for input/output. The transfer electrodes are 250 by 40 microns and are contacted through diffused buses. A P-type substrate was chosen for two reasons. First, in a P-type substrate the minority carriers are



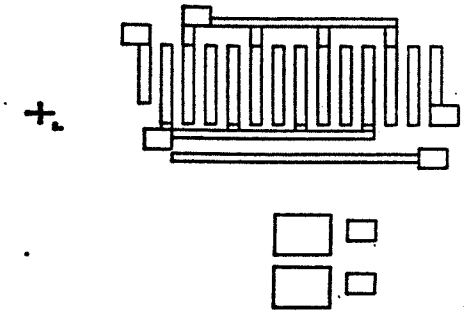
LEVEL 1: P-type channel stop



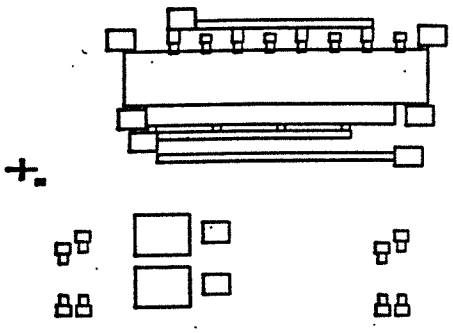
LEVEL 2: Diode and clock bus
N Diffusion



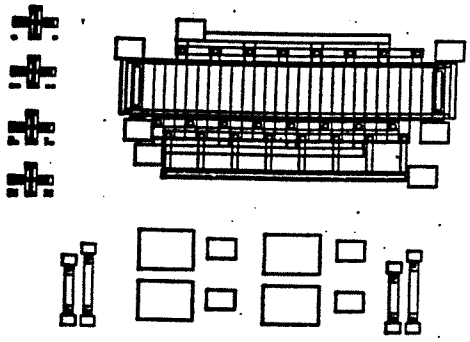
LEVEL 3: Contact cuts



LEVEL 4: Every other electrode
Metal 1



LEVEL 5: Remaining device features
Metal 2



An overlay of all levels

Figure 3: Masking levels for a single level metal CCD.

are electrons, which have a higher mobility than holes and should therefore result in a higher charge-transfer efficiencies. Second, for a silicon dioxide insulator on a P-type substrate the fixed charge held near the surface is positive and the silicon at the interface is held in depletion even at zero volts bias, again improving the efficiency of the device. The transfer channel was surrounded by a P-type channel-stop diffusion. The resulting high majority carrier concentration prevents the formation of a depletion region of a significant width, creating a surface potential wall around the transfer channel. This serves to laterally confine the direction of charge transfer, and electrically isolate the device.

The masking levels for this project are shown in Figure 3. Fabrication started with the growth of a masking oxide for the ring diffusion. This oxide is 5500 angstroms thick and was grown on P<100> 5-8 ohm-cm substrate in wet 02 for one hour. Windows were opened and a boron diffusion was done to define this channel stop. The masking oxide was then stripped and regrown to approximately 5000 angstroms, windows were opened and the input/output diodes were defined along with the clock buses for each phase. A phosphorus diffusion was used to define these regions. The masking oxide was then stripped and the gate oxide was then grown. This oxide was 800 angstroms thick and grown in dry 02 with TCA, contacts to the diffusions were cut through this oxide. The wafer will then be coated with a thick layer of aluminum, and using the shadow mask technique, the electrode structure will be fabricated.

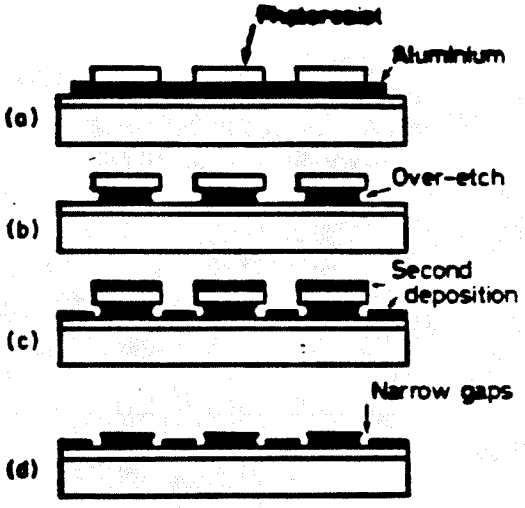


Figure 4: Technique for sub-micron electrode spacing[4].

Figure 4 is a illustration of the "shadow mask" technique that was employed to obtain electrode spacings necessary for the proper operation of the CCD. The process was developed by Browne and Perkins [3,4]. This technique involves defining every other electrode in the array with photoresist on a thick layer of aluminum. The metal is then etched to clear, and then carefully overetched, producing an overhung structure. A second thinner layer of metal is then deposited over the entire wafer. By

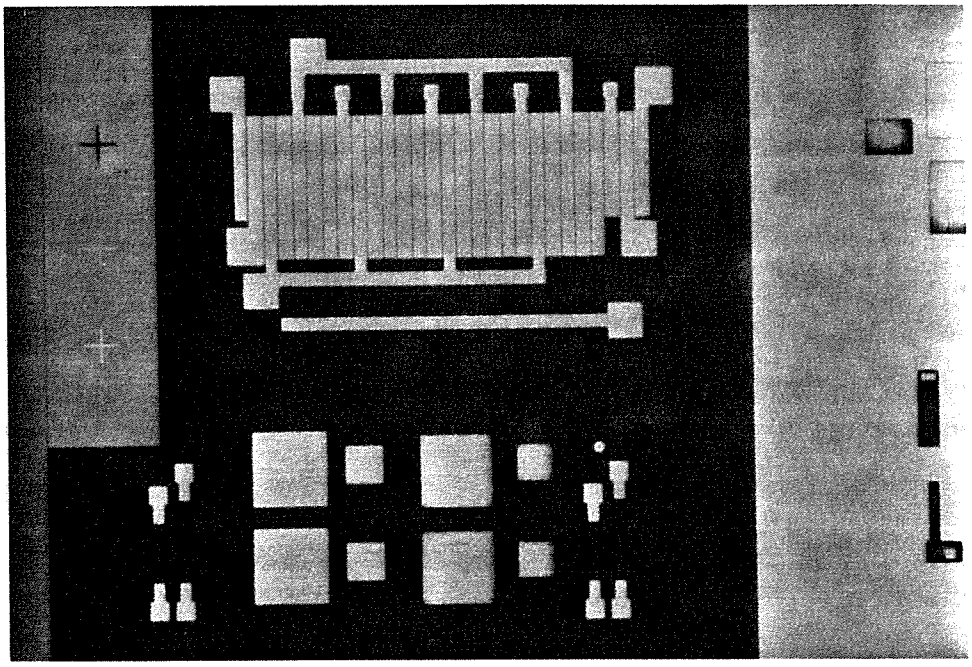


Figure 5a: Picture of completed device.

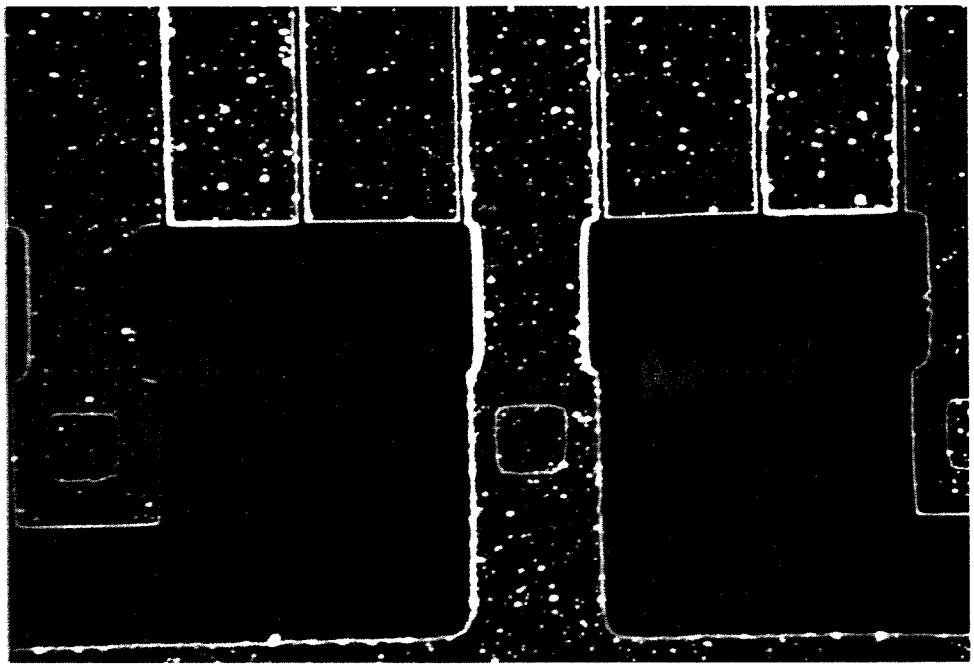


Figure 5b: Close up of electrodes using dark field illumination. Spacing is 2.5 microns.

virtue of the overhang, solvent can access the photoresist and lift off the unwanted metal over the resist in an ultrasonic acetone soak. The remaining device features are defined in a subsequent photoresist application. The result was a linear array of electrodes, with the separations between them determined by the degree of overetch. Using this technique it was possible to fabricate single level metal structures with spacings as close as one half of a micron. This lower limit is imposed to allow for possible lateral surface migration of aluminum during the second metal deposition, which could short the device.

RESULTS/DISCUSSION

Figure 5a shows an optical micrograph of the completed device. Figure 5b shows a close view of the electrode structure using dark field illumination. Using the "shadow mask" technique, electrode separations of two and a half microns were obtained for a one minute time to clear and two minute overetch. The yield for this step was very high. Subsequent attempt may obtain closer spacing using shorter overetch time.

Future attempts at this project would require that some modifications be made to the layout. Changes include removing the input/output electrodes which allow the packets to be written into and read out of the array. These electrodes complicate testing and do not affect device performance. For easier testing of the devices the pad layout should be modified so the probe card can be used instead of attempting to place multiple probes.

Figure 6 shows my suggestion for the testing circuitry. Without the input/output electrodes testing is made easier. D Flip-flops can be used in conjunction with a function generator to develop the necessary three-phase overlapping clock and one other function generator would be necessary to inject the pulse into the array. An oscilloscope can be used to monitor the output as well as the clocking circuitry.

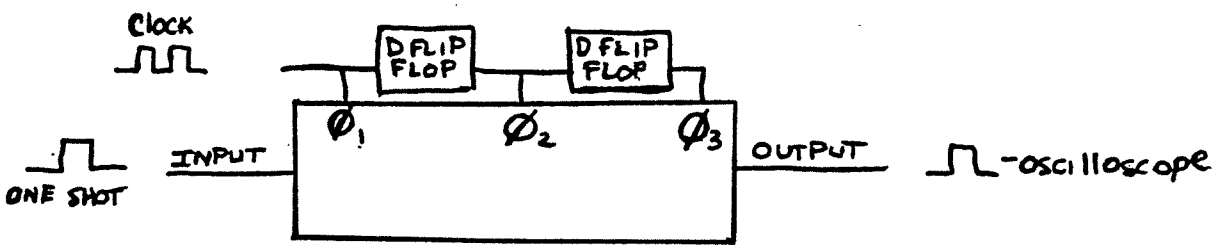


Figure 6: Testing circuitry for three phase CCD.

CONCLUSION

An 8-bit three phase single level CCD shift register with 2.5 micron separation between electrode was successfully fabricated using the "shadow mask" technique.

ACKNOWLEDGEMENTS

I would like to acknowledge Scott Blondell for his assistance with equipment difficulties, Mike Jackson for obtaining supplies and Rob Pearson for his redesign which may benefit future attempts at this project.

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