CHARACTERIZATION OF INTEGRATED INJECTION LOGIC

Tu T. Phan
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

Integrated Injection Logic gates (IIL) were fabricated at RIT by the use of a double diffused, four mask process. The IIL devices contained neither a buried contact nor an epitaxial layer. The propagation delay time of invertor gates was measured at different injection current levels.

INTRODUCTION

Integrated Injection Logic (IIL) was invented in 1972. It is the most recent logic system to be introduced to commercial applications, and is used in electronic watches and timers, microprocessors, and Analog/Digital and Digital/Analog converters. Finally, large-scale integrated circuits using IIL can be built over the full military temperature range and exibit good radiation resistance characteristics.

IIL represents an innovation in bipolar integrated circuits that achieves superior advantage in packing density and power-delay product, as compared with the transistor-transistor logic (TTL). First,the IIL gates can be packed with a density between 120 to 200 gates per square millimeter which is almost ten times higher than of TTL gates packing density. Second,the speed-power product of IIL is in the range of 0.1 pJ to 0.7 pJ, where the speed-power product of TTL is typically 100 pJ. In addition, the design of IIL eliminates the current sources and the load resistors of TTL which occupy much of the real estate on the chip.

Integrated Injection Logic (IIL) is an extension of bipolar technology into LSI by new circuit design technique. Figure 1 shows a cross-sectional profile and a schematic of an IIL cell. The basic IIL cell consists of a lateral pnp transistor (Q2) and a vertical npn transistor (Q1) with multiple collectors (C1, C2). The emitter of Q1 and the base of Q2 are grounded. The collector of Q2 is connected to the base of Q1 which is the input B.

The basic IIL cell of Figure 1 is also an invertor gate whose input is B and outputs are C1 and C2. When the input B at logic low (0 V) the outputs C1 and C2 will be at logic high which depend on the external supplied voltage. If the input B changes from logic low to logic high (.7 V), the injection current will flow into the base of Q1. Thus Q1 is saturated and the outputs C1 and C2 will change from logic high to low which is the Vce of Q1 at saturation. Inversely, when the input B goes from high to low, the outputs C1 and C2 will change from low to high.

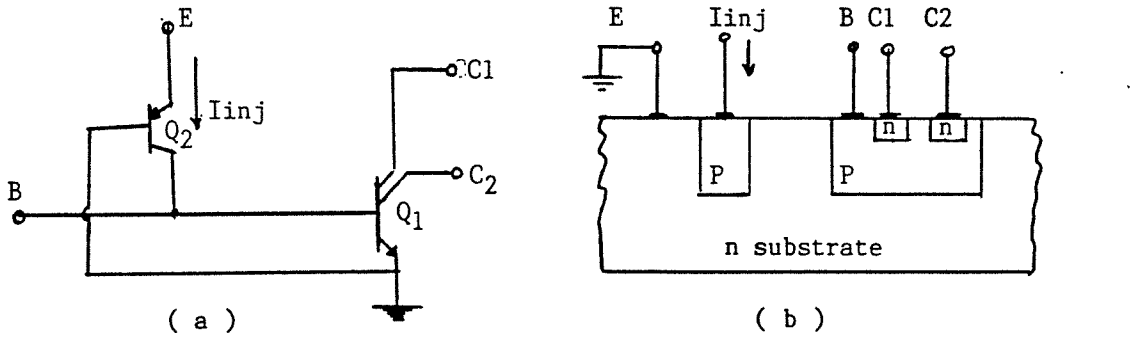

Figure 1: A basic IIL cell: schematic (a), and cross-sectional profile (b).

Delay time is the time needed for an output to response an input signal such as from high to low or vice versa. Figure 2 describes the delay time from high to low and from low to high respectively. In an IIL circuit, the delay time is inversely proportional to the injection current, Icc, as expleined below.

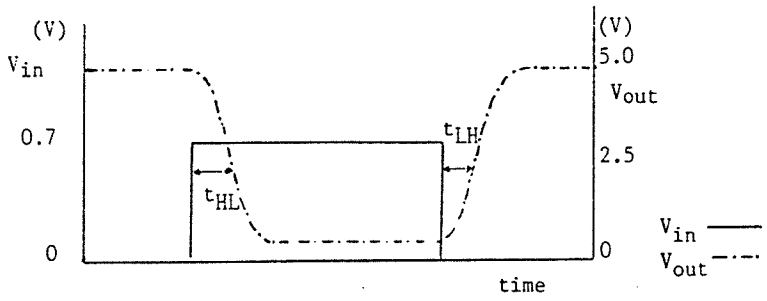

Figure 2: Delay time from high to low and low to high

At low injection current level, the propagation delay time of an IIL gate is the time required to charge junction and parasitic capacitors of Q1. Since the injection current Icc will distribute the charge to these conducting capacitors, the propagation delay time is inversely proportional to the number of these capacitors.

At medium injection current level, the propagation delay time is the time needed to establish or remove excess minority carriers in the baseof Q1. This charge is proportional to the transistor current available to remove it, and hence the delay

time is independent of the injection current.

Finally, at high injection current level, the propagation delay time will increase with the increase of injection current because the npn transistor is driven into saturation in which the stored base charge increases more than in proportion to transistor current. Figure 3 displays the normalized propagation delay time versus injection current [1].

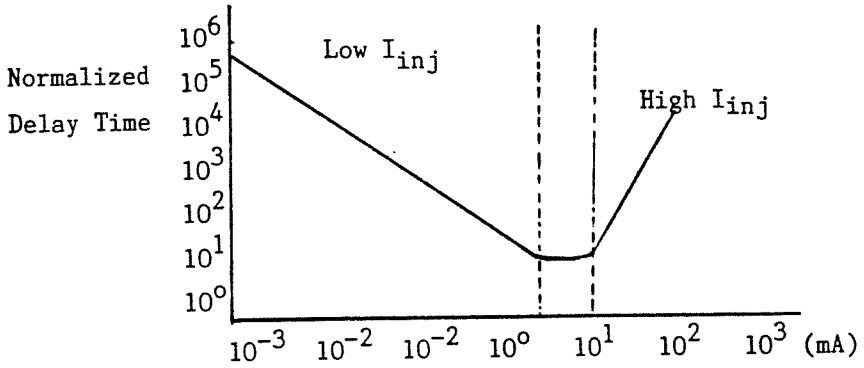

Figure 3: Normalized propagation delay time VS injection current.

EXPERIMENT

This project was to measure the propagation delay time of IIL invertor logic gates which were designed and fabricated in the class EMCR-650. The HP4145 was used to check the performance of all individual transistors of the circuit to be tested prior to take the measurement of the propagation delay time. The program BETA of HP4145 was used to measure the gains and obtain the plots of Ic versus Vce of npn (Q1) and pnp (Q2) transistors. In this program, the emitter of Q1 and base of Q2 were conneceted to ground, and the base of Q1 was the input which was connected to the collector of Q2. The input signal was a square-wave whose amplitude and period were 0.7 V and 50 nano-seconds respectively. The external connections for the input, output and injection current are shown in Figure 4. The delay time was measured on an oscilloscope.

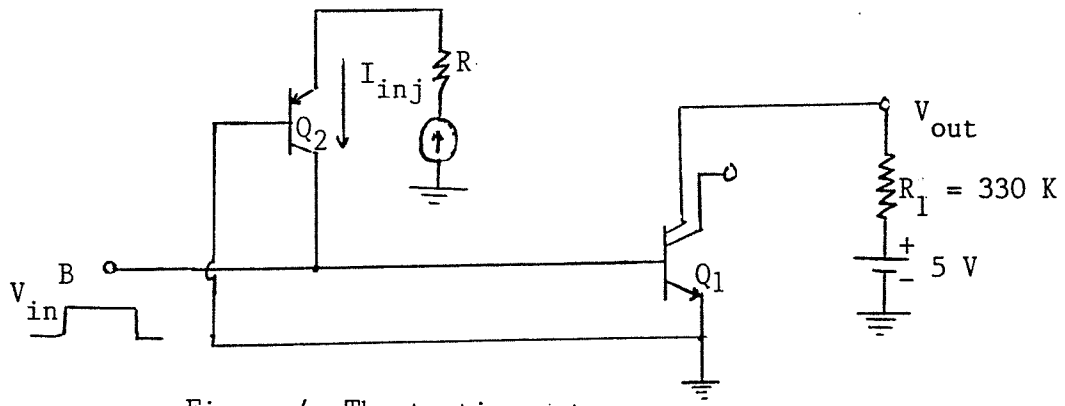

Figure 4: The testing set up

RESULTS AND ANALYSIS

The output voltage at C1 was measured to be 3.0 V when the input was high. This voltage was expected to be lower than 1.0 V. The 2.0 V higher than the expected value was caused by the large internal emitter resistant. When the input was low, the output did not go higher than 3.5 V. This is the problem of large leakage current Iceo. The circuits behaved like a voltage divider between R1 and the internal emitter resistor. Individual transistors Q1 and Q2 were then tested to check its performance. None of transistors worked properly. The npn transistor did not work with the collector is heavily doped. When the polarities of emitter and collector were interchanged, the Q1 showed a large leakage current Iceo (see the attached plots). In addition, the Vce was always low with all level of input voltage B which means the npn transistor suffered a large leakage current and large internal emitter resistance. The pnp lateral transistor had a long base width of 10 um which caused all minority carriers to be recombined within the base; therefore, the current gain Beta was significantly small. The propagation delay time coud not be measured because the logic gates did not function properly.

CONCLUSION

The IIL logic gates of this project could not work because of the reasons described above. To improve the performance of an IIL circuits the design should include the following: First, a short base width for the lateral transistor (less than 2 um)to increase the current gain Beta. Second, the emitter contact of the npn transistor (ground) should be doped and located slose to the main devices in order to reduce the internal emitter resistance. Third, a burried contact should be included in the design to promote the current gain of npn transistor.

ACKNOWLEDGMENTS

Mr. R. Pearson for lending the wafers of EMCR-650 class.
Dr. R. Turkman for the instruction of circuits testing.

REFERENCES

[1] Herbert Taub, Donald Schilling. Digital Integrated Electronics. New York: McGraw-Hill Book Company, 1983, chapter 4.