DESIGN OF A EEPROM CELL AND THIN OXIDE EVALUATION

Kenneth Obuszewski
Fifth Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

An electrically erasable programmable read only memory (EEPROM) device, utilizing a double polysilicon structure was designed. An extremely thin gate oxide (100) was required to allow for Fowler-Nordheim tunneling. Thin oxide polysilicon gate capacitors were fabricated, and evidence of tunneling was existent. However, the oxide integrity was generally poor, and processing did not proceed past this point.

INTRODUCTION

A EEPROM is a non-volatile memory; therefore, memory contents are retained when power to the chip is off. It possesses the capability of programming or erasing memory contents in a matter of milliseconds. Successful fabrication may allow the device to be programmed and erased up to 100,000 times. The outstanding feature of the EEPROM is that it is erased electrically, unlike an EPROM. An EPROM must be erased with ultraviolet light for up to 30 minutes. Consequently, while an EPROM must be removed from its setup to be erased, a EEPROM may be programmed and erased entirely by software. The major drawback of a EEPROM is that it is very difficult to fabricate successfully.

Both an EPROM and a EEPROM require two polysilicon gates. The difference is that a EEPROM utilizes a very thin first gate oxide which allows current to flow between the gate and the drain under proper bias. This current flow is termed Fowler-Nordheim tunneling. Subsequently, this oxide is termed the tunnel oxide, and it is responsible for the ability of the EEPROM to erase electrically.

A typical EEPROM is shown in Figure 1. The first gate, called the floating gate, can be charged and discharged depending on whether the cell is being programmed or erased. The tunnel oxide must be very thin, probably no more than 130 Angstroms. The thinner the oxide, the more current that will tunnel at a lower voltage. The second polysilicon layer is used to form the control and select gates. A normal gate oxide thickness is required, as the select gate is a standard NMOS transistor. Thus, EEPROM processing is similar to standard NMOS processing with the exception of the extra gate.

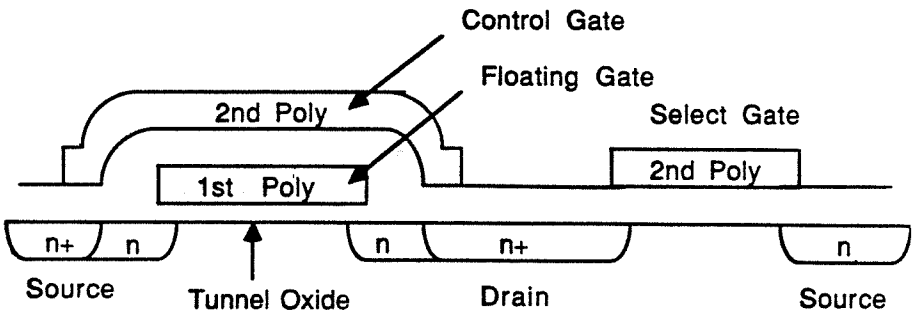
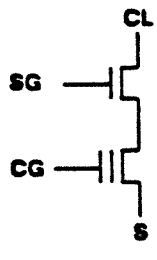


Figure 1: Typical EEPROM cross-section.

A EEPROM cell is programmed by grounding the control gate and applying 20 volts to the select gate. This causes electrons to tunnel from the floating gate to the drain region overlapped by the floating gate. This leaves the floating gate at a more positive charge. In order to erase the device, 20 volts is applied to both the control and select gates, while each source is grounded. Electrons from the source, drain and channel regions subsequently charge the floating gate to a more negative potential [2]. The state of the cell can read using the select gate in a current sensing mode [2]. The control gate is grounded and 5 volts placed on the select gate during this operation. Figure 2 show the operating modes of the cell.



	SG	CL	CG	S
ERASE	20	0	20	0
PROGRAM	20	20	0	5
READ	5	1	0	0
UNSELECTED	0	X	0	0

FIGURE 2 OPERATING MODES OF MEMORY CELL

Figure 2: EEPROM schematic and voltage levels [2].

Perhaps the most vital part of EEPROM processing is the thin oxide growth. Very high integrity thin oxides are difficult to produce. The oxide cycle must be carefully developed through extensive characterizations. The tunnel oxide utilized in a EEPROM must be of higher quality than a standard gate oxide, since it must withstand voltages near or at the breakdown voltage. Care must be taken in further processing to prevent damage to the thin oxide. This includes high temperatures and exposure to plasma.

EXPERIMENT

The basic process steps to be followed in the EEPROM process are:
1) Threshold adjust implant
2) Grow and pattern field oxide
3) Grow tunnel oxide
4) Deposit first poly and pattern
5) Implant poly and source/drain regions
6) Grow interlevel oxide
7) Deposit second poly and pattern
8) Implant second poly and source/drain regions
9) Grow contact cut oxide and pattern
10) Deposit metal, pattern, and sinter

Since SUPREM II does not model polysilicon, simulations were not very useful.

Several single bit EEPROM cells were designed on an in-house CAD tool. Seven masking layers were required to achieve the desired process. Gate lengths and widths were varied to achieve a range of values for the voltage dropped across the tunnel oxide. Standard NMOS transistors were also laid out, for first and second poly transistors. Gate lengths of 6, 10, and 50 microns were utilized. Six microns is near the minimum gate length at RIT, and 10 microns is standard. The 50 micron device will allow effective channel length to be calculated. Subsequently gate underlap of the source and drain could be determined. This is a very important parameter in EEPROM fabrication. The greater the underlap, the more of the gate oxide that is tunneled through. This reduces the current density and charge trapping. A field transistor is included to calculate the field threshold value. This is a concern since 20 volts will be passing across the field. Poly resistors and capacitors are also included to evaluate poly sheet resistance and oxide integrity. Figure 3 shows the chip layout.

Initially, a complete EEPROM cell was to be fabricated. However, after mask generation and initial processing, it was determined that time would not permit processing to be completed. Instead, a thin oxide capacitor was evaluated. A threshold adjust implant of boron was performed. The energy and dose were chosen because of previous results in NMOS pojects at RIT. An oxide of approximately 4000 Angstroms was grown and subsequently etched away. The temperature served to activate the implant and the oxide served as a sacrificial gate for the thin oxide growth.

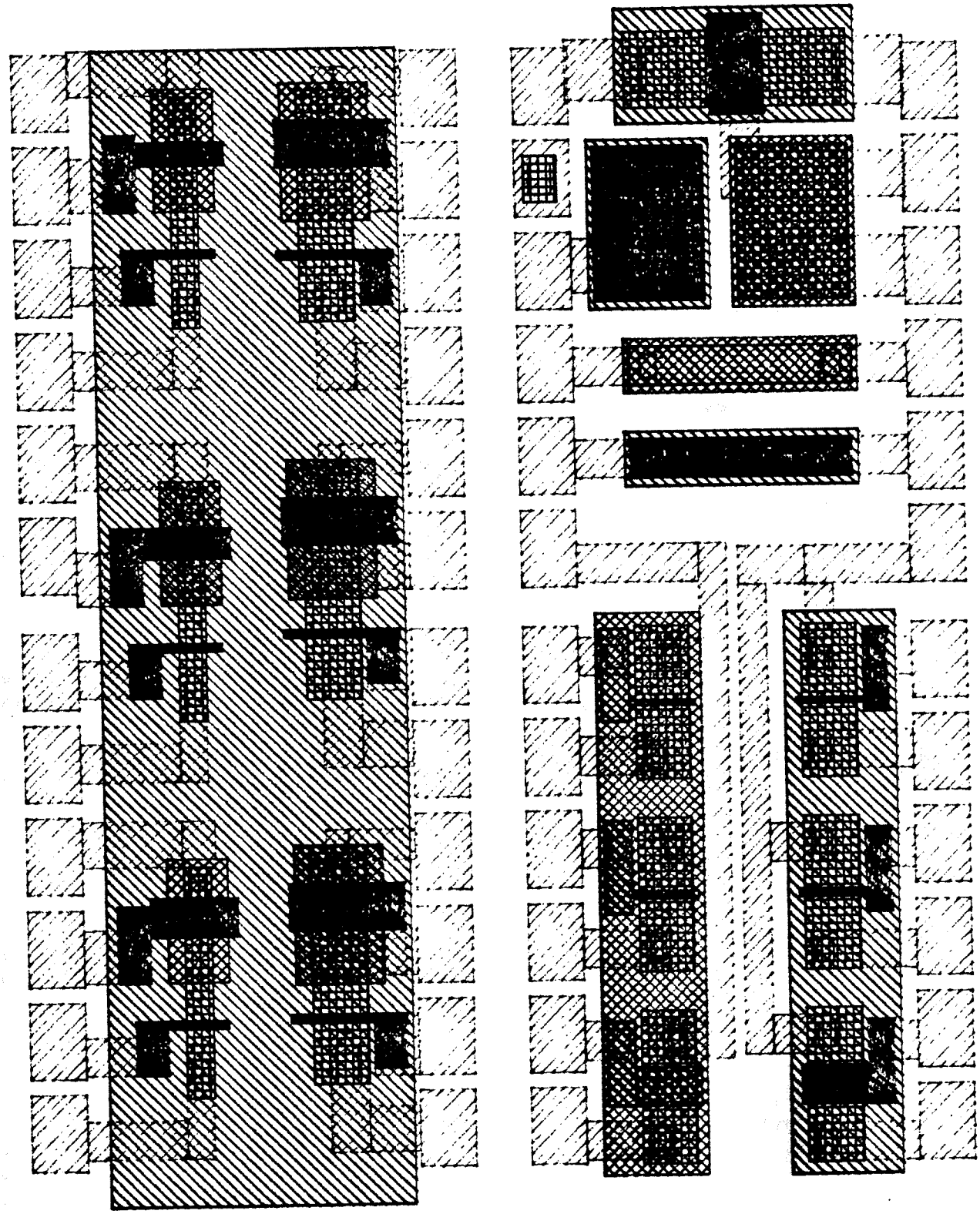


Figure 3: Cell layout.

Tests were performed to determine the proper time for an oxide thickness of close to 100 Angstroms. Ten minutes in a dry oxygen ambient at 900 C was sufficient. The wafers were pushed in at 700 C in a nitrogen atmosphere to prevent initial oxide growth. After stabilization at 900 C, oxygen and TCA were turned on for 5 minutes. The temperature was ramped to 1050 C in nitrogen and annealed for 15 minutes. This was to help remove interface trap sites. The temperature was then ramped back down to 900 C, and the oxygen and TCA turned on for another 5 minutes. The TCA helps to reduce oxide defects, fixed charge, and mobile ionic charge. One last anneal at 900 C in nitrogen and pull out at 700 C finished the cycle.

The wafers were immediately transferred to the polysilcon furnace for deposition, since exposure to the air greatly damages a thin oxide. After deposition, the poly was implanted with phosphorous. An implant was chosen rather than a diffusion since the implant depth can be controlled. Phosphorous entering the oxide would affect the integrity. An anneal at 900 C in nitrogen was utilized to activate the implant. A low temperature was used since high temperatures are detrimental to a thin oxide. The poly was wet etched and the resist stripped with acetone in order to avoid a plasma. Plasma also damages thin oxide integrity.

RESULTS

Ellipsometry measurements of test wafers showed a thickness of between 80 and 150 Angstroms. However, the accuracy of the ellipsometer comes into question. By ramping the gate voltage and plotting versus the current between gate and substrate showed leakage in the nanoamp range until between 7 and 12 volts. At this time tunneling seemed to be apparent. This is a reasonable voltage for a 100 Angstrom oxide since oxides should breakdown at 10 Mv/cm2, which would be 10 volts for 100 Angstroms.

After further investigation the oxide appeared to be of poor quality. After being exposed to 100 microamps of current, the capacitor starts tunneling at a lower voltage. This agrees with literature; however, at times the difference in voltage was as much as 5 volts. This suggests that the oxide is becoming porous and is of poor quality. It almost behaves as a diode formed by a n-type poly layer and a p-type substrate. Figure 3 shows a typical curve generated by the 4145 Analyzer. Curve A was ramped until the current through the oxide reached 10 microamps. Curve B was allowed to reach 100 microamps. The differe nce in tunneling voltages can be clearly seen.

Capacitance-voltage analysis was attempted. Results were very inconclusive. Most capacitors had high frequnecy C-V curves that looked as if they were low frequency curves. This might lead one to believe that excess minority carriers were present in the substrate. Perhaps this could have been prevented by guard banding, which consists of a heavy implant surrounding the capacitor. It is also possible that phosphorous channeled through grain boundaries in the poly and into the thin oxide.

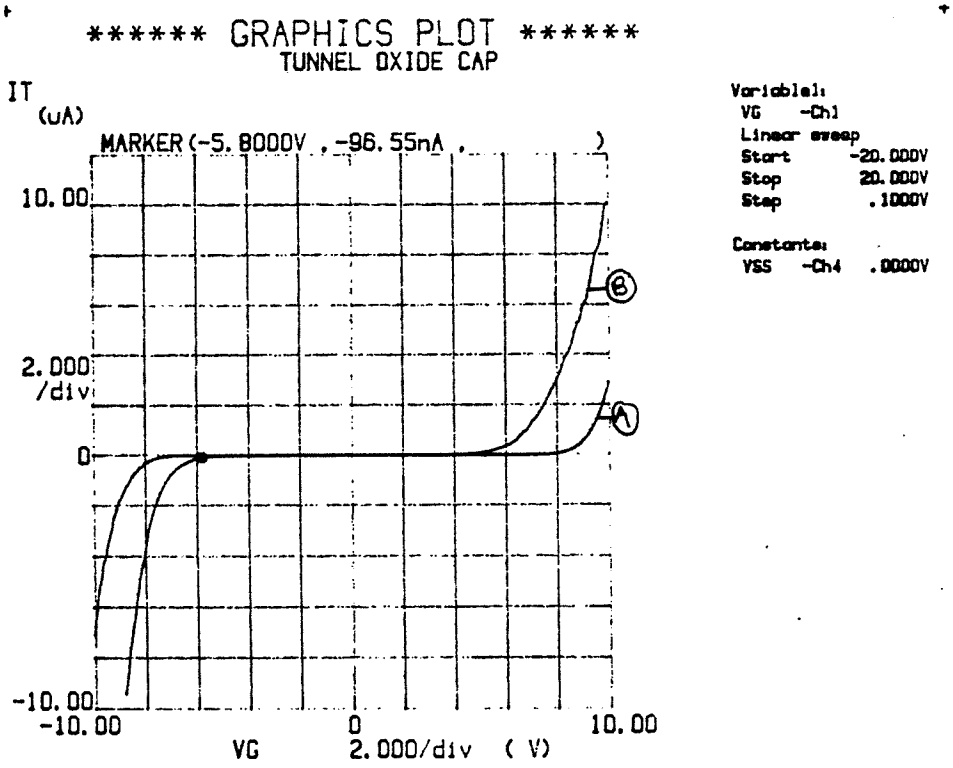


Figure 4: I-V Curve of a thin oxide capacitor.

SUMMARY

Fowler-Nordheim tunneling appears to be achievable with thin oxides at RIT. Unfortunately, further testing could not be performed to confim Fowler-Nordheim tunneling. Nonetheless, oxide integrity needs to be improved. The poor quality thin oxide may be attributable to several factors. The oxide cycle may not yield a high quality oxide. Pinholes may be present in the oxide. Problems may exist with the silicon-silicon dioxide interface or the polysilicon-silicon dioxide interface. It is likely that the gate oxide and/or polysilicon furnace(s) may not be capable of producing high quality oxides. A further investigation into thin oxide growth is certainly warranted. With smaller geometries in RIT's future, thinner gate oxides will need to follow.

ACKNOWLEDGEMENTS

Richard Lane for a poly run, Frank Schmitt and Scott Blondell for implants, and Alex Pepe and Mark Chonko of Motorola, Inc. in Austin, Texas for technical advice.

REFERENCES

[1] Wolters, D.R., and Peek, H.L. "Fowler-Nordheim Tunneling in Implanted MOS Devices." Solid State Electronics. Vol. 30, No. 8, 1987, pp.835-839.

[2] Yeargain, John R., and Kuo, Clinton. "A High Density Floating- Gate EEPROM Cell." IEEE. 1981, pp. 24-27.