CONSTRUCTION OF A QUASI-STATIC C-V TEST STATION

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ABSTRACT

The construction of a Quasi-Static C-V measurement tool and proper operation are presented. Gate oxides were analyzed for ion implanted regions. Guidelines for obtaining higher quality Quasi-Static C-V measurements will be presented.

INTRODUCTION

The physical and electrical properties of the metal-oxide-semiconductor (MOS) capacitor are the cornerstone to building, developing, and monitoring a MOS process. New processes such as plasma etching, rapid thermal processing (RTP), and e-beam lithography are placing increased concerns on the quality of gate oxides. The MOS capacitor is widely used to evaluate gate oxides because it has a simple structure and can be easily fabricated. Quasi-Static C-V curves of the MOS capacitor can be used to determine such properties as:

1. Oxide Thickness
2. Charges in the Oxide
3. Work Function Differences
4. Interface Trap Densities
5. Properties of Electron and Hole traps

Of these parameters the Quasi-Static C-V curves are used primarily for measuring interface trap densities and the distribution of these traps across the bandgap.

Quasi-Static (Q-S) C-V curves can be obtained by several methods. One common method is to use an extremely low frequency signal and monitor the change in current as a function of voltage variations. Typical frequencies range on the order of 10hz and below, due to the long minority carrier lifetimes in device quality silicon. An alternative method involves ramping an applied voltage slowly and monitoring the displacement current in the MOS capacitor. This technique (developed by M. Kuhn [1]) enables MOS capacitors with long minority carrier lifetimes to be evaluated.

A low frequency curve is similar to a high frequency (1Mhz) C-V curve until the onset of inversion in the MOS capacitor. Figure 1 shows the difference between a high frequency and low frequency curve. In a high frequency C-V curve the minority

carriers are unable to respond to the changes in the AC signal thus the depletion region edge expands and contracts. In a Q-S C-V curve the minority carriers are able to respond to the variations in the applied voltage. Therefore the capacitance rises back up to the oxide capacitance after strong inversion of the surface of the semiconductor has taken place. If the applied voltage is varied to quickly a C-V curve which lies between the true low frequency and high frequency curves will be the result, because not all of the minority carriers are in equilibrium.

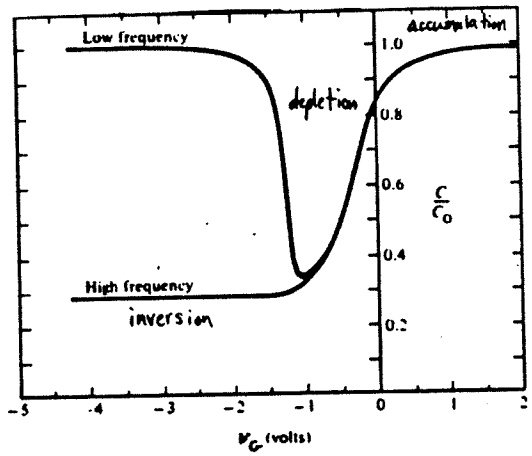

Figure 1: Ideal High Frequency and Low Frequency Curves

Concentrating on the displacement current technique, the measured current (I) in the MOS capacitor is proportional to the voltage ramp rate (dV/dt).

$$I = \text{Capacitance}/(dV/dt)$$

An electrometer must be used to measure the displacement current due to the extremely small currents associated with lower voltage ramp rates. Currents on the order of several picoamps are typical for low voltage ramp rates of 3 to 5mv/sec. A properly designed and shielded probe station is essential to generating accurate high frequency C-V curves but is necessitated for a Quasi-Static test station. A Faraday cage is required to shield the device under test (DUT) from external fields. The Faraday cage must enclose the DUT entirely, shield the MOS capacitor from light, and must be electrically conductive. Light must be shielded from the device to prevent the generation of minority carriers under the capacitor.

Ground loops must be avoided in the design of the test station. The electrometer is accurate enough to measure currents flowing in such loops. Ground loops can be avoided by having one central test station ground and connecting all other grounds directly to the test station ground only once. The shielded cables used for all conductors in the current path were tied directly to ground also.

While Quasi-Static C-V measurement techniques are susceptible to parasitic resistances and capacitances shielded cables are appropriate. Care should be taken in choosing the coaxial cables. A total resistance from the core to the shield should be greater than 1e12 ohms over the entire path of the circuit. The coaxial cable should be anchored to prevent movement. When coaxial cable vibrates the shield can generate triboelectric currents this can be avoided by using cable in which the shield is lubricated with graphite [2]. Cable lengths should be minimized to prevent parasitic impedances from affecting the Quasi-Static C-V measurement. Any cable only acts to degrade the signal no matter how long or short.

The drawbacks to the Quasi-Static C-V technique are the non-idealities associated with the resultant curve. A higher current than theoretically expected is often observed with slower voltage ramp rates. This is due to parasitic capacitances in the measurement tool. One will also note that the curve may be slightly tilted. This is due to parasitic resistances in the measurement tool. This can be minimized by using a higher rate of change in the applied voltage. The measured curve can be the additive result of the real low frequency curve, an offset current due to parasitic capacitances, and a slight tilt due to the parasitic resistances. The following equation describes the capacitance at any point on the Q-S C-V curve.

$$C = [I - (Va/Rp)]/(dV/dt) - Cp$$

This equation takes into account the offset due to the parasitic capacitances (Cp), and the tilt due to the current drawn by parasitic resistances, Va/Rp, where Va is the applied voltage.

EXPERIMENT

The voltage ramp circuit shown below was used to generate the applied voltage. This circuit was built to provide a linear voltage ramp rate which would remain constant regardless of the magnitude or polarity of the output voltage.

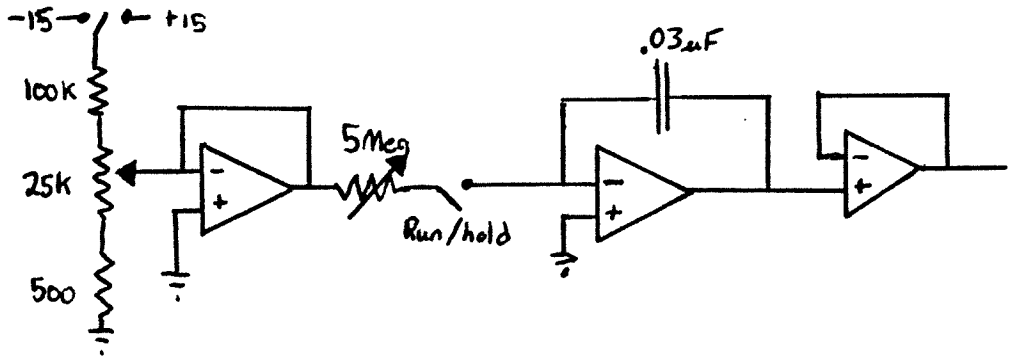

Figure 2: Voltage Ramp Circuit Schematic

The circuit has several additional features to aid in the characterization of MOS capacitors or in the trouble shooting of

the test equipment. The voltage ramp rate can be varied by both a fine and course controls. This allows faster voltage ramp rates to be used when measuring devices with shorter minority carrier lifetimes. The voltage can be ramped in both directions between +16 volts and -16 volts. This allows one to plot the Q-S C-V curve in both the positive and negative directions which aids when adjusting the measurements for parasitic impedances. The voltage ramp can be stopped at any time. This can be a useful feature in ionic contamination studies or in oxide charging experiments. The output of this circuit was buffered to help isolate the circuit from noise which might be picked up on the output cables. The circuit is battery powered to provide a noiseless DC voltage, and eliminate any AC signals from within the box. An external DC power supply was not used because the input leads would be susceptible to noise from the environment and ripple voltage on the DC level.

RESULTS/DISCUSSION

The circuit which was designed to generate the voltage ramp was found to be controllable and extremely immune to noise. The parasitic shunt resistance was determined to be on the order of 1e12 ohms. This was not significant until the voltage ramp was decreased below 10mV/sec. The voltage ramp rate was linear through zero and did not vary by more than 5 percent across the desired range. The ramp voltage hold switch did not function to the desired standards. When the hold function was initiated the voltage would decrease in magnitude at approximately 1mV/sec. This is believed to be due to leakage in the integrator capacitors.

Several Q-S C-V curves have been generated with different ramp rates. Shown below are two Q-S C-V curves, one ideal curve and one measured curve. Notice that the measured curve is tilted slightly in the parasitic resistance example.

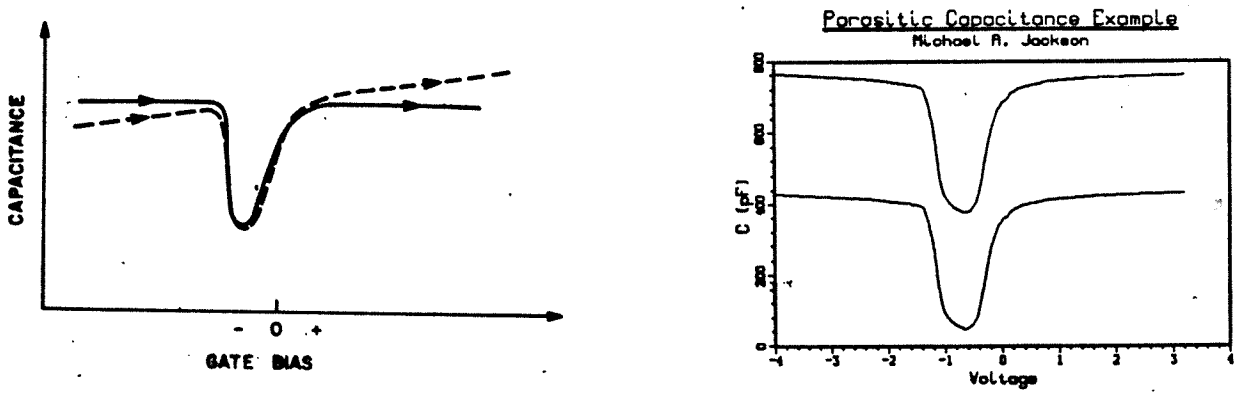

Figure 3: Parasitic Impedance Effects on Q-S C-V Curves [3]

It was found that if the circuit was allowed to stabilized at the starting voltage for about one minute prior to the measurement a more accurate curve could be generated. Also notice the current offset in the measured curve from the theoretical Q-S C-V curve. This is due to parasitic capacitances in the current loop. The integrator operational amplifier was changed from a 741 op-amp to a FET input op-amp. This was found to decrease the amount of change in the applied voltage when the hold function was initiated.

CONCLUSIONS

This project has shown that low frequency C-V measurements can be made using a Quasi-Static technique. The attention to detail when designing the Faraday cage was demonstrated by the test stations excellent immunity to external noise. The non-idealities associated with the Quasi-Static C-V measurement technique were not apparent until the lowest voltage ramp rates were used. The electrometer also proved to be an accurate instrument when measuring currents in the 1pA to 50pA range. In the future a short triaxial cable leading to the electrometer may even increase the immunity to external noise.

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