THE CHARACTERIZATION OF AN ALL ENHANCEMENT PMOS OP-AMP

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ABSTRACT

In present day electronic systems a basic building block is the operational amplifier. Therefore, a better understanding of characteristics of Op-Amps and their importance to overall circuit operation is essential. In the electronics industry manufacturers supply data sheets for the IC's they produce. These data sheets provide a wealth of information: absolute maximum ratings, intended applications, electrical characteristics, performance limitations, equivalent circuits of devices, and more. These defined parameters make the design of more complex systems a much easier task. As do manufacturers in the industry so too must RIT characterize their devices. This project will characterize the important parameters of an All Enhancement Pmos Op-Amp designed and fabricated using RIT's standard 10 micron design rules and pmos metal gate process. More specifically, the parameters characterized will be the input offset voltage, output offset voltage, input voltage range, output voltage swing, supply voltage rejection ratio, large signal voltage gain, common mode gain, common mode rejection ratio, power consumption, and slew rate. These parameters will be defined, measured, and compared to a SPICE simulation for the given Op-Amp.

INTRODUCTION

It is known that the Op-Amp can be used as an inverting, non-inverting, or differential amplifier, and that the negative feedback can be used to stabilize the voltage gain and increase the bandwidth of the Op-Amp circuit. It is also known that when treated as an ideal device it provides characteristics such as high input impedance, low output impedance, high voltage gain, and broader bandwidth, if the appropriate external components are used. These ideal characteristics, although very desirable, are not fully present in practical Op-Amp circuits. The nonidealities that are present are due to the limitations and imperfections involved in fabricating these devices. These imperfections, of course must be characterized along with the various parameters of an Op-Amp.

THEORY

Even though all the components are integrated on the same chip, it is not possible to have two transistors in the input differential amplifier stage with exactly the same characteristics. This mismatching between the two input terminals causes an output offset voltage. The output offset voltage Voo is a d.c. voltage, and it may be positive or negative in polarity depending on whether the potential difference between two input terminals is positive or negative. This voltage is measured at the output when no external inputs are applied.

The input offset voltage Vio is the differential input voltage that exists between input terminals of an Op-Amp without external inputs applied. In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero. The polarity of Vio depends on the mismatching at the inputs. A typical value of Vio for the 741C Op-Amp is 6mv d.c.. The smaller the value of Vio, the better the input terminals are matched.

When the same voltage is applied to both input terminals, the voltage is called a common-mode voltage Vcm and the Op-Amp is said to be operating in the common-mode configuration. For the 741C the range of the input common mode voltage is +/- 13v maximum. This means that the common-mode voltage applied to both input terminals can be as high as +13v or as low as -13v without disturbing proper functioning of the Op-Amp. In other words, the input voltage range is the range of common-mode voltages over which the offset specifications apply. As shown in figure 3 the common mode configuration is generally used only for test purposes to determine the degree of matching between the inverting and non-inverting input terminals.

Because ideally an Op-Amp amplifies only differential input voltages, no common mode output voltage Vocm should appear at the output. However, due to imperfections within an actual Op-Amp, some common-mode voltage Vocm will appear at the output. The amplitude of this Vocm is very small and often insignificant compared to Vcm. Therefore, in practice the ratio of the output common-mode voltage Vocm to the input common-mode voltage Vcm, which is called the common-mode voltage gain Acm, is generally much smaller than 1. In equation form,

$$Acm = Vocm / Vcm$$

Ideally, the common-mode voltage gain Acm is zero.

Acm can be calculated for a given Op-Amp by applying a known value of common-mode input voltage Vcm and measuring the resultant output common-mode voltage Vocm. Op-Amp manufacturers usually list a common-mode rejection ratio CMRR. Generally, it can be defined as the ratio of the differential gain Ad to the common-mode gain Acm,

$$CMRR = Ad / Acm$$

The CMRR can also be expressed as the ratio of the change in input offset voltage to the total change in common-mode voltage.

$$CMRR = Vio / Vcm$$

Generally, the CMRR value is very large and is therefore usually specified in decibels (dB), where

$$CMRR\ (dB) = 20 \log (Ad / Acm)$$

or,

$$CMRR\ (dB) = 20 \log (Vio / Vcm)$$

CMRR is a measure of the degree of matching between two input terminals; that is , the larger the value of CMRR (dB), the better is the matching between the two input terminals and the smaller is the the output common-mode voltage Vocm. On the other hand, a large voltage Vocm for a given common-mode input voltage Vcm is and indication of a large degree of imbalance between the two input terminals of poor common-mode rejection.

As supply voltages change because of poor regulation and filtering, for a given Op-Amp any change in the values of the supply voltages results in a change in the input offset voltage, which in turn causes a change in the output offset voltage. The change in Op-Amps input offset voltage caused by variations in the supply voltage is generally specified by a variety of terms: the input offset voltage sensitivity, the power supply rejection ratio, the power supply sensitivity, and the supply voltage rejection ratio are some of them. All of these terms are equivalent since they convey the same information. These terms are expressed either in microvolts per volt or in decibels.

$$SVRR = \Delta Vio / \Delta V$$

$$SVRR = 20 \log (\Delta V / \Delta Vio)$$

Note that the higher the value of SVRR in decibels, the lower is the change in input offset voltage due to the change in supply voltages or, in others words, the lower the value of SVRR in uV/V, the

better for Op-Amp performance. In fact, ideally the value of SVRR in uV/V should be zero.

Slew rate (SR) is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microseconds. In equation form,

$$SR = dVo / dt\,|_{max} \quad V/us$$

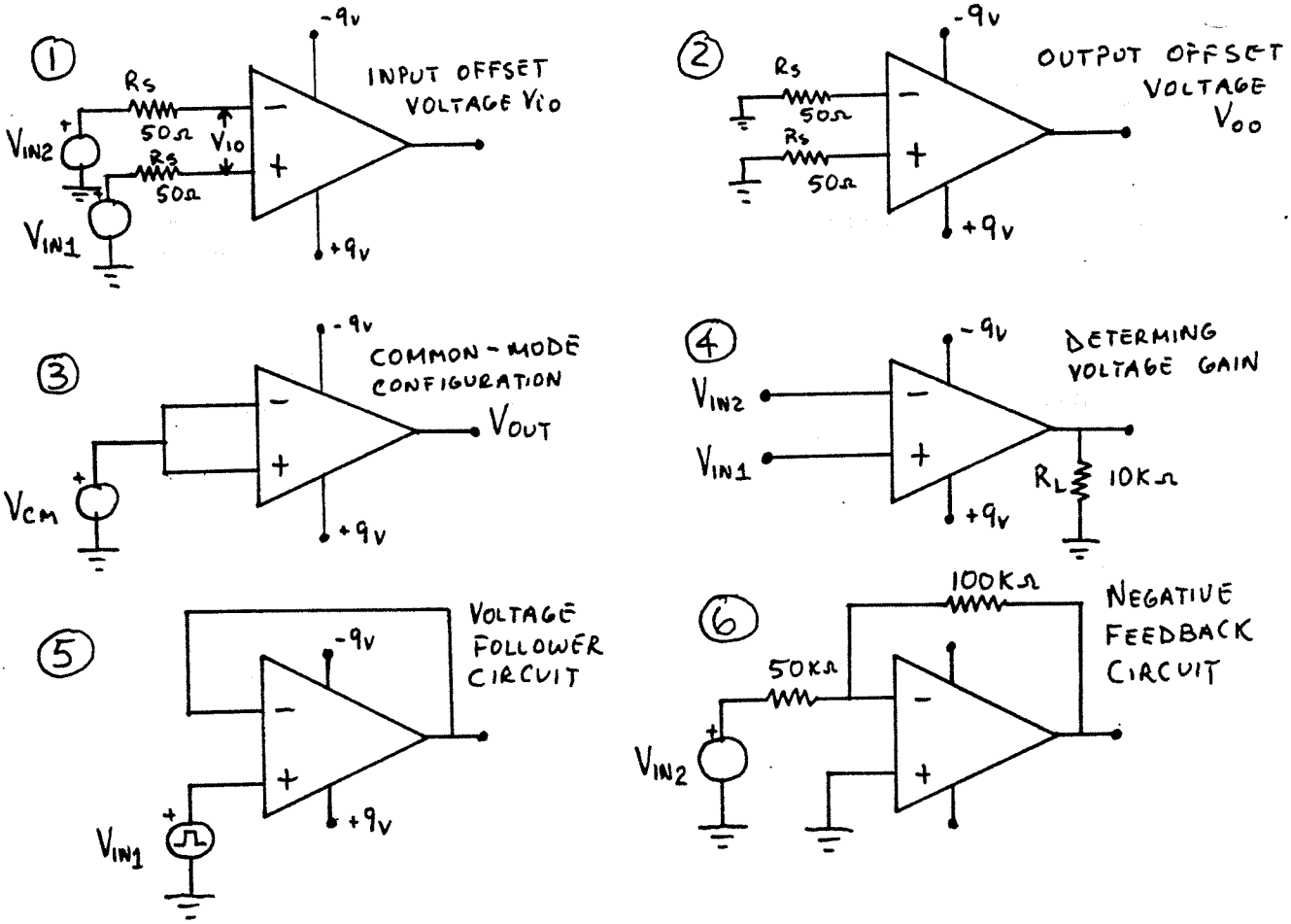
Slew rate indicates how rapidly the output of an Op-Amp can change in response to changes in the input frequency. Ideally, we would like an infinity slew rate so that the Op-Amps output voltage would change simultaneously with the input. Practical Op-Amps are available with slew rates from 0.1 V/us to well above 1000 V/us. Generally, the slew rate is specified for unity gain and is measured by applying a step input (d.c.) voltage. Slew rate is sometimes given indirectly as output voltage swing as a function of frequency or as voltage follower large signal pulse response. The slew rate of an Op-Amp is fixed; therefore, if the slope requirements of the output signal are greater than the slew rate, the distortion occurs. Thus slew rate is one of the important factors in selecting the Op-Amp for a.c. applications, particularly high frequencies.

Power consumption Pc is the amount of quiescent power (Vin = 0v) that must be consumed by the Op-Amp in order to operate properly. The amount of power consumed by the 741C is 85mW.

EXPERIMENT

To test the Op-Amp parameters the circuit shown in figures 1 through 6 were set up and the appropriate voltages were measured. Prior to that a SPICE analysis was performed for each of the aforementioned circuits. The SPICE output files for each analysis is shown in the appendix.

FIGURES



RESULTS

Shown below are the tabulated parameters generated by the SPICE analysis compared to the measured parameters, complete with test conditions and percent difference where applicable.

	COND	SPICE	MEASURED	% DIFF
input offset voltage	Rs=50Ω Vcm=0	15.3uV	---	---
output offset voltage		-38.2mV	-1.56V	>100%
input voltage range		-2.5 to 1.4	---	---
output voltage swing	Rl=0Ω	-4.2 to 5.4	-5.2 to 1.0	---
supply voltage rejection ratio	Rs=50Ω	58.41 dB	---	---
large signal voltage gain	Rl=10KΩ	1.5K	27	98%
common mode gain	Vcm=1.0 Rl=10KΩ	3.0	0.32	89%
common mode rejection ratio	Rs=50Ω	54dB	38bB	30%
power consumption	Vin=0	13.2mW	---	---
slew rate	Rl=0Ω Av=1.0	0.58V/usec	0.14V/usec	76%

DISCUSSION OF RESULTS

The SPICE analysis served to fully characterized the All Enhancement Pmos Op-Amp. Given ideal process conditions this design will produce and operational amplifier capable of a 15.3uV input offset voltage, -38.2mV output offset voltage, -2.5V to 1.4V input voltage range, -4.2V to 5.4V output voltage swing, 58.4dB SVRR, 1.5K large signal voltage gain, 3.0 common mode gain, 54dB CMRR, 13.2mW power consumption, and a 0.58V/usec slew rate.

Note that the input bias current and offset current were not characterized due to their insignificance when using Pmos Op-Amps. The inputs terminals are actual Pmos gates in which very negligible current flows by definition.

In comparison to typical Op-Amp parameters the input offset voltage obtained was very low. This implies a good match at the input terminals, which is quite believable considering that the transistors used were Pmos and not Bipolar. Pmos transistors provided a higher input resistance and a negligible offset current at the input terminals. The range of input voltage that can be applied common mode without disturbing the proper functioning of the Op-Amp generated by SPICE was -2.5V to 1.4V. This input range is non-symmetric about zero volts and might suggest that a few transistor channel ratio changes are in order. These changes might also help the output voltage swing of -4.2V to 5.4V. This voltage range means that the output voltage is directly proportional to the input difference & gain only until it reaches the saturation voltages and thereafter output voltage remains constant. When calculating the large signal and common mode gain of 1.5k and 3.0 respectively, the inputs had to be within the appropriate ranges to avoid the clipping of the output. This clipping effect will cause invalid voltage gains to be measured. The large signal voltage gain obtained by SPICE, however, was very low. This produced a common mode rejection ratio that

was also low. Since the CMRR is a measure of the degree of matching between the two input terminals, a high ratio would be expected to correspond to the low input offset voltage obtained. This, however, was not the case. Typical Op-Amp power consumption ranges from 75mW to 165mW. The SPICE analysis determined the device dissipates a low 13.2mW, which is a very favorable consumption. The slew rate obtained was 0.58V/usec. This value is usually merited depending on it's intended a.c. application.

As predicted, the ideal characteristics provided by SPICE for the given design were not fully present in the fabricated circuit. The realized Op-Amp produced a -1.56V input offset voltage, -5.2V to 1.0V output voltage swing, 27 unit large signal voltage gain, and 0.32 unit common mode gain. Due to the small voltages envolved, in addition to the apparent poor fabrication of the device, these were the only measurable parameters. Appendix E shows the output voltage obtained by the Op-Amp in the Voltage Follower configuration for the specified input. Theoretically the output should follow the input over the operating input voltage range. However, the output remains constant at 0.82V for negative input voltages up to 1.5V, at which point it then begins to follow the input. This effect might be explained by any number of process considerations. The output transfer function for the Op-Amp connected in the negative feedback configuration is also shown in appendix E. The transfer characteristic is accurate for negative feedback, however the output voltage swing is offset for both positive and negative voltages.

CONCLUSION

The designed All Enhancement Pmos Operational Amplifier has shown favorable device characteristics for applications desiring low power consumption, low voltage gain, low input offset voltage, and high input resistance. When the actual Op-Amp circuit was realized, the ideal parameters where not fully present, due primarily to the fabrication imperfections. Furthermore, an optimization of the circuit design, which can be realized by reassigning transistor channel ratios, may prove to enhance the existing input voltage range, and output voltage swing.

REFERENCES

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3. K.R. Roberge: "Operational Amplifiers: Theory and Practice", John Wiley and Sons, Inc., New York, 1975.

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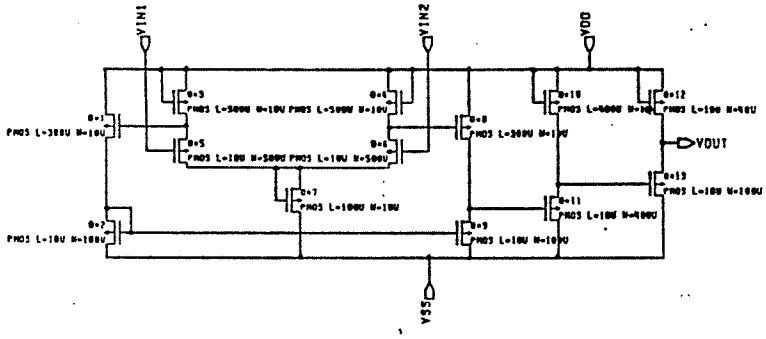
R. Pearson: for providing insight on the methodology of my testing and analysis.

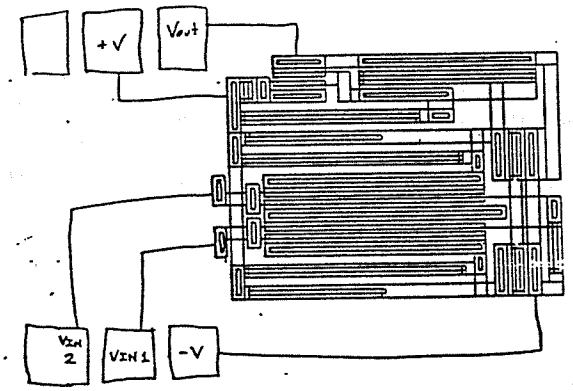
L. Fuller: for providing the Op-Amp design to fabricate and characterize.

APPENDIX

APPENDIX A Circuit Schematic of the All Enhancement P-type Op-Amp.



APPENDIX B Layout Design for the Op-Amp.



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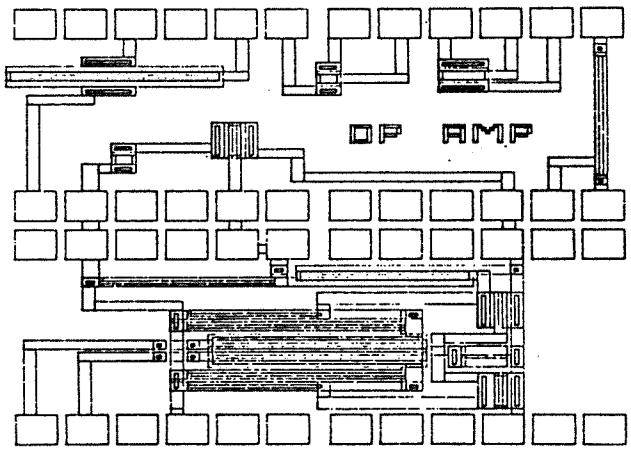
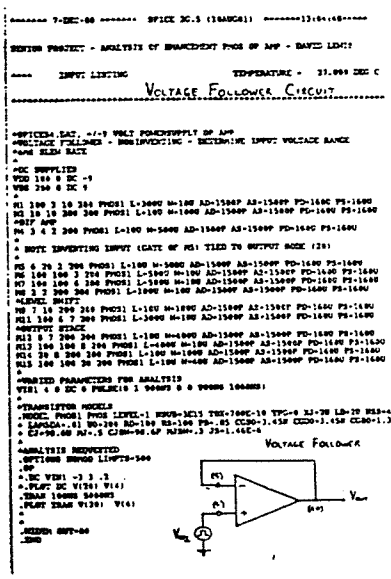
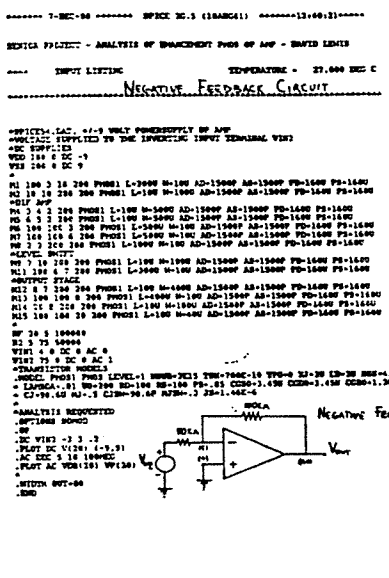
APPENDIX C Alternate Layout Design for the Op-Amp with test structures.

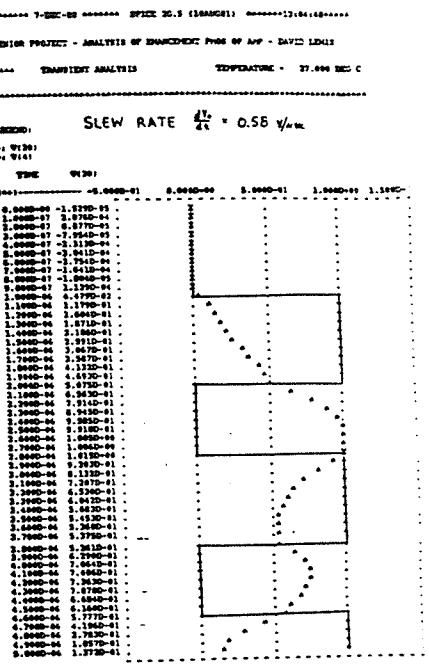


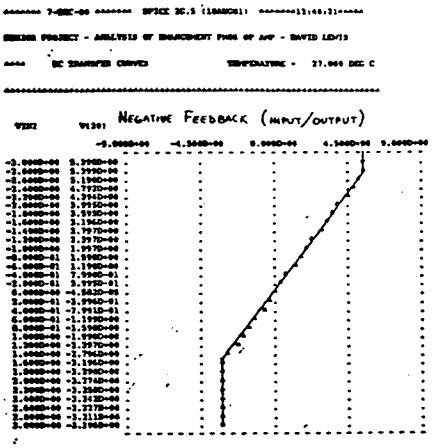
APPENDIX D

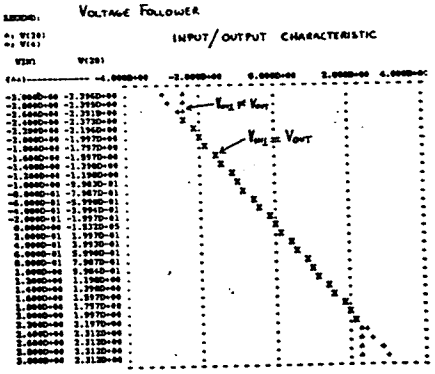
SPICE Simulations for the Op-Amp Voltage Follower and Negative Feedback Circuit.











APPENDIX F

Table 15-1 Typical parameters of monolithic operational amplifier at 25°C

Input offset voltage V_{io}	5 mV
Input offset current I_{io}	20 nA
Input bias current I_B	100 nA
Common-mode rejection ratio ρ	100 dB
PSRR	20 μV/V
I_{io} drift	0.1 nA/°C
V_{io} drift	5 μV/°C
Slew rate	1 V/μs
Unity gain frequency	1 MHz
Full-power bandwidth	50 kHZ
Open-loop difference gain A_d	100,000
Open-loop output resistance R_o	100 Ω
Open-loop input resistance R_i	1 MΩ
R_i for a JFET input stage	10^{12} Ω

APPENDIX E

Measured Output Characteristics for the Voltage Follower and Negative Feedback Circuit.