FOUR BIT CMOS ALU

Frank Leilich
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

A four bit CMOS arithmetic logic unit was designed. The design was layed out in ICE (integrated circuit editor).

INTRODUCTION

The ALU or arithmetric logic unit is the heart of the microprocessor. It performs all the arithmetic and logic operations that give the computer its power. Its design would be one of the first steps in creating a microprocessor. The current technology being used most in industry is CMOS. It has the advantages requiring only one power supply, operating in a wide voltage range with good noise immunity, and dissipating very little power when in a high or low state.

The most basic operations an arithmetric logic unit should perform are the add, subtract, and, or, not, exclusive or, and decrement. The seven functions necessitate the use of three select lines - one select option will not be used. The start of an ALU can be reduced to the design of the operation for one bit. The design of the one bit is then replicated and interconnected to get a full bit ALU.

The first step in the design was to draw up the possible truth tables for the one bit. The truth table that produced the shortest expression for the bit was used for the design. This ensured that the design would be as small as possible by using the fewest gates in the design.

The easiest gates to implement in CMOS are the NAND and the NOR. The layout of the project began with the design of standard NAND, NOR and inverter cells. The cells were then used to make the design of the bit. The bit was then copied four times into a chip. The individual bits were oriented and interconnected from the center of the chip. The output pads were added and the connections completed.

The process choosen for the CMOS uses a 2 micrometer deep P-well in a n-type wafer. The transistors are made using the self-aligned gate process. The steps were simulated using SUPREM. Times and temperatures for the growing of the oxides were computed and the doses and acceleration voltages for the ion implants were estimated.

DESIGN

Figure 1 is the truth table for the shortest expression of a bit. A Karnaugh map was made for each possible order the functions could be placed in and the table resulting in the shortest expression was used for the design. The total number of possible orders is eight factorial, which is 40,320. For finding the shortest expression a computer program was written in BASIC and run. The design of a bit for the ALU is shown in Figure 2.

One Bit Truth Table

Ax	Bx	S2	S1	S0	Dx
0	0	0	0	0	X
0	1	0	0	0	X
1	0	0	0	0	X
1	1	0	0	0	X
0	0	0	0	1	0
0	1	0	0	1	1
1	0	0	0	1	1
1	1	0	0	1	0
0	0	0	1	0	1
0	1	0	1	0	1
1	0	0	1	0	0
1	1	0	1	0	0
0	0	1	0	0	0
0	1	1	0	0	0
1	0	1	0	0	0
1	1	1	0	0	1
0	0	1	0	1	0
0	1	1	0	1	1
1	0	1	0	1	1
1	1	1	0	1	0
0	0	1	1	0	1
0	1	1	1	0	1
1	0	1	1	0	1
1	1	1	1	0	0
0	0	1	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	1	1	1	1

Select Function

State	S2	S1	S0	Function	State	S2	S1	S0	Function
0	0	0	0	not used	4	1	0	0	AND
1	0	0	1	SUBTRACT	5	1	0	1	ADD
2	0	1	0	DECREMENT	6	1	1	0	NOT
3	0	1	1	XOR	7	1	1	1	OR

Figure 1

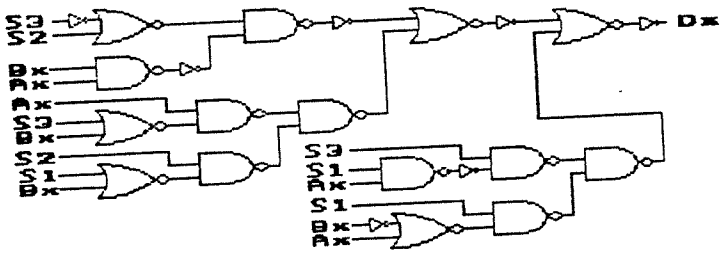


Figure 2

The three most used technologies for making CMOS in silicon are the P-well process, the N-well process, and the twin tub process[2]. The twin tub design was not used because of the extra processing steps that would be required. The reason the P-well process was choosen over the N-well is that most of the processing done at RIT is done on n-type wafers and the P-well process is the more common of the two. The design rule is 10 microns with 10 micron gates.

The process involves seven levels of masks. The steps involve taking a clean n-type wafer and growing a thick field oxide. The first mask then defines the p-well for the n-channel transistors and is shown in Figure 3a. The thick oxide is etched and the p-type diffusion is done. The second mask is the thin oxide mask, it defines where the transistors are going to be on the wafer, and is shown in Figure 3b. Photoresist is patterned on the wafer and the thick oxide is etched. The thin oxide is then grown around 500 Angstroms thick and now covers where the gates, sources, and drains of the transistors will be. The gates are polysilicon and the poly is deposited on the wafer at this time. The third mask defines the gates and is used now to etch the pattern into the polysilicon. This mask in shown in Figure 3c. In the process the "self-aligned" gate technique is used. The forth mask is the "p-select" and is shown in Figure 3d. The mask defines where the p-type implants go for the p-transistors. The fifth mask is the negative of the "p-select" mask and serves to define where the n-type implant goes for the n-type transistors. The mask is shown in Figure 3d. The wafer is covered with a deposited glass for protection. The six mask level defines the contact cuts and is shown in Figure 3f. Lastly the aluminum is deposited on the wafer and patterned with the metal pattern mask. The metal mask is shown in Figure 3e[2]. The final cross-section of a CMOS gate is shown in Figure 4.

The gate designs were made to allow the use of one supply rail to power gates above and below it. This eliminated the need to have two metal lines carring different voltages running next to each other. The standard cell layouts are shown in Figure 5. The construction of one bit layout was done by connecting the gates and making changes as needed. The final one bit layout occupies an area of 1170 microns from top to bottom and 810 microns from input to output and is shown in Figure 6. The final design of the ALU with all the inputs and outputs labeled is shown in Figure 7.

The processing was simulated using SUPREM. The six different regions in the cross section of the CMOS were simulated and can be identified in Figure 4. Region A is the P-well and gate of the NMOS transistor. The minimum desired depth of the P-well is 3 micrometers. The Boron was implanted into the wafer so that there would not be a high surface concentration which would lead to a high threshold voltage. The drive in was then done for 9 hours at 1100 degrees Celsius and the gate oxide was grown in dry oxygen for 35 minutes at 1000 degrees Celsius. The final estimated junction depth was 3.015 microns and the gate oxide thickness was 475.2 Angstroms. The ion implant was done with an acceleration voltage of 180 Kiloelectron volts and a dose of 3.65 E12 atoms per centimeter. The final estimated surface concentration was 4.8 E14 atoms per centimeter and a threshold voltage of 0.97 volts. Region B is the diffusion of the n-type drain and source in the P- well. The goal was to get a sheet resistance of around 60 ohms per square. This was done with a diffusion of Phosphorus for 15 minutes at 890 degrees Celsius. The final estimated sheet resistance was 62.75 ohms per square

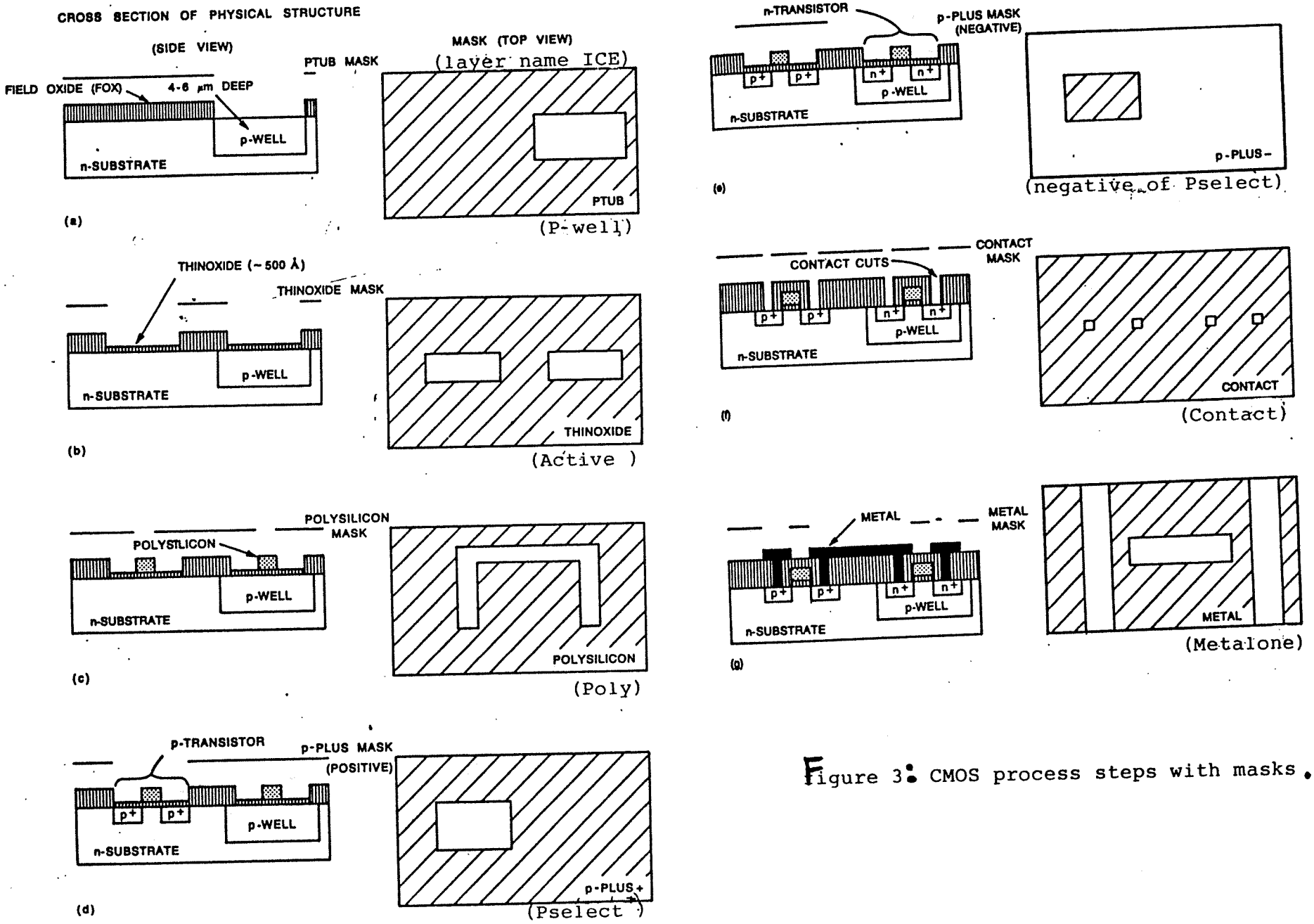


Figure 3: CMOS process steps with masks.

and a junction depth of 0.438 microns. Region C is the gate oxide over the n-type wafer for the PMOS transistor. The oxide is grown with the gate on the NMOS and was simulated with the same time and temperature. The final estimated thickness was 475.2 microns and the threshold voltage was -1.25 volts. Region D is the diffusion of the p-type drain and source for the PMOS transistor. The goal was to get a sheet resistance of 10 to 100 ohms per square. This was done by diffusion of Boron for 15 minutes at 890 degrees Celsius. The final estimated resistance was 35.74 ohms per square and a junction depth of 0.292 microns. Region E is the field oxide over the P-well. To provide protection from the 180 Kilo- electronic Volt implant the oxide had to be at least 8000 Angstroms thick. It was grown with steam for 1 hour and 40 minutes at 1100 degrees Celsius. The gate oxide is grown on the field oxide in this region and was simulated also. The final estimated thickness was 8121 Angstroms. Region F is the field oxide over the rest of the wafer. This is simulated the same as region E except with out the ion implant. The final thickness was also 8121 Angstroms.

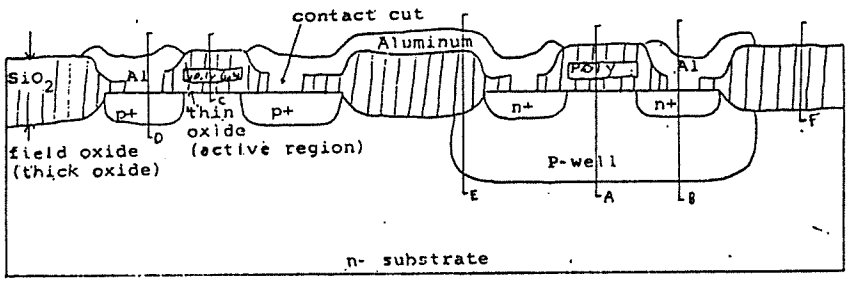


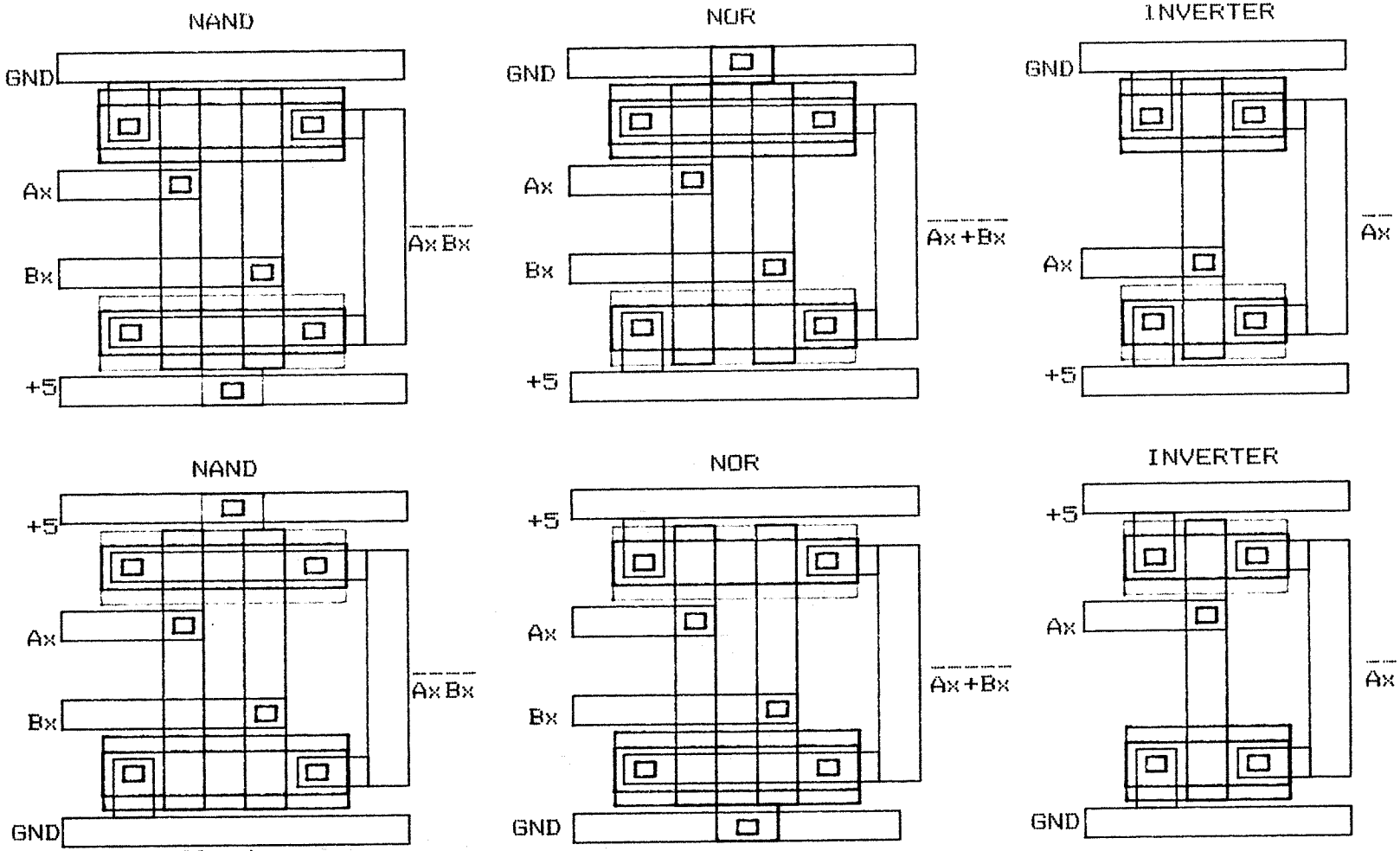
Figure 4

CONCLUSIONS

The ALU or arithmetic logic unit is the heart of the microprocessor. It performs all the arithmetic and logic operations that give the computer its power. A four bit ALU designed as part of the first step in creating a microprocessor. The current technology now available at RIT is CMOS. The CMOS technology has the advantages of requiring only one power supply, operating in a wide voltage range with good noise immunity, and dissipating very little power when in a high or low state.

ACKNOWLEDGMENTS

I would like to thank Rob Pearson for his help in designing the standard CMOS cells and the simulation in SUPREM.



Blue - Aluminum
Red - Polysilicon
Black - Contact Cut
Green - Active (thin oxide)
Orange - Pwell
Purple - Pselect (ion implant)

Figure 5: Layouts for ALU Gates

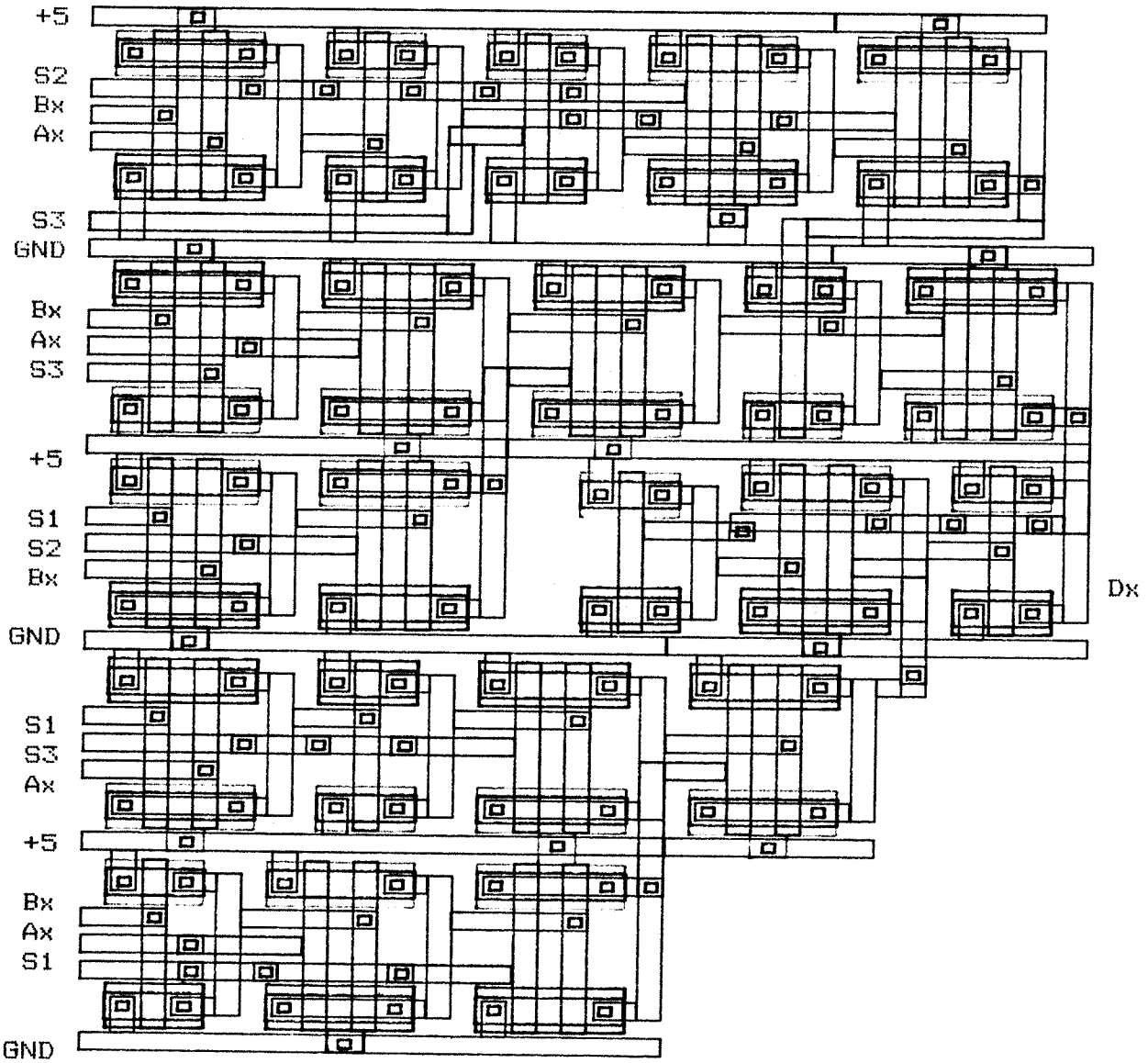


Figure 6: Layout for one Bit of ALU

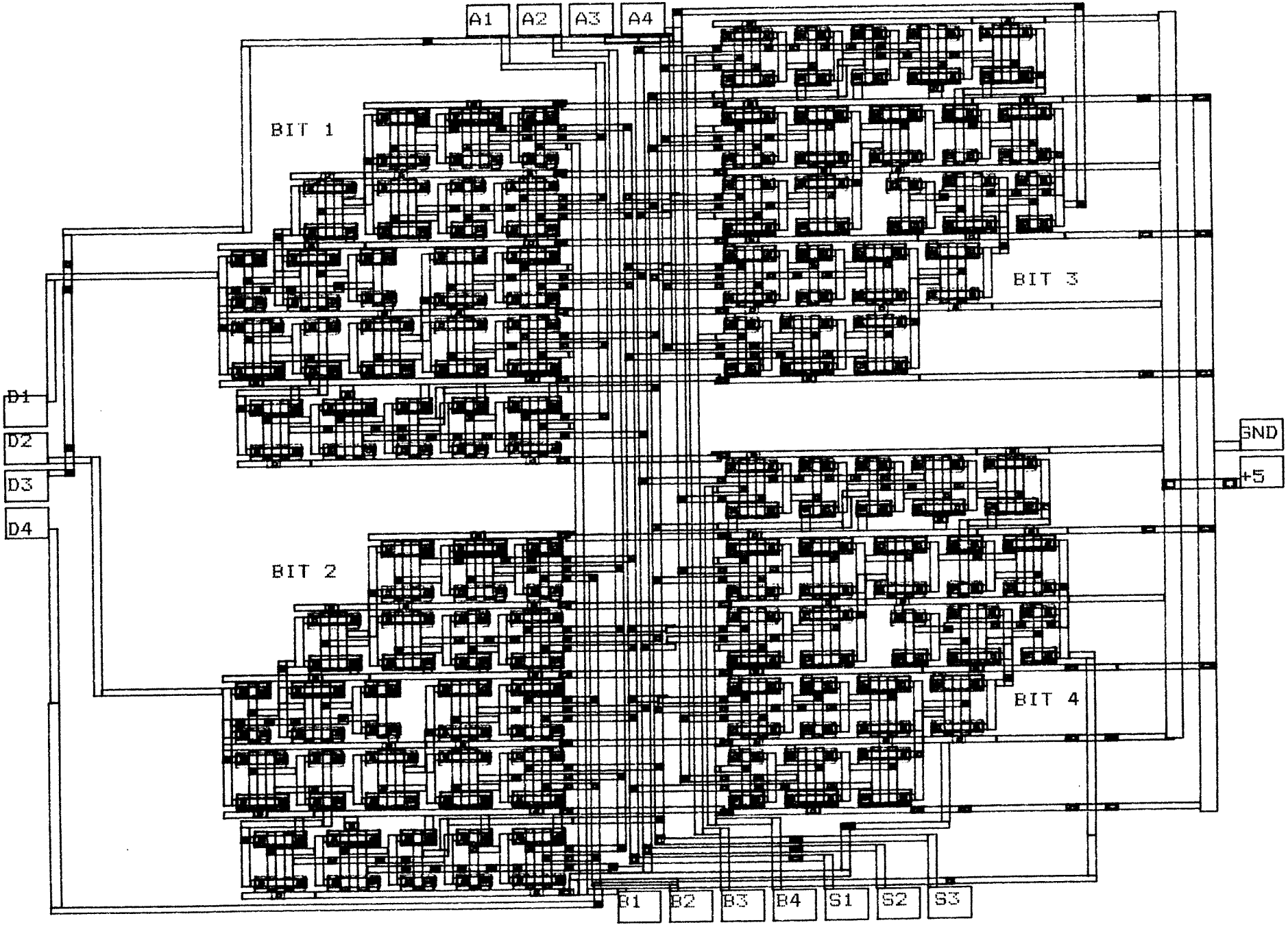


Figure 7: Four Bit CMOS ALU

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