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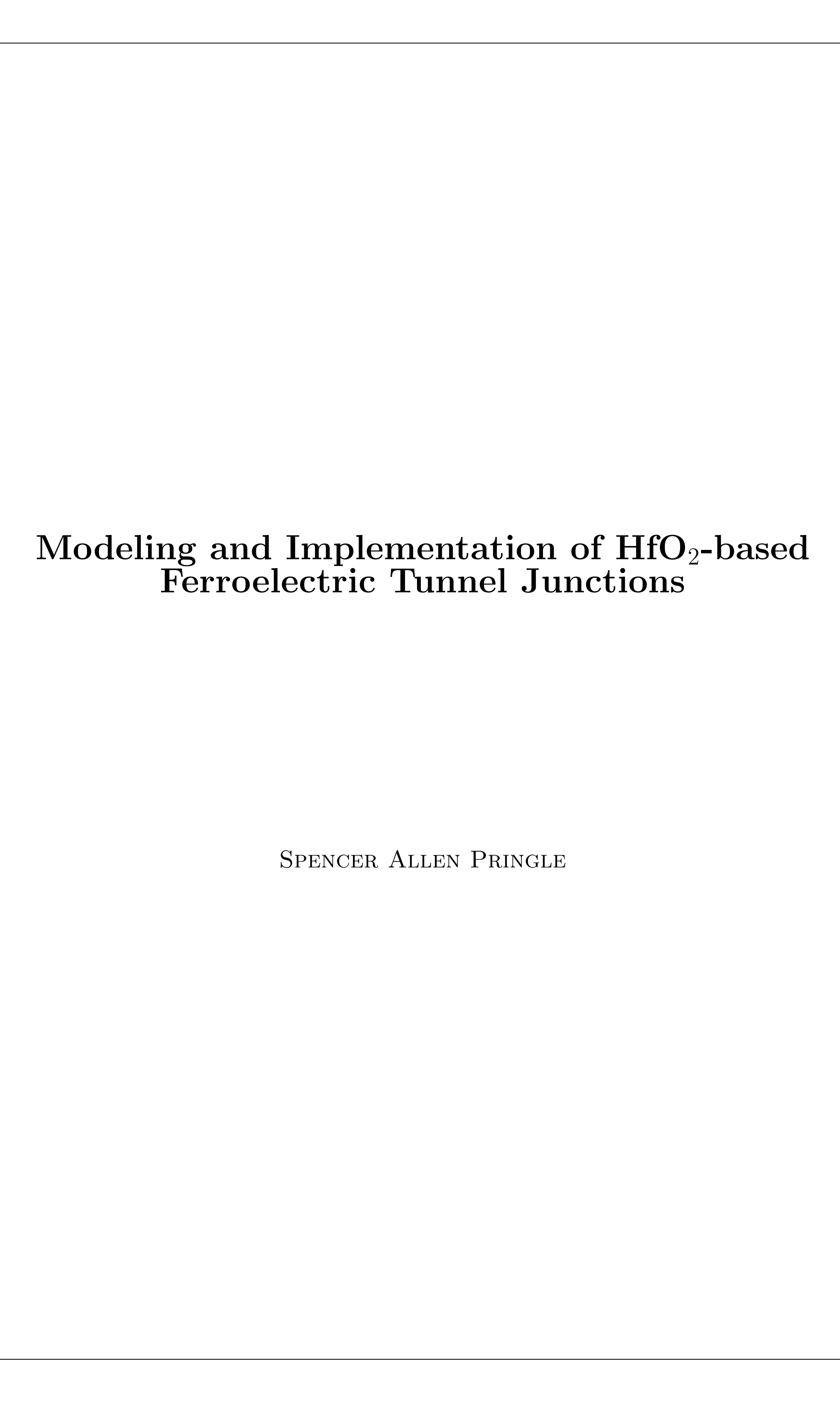

Modeling and Implementation of HfO_2-based Ferroelectric Tunnel Junctions

Spencer Allen Pringle

Modeling and Implementation of HfO_2-based Ferroelectric Tunnel Junctions

Spencer Allen Pringle

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in Partial Fulfillment
of the Requirements for the Degree of
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in
Microelectronic Engineering

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Department of Electrical and Microelectronic Engineering

Modeling and Implementation of HfO_2-based Ferroelectric Tunnel Junctions

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I would like to dedicate this work to my mother, Sharon Allen Pringle. Without your encouragement and help, none of this would have been possible. You're my inspiration to keep striving to be a better person.

Love, Spencer

Abstract

HfO_2-based ferroelectric tunnel junctions (FTJs) represent a unique opportunity as both a next-generation digital non-volatile memory and as synapse devices in brain-inspired logic systems, owing to their higher reliability compared to filamentary resistive random-access memory (ReRAM) and higher speed and lower power consumption compared to competing devices, including phase-change memory (PCM) and state-of-the-art FTJ. Ferroelectrics are often easier to deposit and have simpler material structure than films for magnetic tunnel junctions (MTJs). Ferroelectric HfO_2 also enables complementary metal-oxide-semiconductor (CMOS) compatibility, since lead zirconate titanate (PZT) and $BaTiO_3$-based FTJs often are not.

No other groups have yet demonstrated a HfO_2-based FTJ (to best of the author's knowledge) or applied it to a suitable system. For such devices to be useful, system designers require models based on both theoretical physical analysis and experimental results of fabricated devices in order to confidently design control systems. Both the CMOS circuitry and FTJs must then be designed in layout and fabricated on the same die.

This work includes modeling of proposed device structures using a custom python script, which calculates theoretical potential barrier heights as a function of material properties and corresponding current densities (ranging from 8×10^3 to 3×10^{-2} A/cm^2 with $R_{\text{HRS}}/R_{\text{LRS}}$ ranging from 5×10^5 to 6, depending on ferroelectric thickness). These equations were then combined with polynomial fits of experimental timing data and implemented in a *Verilog-A* behavioral analog model in *Cadence Virtuoso.* The author proposes tristate CMOS control systems, and circuits, for implementation of FTJ devices as digital memory and presents simulated performance. Finally, a process flow for fabrication of FTJ devices with CMOS is presented. This work has therefore enabled the fabrication of FTJ devices at RIT and the continued investigation of them as applied to any appropriate systems.

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List of Symbols

Term	Description	Units/Value
P	Polarization	$\mu C/cm^2$
P_r	Remanent polarization	$\mu C/cm^2$
t_{sat}	Saturation time	s
t_{pdf}	Propagation delay falling	s
t_{pdr}	Propagation delay rising	s
t_{f}	Fall time	s
t_{r}	Rise time	s
σ_p	Polarization surface charge density (in ferroelectric)	$\mu C/cm^2$
σ_s	Screening charge density (in electrode)	$\mu C/cm^2$
$\mathcal{E}$	Electric field	V/cm
$\mathcal{E}_{\text{c}}$	Coercive electric field of ferroelectric	V/cm
V_{c}	Coercive voltage of ferroelectric film	V
V	Applied voltage	V
d	Thickness of ferroelectric	nm
δ_x	Screening length in electrode "x"	nm
E_c	Energy at the conduction band edge	eV
E_v	Energy at the valence band edge	eV
E_F	Fermi level	eV
E_g	Band gap energy	eV
χ_x	Work function of metal "x"	eV
E_a	Electron affinity of dielectric	eV
ψ	Potential	eV
k_B	Boltzmann's constant	8.617×10^{-5} eV/K
J_{tun}	Fowler-nordheim tunneling current density	A/cm^2
J_{th}	Thermionic emission current density	A/cm^2
$\bar{\psi}$	Average potential barrier	eV
ψ'	Maximum potential barrier	eV
m^*	Electron effective mass	kg
m_e	Electron rest mass	9.11×10^{-31} kg
N_A	Acceptor concentration	cm^{-3}
N_D	Donor concentration	cm^{-3}

Term	Description	Units/Value
N_x	Carrier concentration (of appropriate type)	cm^{-3}
c_0	Atomic density	cm^{-3}
V_{DD}	Write voltage high rail	V
V_{SS}	Write voltage low rail	V
v_{dda}	Read voltage high rail	V
v_{ssa}	Read voltage low rail	V
gnd	0V, ground	V
q	Elementary charge	1.602×10^{-19} C
T	Temperature	K
ε_0	Vacuum permittivity	8.854×10^{-14} F/cm
ε_{f}	Ferroelectric permittivity	F/cm
$\varepsilon_{\mathrm{Si}}$	Silicon permittivity	11.7 F/cm

Chapter 1

Introduction

Traditional CMOS devices are reaching fundamental physical limits of scaling and nonvolatile memory devices based on charge-storage are no longer meeting requirements for future high-speed systems [9–12]. In addition, the trend towards portable computers, smart phones, health telemetry, and smart building integration has renewed desire for ultra-low-power devices [13]. Neuromorphic computing (NMC) systems show huge potential to enable such power performance; taking inspiration from information processing in electro-chemical biological systems (specifically the brain) and emulating or reproducing that operation using electronic devices [11].

Any system for neuromorphic computing (NMC) endeavors to mimic the stimuli response of the human brain. Often such a system is composed of an array of elements which emulate the response of synapses (two-terminal connections) between two neurons, interconnected appropriately as the system requires, which exhibit increasing output in response to more frequent potentiation, called spike-timing dependent plasticity (STDP) [14]. In simpler terms; an element which has not seen stimulus for a long time will provide less response when presented with stimulus than an element which has recently seen many stimulus events. Though less accurate than traditional Von-Neumann computation schemes, neuromorphic systems have been shown to have incredible speed and power consumption advantages when working with images, pattern recognition, etc. Specifically, the "CAVIAR" system reports speed increase of

more than 3 orders of magnitude compared to conventional image processing [15], and the SpiNNaker chip proves power consumption improvement by consuming merely a few nanojoules per neuron event [16]. Further, one can look to the IBM TrueNorth and SyNAPSE chips for more proof of high speed and low power computation. However, optimal synapse devices must be two-terminal devices which exhibit low power operation, high speed, high reliability, high endurance, and good memory window with continuous states. Three potential candidates are ReRAM, covered more completely in Section 3.4.1, MTJs, and FTJs.

1.1 Research objectives

This thesis work evaluates incorporation of HfO_2-based FTJ in NMC and nonvolatile digital memory applications, specifically focusing on device performance/optimization and system enablement. It explores material properties, basic device performance, process development for CMOS integration, and related system design including simulated performance. By optimizing material properties of its various parts, the device can exhibit a range of performance from ultra low power with large memory window to low power with better speed performance when implemented with address systems (lower $\tau = RC$). This research work thereby endeavors to provide a full foundation, see Figure 1.1, for further exploration and fabrication of HfO_2-based FTJ, both specifically at RIT and (with process modifications for varying CMOS device types and sizes) at any facility.

1.2 Thesis organization

This introductory Chapter 1 highlights applications for which FTJ devices can enhance performance and simplify implementation and documents the research objectives and organization of this thesis. Chapter 2 presents an overview of the physical

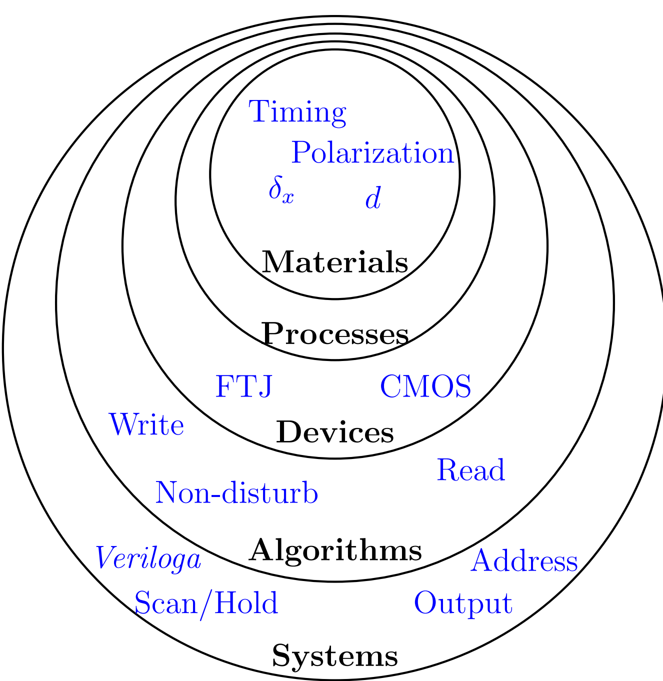


Figure 1.1: Diagram representation of the dependencies of various implementation stages of the technology presented in this thesis.

properties of ferroelectric materials and highlights some specific aspects which are of concern to their implementation in FTJs. Chapter 3 reviews the history of ferroelectric memories, the discovery and subsequent explanation of FTJs, and the ideal applications of these devices while also presenting alternative technologies and comparing their performance. After demonstrating the advantages of FTJs, Chapter 4 presents simulation (from quantum-mechanical basis) of device operation, with corresponding band structures and current densities in each memory state (using a custom python script). Finally, an FTJ using ferroelectric HfO_2 is designed and simulated in Chapter 5 and its performance is compared to other state of the art FTJs. In this same chapter, a CMOS-integrated fabrication process for HfO_2-based FTJ devices is designed and discussed. Chapter 6 presents related address schemes and systems; with schematics, simulations, *Verilog* descriptions, and layouts, designed for digital memory applications using *Cadence Virtuoso* and a 45-nm process design kit (PDK). Finally, the results of this work are summarized in Chapter 7 and future work is pre-

sented. This work therefore provides a nearly comprehensive overview of FTJ devices from materials to systems, including ferroelectric HfO_2 device simulation, the design of a full CMOS-integrated fabrication process, and *Cadence Virtuoso* system design and simulation with custom *Verilog-A* behavioral analog models of designed FTJs.

1.3 Neuromorphic Computing with Memristors, ReRAM

Neuromorphic systems with ReRAM as synapse elements have been reported which take advantage of the intrinsic similarity between such devices and synapses (both are two-terminal and behave memristively). ReRAM devices inherently pass more current as they are programmed further (provided they can be so-designed) and therefore provide both space-reduction (compared to larger CMOS elements or register implementation) and simplification of STDP response generation. In their papers, Ambrogio et. al report low-power ($\approx 10^5$ power reduction) generation of STDP signals with ReRAM 1 transistor - 1 resistor (1T1R) synapse elements constituting a neuromorphic system capable of unsupervised learning of MNIST handwritten digits achieving 86% accuracy [17]. Further, the power consumption of the system was reduced to $1{\times}10^{-12}$ Joules per neuron event, using a series of short pulses for write/read, and enable ultra-low power computation [18]. Park et. al used TiO_x-based ReRAM in a neuromorphic system having a 250 node hidden layer followed by a 125 node secondary hidden layer and 10 bit output layer for recognition of 528-bit hand-drawn digits (0 through 9) from the MNIST database. The system uses a different scheme for pulse generation, consisting of discretizing element conductivity to 64 "conductance states" and achieves up to 84% accuracy [19]. Resistive devices as synaptic elements therefore provide a unique opportunity in ultra low-power high speed systems for applications requiring highly-parallel computation.

1.4 Using Ferroelectric Tunnel Junctions

An FTJ is very similar to a ReRAM device in function (both two terminal memristors), but differs in mechanism. Where ReRAM elements are either filamentary (create/break a mechanical filament on program/erase) or non-filamentary (often involving changing concentration of oxygen vacancies at the barrier interface) [20], a change in resistance for an FTJ is based on the changing internal polarization field magnitude and direction of a ferroelectric material separated by two electrodes of different materials (specifically having differing Debye lengths) [4]. Since, optimally, a synaptic element will have a smooth (analog) transition from having seen no potentiation (and little response) to many recent potentiations (and large response), an FTJ for such application should include a ferroelectric material with as many domains as possible and a low coercive electric field such that the ferroelectric depolarizes under the absence of repeated stimuli. Such a film will be slightly thicker than typical for FTJ used in non-volatile memory (NVM) and of a larger area. These properties are in contrast to those required for NVM (high coercive field and low # of polarization domains). Ferroelectric HfO_2 is a good candidate due to the large difference in resistive states possible,the ability to get a large number of domains in even small areas, and high speed performance with write/read times of 10 ns [21]. Interestingly, HfO_2-based FTJ can be designed to provide optimal NVM performance or NMC performance, explored more in Sections 5.1 and 5.2.

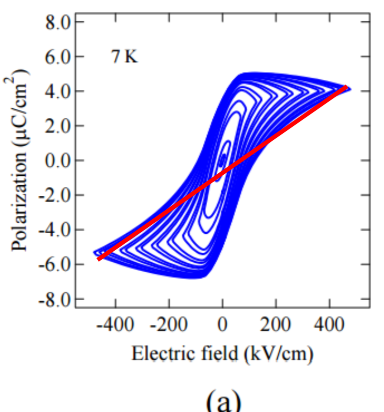
Chapter 2

Physics of Ferroelectric Materials

Ferromagnetism (permanent magnetic moment) was the first ferroic property discovered and was so-named because it occurs often in iron-containing alloys. Ferroelectricity is a property of materials which exhibit spontaneous electric polarization (dipole moment density) and although most ferroelectrics do not contain iron, was so-named because of it's relation to the other ferroics (materials which can polarize in some way) and was classified as such. In a basic sense, a ferroelectric is a dielectric that (once stimulated) exhibits a non-zero reversible polarization at 0 applied electric field, as shown in Figure 2.1. This remanent polarization, P_r, is due to an internal potential, covered in more detail in the next few sections. Most ferroelectrics are either transition metal oxides or chalcogenides. Additionally, materials can exhibit any ferroic property independent of the others, and will also always be piezoelectric, and a material which exhibits any two or more (excluding piezoelectricity) is considered "multiferroic" [22].

2.1 Crystal structure

The internal electric field which ferroelectric materials exhibit, below their curie temperature, is a result of their crystal structures. Though the material can maintain a so-called "prototype" phase above the curie temperature, due to available phonon energy, at lower temperatures the crystal precipitates into a phase which is polar,



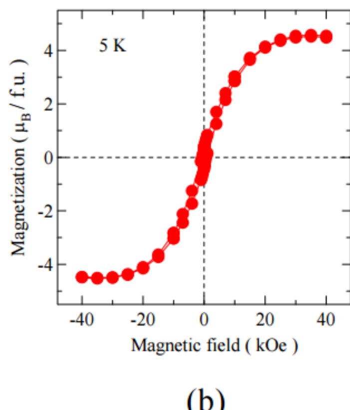
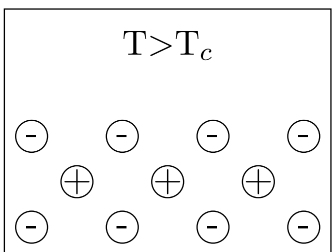
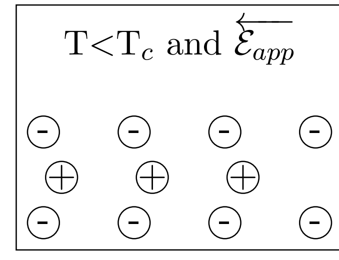


Figure 2.1: Ferroelectric polarization (a) and weak magnetic moment (b) of multiferroic Bi_2NiMnO_6 at 7K, from Shimakawa et. al [1]. The red line on (a) is what this plot would look like for a perfect dielectric.





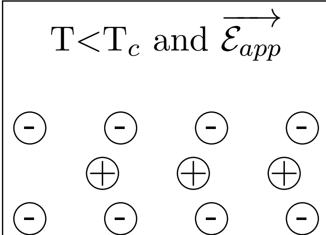


Figure 2.2: Simple representation of the atomic structures of a ferroelectric as its prototype phase (left) relaxes into one of two polar phases (middle and right) after the application of an external field. A ferroelectric would remain in the corresponding state even after the removal of $\mathcal{E}_{app}$, while a dielectric would deflect (as shown) during stimulus application but relax to the non-polar phase (left) once that field was removed.

represented in Figure 2.2, and exhibits an aggregate total polarization field based on the orientation of domains (as a function of defects and grain boundaries). This topic (and more complicated derivations of the physical phenomena of ferroelectrics) is explored more completely in the famous book by Lines and Glass [22].

2.2 Polarization in ferroelectrics and dielectrics

The atoms in dielectric materials respond to external bias, as shown in Figure 2.2, by deflecting from their zero-field position due to the applied electrostatic attraction/repulsion of the field. Considering a single unit cell, the energy required for an

atom to remain in that position (along an arbitrary plane) follows a quadratic curve with only one minimum at the zero-field position. This is because a simple dielectric has a centrosymmetric crystal structure. A similar plot of atomic energy versus position in a ferroelectric unit cell would instead behave as $(x^2 + a)(x^2 + b) + c$ and exhibit two separate minimas. This is because the crystal structure of a ferroelectric is non-centrosymmetric, and is the physical origin of the macroscopic polarizability of a ferroelectric film [22]. Furthermore, the polarization at zero applied field is called remanent polarization, P_r. It can be either expressed in each polarization state (positive $P_{r,+}$ or negative $P_{r,-}$) or as the total of both states $2P_r = P_{r,+} + P_{r,-}$ (often in the case of symmetric states, where $P_{r,+} = -P_{r,-}$). The electric field required to transition from one polarization state to the other (where P passes through 0) is called the coercive electric field, $\mathcal{E}_c = V_c/d$ [22]. Figure 2.1 shows a ferroelectric film with $2P_r = 8\mu\text{C/cm}^2$ and $\mathcal{E}_c = 0.1$ MV/cm.

2.3 Non-intrinsic ferroelectrics

Though most ferroelectrics were classically demonstrated as bulk materials and later implemented as thin films, recent improvements in film deposition technologies have enabled the engineering of materials which could be called "non-intrinsic" ferroelectrics. Typically, the crystallization of a material proceeds in an effort to minimize total energy and occurs unconstrained (meaning the atoms are free to move within the lattice). Recently, a group from NamLAB deposited films of HfO_2 by atomic layer deposition (ALD) and incorporated varying atomic % of Si atoms. After annealing, unconstrained, the material crystallizes to a mixture of typical monoclinic/tetragonal phases (which are centrosymmetric). However, by capping the HfO_2 with a thin film of TiN and annealing at a temperature such that the TiN atoms were likely still in a stable form, the HfO_2 crystallizes to orthorhombic phase and is non-centrosymmetric [23]. This change in state is likely due to a combined interaction

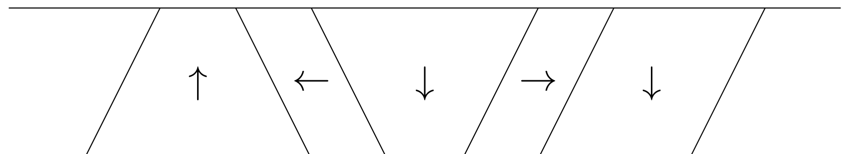


Figure 2.3: Simple diagram of domains in a model ferroelectric film.

of the atomic stress from Si doping, the extra strain energy introduced by the capping material, and the inhibition of relaxation modes available when un-capped. The Ferroelectric Device Research at RIT (FeDR RIT) group, working with NaMLAB, have successfully demonstrated similar material results at RIT by doping HfO_2 with Al, using similar capping and anneal strategies.

2.4 Ferroelectric domains

A realistic ferroelectric film will not be perfectly oriented all the same direction, as considered in Figure 2.2, but instead have many differently oriented crystal clusters, due to defects. A very basic visualization of this effect is shown in Figure 2.3, and is explored more thoroughly in the book by Lines and Glass [22]. In general, the maximum size of a domain can be extracted based on crystal parameters but for most materials is roughly 20 to 100 nm.

2.5 Area-dependent effects

The response of an FTJ can be affected by the domains which exist in the ferroelectric, with reference to the area of the device. Consider, if the maximum domain size is close to the area of FTJ devices, some devices will encompass only one domain which is oriented parallel to the applied field. These devices would have maximum performance, since the entire film contributes to polarization ($P_{\max}$). However, this also means that some devices will happen to lie over a domain which is entirely perpendicular to applied field and therefore cannot be polarized by the electrodes!

These devices would simply not work at all. Therefore, for highest reliability, a film should have maximum domain sizes much smaller than the desired area of FTJ devices. This way, every device will have some domains directed parallel and some perpendicular. Every device in an array would therefore work, but will have reduced performance ($P \approx 0.5 P_{\mathrm{max}}$).

Chapter 3

Brief History and Applications of FTJ Implementations

3.1 Early memory using large-dimension PZT

Though not FTJs, ferroelectric memories were first reported in an MIT masters thesis by Dudley Allen Buck in 1952 [24]. Larger ferroelectric memory arrarys by Bell Labs were also discussed in a Scientific American article in 1955 by Ridenour [25] though a good explanation of such devices was not given until a 1973 IEEE article by Kaufman [2]. These "bender memory" devices used 5 mil (127 μm) thick PZT ferroelectric films sandwiched between conducting electrodes, shown in Figure 3.1, to store data in polarization which creates a positive or negative pulse (while clamped, due to the electrostrictive and piezoelectric response) in response to application of a read voltage. These devices were very high power (30 V/mil write, 45V read) and very slow ($\approx$ 1 ms) [2].

3.2 More recent implementations with $BaTiO_3$

As covered briefly in Section 4.2, Contreras et. al discovered the first FTJ using $BaTiO_3$, a ferroelectric well known since it's initial synthesis as a bulk material. In that paper, the group had investigated both Pt/PZT/$SrRuO_3$ and $SrRuO_3$/$BaTiO_3$/$SrRuO_3$ FTJs. The PZT FTJ displayed poor performance (likely due to vanishing polarization density at small dimensions) while, although having similar electrodes, the $BaTiO_3$-

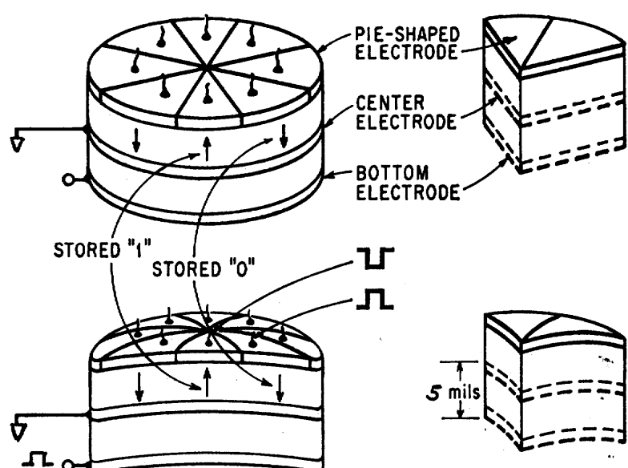


Figure 3.1: "Bender memory" schematic from [2]. This 8-bit device stores data as remanent polarization in the top-most ferroelectric material. Write pulse is ≈ 1 ms of 20-30 V/mil.

based FTJ had a memory window of $HRS/LRS \approx 3$, shown in Figure 3.2 [3]. As already discussed in Section 4.2, the memory window is heavily dependent on the dissimilarity of screening lengths between electrodes and, considering this FTJ has the same material for both electrodes, it's surprising that the performance is so good. The group (Contreras, Kohlstedt, et. al) clears up this incongruity in their 2005 paper where, in addition to using the findings of Zhuravlev et. al [4] to explain FTJ performance, they report that the interface between bottom electrode and ferroelectric exhibits a Ruddelsen-Popper interfacial layer which modifies the effective screening length for that electrode, increasing asymmetry and therefore memory window [26].

Groups have continued to research $BaTiO_3$-based FTJs, including a recent 2013 paper by Wang et. al which presents a device with Co and $La_{0.67}Sr_{0.33}MnO_3$ as electrodes. The group achieves a memory window $HRS/LRS \approx 100$ with a 2 nm ferroelectric and demonstrates switching times as fast as 13 ns (for relatively high write voltages, $\approx 3V_c$). They also use extracted values to design a *Verilog-A* model of their devices [10].

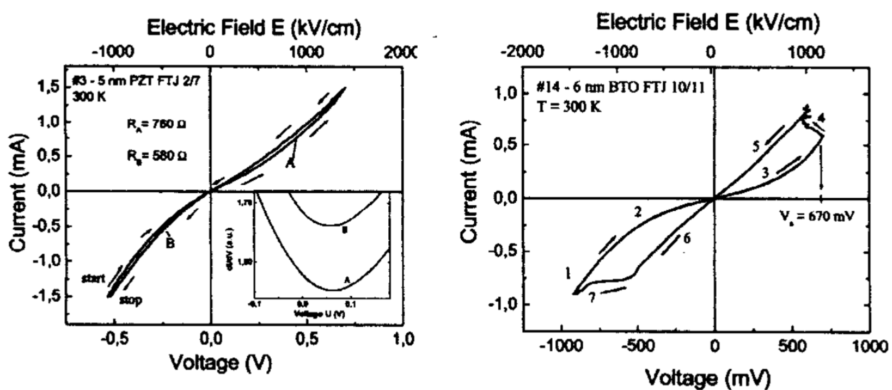


Figure 3.2: Performance of FTJs for (a) fresh device with PZT ferroelectric and (b) device with $BaTiO_3$ ferroelectric after -1.2V priming pulse, taken from Contreras et. al [3].

3.3 Applications of FTJs

FTJ devices are ideal for two main applications; non-volatile digital memory and brain-inspired computing. Portable electronics demand fast, low-power storage devices and, as shown in Table 3.1, FTJ provide the highest speed and lowest power.

Brain-inspired computing is the implementation of CMOS devices, which mimic the integrate-and-fire responses of neurons, interconnected by devices with modifiable signal strength, the function of a synapse, as shown in Figure 3.3. These types of systems are most applicable to spatio-temporal data sets which are tolerant to noise. For instance, facial recognition in video monitoring was demonstrated by Chevitarese et. al using the IBM neuromorphic chip (which uses filamentary ReRAM devices) and achieves 99% accuracy with total power consumption of 222mW [30]. Digitization of pen-stroke inputs and word-detection in audio signals could also benefit from neuromorphic implementation. The easiest type of synapse to implement is a two-terminal memristor which can be programmed to either have a high resistance (low connective strength) or low resistance (high connective strength). Of available memristor devices, shown in Table 3.1, FTJs are at a clear advantage. Though occupying more area than PCM and FTJ devices, FTJs are faster and operate at lower power compared to all other devices. For this reason they are optimal for both neuromorphic

Device	NAND/NOR	ReRAM	PCM	MTJ	FTJ
Visual (Red and blue boxes are two different states in time)	n^+-PolySi Control Gate, SiO_2 Barrier Oxide, n^+-PolySi Floating Gate, SiO_2 Tunnel Oxide, n^+ S/D, n^+ S/D, p^--Si Substrate	M2, M1	M2, M1	M2, ← ←, → ←, M1	M2, ↑ ↓, M1
Mechanism	Vt Shift	O_2 Vac./ Filamentary	Phase change	e^- Spin (Mag)	Polarization
Speed (s)	400u [27]	500n	50n	30n [27]	10n
Power (J)	15u [28]	250n	6p	1.4u	30f
Cell Area	$4F^2$ or $10F^2$ [29]	$25F^2$	$16F^2$	$1.3F^2$	$22F^2$
Material	Si	Ag, a-Si, W	$Ge_2Sb_2Te_5$	MgO(mag)	$BaTiO_2$ (now HfO_2)

Table 3.1: Performance of alternative technologies compiled from various sources. MTJ values from Aziz et. al and Lee et. al. [5, 6], all other from Ebong et. al. and Kim [7, 8] unless otherwise referenced in table.

and non-volatile memory applications.

3.4 Alternative technologies

Memristors can be implemented by a few different technologies, each with their own characteristic strengths and shortcomings, which are discussed in this section.

3.4.1 Filamentary ReRAM

These devices operate by forming and destroying a nanofilament of conducting material in an insulating or high-resistance "switching" medium. Many types of these devices exist, but generally the most used CMOS-compatible versions are Ag/SiO2/Pt or W/SiGe/a-Si/Ag. The first type forms/destroys Ag nanofilaments through the SiO2 layer while the latter forms/destroys Ag nanofilaments through the a-Si layer [31, 32]. Both switching mediums are ≈ 20 nm thick. Though these types of devices

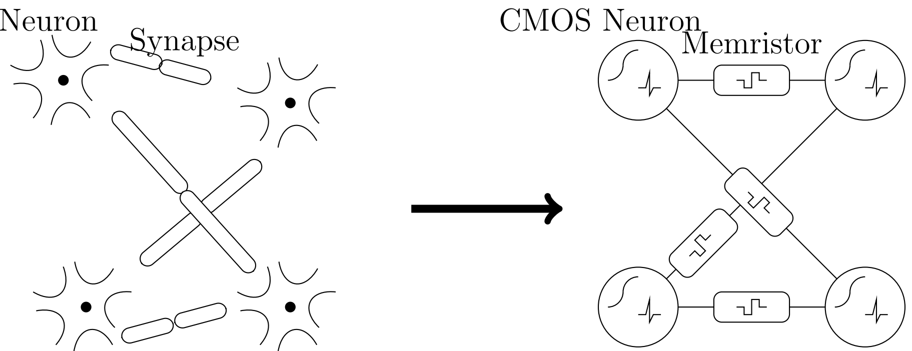


Figure 3.3: Simple diagram of (left) a physical model of neurons and synapses, the brain's computation devices, and (right) their electronic implementation in a typical brain-inspired computing system.

are well-understood and widely used, they are not very low power (3.5V program pulses applied to devices with $R_{\text{avg}} \approx 1M\Omega$) and are rather slow ($\approx$ 100 µs program times, $\approx$ 500 µs read) [32].

3.4.2 Magnetic tunnel junctions

The MTJ is designed as a tunnel oxide sandwiched between two ferromagnetic materials. One of the ferromagnets is pinned to be magnetized in a direction, while the other is free to magnetize parallel or anti-parallel to it (controlled by inducing a magnetic field in it by passing a large current through a nearby conducting material). When both magnetic films are oriented parallel the tunnel resistance through the device is lower than when anti-parallel (due to the effect of spin-transfer torque). These devices can achieve memory windows as high as $HRS/LRS \approx 1000$, but usually have higher current density in both states than FTJs and also require rather large current pulses to write the magnetic state [5, 6].

3.4.3 Phase-change memory

Lastly, PCM stores data by changing the crystal phase of a material in a junction. When fresh, the material is in a crystalline (low resistance) state. By passing sufficient current through a heater, the phase change material is melted and quickly quenched

by passing a large current through it. This forces the material to remain amourphous and have a higher resistance, usually $HRS/LRS \approx 1000$. To return to low resistance state, a moderate current pulse is passed through the material, melting it, and held there long enough melt and facilitate crystalization of the material. Though typical current density in both states are lower than MTJ, they are still not as low as FTJ and, like MTJ, the PCM requires rather large currents to write [33]. Therefore, it is not ideal for low-power computing.

Chapter 4

Analysis of M1-Fe-M2 Structure

At its core, an FTJ is a modified MIM so it's logical to start by examining an MIM and modifying our analysis to reflect the different material properties. All band structure and current density figures in this section, except Figure 4.3, are simulated results performed in this work using a custom python program included in Appendix A.

4.1 Band structure in the absence of polarization field

An MIM with non-ferroelectric insulator has no internal polarization field and therefore returns to the same zero-field band structure, shown in Figure 4.1, after any external field application (for $d = 2$ nm thick insulator with $E_a = 2$ eV and metals having $\chi_1 = 4.08$ eV, $\chi_2 = 4.85$ eV). The thermionic emission current, from electrons which gain sufficient energy from phonon interaction to surmount the barrier, of such a device is calculated using Equation 4.1, and for our example is roughly 1e-41 A/cm^2 (practically "0" current) at 0.5V. Since this MIM has an insulator with thickness less than the penetration distance of the electron wave, an appreciable current occurs due to Fowler-Nordheim tunneling, J_{tun}, when electrons are able to quantum-mechanically tunnel through the triangular or trapezoidal energy barrier. This current, calculated using Equation 4.2, is shown in Figure 4.2 and is the main current contributing mechanism for this type of device (7e4 A/cm^2 at 0.5V for this example). Like most MIMs, this device's tunnel current density has a separation around zero applied voltage

where the current becomes "zero" and also has a slight asymmetry between curves under negative and positive applied voltage.

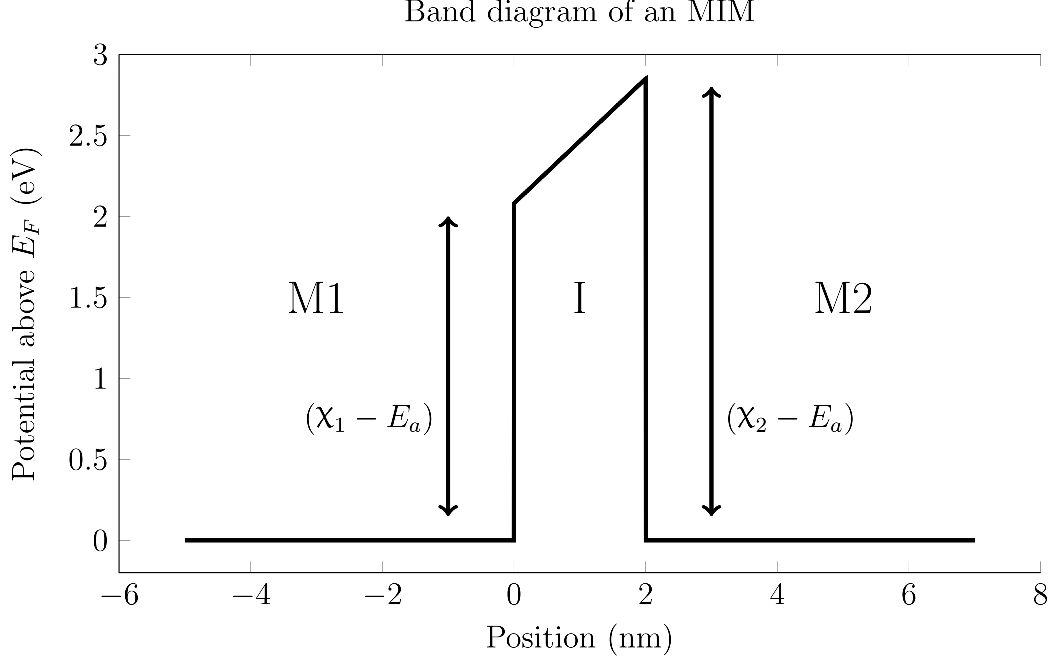


Figure 4.1: The energy band diagram of an MIM with a 2 nm thick insulator with $E_a = 2$ eV and metals having $\chi_1 = 4.08$ eV, $\chi_2 = 4.85$ eV, normalized to the fermi energy.

$$J_{th} = A_{th}T^2 \exp(-\psi'/k_BT)(1 - \exp(-qV/k_BT))$$
$$\text{where,} \quad A_{th} = \frac{4\pi m^* q k_B^2}{h^3} \tag{4.1}$$

$$J_{tun} = J_0 \left\{ \bar{\psi} \exp\left(-A_{tun}\sqrt{\bar{\psi}}\right) - (\bar{\psi} + qV) \exp\left(-A_{tun}\sqrt{\bar{\psi} + qV}\right) \right\}$$
$$J_0 = \frac{q}{2\pi h(\beta d)^2} \quad \bar{\psi} = \frac{1}{d}\int_0^d \psi(x)dx, \text{ is mean barrier height} \tag{4.2}$$
$$A_{tun} = \frac{4\pi\beta d\sqrt{2m^*}}{h} \quad \beta \text{ is a correction factor, usually 1}$$

4.2 Band structure under polarization

When the first FTJ was discovered by Contreras et. al in 2002, $BaTiO_3$ ferroelectric with $SrRuO_3$ and PZT as electrodes, its operation went unexplained and was origi-

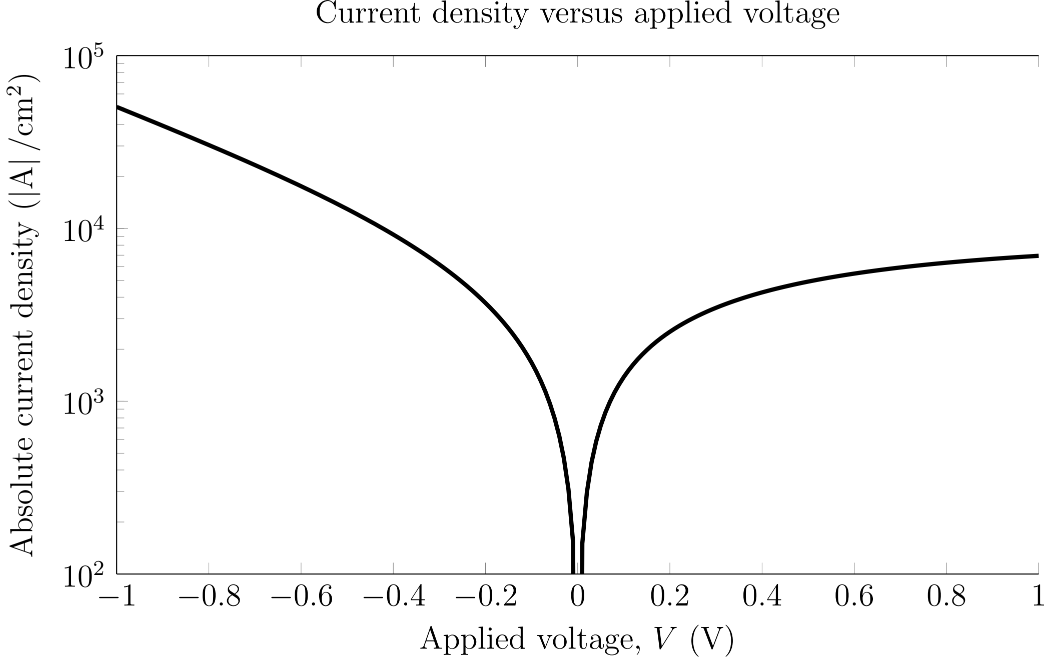


Figure 4.2: The Fowler-Nordheim tunneling current of an MIM with material properties listed in Section 4.1.

nally published purely as a dissemination of experimental results. [3] It was not until 2005 that the phenomenon was explained by Zhuravlev et. al, who postulated that the ferroelectric polarization, P, induces equal and opposite surface charge densities, $\sigma_p = -P$, which exist in infinitessimally thin sheets at the interfaces of each contact and the ferroelectric. Shown in Figure 4.3, the surface charges must then be locally screened by each electrode, thereby inducing screening charge densities, σ_s, as given by Equation 4.3, with screening lengths (or debye lengths) in metal 1, σ_1, and metal 2, σ_2, given by Equation 4.4. Finally, these charges modify the zero-polarization band structure with additional potentials within both electrodes and the ferroelectric, as given by Equation 4.5 and shown in Figure 4.3 by Zhuravlev et. al [4]. Though not explicitly given by the group, it is clear that the additional potential contribution within the ferroelectric is given by Equation 4.6.

$$\sigma_s = \frac{Pd}{\varepsilon_{\mathrm{f}}(\delta_1 + \delta_2) + d} \tag{4.3}$$

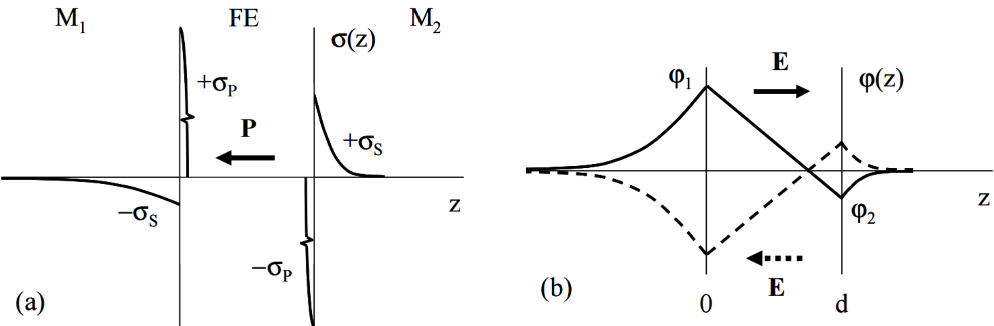


Figure 4.3: (a) Diagram of charge densities created for left polarized ferroelectric and (b) corresponding generated potentials across an FTJ, having electrodes with dissimilar screening lengths, from Zhuravlev et. al [4].

$$\delta_x = L_D = \sqrt{\frac{\varepsilon k_B T}{q^2 N_x}} \text{ where, for a metal } N_x = c_0 \tag{4.4}$$

$$\psi(x) = \begin{cases} \dfrac{\sigma_s \delta_1 \exp(-|x|/\delta_1)}{\varepsilon_0}, & x \leq 0 \\ -\dfrac{\sigma_s \delta_2 \exp(-|x-d|/\delta_2)}{\varepsilon_0}, & d \leq x \end{cases} \tag{4.5}$$

$$\psi(x) = \left\{ \psi(0) + (\psi(d) - \psi(0)) \left(\frac{x}{d}\right), \qquad 0 < x < d \right. \tag{4.6}$$

It's clear to see already that for electrodes with dissimilar screening lengths there will be a non-zero depolarizing field, because of the reduced field contribution from charges further from the interface, and there will be a difference in average potential barriers for polarization towards M1 versus M2. Finally, integrating all the above contributions from polarization-induced charges to the zero-field band structure, an FTJ with material properties consistent with those used in Section 4.1 (and assuming $P = 10\mu$ C/cm^2, $\varepsilon_f = 40\varepsilon_0$, $\delta_1 = 0.06$ nm, and $\delta_2 = 0.4$ nm) would exhibit band structures as shown in Figure 4.4.

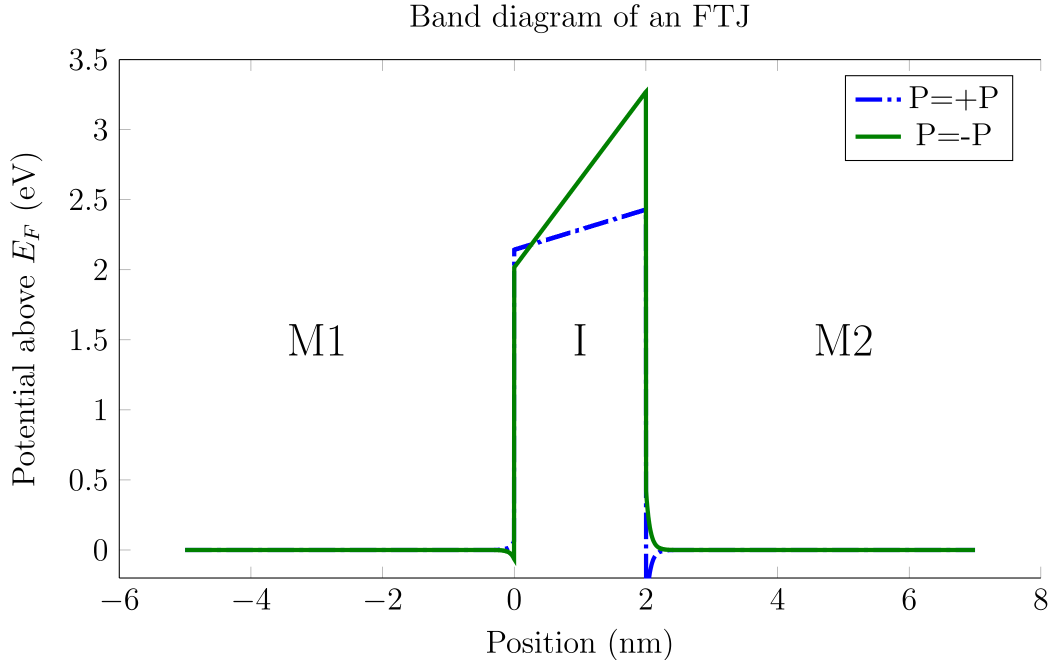


Figure 4.4: The energy band diagrams, at $V = 0$, of an FTJ with material properties given in Section 4.2, for positive (towards M1) and negative (towards M2) polarization.

4.3 Extraction of tunnel Current and (by extension) resistance states

The tunnel current density for each state (positive polarization and negative polarization), is calculated again using Equation 4.2, but now requires the additional potential contributions of equations 4.5 and 4.6. For this case, positive polarization (towards M1) has a lower barrier than negative polarization (towards M2), so we will term each state the LRS and HRS, respectively. The corresponding current density curves are shown in Figure 4.5, and is representative of an FTJ having Al as M1, Al:HfO_2 as ferroelectric, and degenerately doped ($N_a = 1 \times 10^{20}$ cm^{-}3) p+ Si as M2. Since the resistivity is given by $\rho = E/J = V/(dJ)$, the resistance states would correspond directly to the current densities of each state. Lastly, the memory window is a ratio of the device's resistivity (at the same applied voltage, usually the read voltage, v_{dda}) in each state, $HRS/LRS = \rho_{\text{HRS}}/\rho_{\text{LRS}} = J_{\text{LRS}}/J_{\text{HRS}}$.

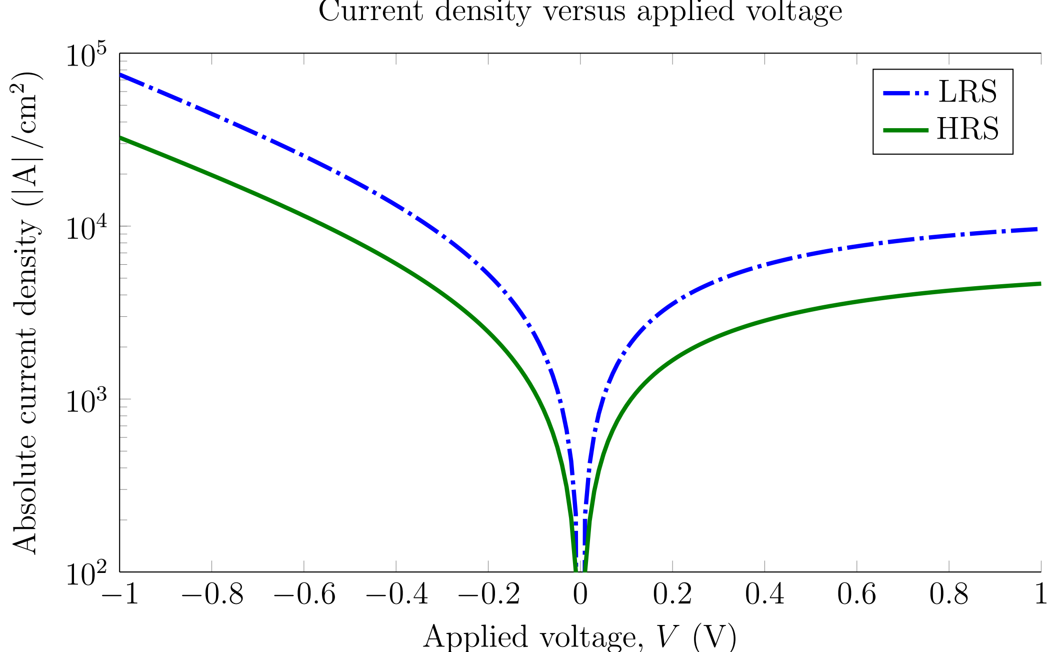


Figure 4.5: The Fowler-Nordheim tunneling current of an FTJ with material properties consistent with those used in Figure 4.4, showing a memory window $HRS/LRS \approx 2.3$.

Chapter 5

Design of Ferroelectric HfO_2-based FTJs and Integration with CMOS Process

For this design, a twin-well polysilicon-gate planar CMOS process flow by Lynn Fuller [34] was modified by the addition of required steps for deposition and patterning of the ferroelectric. If being fabricated at RIT, the author recommends keeping designed CMOS devices at a minimum length of 2 μm to achieve highest yield, though adaptation of these processes to another process with smaller minimum feature size and varying gate material would be relatively straight-forward.

5.1 FTJ design

In an effort to keep the FTJ fully CMOS-compatible the electrodes were chosen to be Al and p- doped Si, as shown to be effective in Section 4.3. Each device is designed as a crossbar such that the area of an FTJ is the width of the p- electrode times the width of the Al electrode. This way, a larger array of FTJ devices are designed as horizontal p- lines (in "oxide" mask level) and vertical Al lines.

In order to predict and optimize FTJ performance, all equations from Section 4 were integrated into a flexible python program with user-interface for input of relevant material properties. The code for this program is given in Appendix A.

Interestingly, extracting memory window as a function of increasing screening length in the poor metal (assuming the other metal has a screening length of $\delta_1 =$

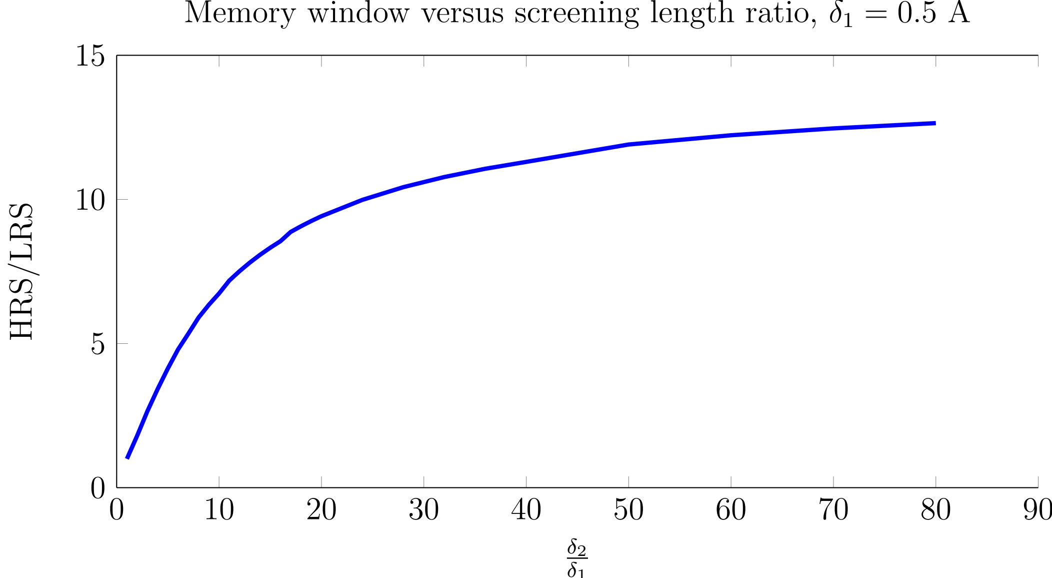


Figure 5.1: Simulated HRS/LRS increases with larger screening length ratio before plateauing around $\frac{\delta_2}{\delta_1} \approx 60$. For an Al/Al:$HfO_2$/p+ Si FTJ with 2 nm ferroelectric.

0.5 Å), as shown in Figure 5.1, shows a saturation starting at around $60 \approx \delta_2/\delta_1$ (corresponding to $\delta_2 = 3$ nm, p+ Si $N_a = 2 \times 10^{18}$ cm^{-}3).

Even more interestingly, varying the screening length in the "good" metal (while keeping the poor metal $\delta_2 = 3$ nm), as shown in figure 5.2, yields two important conclusions. First, a metal with incredibly high carrier concentration ($\delta_1 < 0.05$Å) would actually cause a sharp decay in memory window, owing likely to the total screening of the depolarizing field at that interface and (by extension) a removal of its positive effect on introducing dissimilar barriers. Second, the memory window improves with increased screening length but reaches a maximum at $\delta_1/\delta_2 \approx 0.38$. This is likely due to increasing total available charges to contribute to depolarizing field until maximizing once charges are located too far away from the interface to contribute (as is the case in materials with a larger screening length). The screening length of the Al electrode could be increased by interface defects, oxide charges, or material impurities. The screening length of AlSi (10% Si) would also be larger than pure Al and approach the ideal value ($\delta_1 = 1.14$ nm).

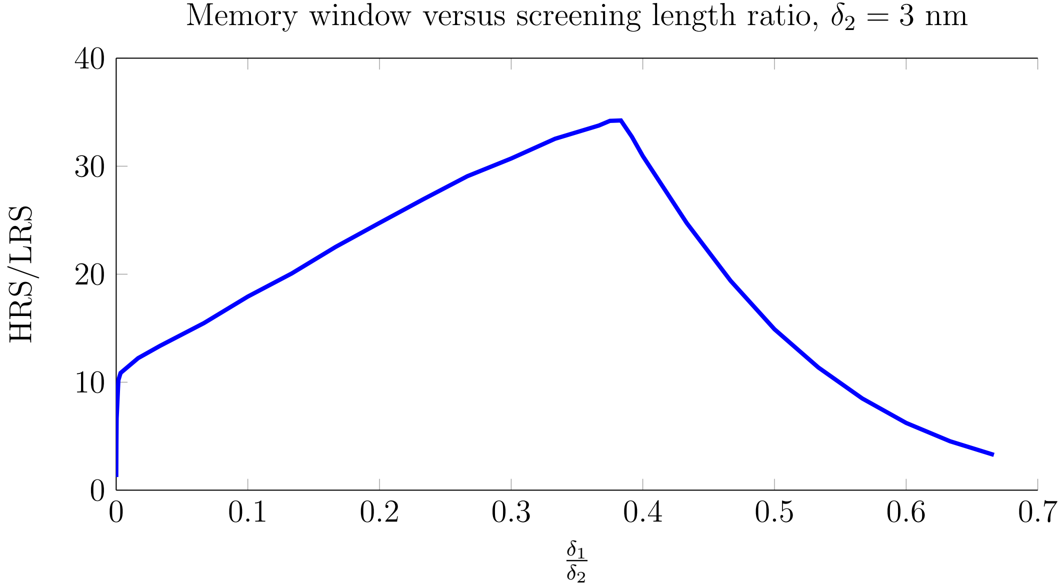


Figure 5.2: Simulated HRS/LRS for increasing δ_1, showing a maximum. For an Al/Al:HfO_2/p+ Si FTJ with 2 nm ferroelectric.

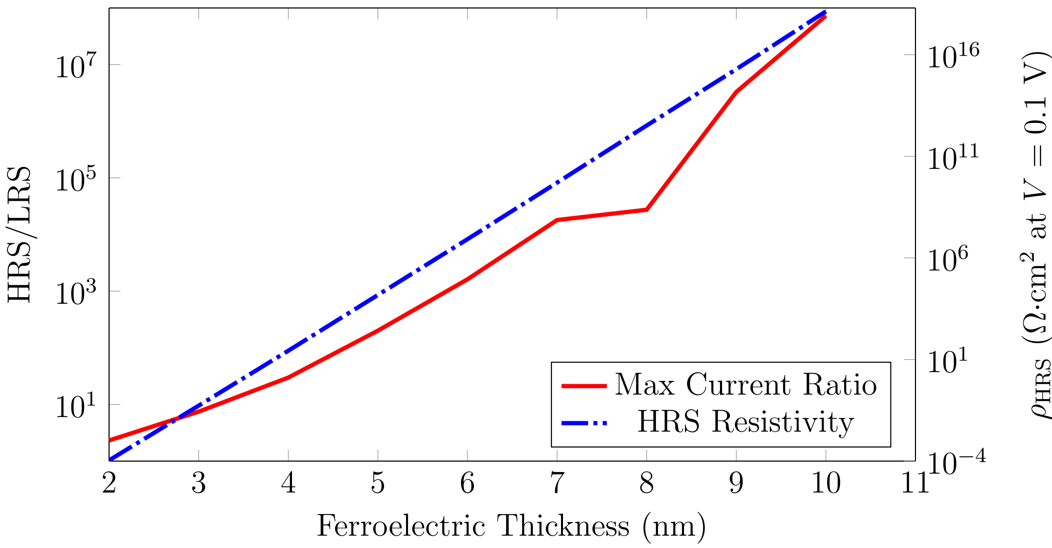


Figure 5.3: Simulated HRS/LRS and HRS resistivity for an Al/Al:HfO_2/p+ Si FTJ with varying ferroelectric thickness.

5.2 State of the art FTJs

For this study, it is best to assume the Al electrode will behave non-optimally (having no impurities) and therefore, the FTJ design for the Al/Al:HfO_2/p-Si device presented in this work has material properties $\delta_1 = 0.06$ nm, $\chi_1 = 4.08$ eV, $\varepsilon_{\mathrm{f}} = 40\varepsilon_0$, $E_a = 2$ eV, $P_r = 15\mu\mathrm{C/cm}^2$, $d = 2, 3,$ or 5, $m^* = 0.11 m_e$, $\delta_2 = 3$ nm, and $\chi_2 = 4.85$ eV. The Al:HfO_2 ferroelectric is adapted from the process used by Polakowski et. Al [35] and is assumed to behave with similar speed, polarization, and endurance performance. A comparison of this device to other state of the art FTJs is shown in Table 5.1. Importantly, the small coercive electric field ($\mathcal{E}_c$) of HfO_2-based ferroelectrics leads to a lower required program voltage (the coercive voltage, V_c), and therefore lower power consumption, compared to $BaTiO_3$ and $BiFeO_3$ FTJs. Speed performance between FTJs are mostly similar, though endurance of HfO_2-based devices is higher than that of $BiFeO_3$ devices. Most importantly, the Al/Al:HfO_2/p-Si FTJ can be designed with either a 2, 3, or 5 nm ferroelectric layer; leading to performance with either lower high-state resistivity (ρ_{HRS}) than all other FTJs (enabling high speed performance by minimizing $\tau = RC$) while only exhibiting moderate power density (Pd) with a 2 nm ferroelectric or very high ρ_{HRS} with a potentially huge memory window of 5×10^5 and extremely low power performance (2.5 fJ for each 500 nm^2 device) with a 5 nm ferroelectric (more ideal for NMC applications where a large memory window permits more memory states). At a more moderate performance optimization, a 3 nm ferroelectric in the Al/Al:HfO_2/p-Si FTJ yields a memory window similar to that of the $BaTiO_3$ FTJ reported by Abuwasib et. Al [9] but achieves lower power consumption by a factor of $\approx1\times10^{-3}$. All three of these simulation results indicate that Al:HfO_2-based FTJs are superior to both alternative technologies and FTJs using competing ferroelectrics for both neuromorphic computing and nonvolatile memory applications, excelling at low-power high-speed performance.

Researcher [cite]	Device	Materials	$\mathcal{E}_c$ (V/cm)	Area	CMOS?
Chanthbouala et. Al [36]	FTJ	Co/$BaTiO_3$/LSMO	1×10^7	0.096	No
Abuwasib et. Al [9]	FTJ	Co/$BaTiO_3$/LSMO	1×10^7	0.303	No
Boyn et. Al [12]	FTJ	Co/$BiFeO_3$/CCMO	3.3×10^6	0.125	No
Mueller, Schroeder et. Al [37, 38]	MIM	Pt/TiN/Si-HfO_2/TiN	1×10^5	10000	Yes
Polakowski et. Al [35]	MIM	TiN/Al:HfO_2/TiN	1×10^5	50	Yes
This Work (Based on Simulations)	FTJ	Al/Al:HfO_2/p-Si	1×10^5	0.25	Yes

Research	d (nm)	ρ_{HRS} ($\Omega\cdot$cm^2)	HRS/LRS	P_r	Speed	Endurance	V_c	Pd (W/cm^2)
[36]	2	4.8×10^{-2}	300	-	10 ns	-	2.0	83.3
[9]	2	4.8×10^{-3}	60	-	-	-	2.0	823
[12]	4.6	5×10^{-2}	1000	100	100 ns	4×10^6	1.5	45
[37, 38]	10	-	-	17	10 ns	1×10^{10}	1.0	
[35]	12	-	-	15	not rep.	2×10^9	1.2	
This Work	2	1.8×10^{-4}	6.2	15	10 ns	2×10^9	0.2	222
	3	1.54×10^{-1}	90				0.3	0.584
	5	2.3×10^5	500000				0.5	1×10^{-6}

Table 5.1: Tables comparing relevant performance data for this research work to state of the art FTJs. LSMO stands for $La_xSr_{1-x}MnO_3$ and CCMO is $Ca_{0.96}Ce_{0.04}MnO_3$. Area units are μm^2. Pd is surface power density and P_r is remanent polarization in (μC/cm^2).

5.3 Designed CMOS-process with FTJ-fabrication steps

Step Number	Step Code	Step Description	Tool	Time (hrs)
1	OX05	pad oxide 500 Å, Tube 4, 45 min at 1000C	Bruce Furnace 4	3
2	CV02	1500 ÅSi3N4 LPCVD Deposition, 30 min at 810C	LPCVD Nitride	4
3	PH03	level 1- Oxide - Clear Field	ASML & SSI	1
4	ET29	Plasma etch Nitride, 1500 Åtarget	LAM 490	0.3
5	ET07	ash all photoresist	Gasonics Asher	0.15
6	CL01	RCA clean	RCA Bench	0.85
7	OX04	First Oxide Tube 1, 3650 ÅBruce 1 Recipe 330, 55 mins at 1000C	Bruce Furnace 1	2.65
8	ET06	Etch Oxide, 3650 Åtarget, BOE 7to1 for 3.6 min	7to1 BOE	0.25
9	OX04	2nd Oxide Tube 1, 3650 Å, Bruce 1 Recipe 330, 55 mins at 1000C	Bruce Furnace 1	2.65
10	ET19	Nitride etch, 30s dip 5:1 BHF, 20 min Hot Phosphoric Acid 175C	Hot Phos Bench	1
11	PH03	level 2 Nwell - Dark Field	ASML & SSI	1
12	IM01	Cover bottom of wafer: Nwell top, 3E13, P31, 170 KeV	Varian Implanter	2
13	ET07	ash all photoresist	Gasonics Asher	0.15
14	PH03	level 3 – Pwell - dark field (or clear field Nwell mask with neg resist)	ASML & SSI	1
15	IM01	Cover top of wafer, Pwell bottom, 8E13, B11, 80 KeV	Varian Implanter	2
16	ET07	ash all photoresist	Gasonics Asher	1
17	OX06	Well Drive, Tube 1 Recipe 11, 480 min at 1100C	Bruce Furnace 1	8
18	PH03	level 4 - NMOS Vt - dark field (or clear field Nwell mask with neg resist)	ASML & SSI	1

Step Number	Step Code	Step Description	Tool	Time (hrs)
19	IM01	NMOS Vt, 7.95e12, P31, 60KeV	Varian Implanter	6
20	ET07	ash all photoresist	Gasonics Asher	0.15
21	PH03	level 5 – PMOS VT adjust - nwell level - dark field	ASML & SSI	1
22	IM01	PMOS Vt, 3.02e12, B11, 30 KeV	Varian Implanter	6
23	ET07	ash all photoresist	Gasonics Asher	0.15
24	ET06	etch 500 Å pad oxide, 50:1 H_2O:HF (3.6 mins)	50:1 HF Etch	0.25
25	CL01	pre-gate oxide RCA clean (with extra etch, next step)	RCA Bench	0.85
26	ET06	etch native oxide (extra 30s 50:1 HF dip)	RCA Bench	0.1
27	OX06	100 Å dry (N_2O) gate oxide, Bruce Tube 4, Recipe 213, 60 mins at 900C	Bruce Furnace 4	3
28	CV01	LPCVD poly deposition, 4000 Å	LPCVD Polysilicon	4
29	PH03	level 6 – poly gate - clear field	ASML & SSI	1
30	ET08	poly gate plasma etch, 4000 Åtarget, FACPOLY recipe	Drytek Quad	0.5
31	ET07	ash all photoresist	Gasonics Asher	0.15
32	CL01	RCA clean	RCA Bench	0.85
33	OX05	poly re-ox, 500 Å, Bruce Tube 4 Recipe 250	Bruce Furnace 4	3
34	PH03	level 7 - p-LDD - dark field	ASML & SSI	1
35	IM01	PMOS LDD, 4E13, B11, 50 KeV	Varian Implanter	4
36	ET07	ash all photoresist	Gasonics Asher	0.15

Step Number	Step Code	Step Description	Tool	Time (hrs)
37	PH03	level 8 – n-LDD - dark field	ASML & SSI	1
38	IM01	PMOS LDD, 4E13, P31, 60 KeV	Varian Implanter	4
39	ET07	ash all photoresist	Gasonics Asher	0.15
40	CL01	RCA clean	RCA Bench	0.85
41	CV02	LPCVD nitride spacer 3500 Å	LPCVD Nitride	4
42	ET39	sidewall spacer etch, 3500 Åtarget, FACSPCR 30sccm SF6 and CVF3 (125nm/min)	Drytek Quad	0.5
43	PH03	level 9 - N+D/S - dark field	ASML & SSI	1
44	IM01	N+D/S, 4E15, P31, 60 KeV	Varian Implanter	2
45	ET07	ash all photoresist	Gasonics Asher	0.15
46	PH03	level 10 - P+ D/S - Pimp - Dark Field	ASML & SSI	1
47	IM01	P+D/S, 4E15, B11, 50 KeV	Varian Implanter	2
47(2)	IM01	Cover bottom of wafer: P+ top 4E15, B11, 50 KeV	Varian Implanter	2
47(2)	IM01	Cover top half of wafer: N+ bottom 4E15, P31, 60 KeV	Varian Implanter	2
48	ET07	ash all photoresist	Gasonics Asher	0.15
49	CL01	RCA clean	RCA Bench	0.85
50	OX08	DS Anneal, Bruce 2, 3, Recipe 284, 45 min at 1000C	Bruce Furnace 2	3
51	ET06	silicide pad ox (500A) etch, 50:1 H2O HF	50:1 HF Etch	0.25

Step Number	Step Code	Step Description	Tool	Time (hrs)
52	ME03	HF dip & Ti Sputter	CVC601	3
53	RT01	RTP 1 min, 650C	RTP	1
54	ET11	Unreacted Ti Etch	Etch Bench	1
55	RT02	RTP 1 min,800C	RTP	1
56	CV03	TEOS, P-5000, 4000 ÅOxide	P5000 TEOS Ch A	0.5
57	PH03	Photoresist mask to remove TEOS for ALD HfO2, Thick Resist COAT-FAC and DEVFAC Recipes - FEHfO2 Level - Dark Field	ASML & SSI	1
58	ET06	TEOS Etch for HfO2 area FACCUT, follow with 50:1 HF dip	Drytek Quad	0.5
59	ET07	Solvent Strip or Ash	Solvent Strip Bench	0.5
60	CV33	ALD HfO2 Deposition w/ TiN	ALD	4
61	RT02	RTP 1 min,800C	RTP	1
62	PH03	(optional) Half wafer protect	Karl Suss Contact Aligner Stepper	0.5
63	ET06	TiN wet etch with RCA 1 NH4OH:H2O2:H2O = 1:2:5 (APM) solution at 60 C. (1nm/s, [39])	Hot Plate with Pyrex Dish	1

Step Number	Step Code	Step Description	Tool	Time (hrs)
64	ET07	(optional) Solvent Strip or Ash	Solvent Strip Bench	0.5
65	PH03	Photoresist mask to remove HfO2 if not selective growth (Negative Resist) - FEHfO2 Level - Dark Field	ASML & SSI	1
66	ET06	HfO2 etch, 50:1 H2O:HF appx. 97s for 3nm HfO2, assuming 1:10 HfO2:SiO2 selectivity. [40]	50:1 HF Etch	0.25
67	ET07	Solvent Strip or Ash	Gasonics Asher	0.15
68	PH03	level 11 - CC, Thick Resist COATFAC and DEVFAC Recipes - Cont level - dark field	ASML & SSI	1
69	ET06	CC etch, FACCUT, 200 W, 100 mT, 50 sccm CHF3, 10 sccm CF4, 100 sccm Ar	Drytek Quad	0.5
70	ET07	ash all photoresist	Gasonics Asher	0.15
71	CL01	RCA clean	RCA Bench	0.85
72	ME01	Aluminum Sputter 7500 Å	CVC601	1
73	PH03	level 12 - Metal1, Thick resist, COATMTL and DEVMTL recipes, clear field	ASML & SSI	1
74	ET15	plasma 125W, Al Etch, BCl, Cl2, Chloroform, Target 7500 Å	LAM4600	1.5

Step Number	Step Code	Step Description	Tool	Time (hrs)
75	ET07	ash all photoresist	Gasonics Asher	0.15
76	CV03	TEOS, P-5000, 4000 ÅOxide	P5000 TEOS Ch A	0.5
77	PH03	Via1 - dark field	ASML & SSI	1
78	ET26	Via Etch	Drytek Quad	0.5
79	ME01	Al Deposition	CVC601	1
80	PH03	Metal 2 - clear field	ASML & SSI	1
81	ET15	plasma 125W, Al Etch, BCl, Cl2, Chloroform, Target 7500 Å	LAM4600	1.5
82	ET07	ash all photoresist	Gasonics Asher	0.15
83	CV03	TEOS, P-5000, 4000 ÅOxide	P5000 TEOS Ch A	0.5
84	PH03	Via2 - dark field	ASML & SSI	1
85	ET26	Via Etch	Drytek Quad	0.5

Step Number	Step Code	Step Description	Tool	Time (hrs)
86	ME01	Al Deposition	CVC601	1
87	PH03	Metal 3 - clear field	ASML & SSI	1
88	ET15	plasma 125W, Al Etch, BCl, Cl2, Chloroform, Target 7500 Å	LAM4600	1.5
89	ET07	ash all photoresist	Gasonics Asher	0.15
90	CV03	TEOS, P-5000, 4000 ÅOxide	P5000 TEOS Ch A	0.5
91	PH03	Via3 - dark field	ASML & SSI	1
92	ET26	Via Etch	Drytek Quad	0.5
93	ME01	Al Deposition	CVC601	1
94	PH03	Metal 4 - clear field	ASML & SSI	1
95	ET15	plasma 125W, Al Etch, BCl, Cl2, Chloroform, Target 7500 Å	LAM4600	1.5
96	ET07	ash all photoresist	Gasonics Asher	0.15
97	SI01	sinter	Bruce	2

To minimize additional process steps, the p-Si electrode is defined by the pseudo-STI field oxide growth (steps 3-9) which also defines the active areas of transistors. This process does exhibit some feature thinning, so a 2 μm line on mask (transferred to nitride) yields approximately a 250 nm line width of exposed silicon for the electrode. The p- doping is introduced during the implant for PMOS-device source/drain, step 47. A modified version of step 47, called step 47(2), can be used to study the affect of n-doping instead of p-doping the lower (M2) electrode, but cannot be used with full CMOS integration. To confine Al:HfO_2 to FTJ areas, the same tetra-ethyl orthosilicate (TEOS) oxide used as an interlevel dielectric (ILD) below each metal layer is deposited, step 56, and patterned, step 57, to open windows to FTJ areas before Al:HfO_2 deposition by ALD, step 60. The Al:HfO_2 is also capped in-situ with TiN before being annealed in RTP (to form the ferroelectric state), step 61. The TiN must then be removed, since it is conducting and would cause device shorts, and is selectively removed, in step 63, by the SC1 chemistry used in a standard RCA clean (at a rate of 1nm/s), as shown by Liu et. al [39]. This must be done in a pyrex dish on a hot plate in a wet etch bench, not in the RCA bench, to avoid contamination. Finally, the same mask used to open windows in the TEOS can be used with negative resist, in step 65, to create a soft mask protecting the FTJ areas and then etch the Al:HfO_2, in step 66, from unwanted areas (though this is not necessary). Having already deposited the TEOS oxide, the contact cuts can be etched, step 69, and metal 1 (Al) deposited, step 72, and patterned, steps 73 and 74. The metal 1 mask is therefore also defining the Al electrodes for the FTJs! In whole, the only extra steps for FTJ-fabrication are the TEOS oxide etch, ferroelectric deposition and anneal, and TiN/ferroelectric etching only requiring one extra mask. A shortened version of this process, with only the required steps to fabricate FTJ devices, is given in Appendix B.

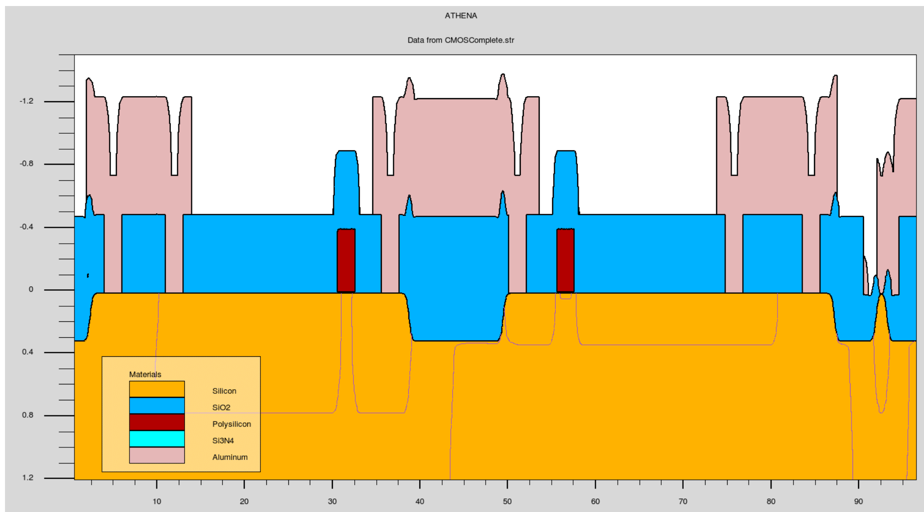


Figure 5.4: Athena simulation of CMOS devices tuned for low threshold voltages (left) and FTJ device (right).

5.4 Process simulation

Silvaco is a semiconductor simulation tool used often in both academic and industry research. It has modules for process simulation, *Athena*, and electrical simulation of a simulated process, *Atlas*; though electrical simulations are more suited to transistor performance and related connections. In order to verify the proposed process design, from Section 5.3, it was simulated using *Athena*. The code is included in Appendix C and important figures are shown in this section. Importantly, the CMOS devices are shown in Figure 5.4, showing appropriate wells and junction depths for source/drain. The window opened in TEOS is shown to be appropriate for isolating ferroelectric to desired areas, shown in Figure 5.5 with SiO_2 substituted for HfO_2 since Athena does not have it. This simulation platform was also used to fine tune the use of wet etch before HfO_2 deposition to accurately reach 250 nm device width, shown in Figure 5.6.

For implementation within another process node or with transistors of differing threshold voltage, *Athena* simulation should be repeated with corrected well, threshold adjust, and source/drain implants. Surface doping of the FTJ region should be extracted and used for recalculation of δ_2 and corresponding memory window.

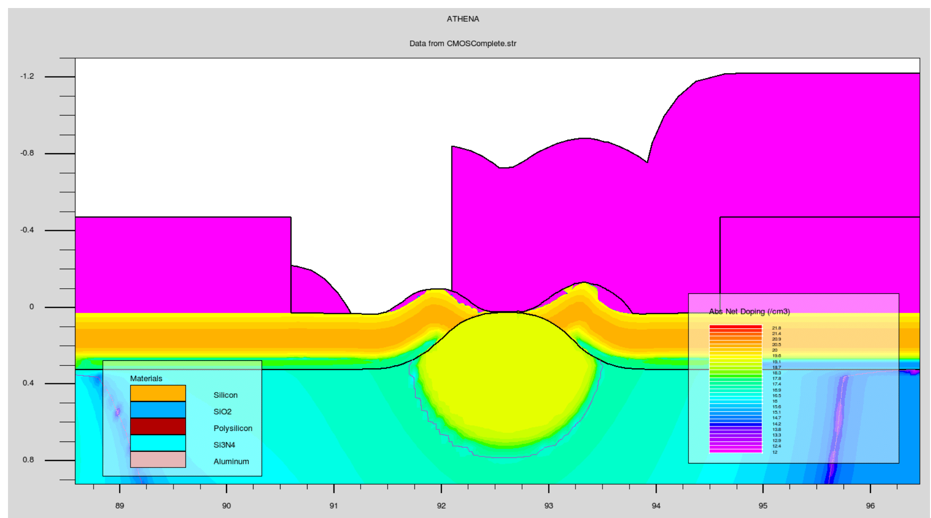


Figure 5.5: Athena simulation of FTJ device (SiO2 substitued for ferroelectric).

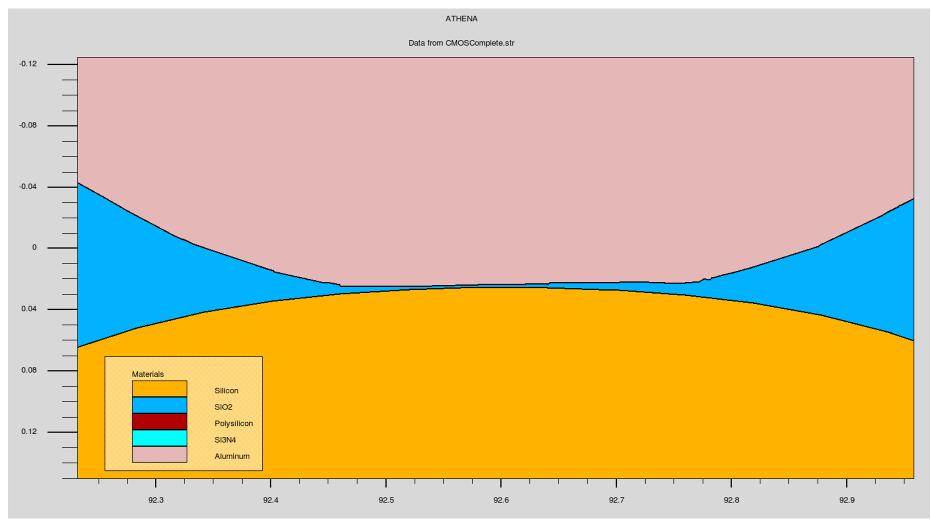


Figure 5.6: Zoom of FTJ device showing ≈ 250 nm device width.

Chapter 6

System Design and Simulations for Digital Memory Applications

The designs of all circuits were performed in *Cadence Virtuoso* using a 45 nm CMOS PDK. The design rules of this PDK are consistent with those required for the 2 um process to be performed at RIT but allowed for easier use of the DRC and LVS tools native to this PDK. Additionally, this allowed for performance simulation representative of implementation with fairly modern devices. When implemented in the 2 um CMOS process at RIT, the mask file from *Virtuoso* was simply scaled up (from 45 nm to 2 um, a factor of 44.44) before mask printing.

6.1 Read/Write scheme

When writing an FTJ, the bias applied across it must meet or exceed the coercive voltage, V_c, in order to flip the polarization to the desired direction (over any reasonable amount of time). While reading, the bias must be less than V_c in order to prevent state disturbance. Let's take, for example, an FTJ with $V_c = 0.5$ V. As shown in Figure 6.1, these schemes would work to write the HRS and LRS as shown and to read the device (since read will always be performed in the same direction).

However, FTJs are often (if not always) designed in an array (like most memory). Within this array, the positive terminals are connected to rows and the negative terminals to columns, as shown in Figure 6.2. Using the address scheme from before,

Write HRS
V=0.6V p n V=0V

Read
V=0.4V p n V=0V

Write LRS
V=0V p n V=0.6V

Figure 6.1: An address scheme which, though appropriate for a stand-alone device, would be inappropriate for devices in an array.

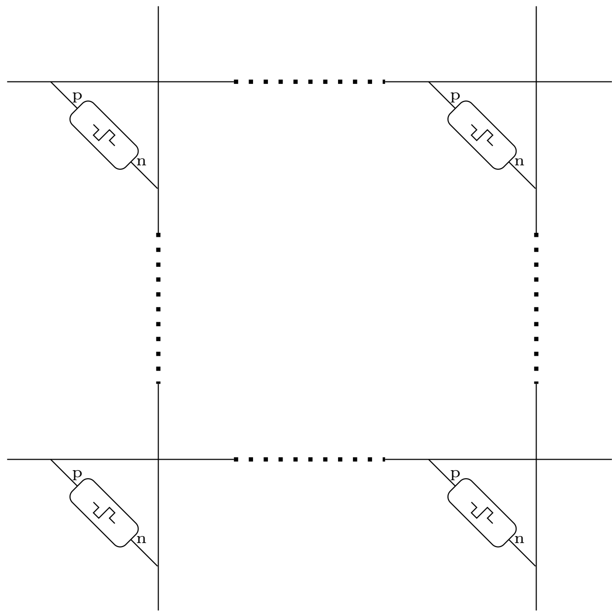


Figure 6.2: A simple schematic showing the typical connectivity of FTJ devices in an array, for both memory or neuromorphic logic applications. Lines and columns only connect through FTJ devices and do not connect at intersections. Dotted lines indicate an arbitrary number of repeated lines and columns.

other non-addressed devices in that row or column would experience the same bias as the addressed device!

Ultimately, the best solution to this will be one of two options and will be up to the system designer. The first option is to have rails centered around ground such that the write rails are (for our example) V_{DD}=0.3 V and V_{SS}=-0.3 V, read rails are v_{dda}=0.2V and v_{ssa}=-0.2V and whenever a column or row is not being addressed it should be grounded. That way, the write scheme follows Figure 6.3 for addressed devices and non-addressed devices, shown in Figure 6.4 (in same row), are not disturbed during

Figure 6.3: An address scheme appropriate for FTJs in an array.

Figure 6.4: Non-addressed devices in the same row, for various write/read states. Non-addressed devices in the same column would experience the opposite bias. In this way, these devices will not be disturbed.

read or write.

Though this address choice does allow non-addressed devices to stay at ground, preventing current flow through the FTJ devices to the bulk silicon (which is typically grounded) it does require CMOS devices with near-zero threshold voltage. If this is undesirable, another option is to shift all rails by $+V_{\mathrm{DD}}$, leaving the write rail low at 0V but requiring all non-addressed lines to be held (for our example) at 0.3V. Ultimately, this is the decision of the system designer and depends on related process constraints.

6.2 Linear resistance change simulation

The most simple way to model the changing resistance of an FTJ is to first calculate, using equations from Chapter 4, the resistance of each state (at the read bias) using material properties appropriate for the chosen device. The model written in *Verilog-A*, given in Appendix D.1.1, assumes that the resistance would change linearly over some chosen "transition time" while biased above $|V_c|$ towards the corresponding

state and saturate once reaching the resistance of that state. Simulation results using CMOS devices from the 45nm PDK of *Cadence Virtuoso* (used for ease of DRC and LVS, and for results more representative of a modern CMOS process) are shown in Figure 6.10 and are useful for digital memory applications, with write times of ≈ 0.6 ns for HRS and ≈ 0.3 ns for LRS and read times of ≈ 10 ns for HRS and ≈ 4 ns for LRS. However, brain-inspired computing systems, which require precise control as the device transitions from one state to the other, need a more complicated simulation which models polarization change versus time and corresponding resistance.

6.3 Timing-based simulation

Working with data for polarization versus program time from Schroeder et. al [41], piece-wise polynomial models were fit to the data and used to direct further study of the general phenomena of timing in ferroelectrics. Some modeled curves are given in Figure 6.5 and the equation and relevant model fit parameters are given by Equation 6.1. Though these curves suggest switching times close to 1 μs, the group posits that this data was influenced by the test setup delay and that realistic switching times are in the 1 ns range [41].

$$
\begin{aligned}
2Pr(V,t) &= MIN\begin{pmatrix} MIN(13.071 * V^{2.929}, 6.339 * V + 27.357) \\ , MAX(MIN(D + E * \ln(t), MAX(A + B\log(t) + C\log^2(t), 0)), 0) \end{pmatrix} \\
A &= MAX(445.4V - 416.102, 22V) \\
B &= MAX(118.125V - 112.071, 5.8V) \\
C &= MAX(7.782V - 7.525, 0.26V) \\
D &= MIN(9.904V + 17.865, 19.375V^2 - 6.3V + 1.4) \\
E &= MAX(9.105V - 5.152 - 3.387V^2, 0.217)
\end{aligned}
\tag{6.1}
$$

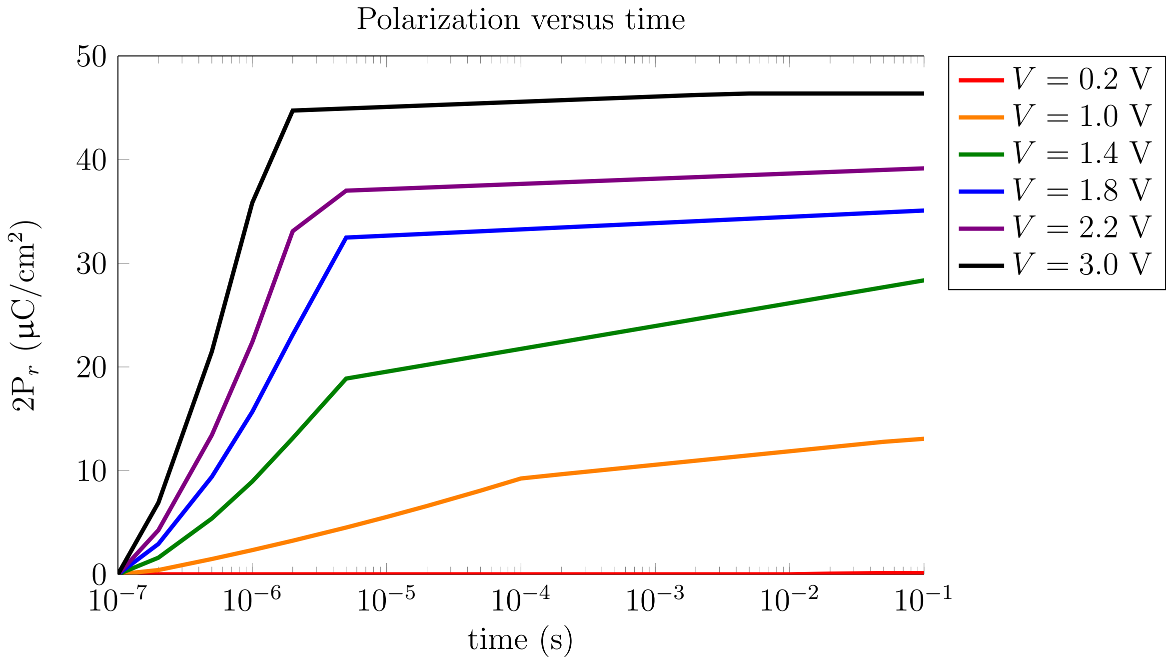


Figure 6.5: Changing polarization as a function of time for varying applied voltages for a sample with $V_c \approx 0.9$ V.

As discussed in Section 2.4, total polarization in ferroelectric materials is the aggregate contribution of many domains, each having their own switching voltages and times depending upon their orientation (referenced to the applied field). As such, the model was binned into domains by subtracting a total curve of $V = V_a - 0.2$ from $V = V_a$, therefore giving the polarization contribution for ferroelectric domains having switching voltages $V_a - 0.2 < V_c < V_a$. These curves were modified by capping at maximum (removing decreasing polarization for increasing time) and are shown in Figure 6.6.

One would logically expect a normal distribution of domains; with very few having low coercive voltage, very many switching at some moderate voltage, and very few being oriented so close to 90° from the applied field to have very high coercive voltage. Though a bit noisy, owing likely to the multiple normalizations performed on the curves in previous model steps, the maximum domain contributions shown in Figure 6.7 do suggest this type of normal distribution, centered around $V_c = 0.9$ V but

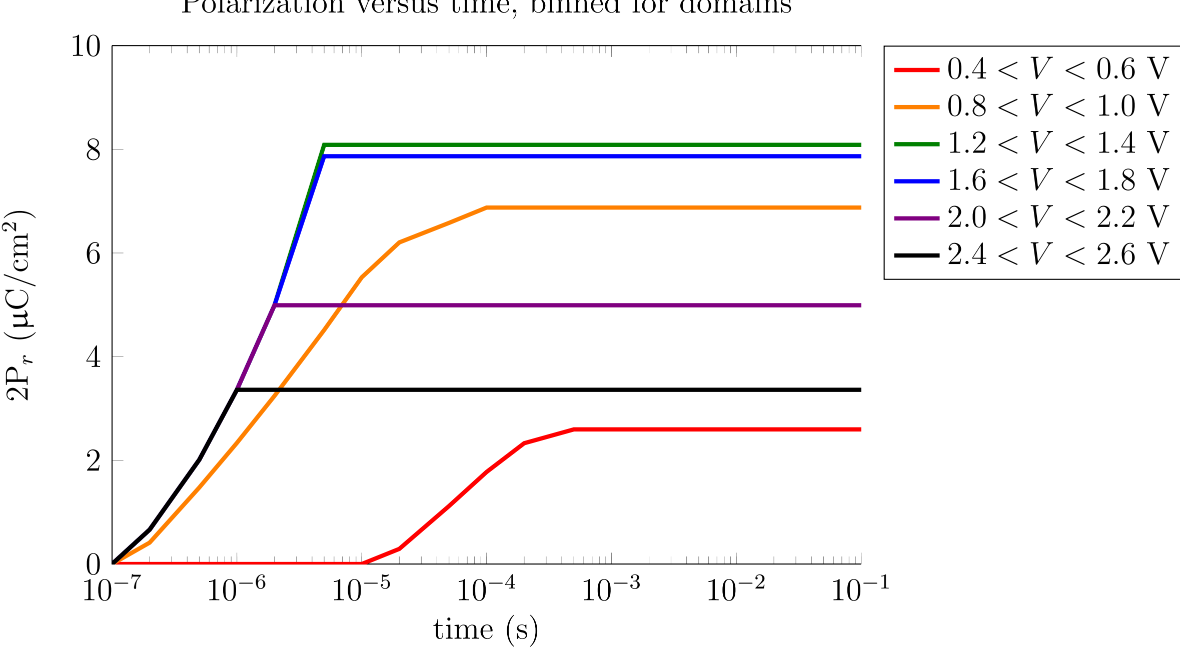


Figure 6.6: Changing polarization as a function of time binned for domains existing in 0.2V intervals for a sample with $V_c \approx 0.9$ V. Only a subset of curves are plotted. The models work best when binned from 0.2V to 3V in 0.2V intervals.

having a very long right-sided tail. Further, Figure 6.8 plots switching times binned for domains and shows that for higher voltages the switching times decrease. This should make some sense, considering domains which require larger voltages to switch have more excess energy while switching and therefore transition faster.

Finally, the model equations for polarization versus time binned for domains were implemented in a *Verilog-A* model, given in Appendix D.2.1, which keeps track of each domain's contribution based on applied voltage and aggregate time. The model then calculates corresponding resistance based on the current total polarization, given material constants, using equations from Section 4.3.

6.4 Address systems

The interconnectivity described is shown in Figure 6.9 connected to a single FTJ which uses the linear resistance *Verilog-A* model, from Appendix D.1.1. Systems for

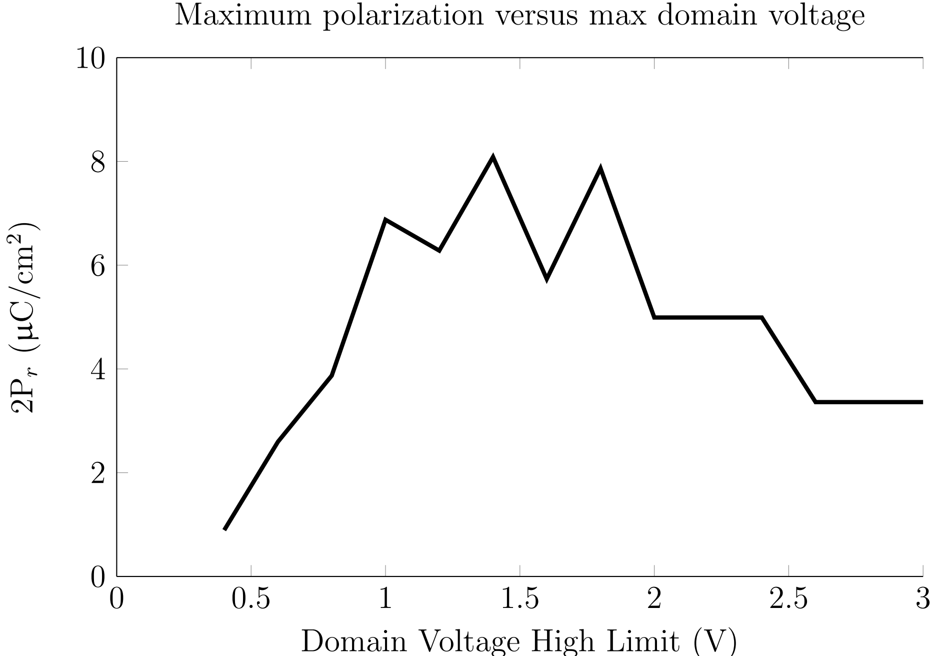


Figure 6.7: Maximum polarization for domains binned to 0.2V intervals, resembling a noisy normal distribution with a long right-sided tail.

addressing FTJ devices, following the read/write scheme given in Section 6.1, were designed as tristate CMOS cells using both 45 nm devices and 2 µm devices, though only 45 nm system performance will be examined here (since those results more closely describe the capabilities of these memories). The tristate devices, shown in Appendices D.3 through D.7, accept read enable (Ren), write enable (Wen), and write line (W) signals and toggle the output to desired voltages. SAP_ADDRESS_ROW_W and SAP_ADDRESS_COLUMN_W are used to toggle a connected row and column (positive and negative FTJ terminal) to high (V_{DD}) and low (V_{SS}) write voltages, respectively when Wen is high and W is high (writing the HRS). When Wen is high but W is low (writing LRS) the row is pulled to low write voltage and column to high. Read voltages applied by SAP_ADDRESS_ROW_R and SAP_ADDRESS_COLUMN_R, when Ren is high, always bring the row to read high (v_{dda}) and the column to read low (v_{ssa}). The column read voltage is applied to a reference resistor in series with the FTJ (and the rest of the column) and output is taken from an inverter taking its

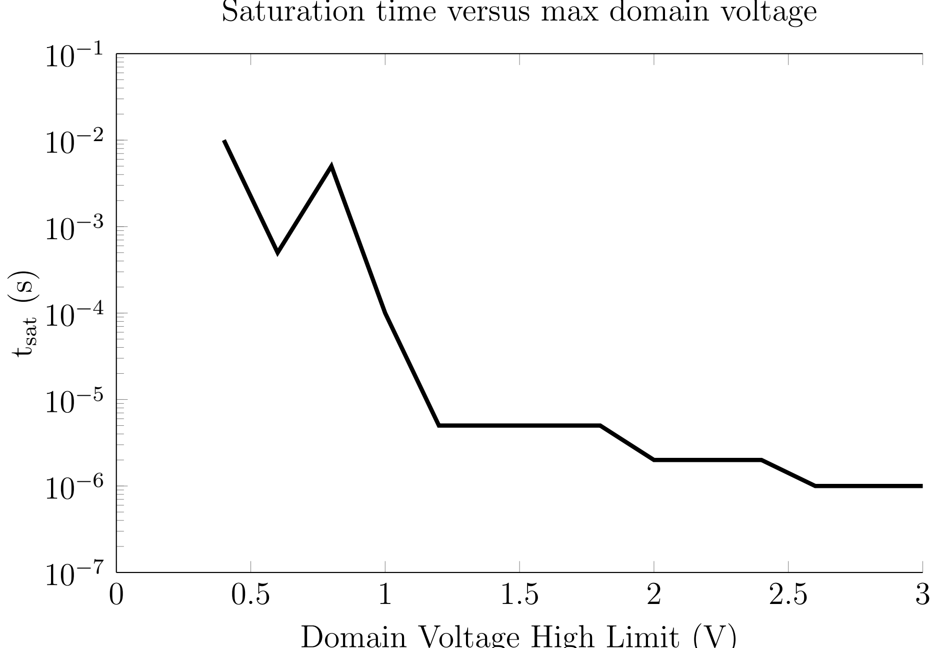


Figure 6.8: Time until polarization saturation for domains binned to 0.2V intervals. Higher energy domains (oriented less parallel to the applied field) switch faster due to excess energy.

input from the node (V_o) between the reference resistor and the FTJ. In this way, if $R_{\text{FTJ}} > R_{\text{ref}}$ then V_o pulls to v_{ssa} and the inverter pulls to V_{DD}. If $R_{\text{FTJ}} < R_{\text{ref}}$, then V_o pulls to v_{dda} and the inverter transitions to V_{SS}. SAP_ADDRESS_GND_vcc is used to hold rows and/or columns at vcc whenever not being written or read, to prevent write/read disturbs. To ensure all of the write voltage and vcc makes it to the FTJ, a pass transistor is connected in series with the reference resistor and is set to be off only while reading. Shown in figures 6.10 and 6.11 are simulation outputs of this system, showing read times of 10 ns and write times as short as 0.3 ns.

6.5 Simulation results - 4×4 Array

A testbench, code given in Appendix D.10, was written in *Verilog* which programs a 4×4 array of FTJ, as shown in Appendix D.9, all to HRS and then writes binary numbers 0 through 15 on the first row. Writing devices in an array is a two-step

process; one step writes devices to HRS and the next step to LRS. After writing each number, the row is read to check for write errors, then the row below it is read to check for write disturbs, and finally the original row is read again to check for read disturbs. A small portion of waveforms are shown in Figure 6.12, showing 10ns read and write pulses separated by 10ns guard times for relaxation of excess voltage from capacitive discharging. This system exhibits no write errors, write disturbs, or read disturbs.

A series of tests writing random binary numbers from 0 to 15 to random rows of the array exhibits 100% accuracy, shown in Figure 6.13, but often causes *Spectre* simulation to crash by not converging. Minor modifications may need to be made to the *Verilog-A* model to smooth edges and prevent convergence issues.

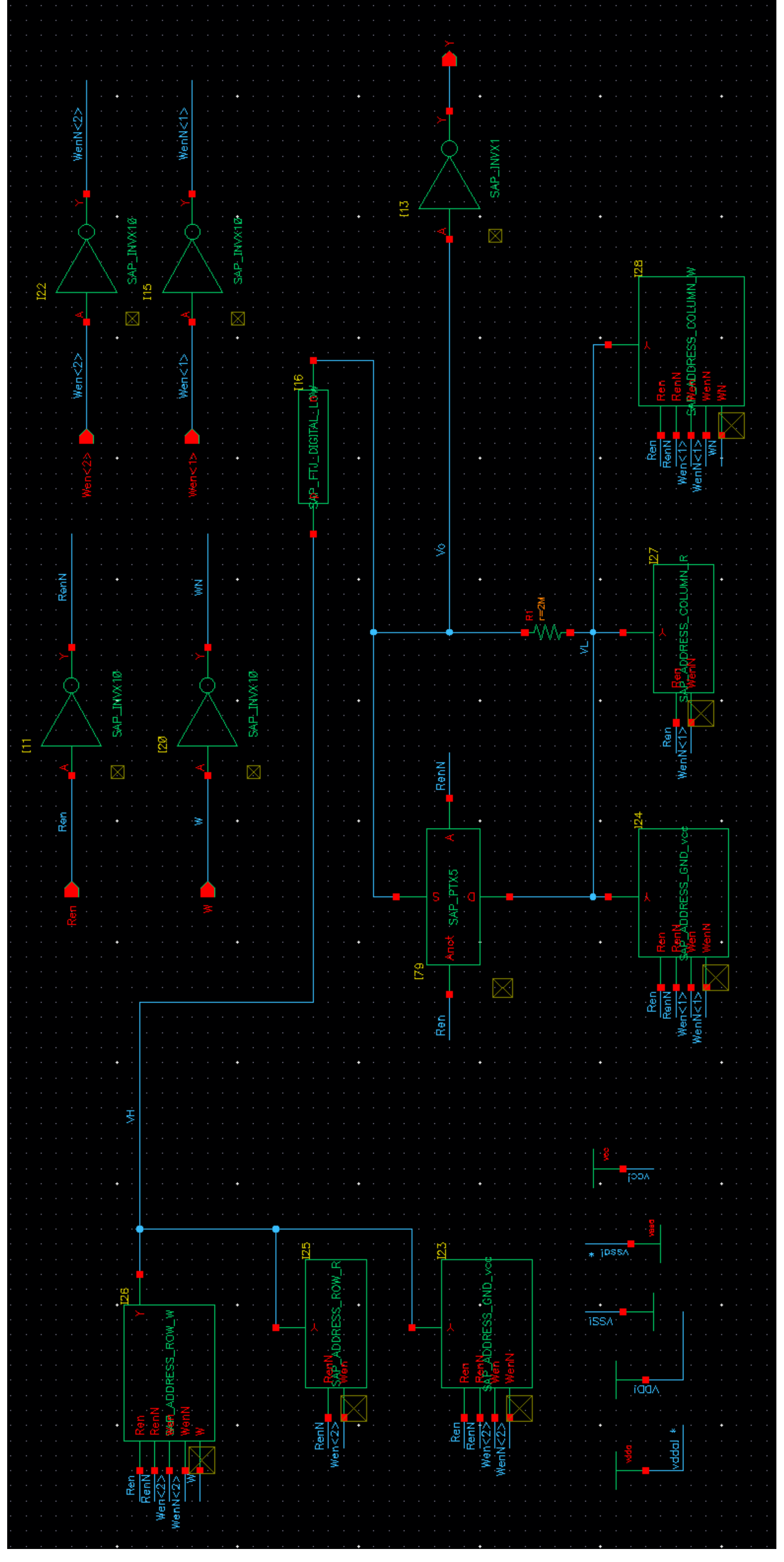


Figure 6.9: Schematic of address systems connected to a single FTJ. Note the inverted output taken above the reference resistor and the pass transistor to bypass that resistor while writing and applying vcc. The FTJ simulates with a LRS of 300 KΩ and HRS of 10 MΩ. The reference resistor is 2 MΩ.

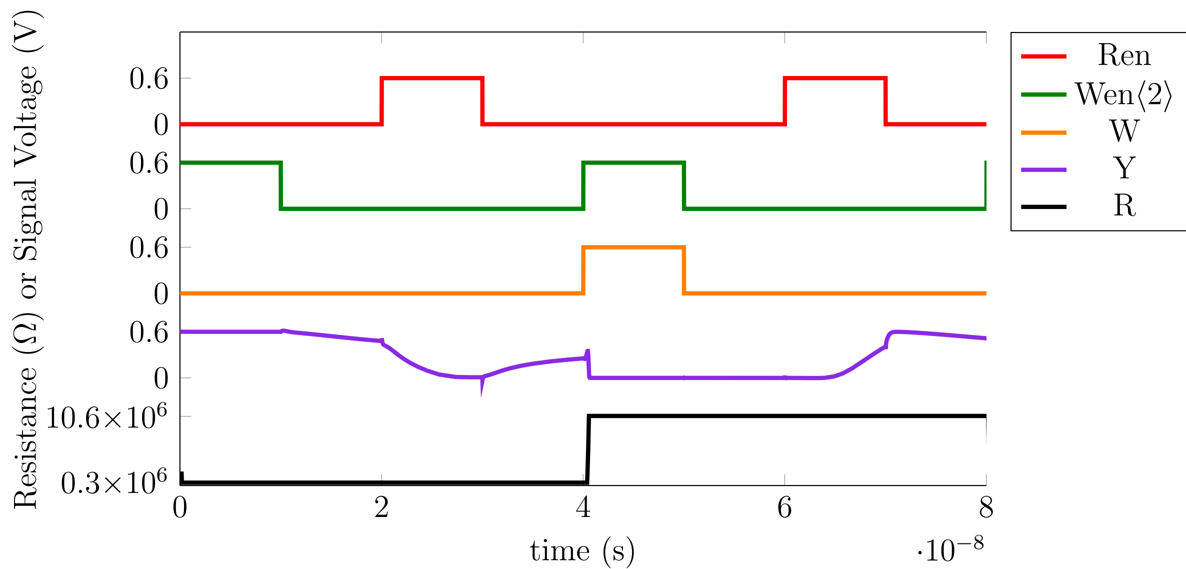


Figure 6.10: Simulation results from a single FTJ device connected to address circuitry designed with 45 nm CMOS. Wen⟨1⟩ follows the same curve as Wen⟨2⟩ in this simulation. Notice that the output, Y, transitions low when reading (Ren high) an FTJ in LRS and transitions high when reading an HRS FTJ. Write and read times are 10 ns.

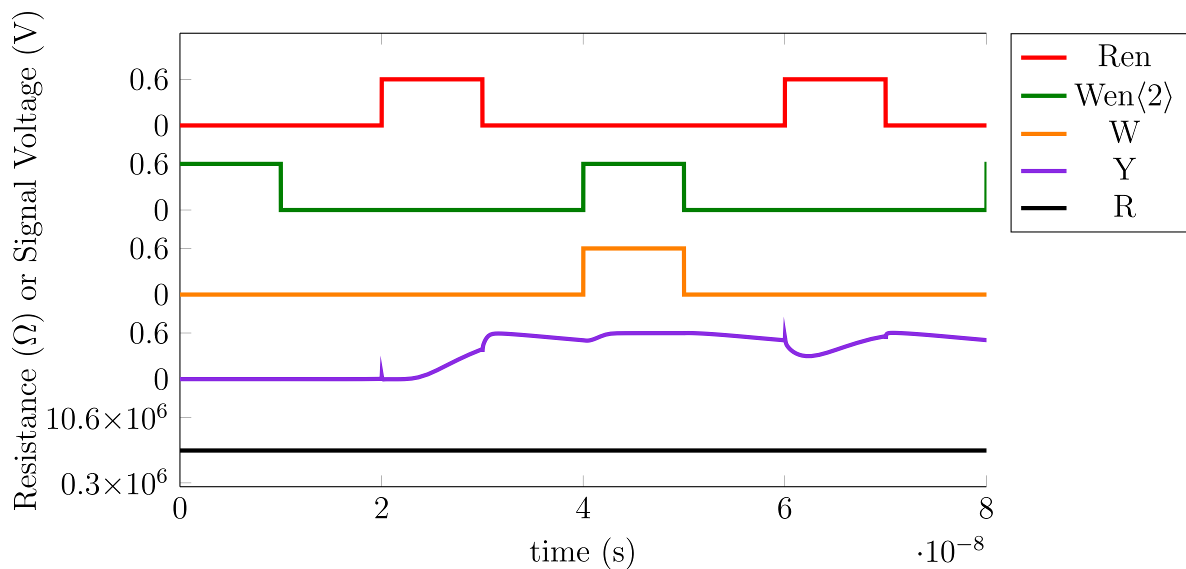


Figure 6.11: Simulation results from a single FTJ device connected to address circuitry designed with 45 nm CMOS. Wen⟨1⟩ is constantly off in this simulation; testing for write disturb when programming a different device in the same row, once in an array. The FTJ state remains unchanged even after write enable toggles for high and low writes, verifying that this system is robust against write disturbs of non-addressed devices.

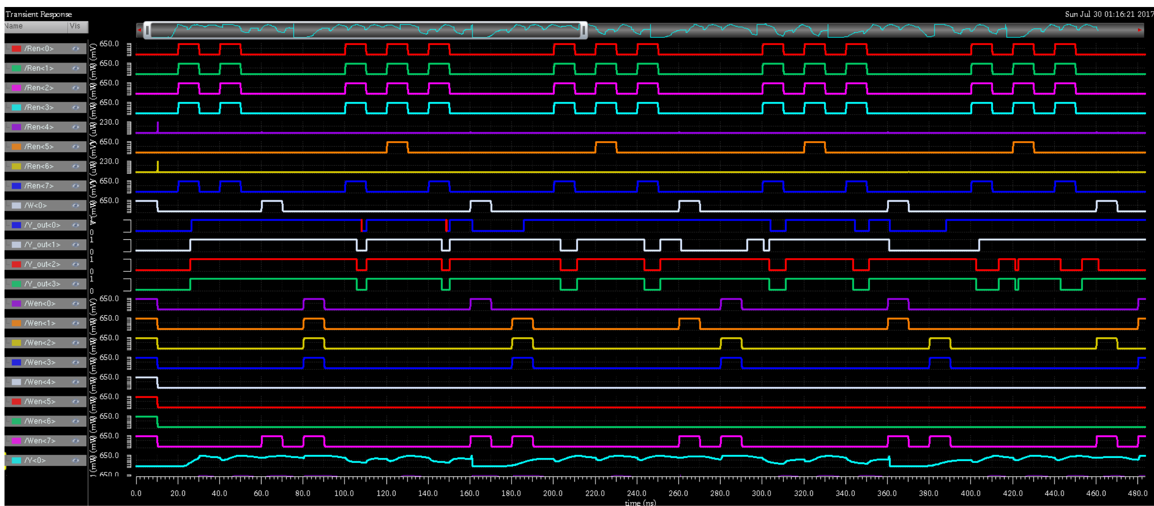


Figure 6.12: Small portion of waveform while writing binary 0 to 15 in one row while all other FTJ in the 4×4 array are in HRS.

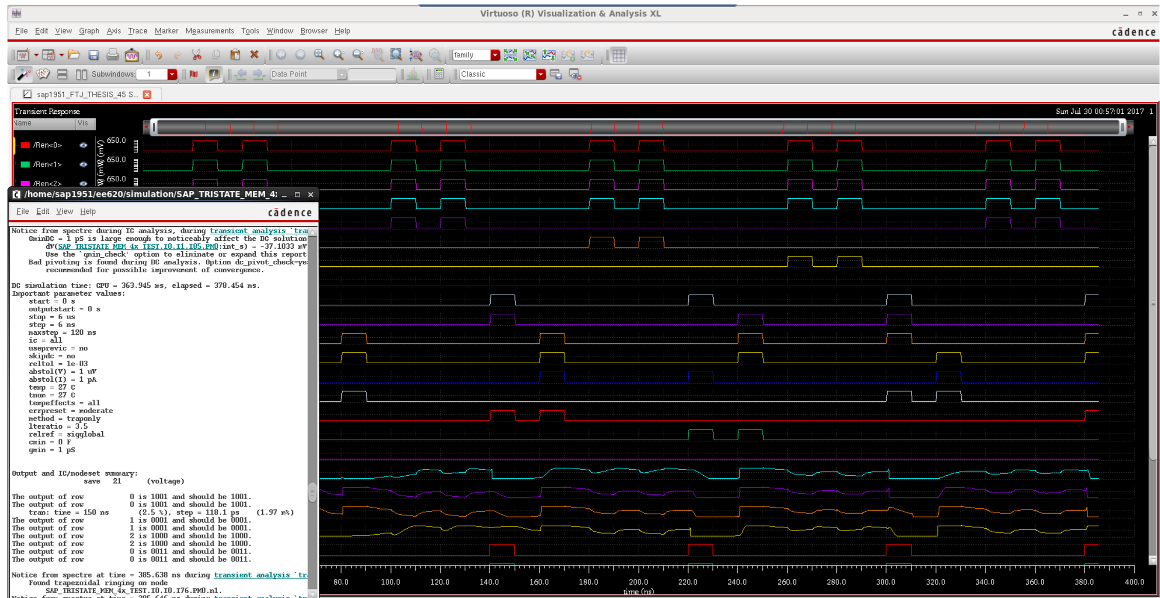


Figure 6.13: Waveform and simulation log for random binary numbers being written to random rows of the 4×4 array.

Chapter 7

Conclusions

This work has laid a nearly comprehensive framework for fabrication of FTJ devices with/without connected CMOS devices, from material to architecture. The physical phenomena present within ferroelectric materials was examined as a function of crystal structure and domains. FTJ device structures were modeled as a function of material properties and methods of extracting corresponding performance metrics (using a custom-built python code) were presented and evaluated for the proposed Al/Al:HfO_2/p-Si FTJ (having $\delta_1 = 0.06$ nm, $\chi_1 = 4.08$ eV, $\varepsilon_f = 40\varepsilon_0$, $E_a = 2$ eV, $P_r = 15\mu C/cm^2$, $d = 2, 3,$ or 5, $m^* = 0.11m_e$, $\delta_2 = 3$ nm, and $\chi_2 = 4.85$ eV) which exhibits a memory window as high as HRS/LRS $\approx 5\times10^5$ with max current density of $\approx 3\times10^{-2}$ A/cm^2 and power density of 1 $\mu W/cm^2$ with a 5 nm ferroelectric, enabling ultra-low power computing (compared to 45 W/cm^2 for competing FTJ devices) at high speeds. Using a 2 nm ferroelectric, the FTJ can achieve current density as high as 8×10^3 A/cm^2 with a memory window of HRS/LRS ≈ 6, targeting higher speed applications. These devices are therefore capable of lower power and higher speed performance than any alternative memristor technology, shown in sections 3.4 and 5.1, including competing FTJ devices.

The FTJs designed and simulated were then integrated into a new process flow, based on a twin-well polysilicon gate planar-CMOS technology, which was verified by *Silvaco Athena* simulation. Algorithms for read and write of devices in an array were

proposed, implemented by systems designed using a 45nm CMOS process design kit in *Cadence Virtuoso Design Suite*, and successfully simulated (using a Verilog testbench for stimulation) as digital memory storage devices in a 4×4 array architecture, with write and read times as low as 0.3 ns and 10ns, respectively.

7.1 Future Work

Ten device wafers are currently at step 22 of the FTJ-only process, shown in Appendix B, and will be completed by a future student. These wafers will be split into three groups of three wafers(with one left over), two of which will be sent to NamLAB and UCB for Si:HfO_2 and $HfZrO_2$ film deposition, respectively, on each wafer at one of three different thicknesses (the author recommends 2, 5, and 8nm). Once samples are completed, experimental results for P_r, t_{sat}, E_c, and resistances/current densities in each state, along with more detailed timing data for switching transitions, should be compiled and implemented in the polarization-timing FTJ model *Verilog-A* code, shown in Appendix D.2.1, which will be stored on the RIT gitlab. Finally, these models based on experimental data should be implemented with a brain-inspired computing system to examine performance of these devices in such an application. These designs could then be fabricated either by RIT (scaled to 2 μm CMOS) or an external foundry.

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Appendix A: Python Program Code

A.1 Core Code

```
1  #-*- coding: utf-8-*-
2  """
3  Created on Sun May 15 18:23:58 2016
4
5  @author: Spencer Pringle @ Rochester Institute of Technology
6  """
7
8  from pylab import *
9  from PyQt4 import QtGui, QtCore
10 from matplotlib.backends.backend_qt4agg import (
11         FigureCanvasQTAgg as FigureCanvas,
12         NavigationToolbar2QT as NavigationToolbar)
13 from matplotlib.figure import Figure
14 import sys
15 import GUI_NEW
16
17 class ExampleApp(QtGui.QMainWindow, GUI_NEW.Ui_MainWindow):
18         def __init__(self):
19                 super(self.__class__, self).__init__()
20                 self.setupUi(self)
21
22                 self.ModelingProgress.setValue(0)
23                 self.Metal1Box.addItems(['SrRuO_3','Co','Al','Metal 1'])
24                 self.Metal1Box.setCurrentIndex(0)
```

```
25             self.Metal2Box.addItems(['PZT','La_(0.67)Sr_(0.33)MnO_3','p+ Silicon'
                   , 'Metal 2'])
26             self.Metal2Box.setCurrentIndex(0)
27             self.FerroBox.addItems(['BaTiO_3','Al—HfO_2', 'Ferro'])
28             self.FerroBox.setCurrentIndex(0)
29
30             self.RunModeling.clicked.connect(self.Model)
31             self.Metal1Box.currentIndexChanged.connect(self.Metal1Update)
32             self.Metal2Box.currentIndexChanged.connect(self.Metal2Update)
33             self.FerroBox.currentIndexChanged.connect(self.FerroelectricUpdate)
34
35             self.Metal1Box.setCurrentIndex(2)
36             self.Metal2Box.setCurrentIndex(2)
37             self.FerroBox.setCurrentIndex(1)
38
39         def Model(self):
40             self.ModelingProgress.setValue(0)
41             self.FrontOutput.clear()
42             self.PotentialOutput.clear()
43             global sigma_p, sigma_s, q, epsilon_0, phi, sigma, k_1, k_2, a_0, x,
                   y, meshSpace, potentialMesh, phi_2, phi_1, positiveMesh,
                   negativeMesh
44             global e0, m0, kT, kb, h, m_0
45             global d, E_a, epsilon_f, P, h, h_eV
46             global delta_1, a_1, E_f_1
47             global delta_2, a_2, E_f_2
```

```
48            global G_2, G_1, x_1, x_2, phi_bar_pos, phi_bar_neg, x_1_index,
                  x_2_index, m_0, A_tun, J_0, J, v_app, phi_diff
49            global Ath_pos, Jth_pos, Ath_neg, Jth_neg, phi_prime, phi_prime_pos,
                  phi_prime_neg
50            global Atun_pos, J0_pos, Jtun_pos, Atun_neg, J0_neg, Jtun_neg, V, T,
                  R_pos, R_neg, m_star
51            global Ran, numchild, i, w, items, WellDir, WellFermi, Bar_Length_Pos
                  , Bar_Length_Neg, x_1_pos, x_2_pos, V, h_bar
52
53            epsilon_0=8.854E-12 #free space perm [F/m]
54            T=300 #Temperature (K)
55            #Non-adjustable Constants
56            e0=8.854E-14  #Permittivity of free space [F/cm]
57            m_0=9.11E-31  #Electron rest mass (kg)
58            h=6.626E-34   #Planck's constant (m^2*kg/sec)
59            q=1.6E-19     #Electron charge (C)
60            kb=1.38E-23   #Boltzman constant(J/K)
61            kT=(kb/q)*T          #[eV]
62            a_0=5.291E-11
63            h=6.626E-34
64            h_bar=h/(2*pi)
65            h_eV=4.13E-15
66            meshSpace=2/1000
67            v_app=.1
68
69            #Initialize Ferroelectric Material Values
70            epsilon_f=self.FerroDielectricConst.value()
```

```
71            E_a=self.FerroEA.value()
72            m_star=self.FerroEMass.value()
73            P=self.FerroPolarization.value()
74            d=self.FerroThick.value()*1E-9
75
76            #Initialize Metal 1 Values
77            E_f_1=self.Metal1FermiEnergy.value()
78            if self.Metal1ScreenLength.value()==0:
79                    delta_1=(E_f_1/(4*pi*q*self.Metal1Lattice.value()*1E-10))
                        **(1/2)
80            else:
81                    delta_1=self.Metal1ScreenLength.value()*1E-9
82
83            #Initialize Metal 2 Values
84            #if self.Metal2Box.currentIndex()==2:
85            E_f_2=self.Metal2FermiEnergy.value()
86            #else:
87            #      E_f_2=self.Metal2FermiEnergy.value()
88            if self.Metal2ScreenLength.value()==0:
89                    delta_2=(E_f_2/(4*pi*q*self.Metal2Lattice.value()*1E-10))
                        **(1/2)
90            else:
91                    delta_2=self.Metal2ScreenLength.value()*1E-9
92
93            #Calculate and store charges and wave vector magnitudes...
94            sigma_p=P*1E-2
95            sigma_s=sigma_p*d/(epsilon_f*(delta_1+delta_2)+d)
```

```
96
97          V=np.linspace(-1,1,201)
98          self.Potential()
99          x_1_pos=x_1
100         x_2_pos=x_2
101         positiveMesh=potentialMesh
102         phi_prime_pos=phi_prime
103         Ath_pos=(4*pi*m_0*(kb**2)*q)/((h**3))
104         Jth_pos = Ath_pos*1E-4*(T**2)*exp(-phi_prime_pos/kT)*(1-exp(-abs(V)/
                kT))
105         phi_diff=phi_1-phi_2
106         Bar_Length_Pos=x_2-x_1
107         phi_bar_pos=mean(y[x_1_index:x_2_index])
108         Atun_pos=((2*m_0*q*m_star)**(1/2))*(Bar_Length_Pos)*(2e-9)/h_bar
109         #Atun_pos=(4*pi*(x_2-x_1)*1e-9*(2*m_0)**(1/2))/h
110         #J0_pos=(q)/(2*pi*h*(((x_2-x_1)*1E-9)**2))
111         J0_pos=(6.08e8)/((Bar_Length_Pos)**2)
112         Jtun_pos=J0_pos*((phi_bar_pos)*exp(-Atun_pos*((phi_bar_pos)**(1/2)))
                -(phi_bar_pos+V)*exp(-Atun_pos*((phi_bar_pos+V)**(1/2))))
113         R_pos=np.zeros(size(V))
114         for i in range(0, size(V)):
115             if Jtun_pos[i]!=0 and Jtun_pos[i]!='nan':
116                 R_pos[i]=V[i]/Jtun_pos[i]
117             else:
118                 R_pos[i]='nan'
119         np.nanmean(abs(R_pos))
120         Jtun_pos=abs(Jtun_pos)
```

```
121                    Itun_pos=Jtun_pos[np.where(V==.5)[0]]*(250e-7)**2
122                    Itun_pos_1_250=Jtun_pos[[110][0]]*(250e-7)**2
123                    Itun_pos_2_250=Jtun_pos[[120][0]]*(250e-7)**2
124                    Itun_pos_1_500=Jtun_pos[[110][0]]*(500e-7)**2
125                    Itun_pos_2_500=Jtun_pos[[120][0]]*(500e-7)**2
126                    Rtun_pos_250=.5/Itun_pos
127                    Rtun_pos_1_250=.1/Itun_pos_1_250
128                    Rtun_pos_1_500=.1/Itun_pos_1_500
129                    Rtun_pos_2_250=.2/Itun_pos_2_250
130                    Rtun_pos_2_500=.2/Itun_pos_2_500
131                    rho_pos=.5/Jtun_pos[np.where(V==.5)[0]]
132                    rho_pos_1=.1/Jtun_pos[[110][0]]
133                    self.FrontOutput.insertPlainText('Under Positive Polarization (toward
                            Metal 1), at .5V bias:')
134                    self.FrontOutput.insertPlainText('\n')
135                    self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_pos[np.where(V
                           ==.5)[0]] +' A/cm^2')
136                    self.FrontOutput.insertPlainText('\n')
137                    self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_pos[np.where
                           (V==.5)[0]] +' A/cm^2')
138                    self.FrontOutput.insertPlainText('\n')
139                    self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                           Itun_pos +' A')
140                    self.FrontOutput.insertPlainText('\n')
141                    self.FrontOutput.insertPlainText('\n')
142                    self.FrontOutput.insertPlainText('Under Positive Polarization (toward
                            Metal 1), at .2V bias:')
```

```
143                 self.FrontOutput.insertPlainText('\n')
144                 self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_pos[[120][0]]
                        +' A/cm^2')
145                 self.FrontOutput.insertPlainText('\n')
146                 self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_pos
                        [[120][0]] +' A/cm^2')
147                 self.FrontOutput.insertPlainText('\n')
148                 self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                        Itun_pos_2_250 +' A')
149                 self.FrontOutput.insertPlainText('\n')
150                 self.FrontOutput.insertPlainText('\n')
151                 self.FrontOutput.insertPlainText('Under Positive Polarization (toward
                         Metal 1), at .1V bias:')
152                 self.FrontOutput.insertPlainText('\n')
153                 self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_pos[[110][0]]
                        +' A/cm^2')
154                 self.FrontOutput.insertPlainText('\n')
155                 self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_pos
                        [[110][0]] +' A/cm^2')
156                 self.FrontOutput.insertPlainText('\n')
157                 self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                        Itun_pos_1_250 +' A')
158                 self.FrontOutput.insertPlainText('\n')
159
160                 P=-P
161                 sigma_p=P*1E-2
162                 sigma_s=sigma_p*d/(epsilon_f*(delta_1+delta_2)+d)
```

```
163                 self.Potential()
164                 x_1_neg=x_1
165                 x_2_neg=x_2
166                 negativeMesh=potentialMesh
167                 phi_prime_neg=phi_prime
168                 Ath_neg=(4*pi*m_0*(kb**2)*q)/((h**3))
169                 Jth_neg = Ath_neg*1E-4*(T**2)*exp(-phi_prime_neg/kT)*(1-exp(-abs(V)/
                        kT))
170
171                 Bar_Length_Neg=x_2-x_1
172                 phi_bar_neg=mean(y[x_1_index:x_2_index])
173                 Atun_neg=((2*m_0*q*m_star)**(1/2))*(Bar_Length_Neg)*(2e-9)/h_bar
174                 J0_neg=(6.08e8)/((Bar_Length_Neg)**2)
175                 Jtun_neg=J0_neg*((phi_bar_neg)*exp(-Atun_neg*((phi_bar_neg)**(1/2)))
                        -((phi_bar_neg)+V)*exp(-Atun_neg*(((phi_bar_neg)+V)**(1/2))))
176                 R_neg=np.zeros(size(V))
177                 for i in range(0, size(V)):
178                         if Jtun_neg[i]!=0 and Jtun_neg[i]!='nan':
179                                 R_neg[i]=V[i]/Jtun_neg[i]
180                         else:
181                                 R_neg[i]='nan'
182                 Jtun_neg=abs(Jtun_neg)
183                 Itun_neg=Jtun_neg[np.where(V==.5)[0]]*(250e-7)**2
184                 Itun_neg_1_250=Jtun_neg[[110][0]]*(250e-7)**2
185                 Itun_neg_1_500=Jtun_neg[[110][0]]*(500e-7)**2
186                 Itun_neg_2_250=Jtun_neg[[120][0]]*(250e-7)**2
187                 Itun_neg_2_500=Jtun_neg[[120][0]]*(500e-7)**2
```

```
188                Rtun_neg_250=.5/Itun_neg
189                Rtun_neg_1_250=.1/Itun_neg_1_250
190                Rtun_neg_1_500=.1/Itun_neg_1_500
191                Rtun_neg_2_250=.2/Itun_neg_2_250
192                Rtun_neg_2_500=.2/Itun_neg_2_500
193                rho_neg=.5/Jtun_neg[np.where(V==.5)[0]]
194                rho_neg_1=.1/Jtun_neg[[110][0]]
195                self.FrontOutput.insertPlainText('\n')
196                self.FrontOutput.insertPlainText('Under Negative Polarization (toward
                     Metal 2), at .5V bias:')
197                self.FrontOutput.insertPlainText('\n')
198                self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_neg[np.where(V
                    ==.5)[0]] +' A/cm^2')
199                self.FrontOutput.insertPlainText('\n')
200                self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_neg[np.where
                    (V==.5)[0]] +' A/cm^2')
201                self.FrontOutput.insertPlainText('\n')
202                self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                    Itun_neg +' A')
203                self.FrontOutput.insertPlainText('\n')
204                self.FrontOutput.insertPlainText('\n')
205                self.FrontOutput.insertPlainText('Under Negative Polarization (toward
                     Metal 2), at .2V bias:')
206                self.FrontOutput.insertPlainText('\n')
207                self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_neg[[120][0]]
                    +' A/cm^2')
208                self.FrontOutput.insertPlainText('\n')
```

```
209                 self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_neg
                        [[120][0]] +' A/cm^2')
210                 self.FrontOutput.insertPlainText('\n')
211                 self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                        Itun_neg_2_250 +' A')
212                 self.FrontOutput.insertPlainText('\n')
213                 self.FrontOutput.insertPlainText('\t I_tun(500nm x 500nm)='+'%.2e'%
                        Itun_neg_2_500 +' A')
214                 self.FrontOutput.insertPlainText('\n')
215                 self.FrontOutput.insertPlainText('\n')
216                 self.FrontOutput.insertPlainText('Under Negative Polarization (toward
                         Metal 2), at .1V bias:')
217                 self.FrontOutput.insertPlainText('\n')
218                 self.FrontOutput.insertPlainText('\t J_th='+'%.2e'%Jth_neg[[110][0]]
                        +' A/cm^2')
219                 self.FrontOutput.insertPlainText('\n')
220                 self.FrontOutput.insertPlainText('\t J_tun='+'%.2e'%Jtun_neg
                        [[110][0]] +' A/cm^2')
221                 self.FrontOutput.insertPlainText('\n')
222                 self.FrontOutput.insertPlainText('\t I_tun(250nm x 250nm)='+'%.2e'%
                        Itun_neg_1_250 +' A')
223                 self.FrontOutput.insertPlainText('\n')
224                 self.FrontOutput.insertPlainText('\t I_tun(500nm x 500nm)='+'%.2e'%
                        Itun_neg_1_500 +' A')
225                 self.FrontOutput.insertPlainText('\n')
226
227                 phi_diff=abs(phi_bar_pos-phi_bar_neg)
```

```
228             if Jtun_neg[np.where(V==.5)[0]]>Jtun_pos[np.where(V==.5)[0]]:
229                 Jtun_Ratio=Jtun_neg[np.where(V==.5)[0]]/Jtun_pos[np.where(V
                        ==.5)[0]]
230                 LRSR=np.nanmean(abs(R_neg))
231                 HRSR=np.nanmean(abs(R_pos))
232             else:
233                 Jtun_Ratio=Jtun_pos[np.where(V==.5)[0]]/Jtun_neg[np.where(V
                        ==.5)[0]]
234                 LRSR=np.nanmean(abs(R_pos))
235                 HRSR=np.nanmean(abs(R_neg))
236             self.FrontOutput.insertPlainText('\n')
237             self.FrontOutput.insertPlainText('\n')
238             self.FrontOutput.insertPlainText('Difference in Average Potential
                    Barriers:\n')
239             self.FrontOutput.insertPlainText('\t'+'%.3f'%phi_bar_pos+'-'+'%.3f'%
                    phi_bar_neg +'='+'%.3f'%phi_diff + ' eV\n')
240             self.FrontOutput.insertPlainText('\n')
241             self.FrontOutput.insertPlainText('Ratio of Tunnel Current at .5V Bias
                     in HRS vs. LRS:\n')
242             self.FrontOutput.insertPlainText('\t'+'%.3f'%Jtun_Ratio+'\n')
243             self.FrontOutput.insertPlainText('\n')
244             self.FrontOutput.insertPlainText('LRS and HRS Resistances (250nm x
                    250nm, at .5V):\n')
245             self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%Rtun_pos_250 +' Ohm
                    \n\t Neg:'+'%.3e'%Rtun_neg_250 +' Ohm\n')
246             self.FrontOutput.insertPlainText('\n')
247             self.FrontOutput.insertPlainText('LRS and HRS Resistivity @ .5V:\n')
```

```
248                 self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%rho_pos +' Ohm cm
                        ^2\n\t Neg:'+'%.3e'%rho_neg +' Ohm cm^2\n')
249                 self.FrontOutput.insertPlainText('\n')
250                 self.FrontOutput.insertPlainText('\n')
251                 self.FrontOutput.insertPlainText('LRS and HRS Resistivity @ .1V:\n')
252                 self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%rho_pos_1 +' Ohm cm
                        ^2\n\t Neg:'+'%.3e'%rho_neg_1 +' Ohm cm^2\n')
253                 self.FrontOutput.insertPlainText('\n')
254                 self.FrontOutput.insertPlainText('\n')
255                 self.FrontOutput.insertPlainText('LRS and HRS Resistances (250nm x
                        250nm, at .2V):\n')
256                 self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%Rtun_pos_2_250 +'
                        Ohm\n\t Neg:'+'%.3e'%Rtun_neg_2_250 +' Ohm\n')
257                 self.FrontOutput.insertPlainText('\n')
258                 self.FrontOutput.insertPlainText('LRS and HRS Resistances (500nm x
                        500nm, at .2V):\n')
259                 self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%Rtun_pos_2_500 +'
                        Ohm\n\t Neg:'+'%.3e'%Rtun_neg_2_500 +' Ohm\n')
260                 self.FrontOutput.insertPlainText('\n')
261                 self.FrontOutput.insertPlainText('\n')
262                 self.FrontOutput.insertPlainText('LRS and HRS Resistances (250nm x
                        250nm, at .1V):\n')
263                 self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%Rtun_pos_1_250 +'
                        Ohm\n\t Neg:'+'%.3e'%Rtun_neg_1_250 +' Ohm\n')
264                 self.FrontOutput.insertPlainText('\n')
265                 self.FrontOutput.insertPlainText('LRS and HRS Resistances (500nm x
                        500nm, at .1V):\n')
```

```
266                    self.FrontOutput.insertPlainText('\t Pos:'+'%.3e'%Rtun_pos_1_500 +'
                           Ohm\n\t Neg:'+'%.3e'%Rtun_neg_1_500 +' Ohm\n')
267                    self.FrontOutput.insertPlainText('\n')
268
269                    Jtunratiomax = max(np.nan_to_num(np.divide(Jtun_pos, Jtun_neg)))
270                    self.FrontOutput.insertPlainText('Max Current Ratio: '+'%.3e'%
                           Jtunratiomax)
271
272
273                    self.closeall()
274                    fig1 = Figure()
275                    ax1f1 = fig1.add_subplot(111)
276                    ax1f1.plot(positiveMesh[0,:], positiveMesh[1,:])
277                    ax1f1.plot(negativeMesh[0,:], negativeMesh[1,:])
278                    ExampleApp.addmpl(self,fig1)
279                    fig2=Figure()
280                    ax1f2 = fig2.add_subplot(111)
281                    ax1f2.plot(V, Jth_pos)
282                    ax1f2.plot(V, Jth_neg)
283                    ExampleApp.addmpl(self,fig2)
284                    fig3=Figure()
285                    ax1f3 = fig3.add_subplot(111)
286                    ax1f3.plot(V, Jtun_pos)
287                    ax1f3.plot(V, Jtun_neg)
288                    ax1f3.set_yscale('log')
289                    ExampleApp.addmpl(self,fig3)
290
```

```
291                 self.PotentialOutput.insertPlainText('V\tJtunpos\tJtunneg\n')
292                 for i in range(0, size(V)):
293                         self.PotentialOutput.insertPlainText('%.3f'%V[i] + '\t' + '
                                %.3e'%Jtun_pos[i] + '\t' + '%.3e'%Jtun_neg[i] + '\n')
294                 self.PotentialOutput.insertPlainText('\n')
295                 self.PotentialOutput.insertPlainText('X\tV1pos\tV2neg\n')
296                 for p in range(0, size(x)):
297                         self.PotentialOutput.insertPlainText('%.3f'%x[p] + '\t' + '
                                %.3f'%positiveMesh[1,p] + '\t' + '%.3f'%negativeMesh[1,p]
                                 + '\n')
298 
299         def unfill(self):
300                 global numchild, i, w, items
301                 numchild=self.PotentialMPlay.count()
302                 items = (self.PotentialMPlay.itemAt(i) for i in range(self.
                        PotentialMPlay.count()))
303                 for w in items:
304                         try:
305                                 self.PotentialMPlay.removeWidget(w.widget())
306                         except AttributeError:
307                                 pass
308                         try:
309                                 self.PotentialMPlay.removeItem(w.item())
310                         except AttributeError:
311                                 pass
312 
```

```
313     def closeall(self): #solution found on http://python.6.x6.nabble.com/
            Completely-removing-items-from-a-layout-td1924202.html
314         def deleteItems(layout):
315             if layout is not None:
316                 while layout.count():
317                     item = layout.takeAt(0)
318                     widget = item.widget()
319                     if widget is not None:
320                         widget.deleteLater()
321                     else:
322                         deleteItems(item.layout())
323         deleteItems(self.PotentialMPlay)
324 
325     def Potential(self):
326         global P, x, index, y, x_prime, potentialMesh, delta_1, delta_2,
                E_f_1, E_f_2, phi_2, phi_1, x_1, x_2, x_1_index, x_2_index,
                phi_prime, WellDir, WellFermi
327 
328         x = np.linspace(-5,5+(d*1E9),(5+(d*1E9))/meshSpace)
329         y = np.zeros(size(x))
330         index = 0
331         flag = 0
332         y_flag=0
333 
334         if delta_1<delta_2:
335             WellFermi=E_f_2
336             WellDir=-1
```

```
337             else:
338                 WellFermi=E_f_1
339                 WellDir=1
340 
341             for x_prime in x:
342                 if x_prime<=0:
343                     y[index]=(sigma_s*delta_1/epsilon_0)*exp(-abs(x_prime
                            *1E-9)/(delta_1))
344                 elif x_prime>=(d*1E9):
345                     y[index]=(-sigma_s*delta_2/epsilon_0)*exp(-abs((
                            x_prime*1E-9)-d)/(delta_1))
346                 if x_prime<=0:
347                     phi_1=y[index]
348                 if x_prime>=(d*1E9) and flag==0:
349                     phi_2=y[index]
350                     flag=1
351                 index=index+1
352                 self.ModelingProgress.setValue(index*50/size(x))
353             index = 0
354             for x_u in x:
355                 if x_u>0 and x_u<(d*(1E9)):
356                     y[index]=phi_1-((x_u/(d*1E9))*(phi_1-phi_2))
357                 index=index+1
358                 self.ModelingProgress.setValue(50+(index*25/size(x)))
359             index = 0
360             for x_u in x:
361                 if x_u>0 and x_u<(d*(1E9)):
```

```
362                     y[index]=y[index]+(E_f_1-E_a)+((x_u/(d*1E9))*(E_f_2-
                            E_f_1))
363                 if x_u<=0:
364                     phi_1=y[index]
365                 if x_u>=(d*1E9) and flag==0:
366                     phi_2=y[index]
367                     flag=1
368                 index=index+1
369                 self.ModelingProgress.setValue(50+(index*25/size(x)))
370             phi_prime=max(y)
371             index=0
372             for x_u in x:
373                 if y_flag==0 and y[index]>phi_prime/10:
374                     x_1=x_u
375                     x_1_index=index
376                     y_flag=1
377                 if y_flag==1 and y[index]<phi_prime/10:
378                     x_2=x_u
379                     x_2_index=index-1
380                     y_flag=2
381                 index=index+1
382                 self.ModelingProgress.setValue(75+(index*25/size(x)))
383             potentialMesh=vstack((x,y))
384
385         def addmpl(self, fig):
386             for clos in range(self.PotentialMPlay.count()):
387                 try:
```

```
388                     self.canvas.close()
389                     self.toolbar.close()
390                 except AttributeError:
391                     pass
392             self.canvas = FigureCanvas(fig)
393             self.PotentialMPlay.addWidget(self.canvas)
394             self.canvas.draw()
395             self.toolbar = NavigationToolbar(self.canvas,
396                     self.verticalWidget_6, coordinates=True)
397             self.PotentialMPlay.addWidget(self.toolbar)
398 
399         def Metal1Update(self):
400             if self.Metal1Box.currentIndex()==0:
401                 self.Metal1ScreenLength.setValue(.6)
402                 self.Metal1FermiEnergy.setValue(1.5)
403                 self.Metal1Lattice.setValue(0)
404             elif self.Metal1Box.currentIndex()==1:
405                 self.Metal1ScreenLength.setValue(.05)
406                 self.Metal1FermiEnergy.setValue(5)
407                 self.Metal1Lattice.setValue(0)
408             elif self.Metal1Box.currentIndex()==2:
409                 self.Metal1ScreenLength.setValue(.06)
410                 self.Metal1FermiEnergy.setValue(4.08)
411                 self.Metal1Lattice.setValue(0)
412         def FerroelectricUpdate(self):
413             if self.FerroBox.currentIndex()==0:
414                 self.FerroDielectricConst.setValue(2000)
```

```
415                 self.FerroEA.setValue(2.5)
416                 self.FerroPolarization.setValue(20)
417                 self.FerroThick.setValue(2)
418                 self.FerroEMass.setValue(1)
419             elif self.FerroBox.currentIndex()==1:
420                 self.FerroDielectricConst.setValue(40)
421                 self.FerroEA.setValue(2.0)#http://e-citations.ethbib.ethz.ch/
                    view/pub:28311
422                 self.FerroPolarization.setValue(10)
423                 self.FerroThick.setValue(2)#http://e-citations.ethbib.ethz.ch
                    /view/pub:28311
424                 self.FerroEMass.setValue(.11)
425         def Metal2Update(self):
426             if self.Metal2Box.currentIndex()==0:
427                 self.Metal2ScreenLength.setValue(.07)
428                 self.Metal2FermiEnergy.setValue(3.5)
429                 self.Metal2Lattice.setValue(0)
430             elif self.Metal2Box.currentIndex()==1:
431                 self.Metal2ScreenLength.setValue(.1)
432                 self.Metal2FermiEnergy.setValue(4.8)#From Abuwasib_15
433                 self.Metal2Lattice.setValue(0)
434             elif self.Metal2Box.currentIndex()==2:
435                 self.Metal2ScreenLength.setValue(.4)
436                 self.Metal2FermiEnergy.setValue(4.85)
437                 self.Metal2Lattice.setValue(0)
438
439
```

```
440 def main():
441         if QtCore.QCoreApplication.instance() != None:
442                 app = QtCore.QCoreApplication.instance()
443         else:
444                 app = QtGui.QApplication(sys.argv)  #A new instance of QApplication
445         form = ExampleApp()                     #We set the form to be our
            ExampleApp (design)
446         form.show()                             #Show the form
447         app.exec_()                             #and execute the app
448
449
450 if __name__ == '__main__':              # if we're running file directly and not
        importing it
451         main()                                  #run the main function
```

A.2 GUI Code

```
1  # -*- coding: utf-8 -*-
2
3  #Form implementation generated from reading ui file 'FTJ_GUI_Pringle_Single_Page.ui'
4  #
5  # Created by: PyQt4 UI code generator 4.11.4
6  #
7  #WARNING! All changes made in this file will be lost!
8
9  from PyQt4 import QtCore, QtGui
10
```

```
11  try:
12          _fromUtf8 = QtCore.QString.fromUtf8
13  except AttributeError:
14          def _fromUtf8(s):
15                  return s
16
17  try:
18          _encoding = QtGui.QApplication.UnicodeUTF8
19          def _translate(context, text, disambig):
20                  return QtGui.QApplication.translate(context, text, disambig,
                        _encoding)
21  except AttributeError:
22          def _translate(context, text, disambig):
23                  return QtGui.QApplication.translate(context, text, disambig)
24
25  class Ui_MainWindow(object):
26          def setupUi(self, MainWindow):
27                  MainWindow.setObjectName(_fromUtf8("MainWindow"))
28                  MainWindow.resize(941, 739)
29                  self.centralwidget = QtGui.QWidget(MainWindow)
30                  self.centralwidget.setObjectName(_fromUtf8("centralwidget"))
31                  self.gridLayout = QtGui.QGridLayout(self.centralwidget)
32                  self.gridLayout.setObjectName(_fromUtf8("gridLayout"))
33                  self.splitter_5 = QtGui.QSplitter(self.centralwidget)
34                  self.splitter_5.setOrientation(QtCore.Qt.Vertical)
35                  self.splitter_5.setObjectName(_fromUtf8("splitter_5"))
36                  self.splitter = QtGui.QSplitter(self.splitter_5)
```

```
37          self.splitter.setOrientation(QtCore.Qt.Horizontal)
38          self.splitter.setObjectName(_fromUtf8("splitter"))
39          self.layoutWidget = QtGui.QWidget(self.splitter)
40          self.layoutWidget.setObjectName(_fromUtf8("layoutWidget"))
41          self.verticalLayout_7 = QtGui.QVBoxLayout(self.layoutWidget)
42          self.verticalLayout_7.setObjectName(_fromUtf8("verticalLayout_7"))
43          self.verticalLayout_4 = QtGui.QVBoxLayout()
44          self.verticalLayout_4.setObjectName(_fromUtf8("verticalLayout_4"))
45          self.verticalLayout = QtGui.QVBoxLayout()
46          self.verticalLayout.setObjectName(_fromUtf8("verticalLayout"))
47          self.groupBox = QtGui.QGroupBox(self.layoutWidget)
48          self.groupBox.setObjectName(_fromUtf8("groupBox"))
49          self.gridLayout_3 = QtGui.QGridLayout(self.groupBox)
50          self.gridLayout_3.setObjectName(_fromUtf8("gridLayout_3"))
51          self.verticalLayout_3 = QtGui.QVBoxLayout()
52          self.verticalLayout_3.setObjectName(_fromUtf8("verticalLayout_3"))
53          self.horizontalLayout_2 = QtGui.QHBoxLayout()
54          self.horizontalLayout_2.setObjectName(_fromUtf8("horizontalLayout_2")
                )
55          self.label = QtGui.QLabel(self.groupBox)
56          self.label.setObjectName(_fromUtf8("label"))
57          self.horizontalLayout_2.addWidget(self.label)
58          self.label_2 = QtGui.QLabel(self.groupBox)
59          self.label_2.setObjectName(_fromUtf8("label_2"))
60          self.horizontalLayout_2.addWidget(self.label_2)
61          self.label_3 = QtGui.QLabel(self.groupBox)
62          self.label_3.setObjectName(_fromUtf8("label_3"))
```

```
63                  self.horizontalLayout_2.addWidget(self.label_3)
64                  self.verticalLayout_3.addLayout(self.horizontalLayout_2)
65                  self.horizontalLayout = QtGui.QHBoxLayout()
66                  self.horizontalLayout.setObjectName(_fromUtf8("horizontalLayout"))
67                  self.Metal1Box = QtGui.QComboBox(self.groupBox)
68                  self.Metal1Box.setObjectName(_fromUtf8("Metal1Box"))
69                  self.horizontalLayout.addWidget(self.Metal1Box)
70                  self.FerroBox = QtGui.QComboBox(self.groupBox)
71                  self.FerroBox.setObjectName(_fromUtf8("FerroBox"))
72                  self.horizontalLayout.addWidget(self.FerroBox)
73                  self.Metal2Box = QtGui.QComboBox(self.groupBox)
74                  self.Metal2Box.setObjectName(_fromUtf8("Metal2Box"))
75                  self.horizontalLayout.addWidget(self.Metal2Box)
76                  self.verticalLayout_3.addLayout(self.horizontalLayout)
77                  self.gridLayout_3.addLayout(self.verticalLayout_3, 0, 0, 1, 1)
78                  self.verticalLayout.addWidget(self.groupBox)
79                  self.verticalLayout_4.addLayout(self.verticalLayout)
80                  self.verticalLayout_7.addLayout(self.verticalLayout_4)
81                  self.splitter_4 = QtGui.QSplitter(self.layoutWidget)
82                  self.splitter_4.setOrientation(QtCore.Qt.Vertical)
83                  self.splitter_4.setObjectName(_fromUtf8("splitter_4"))
84                  self.layoutWidget1 = QtGui.QWidget(self.splitter_4)
85                  self.layoutWidget1.setObjectName(_fromUtf8("layoutWidget1"))
86                  self.verticalLayout_12 = QtGui.QVBoxLayout(self.layoutWidget1)
87                  self.verticalLayout_12.setObjectName(_fromUtf8("verticalLayout_12"))
88                  self.label_14 = QtGui.QLabel(self.layoutWidget1)
89                  self.label_14.setObjectName(_fromUtf8("label_14"))
```

```
90              self.verticalLayout_12.addWidget(self.label_14)
91              self.horizontalLayout_4 = QtGui.QHBoxLayout()
92              self.horizontalLayout_4.setObjectName(_fromUtf8("horizontalLayout_4")
                    )
93              self.Metal1Group = QtGui.QGroupBox(self.layoutWidget1)
94              self.Metal1Group.setObjectName(_fromUtf8("Metal1Group"))
95              self.horizontalLayout_3 = QtGui.QHBoxLayout(self.Metal1Group)
96              self.horizontalLayout_3.setObjectName(_fromUtf8("horizontalLayout_3")
                    )
97              self.verticalLayout_9 = QtGui.QVBoxLayout()
98              self.verticalLayout_9.setObjectName(_fromUtf8("verticalLayout_9"))
99              self.label_4 = QtGui.QLabel(self.Metal1Group)
100             self.label_4.setObjectName(_fromUtf8("label_4"))
101             self.verticalLayout_9.addWidget(self.label_4)
102             self.Metal1ScreenLength = QtGui.QDoubleSpinBox(self.Metal1Group)
103             self.Metal1ScreenLength.setDecimals(5)
104             self.Metal1ScreenLength.setProperty("value", 0.6)
105             self.Metal1ScreenLength.setObjectName(_fromUtf8("Metal1ScreenLength")
                    )
106             self.verticalLayout_9.addWidget(self.Metal1ScreenLength)
107             self.label_5 = QtGui.QLabel(self.Metal1Group)
108             self.label_5.setObjectName(_fromUtf8("label_5"))
109             self.verticalLayout_9.addWidget(self.label_5)
110             self.Metal1FermiEnergy = QtGui.QDoubleSpinBox(self.Metal1Group)
111             self.Metal1FermiEnergy.setProperty("value", 1.5)
112             self.Metal1FermiEnergy.setObjectName(_fromUtf8("Metal1FermiEnergy"))
113             self.verticalLayout_9.addWidget(self.Metal1FermiEnergy)
```

```
114             self.label_7 = QtGui.QLabel(self.Metal1Group)
115             self.label_7.setObjectName(_fromUtf8("label_7"))
116             self.verticalLayout_9.addWidget(self.label_7)
117             self.Metal1Lattice = QtGui.QDoubleSpinBox(self.Metal1Group)
118             self.Metal1Lattice.setDecimals(5)
119             self.Metal1Lattice.setObjectName(_fromUtf8("Metal1Lattice"))
120             self.verticalLayout_9.addWidget(self.Metal1Lattice)
121             self.horizontalLayout_3.addLayout(self.verticalLayout_9)
122             self.horizontalLayout_4.addWidget(self.Metal1Group)
123             self.FerroGroup = QtGui.QGroupBox(self.layoutWidget1)
124             self.FerroGroup.setObjectName(_fromUtf8("FerroGroup"))
125             self.horizontalLayout_5 = QtGui.QHBoxLayout(self.FerroGroup)
126             self.horizontalLayout_5.setObjectName(_fromUtf8("horizontalLayout_5")
                    )
127             self.verticalLayout_11 = QtGui.QVBoxLayout()
128             self.verticalLayout_11.setObjectName(_fromUtf8("verticalLayout_11"))
129             self.label_12 = QtGui.QLabel(self.FerroGroup)
130             self.label_12.setObjectName(_fromUtf8("label_12"))
131             self.verticalLayout_11.addWidget(self.label_12)
132             self.FerroDielectricConst = QtGui.QDoubleSpinBox(self.FerroGroup)
133             self.FerroDielectricConst.setMaximum(500000.0)
134             self.FerroDielectricConst.setProperty("value", 2000.0)
135             self.FerroDielectricConst.setObjectName(_fromUtf8("
                    FerroDielectricConst"))
136             self.verticalLayout_11.addWidget(self.FerroDielectricConst)
137             self.label_6 = QtGui.QLabel(self.FerroGroup)
138             self.label_6.setObjectName(_fromUtf8("label_6"))
```

```
139                     self.verticalLayout_11.addWidget(self.label_6)
140                     self.FerroBandgap = QtGui.QDoubleSpinBox(self.FerroGroup)
141                     self.FerroBandgap.setProperty("value", 2.3)
142                     self.FerroBandgap.setObjectName(_fromUtf8("FerroBandgap"))
143                     self.verticalLayout_11.addWidget(self.FerroBandgap)
144                     self.label_9 = QtGui.QLabel(self.FerroGroup)
145                     self.label_9.setObjectName(_fromUtf8("label_9"))
146                     self.verticalLayout_11.addWidget(self.label_9)
147                     self.FerroPolarization = QtGui.QDoubleSpinBox(self.FerroGroup)
148                     self.FerroPolarization.setProperty("value", 20.0)
149                     self.FerroPolarization.setObjectName(_fromUtf8("FerroPolarization"))
150                     self.verticalLayout_11.addWidget(self.FerroPolarization)
151                     self.label_13 = QtGui.QLabel(self.FerroGroup)
152                     self.label_13.setObjectName(_fromUtf8("label_13"))
153                     self.verticalLayout_11.addWidget(self.label_13)
154                     self.FerroThick = QtGui.QDoubleSpinBox(self.FerroGroup)
155                     self.FerroThick.setProperty("value", 2.0)
156                     self.FerroThick.setObjectName(_fromUtf8("FerroThick"))
157                     self.verticalLayout_11.addWidget(self.FerroThick)
158                     self.horizontalLayout_5.addLayout(self.verticalLayout_11)
159                     self.horizontalLayout_4.addWidget(self.FerroGroup)
160                     self.Metal2Group = QtGui.QGroupBox(self.layoutWidget1)
161                     self.Metal2Group.setObjectName(_fromUtf8("Metal2Group"))
162                     self.horizontalLayout_6 = QtGui.QHBoxLayout(self.Metal2Group)
163                     self.horizontalLayout_6.setObjectName(_fromUtf8("horizontalLayout_6")
                            )
164                     self.verticalLayout_10 = QtGui.QVBoxLayout()
```

```
165         self.verticalLayout_10.setObjectName(_fromUtf8("verticalLayout_10"))
166         self.label_11 = QtGui.QLabel(self.Metal2Group)
167         self.label_11.setObjectName(_fromUtf8("label_11"))
168         self.verticalLayout_10.addWidget(self.label_11)
169         self.Metal2ScreenLength = QtGui.QDoubleSpinBox(self.Metal2Group)
170         self.Metal2ScreenLength.setDecimals(5)
171         self.Metal2ScreenLength.setProperty("value", 0.07)
172         self.Metal2ScreenLength.setObjectName(_fromUtf8("Metal2ScreenLength")
                )
173         self.verticalLayout_10.addWidget(self.Metal2ScreenLength)
174         self.label_8 = QtGui.QLabel(self.Metal2Group)
175         self.label_8.setObjectName(_fromUtf8("label_8"))
176         self.verticalLayout_10.addWidget(self.label_8)
177         self.Metal2FermiEnergy = QtGui.QDoubleSpinBox(self.Metal2Group)
178         self.Metal2FermiEnergy.setProperty("value", 3.5)
179         self.Metal2FermiEnergy.setObjectName(_fromUtf8("Metal2FermiEnergy"))
180         self.verticalLayout_10.addWidget(self.Metal2FermiEnergy)
181         self.label_10 = QtGui.QLabel(self.Metal2Group)
182         self.label_10.setObjectName(_fromUtf8("label_10"))
183         self.verticalLayout_10.addWidget(self.label_10)
184         self.Metal2Lattice = QtGui.QDoubleSpinBox(self.Metal2Group)
185         self.Metal2Lattice.setDecimals(5)
186         self.Metal2Lattice.setObjectName(_fromUtf8("Metal2Lattice"))
187         self.verticalLayout_10.addWidget(self.Metal2Lattice)
188         self.horizontalLayout_6.addLayout(self.verticalLayout_10)
189         self.horizontalLayout_4.addWidget(self.Metal2Group)
190         self.verticalLayout_12.addLayout(self.horizontalLayout_4)
```

```
191                 self.splitter_3 = QtGui.QSplitter(self.splitter_4)
192                 self.splitter_3.setOrientation(QtCore.Qt.Horizontal)
193                 self.splitter_3.setObjectName(_fromUtf8("splitter_3"))
194                 self.RunModeling = QtGui.QPushButton(self.splitter_3)
195                 self.RunModeling.setObjectName(_fromUtf8("RunModeling"))
196                 self.FrontOutput = QtGui.QTextBrowser(self.splitter_3)
197                 self.FrontOutput.setMaximumSize(QtCore.QSize(16777215, 16777215))
198                 self.FrontOutput.setObjectName(_fromUtf8("FrontOutput"))
199                 self.verticalLayout_7.addWidget(self.splitter_4)
200                 self.layoutWidget2 = QtGui.QWidget(self.splitter)
201                 self.layoutWidget2.setObjectName(_fromUtf8("layoutWidget2"))
202                 self.verticalLayout_14 = QtGui.QVBoxLayout(self.layoutWidget2)
203                 self.verticalLayout_14.setObjectName(_fromUtf8("verticalLayout_14"))
204                 self.splitter_2 = QtGui.QSplitter(self.layoutWidget2)
205                 self.splitter_2.setOrientation(QtCore.Qt.Vertical)
206                 self.splitter_2.setObjectName(_fromUtf8("splitter_2"))
207                 self.verticalWidget_6 = QtGui.QWidget(self.splitter_2)
208                 self.verticalWidget_6.setObjectName(_fromUtf8("verticalWidget_6"))
209                 self.verticalLayout_8 = QtGui.QVBoxLayout(self.verticalWidget_6)
210                 self.verticalLayout_8.setObjectName(_fromUtf8("verticalLayout_8"))
211                 self.PotentialMPlay = QtGui.QVBoxLayout()
212                 self.PotentialMPlay.setObjectName(_fromUtf8("PotentialMPlay"))
213                 self.verticalLayout_8.addLayout(self.PotentialMPlay)
214                 self.PotentialOutput = QtGui.QTextBrowser(self.splitter_2)
215                 self.PotentialOutput.setMaximumSize(QtCore.QSize(16777215, 16777215))
216                 self.PotentialOutput.setObjectName(_fromUtf8("PotentialOutput"))
217                 self.verticalLayout_14.addWidget(self.splitter_2)
```

```
218                 self.widget = QtGui.QWidget(self.splitter_5)
219                 self.widget.setObjectName(_fromUtf8("widget"))
220                 self.verticalLayout_2 = QtGui.QVBoxLayout(self.widget)
221                 self.verticalLayout_2.setObjectName(_fromUtf8("verticalLayout_2"))
222                 self.ModelingProgress = QtGui.QProgressBar(self.widget)
223                 self.ModelingProgress.setProperty("value", 24)
224                 self.ModelingProgress.setObjectName(_fromUtf8("ModelingProgress"))
225                 self.verticalLayout_2.addWidget(self.ModelingProgress)
226                 self.horizontalLayout_7 = QtGui.QHBoxLayout()
227                 self.horizontalLayout_7.setSizeConstraint(QtGui.QLayout.
                        SetDefaultConstraint)
228                 self.horizontalLayout_7.setObjectName(_fromUtf8("horizontalLayout_7")
                        )
229                 self.label_16 = QtGui.QLabel(self.widget)
230                 self.label_16.setObjectName(_fromUtf8("label_16"))
231                 self.horizontalLayout_7.addWidget(self.label_16)
232                 self.label_15 = QtGui.QLabel(self.widget)
233                 self.label_15.setObjectName(_fromUtf8("label_15"))
234                 self.horizontalLayout_7.addWidget(self.label_15)
235                 self.verticalLayout_2.addLayout(self.horizontalLayout_7)
236                 self.gridLayout.addWidget(self.splitter_5, 0, 0, 1, 1)
237                 MainWindow.setCentralWidget(self.centralwidget)
238                 self.statusbar = QtGui.QStatusBar(MainWindow)
239                 self.statusbar.setObjectName(_fromUtf8("statusbar"))
240                 MainWindow.setStatusBar(self.statusbar)
241
242                 self.retranslateUi(MainWindow)
```

```
243             QtCore.QMetaObject.connectSlotsByName(MainWindow)
244 
245         def retranslateUi(self, MainWindow):
246             MainWindow.setWindowTitle(_translate("MainWindow", "MainWindow", None
                    ))
247             self.groupBox.setTitle(_translate("MainWindow", "Materials", None))
248             self.label.setText(_translate("MainWindow", "Metal 1", None))
249             self.label_2.setText(_translate("MainWindow", "Ferroelectric", None))
250             self.label_3.setText(_translate("MainWindow", "Metal 2", None))
251             self.label_14.setText(_translate("MainWindow", "If you know the metal
                     screening lengths, enter them below and leave lattice constant
                    as 0.\n"
252 " Otherwise, leave them as 0 and enter the lattice constant, and the program will
        calculate an approx. screening length.", None))
253             self.Metal1Group.setTitle(_translate("MainWindow", "Metal 1", None))
254             self.label_4.setText(_translate("MainWindow", "Screening Length (nm)"
                    , None))
255             self.label_5.setText(_translate("MainWindow", "Fermi Energy (eV)",
                    None))
256             self.label_7.setText(_translate("MainWindow", "Lattice Constant (
                    Angstrom)", None))
257             self.FerroGroup.setTitle(_translate("MainWindow", "Ferroelectric",
                    None))
258             self.label_12.setText(_translate("MainWindow", "Dielectric Constant (
                    E_f/E_0)", None))
259             self.label_6.setText(_translate("MainWindow", "Bandgap (eV)", None))
```

```
260                 self.label_9.setText(_translate("MainWindow", "Polarization (micro C/
                        cm^2)", None))
261                 self.label_13.setText(_translate("MainWindow", "Thickness (nm)", None
                        ))
262                 self.Metal2Group.setTitle(_translate("MainWindow", "Metal 2", None))
263                 self.label_11.setText(_translate("MainWindow", "Screening Length (nm)
                        ", None))
264                 self.label_8.setText(_translate("MainWindow", "Fermi Energy (eV)",
                        None))
265                 self.label_10.setText(_translate("MainWindow", "Lattice Constant (
                        Angstrom)", None))
266                 self.RunModeling.setText(_translate("MainWindow", "Model This!\n"
267 "\n"
268 "Output values\n"
269 "will appear to the\n"
270 " right -->\n"
271 "\n"
272 "Energy band is plotted\n"
273 "at far right.\n"
274 "\n"
275 "Further plots will be found\n"
276 " on other tabs.", None))
277                 self.label_16.setText(_translate("MainWindow", "May 2016, sap1951@rit
                        .edu, (585) 236-9510", None))
278                 self.label_15.setText(_translate("MainWindow", "Created by Spencer
                        Pringle for Rochester Institute of Technology, 1 Lomb Drive,
                        Rochester, NY 14623", None))
```

Appendix B: Partial Process - FTJ-devices only

Step Num/ Full Step	Step Code	Step Description	Tool	Time (hrs)
1/1	OX05	pad oxide 500 Å, Tube 4, 45 min at 1000C	Bruce Furnace 4	3
2/2	CV02	1500 ÅSi3N4 LPCVD Deposition, 30 min at 810C	LPCVD Nitride	4
3/3	PH03	level 1- Oxide - Clear Field	ASML & SSI	1
4/4	ET29	Plasma etch Nitride, 1500 Åtarget	LAM 490	0.3
5/5	ET07	ash all photoresist	Gasonics Asher	0.15
6/6	CL01	RCA clean	RCA Bench	0.85
7/7	OX04	First Oxide Tube 1, 3650 ÅBruce 1 Recipe 330, 55 mins at 1000C	Bruce Furnace 1	2.65
8/8	ET06	Etch Oxide, 3650 Åtarget, BOE 7to1 for 3.6 min	7to1 BOE	0.25
9/9	OX04	2nd Oxide Tube 1, 3650 Å, Bruce 1 Recipe 330, 55 mins at 1000C	Bruce Furnace 1	2.65
10/10	ET19	Nitride etch, 30s dip 5:1 BHF, 20 min Hot Phosphoric Acid 175C	Hot Phos Bench	1
11/11	PH03	level 2 Nwell - Dark Field	ASML & SSI	1
12/12	IM01	Cover bottom of wafer: Nwell top, 3E13, P31, 170 KeV	Varian Implanter	2
13/15	IM01	Cover top of wafer, Pwell bottom, 8E13, B11, 80 KeV	Varian Implanter	2
14/16	ET07	ash all photoresist	Gasonics Asher	1
15/17	OX06	Well Drive, Tube 1 Recipe 11, 480 min at 1100C	Bruce Furnace 1	8
16/24	ET06	etch 500 Åpad oxide, 50:1 H_2O:HF (3.6 mins)	50:1 HF Etch	0.25
17/46	PH03	level 10 - P+ D/S - Pimp - Dark Field	ASML & SSI	1

Step Num/ Full Step	Step Code	Step Description	Tool	Time (hrs)
18/47(2)	IM01	Cover bottom of wafer: P+ top 4E15, B11, 50 KeV	Varian Implanter	2
18/47(2)	IM01	Cover top half of wafer: N+ bottom 4E15, P31, 60 KeV	Varian Implanter	2
19/48	ET07	ash all photoresist	Gasonics Asher	0.15
20/49	CL01	RCA clean	RCA Bench	0.85
21/50	OX08	DS Anneal, Bruce 2, 3, Recipe 284, 45 min at 1000C	Bruce Furnace 2	3
22/56	CV03	TEOS, P-5000, 4000 ÅOxide	P5000 TEOS Ch A	0.5
23/57	PH03	Photoresist mask to remove TEOS for ALD HfO2, Thick Resist COATFAC and DEVFAC Recipes - FEHfO2 Level - Dark Field	ASML & SSI	1
24/58	ET06	TEOS Etch for HfO2 area FACCUT, follow with 50:1 HF dip	Drytek Quad	0.5
25/59	ET07	Solvent Strip or Ash	Solvent Strip Bench	0.5
26/60	CV33	ALD HfO2 Deposition w/ TiN	ALD	4
27/61	RT02	RTP 1 min,800C	RTP	1
28/62	PH03	(optional) Half wafer protect	Karl Suss Contact Aligner Stepper	0.5
29/63	ET06	TiN wet etch with RCA 1 NH4OH:H2O2:H2O = 1:2:5 (APM) solution at 60 C. (1nm/s, [39])	Hot Plate with Pyrex Dish	1

Step Num/ Full Step	Step Code	Step Description	Tool	Time (hrs)
30/64	ET07	(optional) Solvent Strip or Ash	Solvent Strip Bench	0.5
31/65	PH03	Photoresist mask to remove HfO2 if not selective growth (Negative Resist) - FEHfO2 Level - Dark Field	ASML & SSI	1
32/66	ET06	HfO2 etch, 50:1 H2O:HF appx. 97s for 3nm HfO2, assuming 1:10 HfO2:SiO2 selectivity. [40]	50:1 HF Etch	0.25
33/67	ET07	Solvent Strip or Ash	Gasonics Asher	0.15
34/68	PH03	level 11 - CC, Thick Resist COATFAC and DEVFAC Recipes - Cont level - dark field	ASML & SSI	1
35/69	ET06	CC etch, FACCUT, 200 W, 100 mT, 50 sccm CHF3, 10 sccm CF4, 100 sccm Ar	Drytek Quad	0.5
36/70	ET07	ash all photoresist	Gasonics Asher	0.15
37/71	CL01	RCA clean	RCA Bench	0.85
38/72	ME01	Aluminum Sputter 7500 Å	CVC601	1
39/73	PH03	level 12 - Metal1, Thick resist, COATMTL and DEVMTL recipes, clear field	ASML & SSI	1
40/74	ET15	plasma 125W, Al Etch, BCl, Cl2, Chloroform, Target 7500 Å	LAM4600	1.5
41/75	ET07	ash all photoresist	Gasonics Asher	0.15

Appendix C: Athena code

```
1   #Full process for CMOS portion of Thesis
2
3   go athena
4
5   line x loc=0.0 spac=0.02
6   line x loc=96.6 spac=0.02
7   #
8   line y loc=0.00 spac=0.02
9   line y loc=2 spac=0.02
10  line y loc=3 spac=0.1
11  line y loc=5 spac=0.1
12
13  method grid.oxide=.01 gridinit.ox=.01
14
15  # INITIALIZE MATERIAL
16  #
        ---------------------------------------------------
17
18  #
19  init silicon boron resistivity=10 orientation=100
        space.mult=3.0
20
21  #OX05
22  diffus time=27 temp=25 t.final=800 nitro
23  diffus time=20 temp=800 t.final=1000 f.o2=5
24  diffus time=50 temp=1000 f.o2=10
25  diffus time=5 temp=1000 f.n2=15
26  diffus time=40 temp=1000 t.final=800 f.n2=10
27  diffus time=15 temp=800 t.final=25 f.n2=5
28
29  #CV02
30  deposit nitride thick=0.15
31
32  #PH03
33  deposit photoresist thick=1.00
34  etch photoresist start x=39.10 y=-2.00
35  etch cont x=49.10 y=-2.00
36  etch cont x=49.10 y=3.00
37  etch cont x=39.10 y=3.00
38  etch done x=39.10 y=-2.00
39  etch photoresist start x=87.60 y=-2.00
40  etch cont x=91.60 y=-2.00
41  etch cont x=91.60 y=3.00
42  etch cont x=87.60 y=3.00
43  etch done x=87.60 y=-2.00
44  etch photoresist left p1.x=2
45  etch photoresist right p1.x=93.6
46
47  #ET29
48  etch nitride right p1.x=93.6
49  etch nitride start x=39.10 y=-2.00
50  etch cont x=49.10 y=-2.00
51  etch cont x=49.10 y=3.00
52  etch cont x=39.10 y=3.00
53  etch done x=39.10 y=-2.00
54  etch nitride start x=87.60 y=-2.00
55  etch cont x=91.60 y=-2.00
56  etch cont x=91.60 y=3.00
57  etch cont x=87.60 y=3.00
58  etch done x=87.60 y=-2.00
59  etch nitride left p1.x=2
60
61  #ET07
62  etch photoresist all
63
64  #CL01
65
66
67  #OX04
68  diffus time=27 temp=25 t.final=800 nitro
69  diffus time=20 temp=800 t.final=1000 f.n2=5
70  diffus time=5 temp=1000  f.o2=2
71  diffus time=50 temp=1000  f.h2=3.6 f.o2=2
72  diffus time=5 temp=1000 f.n2=15
73  diffus time=40 temp=1000 t.final=800 f.n2=10
74  diffus time=15 temp=800 t.final=25 f.n2=5
75
76  #ET06
77  rate.etch machine=BOE(7to1) oxide u.m wet.etch
        isotropic=0.1
78  etch machine=BOE(7to1) time=3.6 minutes
79
80  #OX04
81  diffus time=27 temp=25 t.final=800 nitro
82  diffus time=20 temp=800 t.final=1000 f.n2=5
83  diffus time=5 temp=1000  f.o2=2
84  diffus time=50 temp=1000  f.h2=3.6 f.o2=2
85  diffus time=5 temp=1000 f.n2=15
86  diffus time=40 temp=1000 t.final=800 f.n2=10
87  diffus time=15 temp=800 t.final=25 f.n2=5
88
89  #ET19
90  etch nitride all
91
92  #PH03
93  deposit photoresist thick=1.00
94  etch photoresist start x=0.00 y=-2.00
95  etch cont x=44.10 y=-2.00
96  etch cont x=44.10 y=3.00
97  etch cont x=0.00 y=3.00
98  etch done x=0.00 y=-2.00
99  etch photoresist start x=90.60 y=-2.00
100 etch cont x=94.6 y=-2.00
101 etch cont x=94.6 y=3.00
```

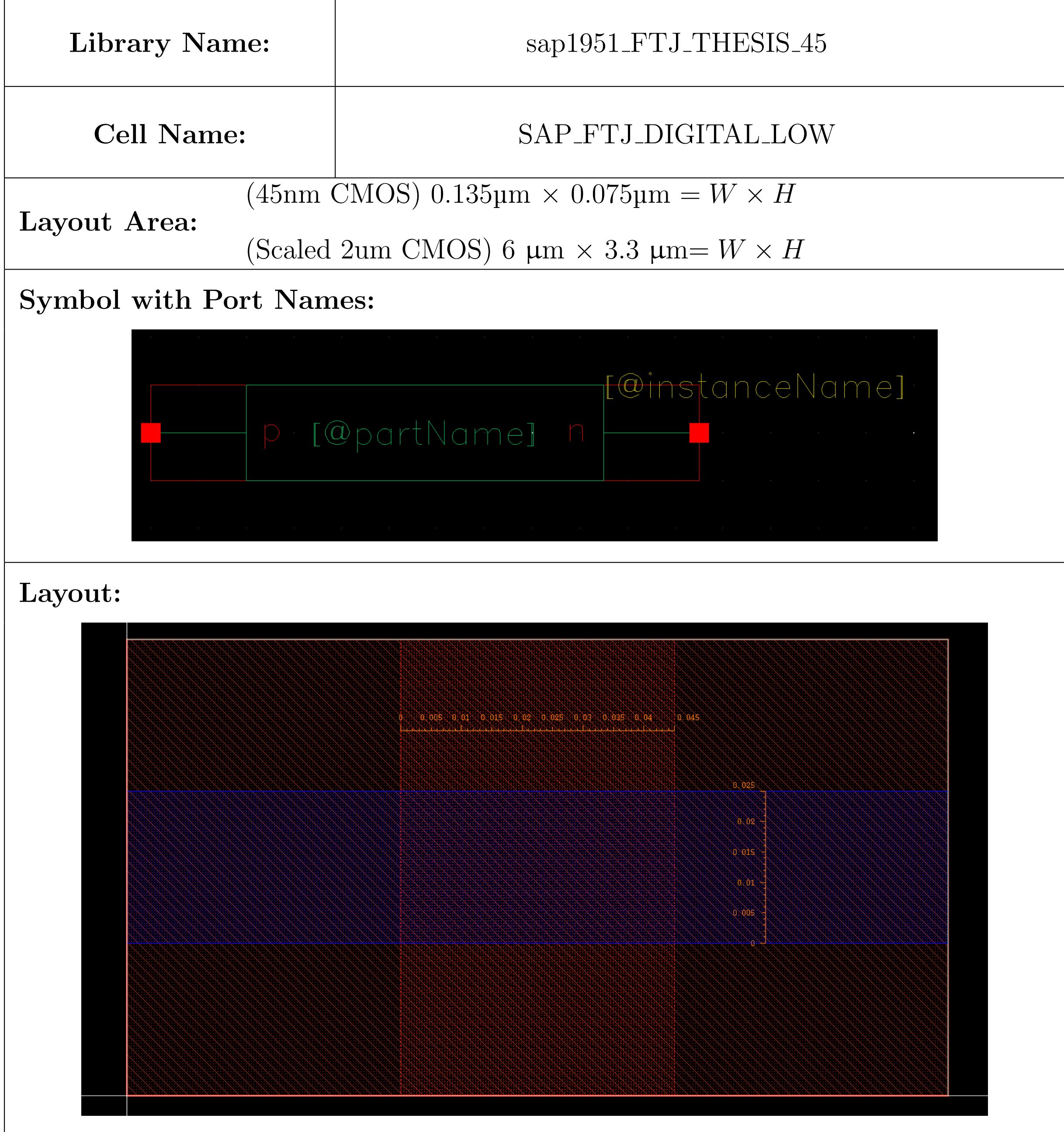
```
102 etch cont x=90.6 y=3.00
103 etch done x=0.00 y=-2.00
104
105 #IM01
106
107 implant phosphor dose=3.0e13 energy=170 tilt=0
        rotation=0 crystal
108
109 #ET07
110 etch photoresist all
111
112 #PH03
113 deposit photoresist thick=1.00
114 etch photoresist start x=44.1 y=-2.00
115 etch cont x=88.6 y=-2.00
116 etch cont x=88.6 y=3.00
117 etch cont x=44.1 y=3.00
118 etch done x=44.1 y=-2.00
119
120 #IM01
121 implant boron dose=8.0e13 energy=80 tilt=0
        rotation=0 crystal
122
123 #ET07
124 etch photoresist all
125
126 #OX06
127 diffus time=27 temp=25 t.final=800 nitro
128 diffus time=30 temp=800 t.final=1100 f.n2=10
129 diffus time=360 temp=1100  f.n2=10
130 diffus time=5 temp=1100 f.n2=10
131 diffus time=60 temp=1100 t.final=800 f.n2=10
132 diffus time=12 temp=800 t.final=25 f.n2=5
133
134 #PH03
135 deposit photoresist thick=1.00
136 etch photoresist start x=44.1 y=-2.00
137 etch cont x=88.6 y=-2.00
138 etch cont x=88.6 y=3.00
139 etch cont x=44.1 y=3.00
140 etch done x=44.1 y=-2.00
141 etch photoresist left p1.x=2
142
143 #IM01
144 implant phosphor dose=7.95e12 energy=60 tilt=0
        rotation=0 crystal
145
146 #ET07
147 etch photoresist all
148
149 #PH03
150 deposit photoresist thick=1.00
151 etch photoresist start x=2.00 y=-2.00
152 etch cont x=44.10 y=-2.00
153 etch cont x=44.10 y=3.00
154 etch cont x=2.00 y=3.00
155 etch done x=2.00 y=-2.00
156
157 #IM01
158 implant boron dose=3.02e12 energy=30 tilt=0
        rotation=0 crystal
159
160 #ET07
161 etch photoresist all
162
163 struct outfile = CMOSWellandVt.str
164 #tonyplot CMOSWellandVt.str
165
166 #ET06
167 rate.etch machine=H2O_HF(50to1) oxide n.m wet.etch
         isotropic=18.7
168 etch machine=H2O_HF(50to1) time=3.6 minutes
169
170 #CL01
171
172
173 #ET06
174
175
176 #OX06
177 deposit oxide thick=0.01
178
179 #CV01
180 deposit polysilicon thick=0.40
181
182 #PH03
183 deposit photoresist thick=1.00
184 etch photoresist left p1.x=30.6
185 etch photoresist start x=32.60 y=-2.00
186 etch cont x=55.60 y=-2.00
187 etch cont x=55.60 y=3.00
188 etch cont x=32.60 y=3.00
189 etch done x=32.60 y=-2.00
190 etch photoresist right p1.x=57.60
191
192 #ET08
193 etch polysilicon left p1.x=30.6
194 etch polysilicon start x=32.60 y=-2.00
195 etch cont x=55.60 y=-2.00
196 etch cont x=55.60 y=3.00
197 etch cont x=32.60 y=3.00
198 etch done x=32.60 y=-2.00
199 etch polysilicon right p1.x=57.60
200
201 #ET07
202 etch photoresist all
203
204 #CL01
205
206
207 #OX05
208 diffus time=27 temp=25 t.final=800 nitro
```

```
209 deposit oxide thick=0.05
210 diffus time=20 temp=800 t.final=1000 f.n2=5
211 diffus time=50 temp=1000 f.n2=10
212 diffus time=5 temp=1000 f.n2=15
213 diffus time=40 temp=1000 t.final=800 f.n2=10
214 diffus time=15 temp=800 t.final=25 f.n2=5
215
216 #PH03
217 deposit photoresist thick=4.00
218 etch photoresist start x=10.00 y=-6.00
219 etch cont x=44.30 y=-6.00
220 etch cont x=44.30 y=3.00
221 etch cont x=10.00 y=3.00
222 etch done x=10.00 y=-6.00
223 etch photoresist start x=80.60 y=-6.00
224 etch cont x=88.6 y=-6.00
225 etch cont x=88.6 y=3.00
226 etch cont x=80.6 y=3.00
227 etch done x=80.6 y=-6.00
228
229 #IM01
230 implant boron dose=4e14 energy=50 tilt=0 rotation
        =0 crystal
231
232 #ET07
233 etch photoresist all
234
235 #PH03
236 deposit photoresist thick=4.00
237 etch photoresist start x=44.30 y=-6.00
238 etch cont x=80.60 y=-6.00
239 etch cont x=80.60 y=3.00
240 etch cont x=44.30 y=3.00
241 etch done x=44.30 y=-6.00
242 etch photoresist left p1.x=10
243
244 #IM01
245 implant phosphor dose=4e14 energy=60 tilt=0
        rotation=0 crystal
246
247 #ET07
248 etch photoresist all
249
250 #CL01
251 struct outfile = CMOSPreNitride.str
252
253 #CV02
254 deposit nitride thick=0.35
255
256 #ET39
257 etch nitride dry thick=0.40
258
259 #PH03
260 deposit photoresist thick=4.00
261 etch photoresist start x=44.30 y=-6.00
262 etch cont x=80.60 y=-6.00
263 etch cont x=80.60 y=3.00
264 etch cont x=44.30 y=3.00
265 etch done x=44.30 y=-6.00
266 etch photoresist left p1.x=10
267
268 #IM01
269 implant phosphor dose=2.7e13 energy=60 tilt=0
        rotation=0 crystal
270
271 #ET07
272 etch photoresist all
273
274 #PH03
275 deposit photoresist thick=4.00
276 etch photoresist start x=10.00 y=-6.00
277 etch cont x=44.30 y=-6.00
278 etch cont x=44.30 y=3.00
279 etch cont x=10.00 y=3.00
280 etch done x=10.00 y=-6.00
281 etch photoresist start x=80.60 y=-6.00
282 etch cont x=88.6 y=-6.00
283 etch cont x=88.6 y=3.00
284 etch cont x=80.6 y=3.00
285 etch done x=80.6 y=-6.00
286 etch photoresist start x=90.60 y=-2.00
287 etch cont x=94.6 y=-2.00
288 etch cont x=94.6 y=3.00
289 etch cont x=90.6 y=3.00
290 etch done x=0.00 y=-2.00
291
292 #IM01
293 implant boron dose=2.7e13 energy=50 tilt=0
        rotation=0 crystal
294
295 #ET07
296 etch photoresist all
297
298 #CL01
299 struct outfile = CMOSPostNitride.str
300
301 #OX08
302 diffus time=27 temp=25 t.final=800 nitro
303 diffus time=20 temp=800 t.final=1000 f.n2=5
304 diffus time=20 temp=1000  f.n2=10
305 diffus time=5 temp=1000 f.n2=15
306 diffus time=40 temp=1000 t.final=800 f.n2=10
307 diffus time=15 temp=800 t.final=25 f.n2=5
308
309 #ET06
310 rate.etch machine=H2O_HF(50to1) oxide n.m wet.etch
         isotropic=18.7
311 etch machine=H2O_HF(50to1) time=3 minutes
312
313 #was 3.6 minutes
314
315 struct outfile = CMOSSD2.str
```

```
316 #tonyplot CMOSSD.str
317
318 #ME03
319
320
321 #RT01
322
323
324 #ET11
325
326
327 #RT02
328
329
330 #CV03
331 deposit oxide thick=0.50 divisions=20
332 #added the divisions=20
333
334 #PH03
335 deposit photoresist thick=1.00
336 etch photoresist start x=4.00 y=-6.00
337 etch cont x=6.00 y=-6.00
338 etch cont x=6.00 y=3.00
339 etch cont x=4.00 y=3.00
340 etch done x=4.00 y=-6.00
341 etch photoresist start x=11.00 y=-6.00
342 etch cont x=13.00 y=-6.00
343 etch cont x=13.00 y=3.00
344 etch cont x=11.00 y=3.00
345 etch done x=11.00 y=-6.00
346 etch photoresist start x=35.60 y=-6.00
347 etch cont x=37.60 y=-6.00
348 etch cont x=37.60 y=3.00
349 etch cont x=35.60 y=3.00
350 etch done x=35.60 y=-6.00
351 etch photoresist start x=50.10 y=-6.00
352 etch cont x=52.10 y=-6.00
353 etch cont x=52.10 y=3.00
354 etch cont x=50.10 y=3.00
355 etch done x=50.10 y=-6.00
356 etch photoresist start x=74.80 y=-6.00
357 etch cont x=76.80 y=-6.00
358 etch cont x=76.80 y=3.00
359 etch cont x=74.80 y=3.00
360 etch done x=74.80 y=-6.00
361 etch photoresist start x=83.60 y=-6.00
362 etch cont x=85.60 y=-6.00
363 etch cont x=85.60 y=3.00
364 etch cont x=83.60 y=3.00
365 etch done x=83.60 y=-6.00
366 etch photoresist start x=90.60 y=-6.00
367 etch cont x=94.60 y=-6.00
368 etch cont x=94.60 y=3.00
369 etch cont x=90.60 y=3.00
370 etch done x=90.60 y=-6.00
371
372
373 #ET06
374 etch oxide dry thick=0.5
375
376 #ET07
377 etch photoresist all
378
379 #CL01
380
381
382 #ME01
383 deposit aluminum thick=0.75
384
385 #PH03
386 deposit photoresist thick=1.30
387 etch photoresist left p1.x=2.00
388 etch photoresist start x=14.00 y=-6.00
389 etch cont x=34.60 y=-6.00
390 etch cont x=34.60 y=3.00
391 etch cont x=14.00 y=3.00
392 etch done x=14.00 y=-6.00
393 etch photoresist start x=53.60 y=-6.00
394 etch cont x=73.80 y=-6.00
395 etch cont x=73.80 y=3.00
396 etch cont x=53.60 y=3.00
397 etch done x=53.60 y=-6.00
398 etch photoresist start x=87.60 y=-6.00
399 etch cont x=92.10 y=-6.00
400 etch cont x=92.10 y=3.00
401 etch cont x=87.60 y=3.00
402 etch done x=87.60 y=-6.00
403
404 #ET15
405 etch aluminum dry thick=1.00
406
407 #ET07
408 etch photoresist all
409
410 struct outfile = CMOSComplete2.str
411 tonyplot CMOSComplete2.str
412
413 quit
```

Appendix D: sap1951_FTJ_THESIS_45

D.1 Linear Resistance FTJ Model



Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_FTJ_DIGITAL_LOW
Layout Area:	(45nm CMOS) 0.135µm × 0.075µm = $W \times H$ (Scaled 2um CMOS) 6 µm × 3.3 µm= $W \times H$
Symbol with Port Names:	
Layout:	

D.1.1 Verilog Model

```
1   // VerilogA for sap1951_FTJ_THESIS_45,
       SAP_FTJ_DIGITAL_LOW, veriloga
2
3   `include "constants.vams"
4   `include "disciplines.vams"
5   `timescale 10ps/1fs
6
7   module SAP_FTJ_DIGITAL_LOW(p, n);
8
9   inout p;
10  electrical p;
11  inout n;
12  electrical n;
13
14  parameter R_pos = 1e6;          // On
       resistance 9e6
15  parameter R_neg = 1e7;    // Off resistance
         1.4e8
16  parameter dr = 34.35e6;    // abs(R_pos -
       R_neg) 1.31e8
17  parameter dt = 40; //20
18  parameter x0 = 0.5;
19  parameter v_pos = 0.3;          //
20  parameter v_neg = -0.3;            //
21
```

```
22          real Rm;
23          real Vm;
24          real Im;
25          integer voltages;          // voltages
               file pointer
26          integer currents;          // currents
               file pointer
27
28          analog begin
29          @(initial_step) begin
30          voltages = $fopen("voltages.out");
31          currents = $fopen("currents.out");
32          Rm = (1-x0)*R_neg + x0*R_pos;
33          end
34
35          // Get the terminal voltage
36          Vm = V(p,n);
37
38          // Change the memristance
39          if ((Rm > R_pos)&&(Vm>=v_pos))
40          begin
41          Rm=Rm-(dr/dt);
42          end
43          if ((Rm < R_neg)&&(Vm<=v_neg))
44          begin
45          Rm=Rm+(dr/dt);
46          end
```

```
47
48                  Im = Vm / Rm;
49                  I(p,n) <+ Im;
50
51                  $fstrobe(voltages,"%g",Vm);
52                  $fstrobe(currents,"%g",Im);
53
54                  @(final_step)
55                  begin
56                  $fclose(voltages);
57                  $fclose(currents);
58                  end
59                  end
60
61                  endmodule
```

D.2 Polarization-Timing FTJ Model

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_FTJ_DIGITAL_LOW_TIMING
Layout Area:	(45nm CMOS)0.135µm $\times$ 0.075µm $= W \times H$ (Scaled 2um CMOS)6 µm $\times$ 3.3 µm$= W \times H$
Symbol with Port Names:	
Layout:	

D.2.1 Verilog Model

```
1  // VerilogA for sap1951_FTJ_THESIS,
     SAP_FTJ_DIGITAL_LOW_TIMING, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5  `timescale 1ns/1ps
6
7  module SAP_FTJ_DIGITAL_LOW_TIMING(p, n);
8
9  inout p;
10 electrical p;
11 inout n;
12 electrical n;
13
14 parameter Vc=0.4;  //0.3
15 parameter Vc0=0.9;
16 parameter kb=1.38e-23;
17 parameter pi=3.14159;
18 parameter m0=9.11e-31;
19 parameter mstar=0.11;
20 parameter q=1.6e-19;
21 parameter h=6.626e-34;
22 real hbar=h/(2*pi);
23 parameter heV=4.13e-15;
24 parameter T=300;
```

```
25                  real kT=(kb/q)*T;
26
27                  real Rm;
28                  real Vm;
29                  real Vd;
30                  real Im;
31                  real sigmap;
32                  real sigmas;
33                  real Pot1;
34                  real Pot2;
35                  real Pot;
36
37                  parameter AA=445.402;
38                  parameter AB=118.125;
39                  parameter AC=7.782;
40                  parameter BA=-416.102;
41                  parameter BB=-112.071;
42                  parameter BC=-7.525;
43                  parameter ALA=22;
44                  parameter ALB=5.8;
45                  parameter ALC=0.26;
46                  real d=10*Vc*1e-9;
47                  parameter delta1=0.06*1e-9;
48                  parameter delta2=3.0*1e-9; //0.4*1e-9
49                  parameter epsilonf=40;
50                  parameter epsilon0=8.854e-12;
51                  parameter Ea=2;
```

```
52                parameter Ef1=4.08;
53                parameter Ef2=5.12;
54                real Atun=sqrt((2*m0*q*mstar))*(d)*(2)/
                     hbar;
55                real J0=(6.08e8)/((d*1e9)**2);
56                parameter Dim=500; //dimension of FTJ (in
                     nm) assuming area of Dim^2
57
58
59                real A;
60                real Av1;
61                real Av2;
62                real B;
63                real Bv1;
64                real Bv2;
65                real C;
66                real Cv1;
67                real Cv2;
68                real D;
69                real Dv1;
70                real Dv2;
71                real E;
72
73                real Pr1;
74                real Pr2;
75                real Pr3;
76                real Pr4;
```

```
77                real Pr5;
78                real Pr6;
79                real Pr7;
80
81                real Pr21;
82                real Pr22;
83                real Pr23;
84                real Pr24;
85                real Pr25;
86                real Pr26;
87                real Pr27;
88
89                real time0;
90                real time1;
91                real currenttime;
92
93
94                real tPr[0:13];
95                real Pr[0:13];
96                real tSat[0:13] = '{1e-2, 5e-4, 5e-3, 1e
                     -4, 5e-6, 5e-6, 5e-6, 5e-6, 2e-6, 2e-6,
                      2e-6, 1e-6, 1e-6, 1e-6};
97
98                real Prtotal;
99                real Jtun;
100
101               integer voltages;
```

```
102         integer currents;
103         integer i;
104
105         analog begin
106         @(initial_step) begin
107         voltages = $fopen("voltages.out");
108         currents = $fopen("currents.out");
109         Rm = 1.3e7;
110         time0 = 1e-13;
111         //$display("The coercive voltage is
               currently %e at %e seconds", Vc,
               $abstime);
112         //$display("J0 is %e and Atun is %e", J0,
               Atun);
113         //$display("4 is %e and 4**2 is %e", 4,
               4**2);
114         end
115         //Get terminal voltage
116         Vm=V(p,n);
117
118         //Move along time values of applicable
               polarization domains
119
120         Vd=0.4;
121
122         time1 = $abstime;
```

```
123                 //$display("time1 became %e at %e", time1,
                        $abstime);
124
125                 for (i=0;i<14;i=i+1)
126                 begin
127                 if (abs(Vm)>(Vd*Vc/Vc0))
128                 begin
129
130                 if ((Vm<0) && (tPr[i]>(0-tSat[i])))
131                 begin
132                 tPr[i] = tPr[i]-(time1-time0);
133                 end
134                 else if ((Vm>0) && (tPr[i]<tSat[i]))
135                 tPr[i] = tPr[i]+(time1-time0);
136                 //if (Vd>1.7)
137                 //      $display("Current time is %e while
                        the saturation time is %e for voltage
                       of %e", tPr[i], tSat[i], Vd);
138                 //$display("The polarization time for
                       domain between %e and %e is %e at time
                       %e",Vd-0.2,Vd,tPr[i],$abstime);
139                 //Calculate A value for Pr .4
140                 Av1 = AA*Vd+BA;
141                 Av2 = ALA*Vd;
142                 if (Av1>Av2)
143                 A=Av1;
144                 else
```

```
145                 A=Av2;
146                 //$display("A = %e",A);
147                 //Calculate B value for Pr .4
148                 Bv1 = AB*Vd+BB;
149                 Bv2 = ALB*Vd;
150                 if (Bv1>Bv2)
151                 B=Bv1;
152                 else
153                 B=Bv2;
154                 //$display("B = %e",B);
155                 //Calculate C value for Pr .4
156                 Cv1 = AC*Vd+BC;
157                 Cv2 = ALC*Vd;
158                 if (Cv1>Cv2)
159                 C=Cv1;
160                 else
161                 C=Cv2;
162                 //$display("C = %e",C);
163                 //Calculate D value for Pr .4
164                 Dv1 = 9.904*Vd+17.865;
165                 Dv2 = 19.375*(Vd**2)-6.3*Vd+1.4;
166                 if (Dv1>Dv2)
167                 D=Dv2;
168                 else
169                 D=Dv1;
170                 //$display("D = %e",D);
171                 //Calculate E value for Pr .4
```

```
172                 E = 9.105*Vd-5.152-3.387*(Vd**2);
173                 if (E<0.217)
174                 E=0.217;
175                 //$display("E = %e",E);
176                 Pr4 = A+B*log((Vc0/Vc)*abs(tPr[i]))+C*(log
                       ((Vc0/Vc)*abs(tPr[i]))**2);
177                 Pr3 = D+E*ln((Vc0/Vc)*abs(tPr[i]));
178                 Pr2 = 6.339*Vd+27.357;
179                 Pr1 = 13.071*(Vd**2.929);
180
181                 if (Pr4<0)
182                 Pr4 = 0;
183                 if (Pr3<Pr4)
184                 Pr5 = Pr3;
185                 else
186                 Pr5 = Pr4;
187
188                 if (Pr5<0)
189                 Pr5 = 0;
190
191                 if (Pr1<Pr2)
192                 Pr6 = Pr1;
193                 else
194                 Pr6 = Pr2;
195
196                 if (Pr5<Pr6)
197                 Pr7 = Pr5;
```

```
198            else
199            Pr7 = Pr6;
200
201            //Calculate A value for Pr .2
202            Av1 = AA*(Vd-0.2)+BA;
203            Av2 = ALA*(Vd-0.2);
204            if (Av1>Av2)
205            A=Av1;
206            else
207            A=Av2;
208            //Calculate B value for Pr .2
209            Bv1 = AB*(Vd-0.2)+BB;
210            Bv2 = ALB*(Vd-0.2);
211            if (Bv1>Bv2)
212            B=Bv1;
213            else
214            B=Bv2;
215            //Calculate C value for Pr .2
216            Cv1 = AC*(Vd-0.2)+BC;
217            Cv2 = ALC*(Vd-0.2);
218            if (Cv1>Cv2)
219            C=Cv1;
220            else
221            C=Cv2;
222            //Calculate D value for Pr .2
223            Dv1 = 9.904*(Vd-0.2)+17.865;
```

```
224                 Dv2 = 19.375*((Vd-0.2)**2)-6.3*(Vd-0.2)
                       +1.4;
225                 if (Dv1>Dv2)
226                 D=Dv2;
227                 else
228                 D=Dv1;
229                 //Calculate E value for Pr .2
230                 E = 9.105*(Vd-0.2)-5.152-3.387*((Vd-0.2)
                       **2);
231                 if (E<0.217)
232                 E=0.217;
233 
234                 Pr24 = A+B*log((Vc0/Vc)*abs(tPr[i]))+C*(
                       log((Vc0/Vc)*abs(tPr[i]))**2);
235                 Pr23 = D+E*ln((Vc0/Vc)*abs(tPr[i]));
236                 Pr22 = 6.339*(Vd-0.2)+27.357;
237                 Pr21 = 13.071*((Vd-0.2)**2.929);
238 
239                 if (Pr24<0)
240                 Pr24 = 0;
241                 if (Pr23<Pr24)
242                 Pr25 = Pr23;
243                 else
244                 Pr25 = Pr24;
245 
246                 if (Pr25<0)
247                 Pr25 = 0;
```

```
248
249                 if (Pr21<Pr22)
250                 Pr26 = Pr21;
251                 else
252                 Pr26 = Pr22;
253
254                 if (Pr25<Pr26)
255                 Pr27 = Pr25;
256                 else
257                 Pr27 = Pr26;
258
259                 Pr[i] = Pr7 - Pr27;
260
261                 if (tPr[i]<0)
262                 Pr[i] = 0-Pr[i];
263
264                 //$display("Polarization values used were
                       (in order) %e %e %e %e %e %e %e %e %e %
                       e %e %e %e %e",Pr1,Pr2,Pr3,Pr4,Pr5,Pr6,
                       Pr7,Pr21,Pr22,Pr23,Pr24,Pr25,Pr26,Pr27)
                       ;
265
266                 end
267                 //$display("The for loop just completed Vd
                        = %e, at time %e", Vd, time1);
268                 Vd = Vd+0.2;
269                 end
```

```
270
271                 Prtotal =0.5*( Pr[0] + Pr[1] + Pr[2] + Pr
                       [3] + Pr[4] + Pr[5] + Pr[6] + Pr[7] +
                       Pr[8] + Pr[9] + Pr[10] + Pr[11] + Pr
                       [12] + Pr[13]);
272
273                 //$display("The total polarization is
                       currently %e at %e seconds", Prtotal,
                       $abstime);
274
275                 sigmap=Prtotal*1e-2;
276                 //$display("sigma_p is %e", sigmap);
277                 sigmas=sigmap*d/(epsilonf*(delta1+delta2)+
                       d);
278                 //$display("sigma_s is %e", sigmas);
279
280                 Pot1=(sigmas*delta1/epsilon0)+Ea;
281                 //$display("Pot1 is %e", Pot1);
282                 Pot2=Ea+Ef2-Ef1-(sigmas*delta2/epsilon0);
283                 //$display("Pot2 is %e", Pot2);
284                 Pot=(Pot1+Pot2)/2;
285                 //$display("Average potential barrier is %
                       e", Pot);
286                 Jtun=J0*((Pot)*exp(-Atun*sqrt(Pot))-(Pot+
                       Vm)*exp(-Atun*sqrt(Pot+Vm)));
287                 //$display("Current density in A/cm^2 is %
                       e", Jtun);
```

```
288
289                 Rm = Vm/(Jtun*((Dim*1e-7)**2));
290
291                 time0 = $abstime;
292                 //$display("time0 became %e at %e", time0,
                        $abstime);
293                 Im = Vm / Rm;
294                 I(p,n) <+ Im;
295
296                 $fstrobe(voltages,"%g",Vm);
297                 $fstrobe(currents,"%g",Im);
298
299                 @(final_step)
300                 begin
301                 $fclose(voltages);
302                 $fclose(currents);
303                 end
304
305                 //$display("The total polarization is
                       currently %e at %e seconds", Prtotal,
                       $abstime);
306
307                 end
308
309
310                 endmodule
```

D.3 SAP_ADDRESS_COLUMN_R

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_ADDRESS_COLUMN_R

Function/Truth Table:

Ren	$WenN$	Y
0	0	X
0	1	X
1	0	X
1	1	v_{ssa}

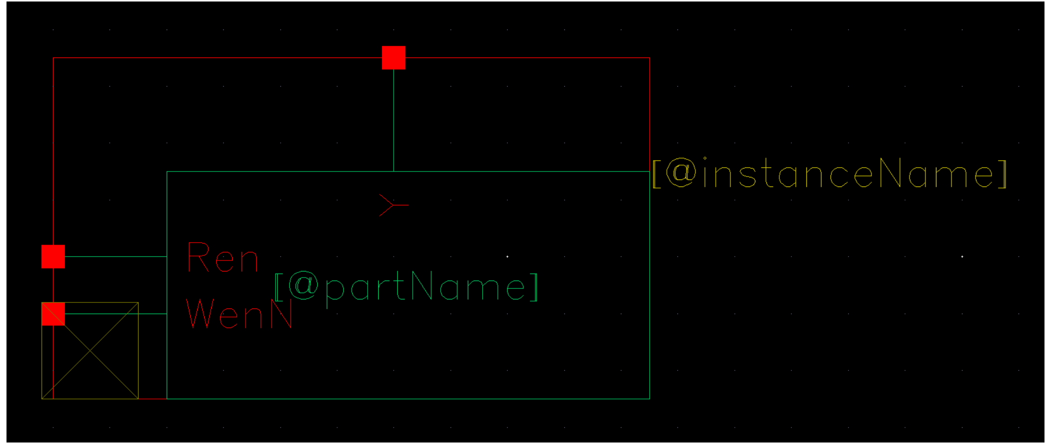
Propagation Delay (t_{pdf} and t_{pdr}) and Output Rise/Fall Time (t_f and t_r):

In	Out	t_{pdf}	t_{pdr}	t_{f}	t_{r}
Ren	Y	561.8×10^{-12}	603.1×10^{-12}	473.3×10^{-12}	1.498×10^{-9}
WenN	Y	552.2×10^{-12}	701.6×10^{-12}	464.5×10^{-12}	1.746×10^{-9}

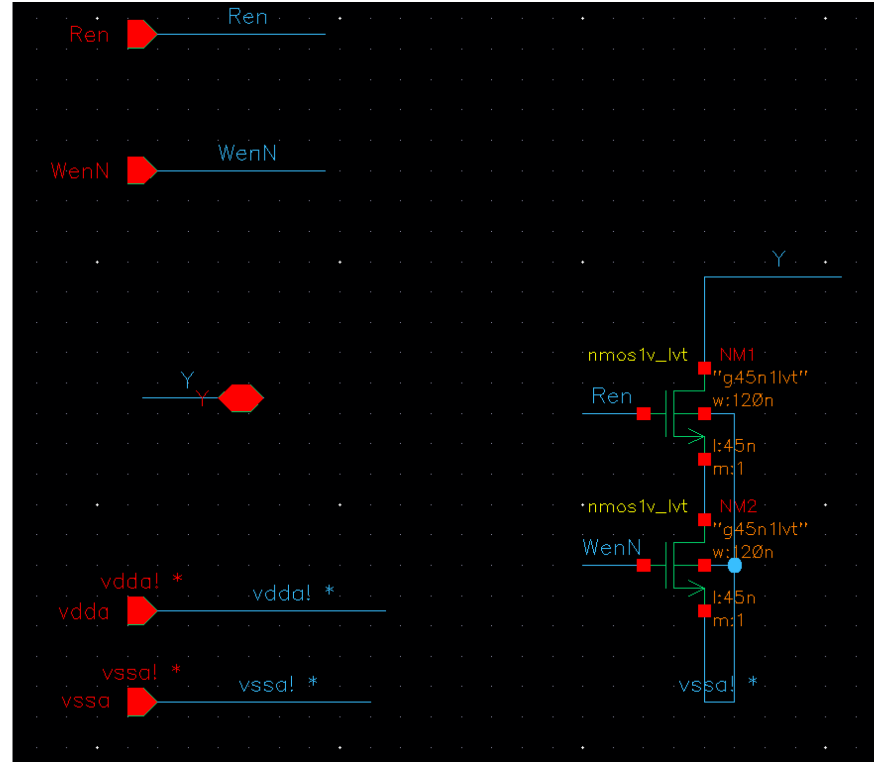
Notice long t_r because this device doesn't drive the output high, it can only drag it down to v_{ssa}.

Layout Area: $0.6\text{µm} \times 1.71\text{µm} = W \times H$

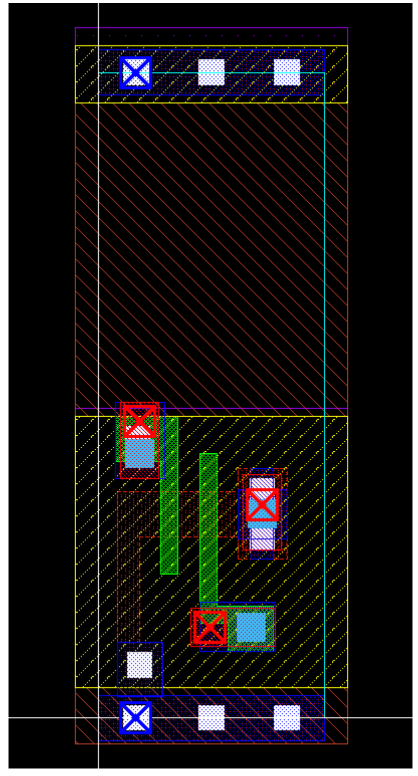
Symbol with Port Names:



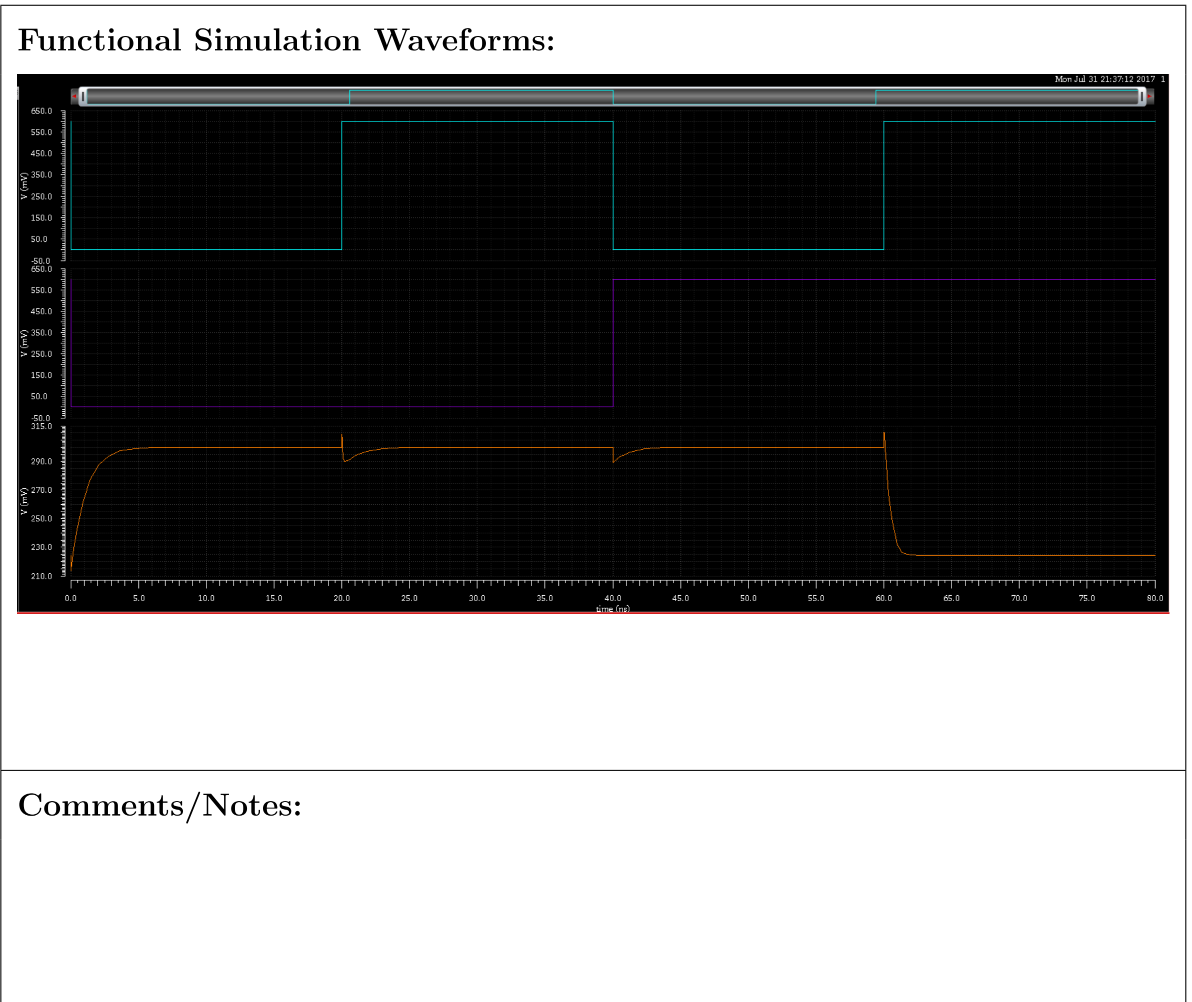
Schematic:



Layout:



Functional Simulation Waveforms:



Comments/Notes:

D.4 SAP_ADDRESS_COLUMN_W

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_ADDRESS_COLUMN_W

Function/Truth Table:

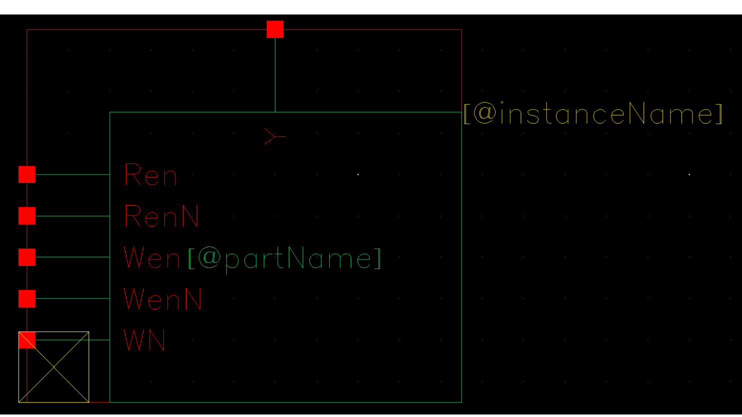
Wen	$WenN$	WN	Ren	$RenN$	Y
0	1	0	1	0	X
0	1	1	1	0	X
0	1	0	0	1	X
0	1	1	0	1	X
1	0	0	1	0	X
1	0	1	1	0	X
1	0	0	0	1	VDD
1	0	1	0	1	VSS

Propagation Delay (t_{pdf} and t_{pdr}) and Output Rise/Fall Time (t_{f} and t_{r}):

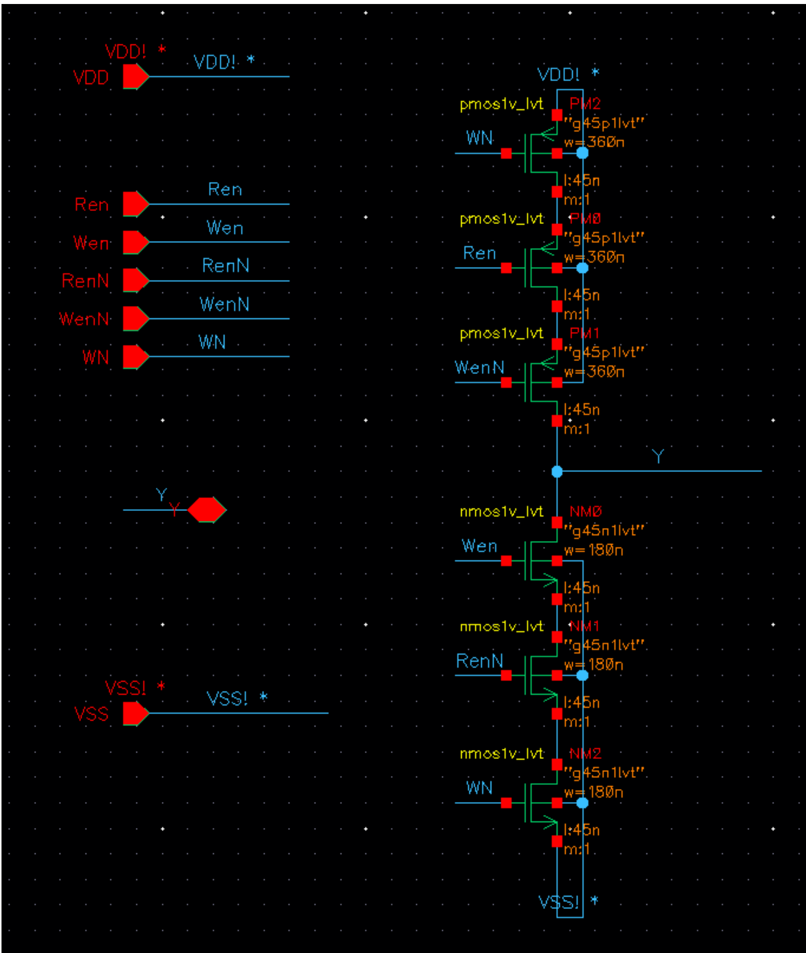
In	Out	t_{pdf}	t_{pdr}	t_{f}	t_{r}
Wen	Y	208×10^{-12}	75.14×10^{-12}	122.4×10^{-12}	97.83×10^{-12}
WN	Y	66.89×10^{-12}	177.0×10^{-12}	54.9×10^{-12}	94.81×10^{-12}
Ren	Y	102.8×10^{-12}	99.16×10^{-12}	191.4×10^{-12}	82.92×10^{-12}

Layout Area: $0.8\mu\mathrm{m} \times 1.71\mu\mathrm{m} = W \times H$

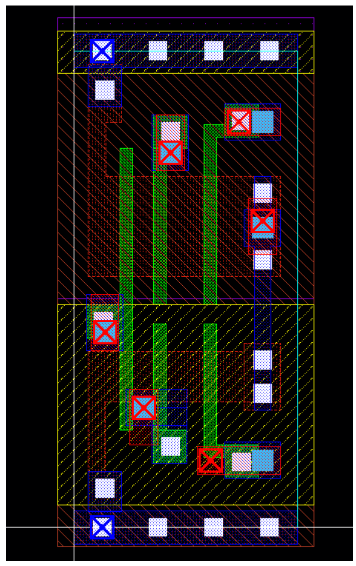
Symbol with Port Names:



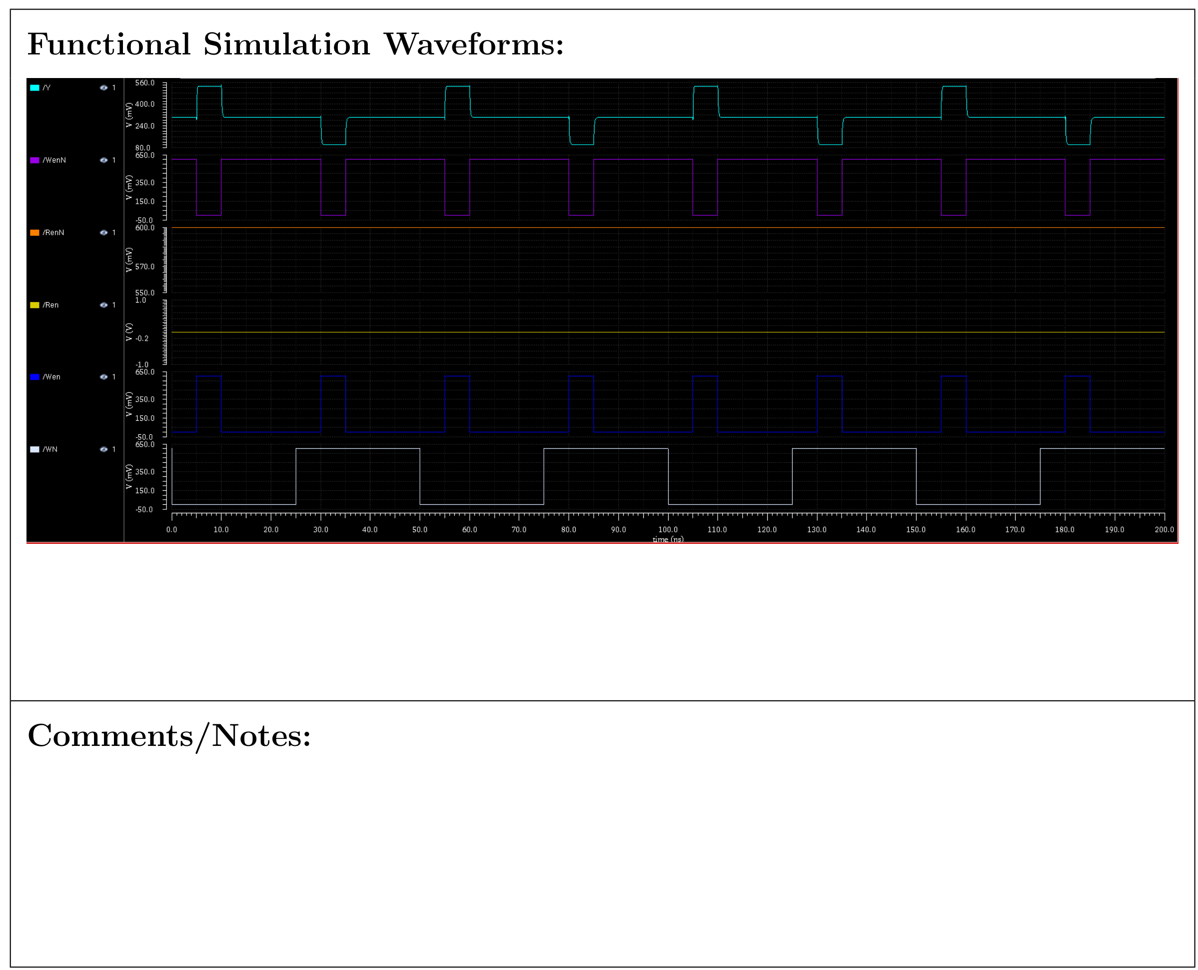
Schematic:



Layout:



Functional Simulation Waveforms:



Comments/Notes:

D.5 SAP_ADDRESS_ROW_R

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_ADDRESS_ROW_R

Function/Truth Table:

$RenN$	Wen	Y
0	0	v_{dda}
0	1	X
1	0	X
1	1	X

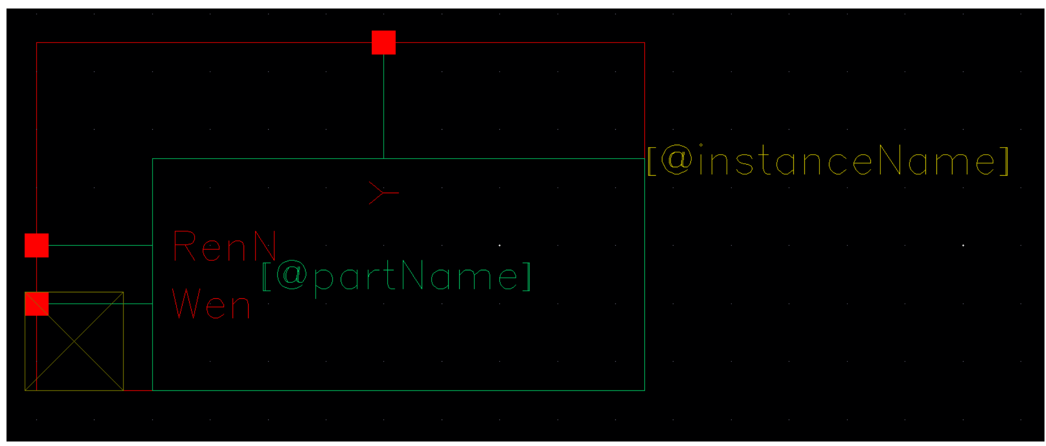
Propagation Delay (t_{pdf} and t_{pdr}) and Output Rise/Fall Time (t_f and t_r):

In	Out	t_{pdf}	t_{pdr}	t_{f}	t_{r}
RenN	Y	-	513.9×10^{-12}	-	433.7×10^{-9}
Wen	Y	-	465.7×10^{-12}	-	451.3×10^{-9}

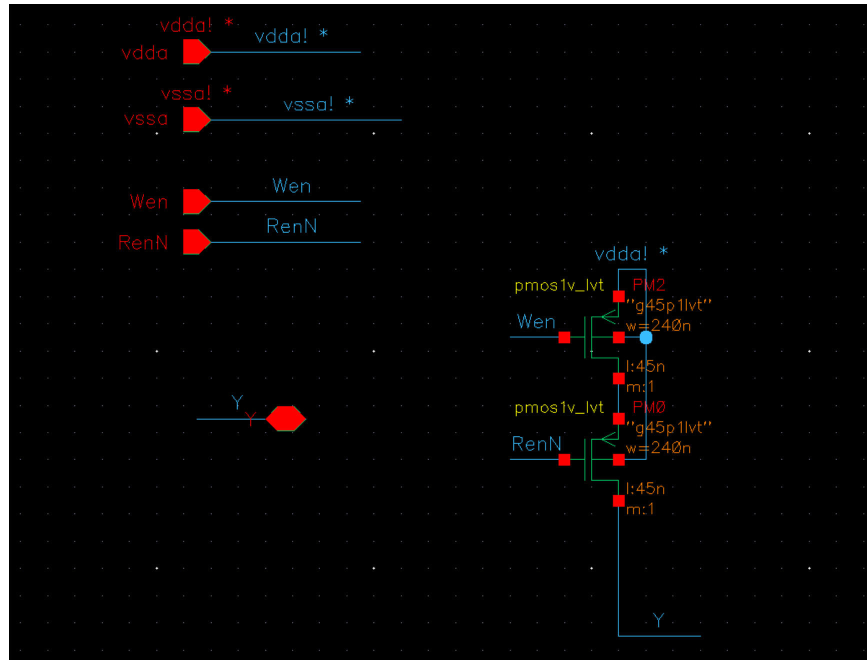
Notice long t_r because this device doesn't drive the output high, it can only drag it down to v_{ssa}.

Layout Area: 0.6µm $\times$ 1.71µm $= W \times H$

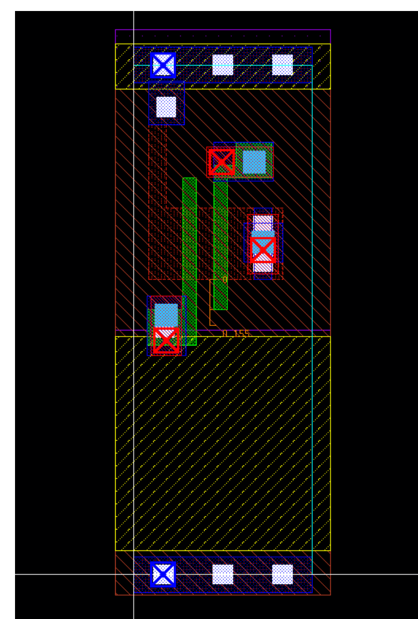
Symbol with Port Names:



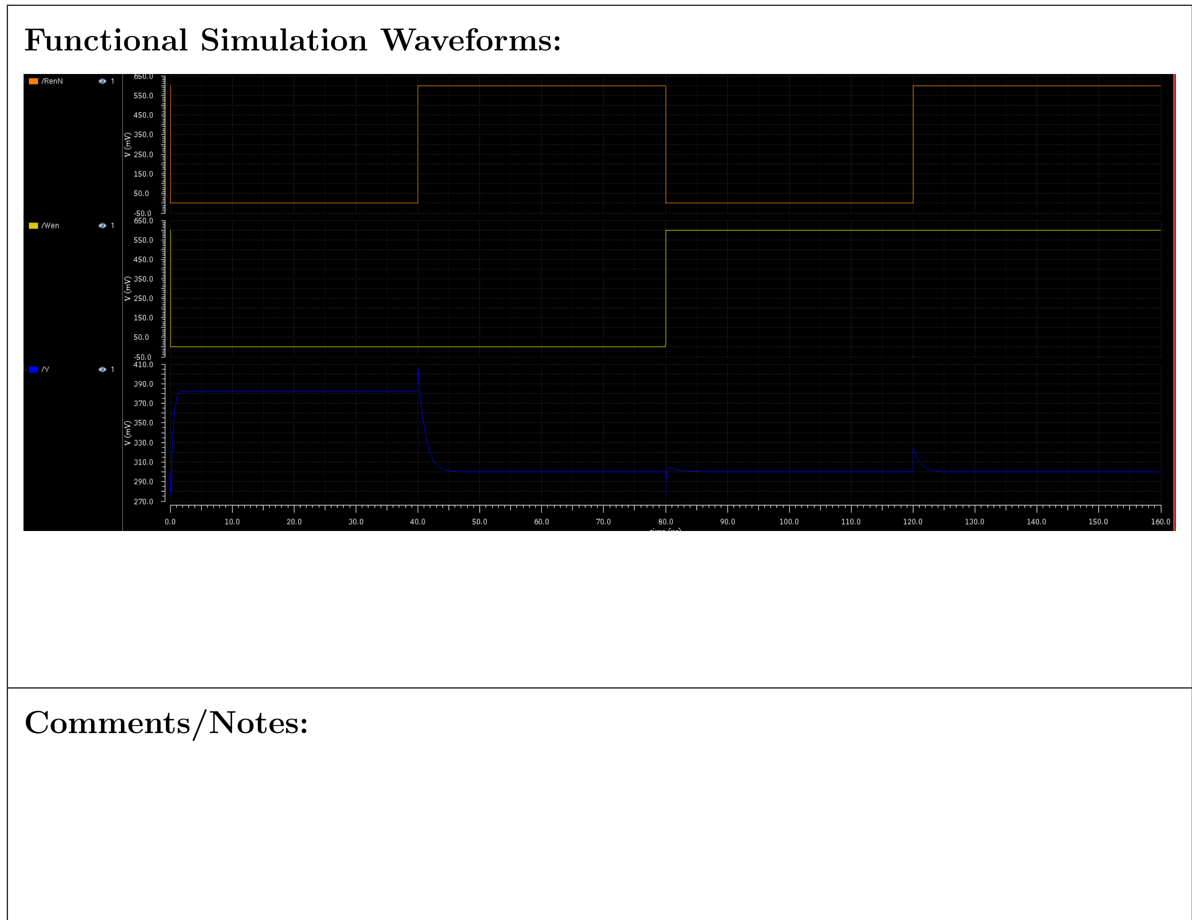
Schematic:



Layout:



Functional Simulation Waveforms:



Comments/Notes:

D.6 SAP_ADDRESS_ROW_W

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_ADDRESS_ROW_W

Function/Truth Table:

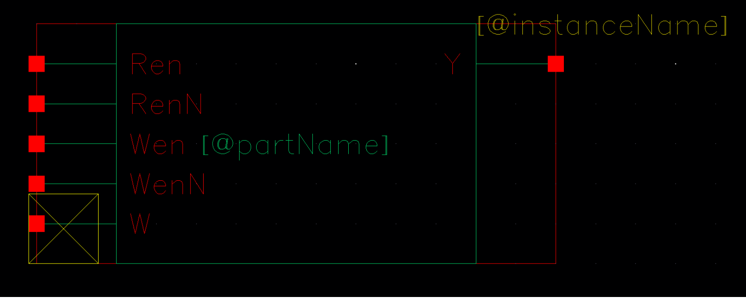
Wen	$WenN$	W	Ren	$RenN$	Y
0	1	0	1	0	X
0	1	1	1	0	X
0	1	0	0	1	X
0	1	1	0	1	X
1	0	0	1	0	X
1	0	1	1	0	X
1	0	0	0	1	VDD
1	0	1	0	1	VSS

Propagation Delay (t_{pdf} and t_{pdr}) and Output Rise/Fall Time (t_{f} and t_{r}):

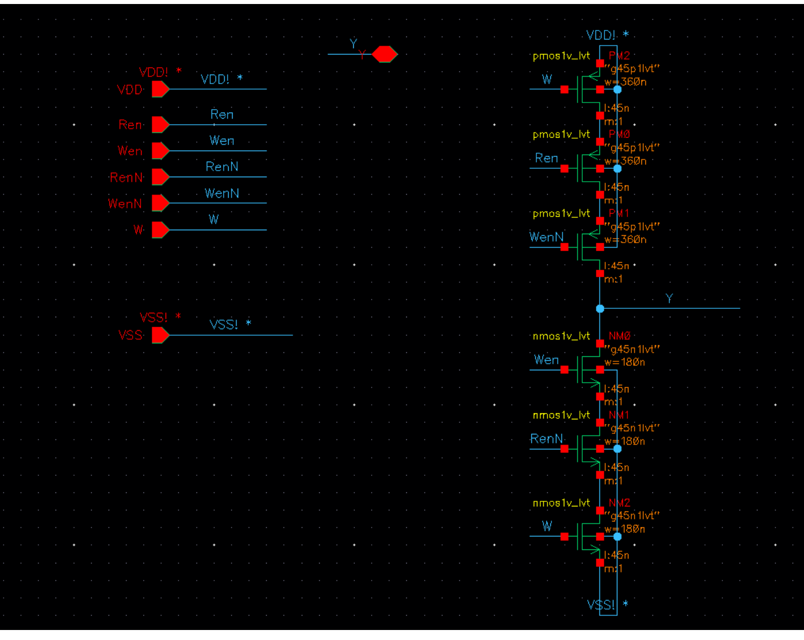
In	Out	t_{pdf}	t_{pdr}	t_{f}	t_{r}
Wen	Y	208.7×10^{-12}	103.4×10^{-12}	124.0×10^{-12}	79.94×10^{-12}
W	Y	68.36×10^{-12}	181.5×10^{-12}	116.8×10^{-12}	94.81×10^{-12}
Ren	Y	102.4×10^{-12}	99.75×10^{-12}	116.2×10^{-12}	90.66×10^{-12}

Layout Area: 0.8µm $\times$ 1.71µm $= W \times H$

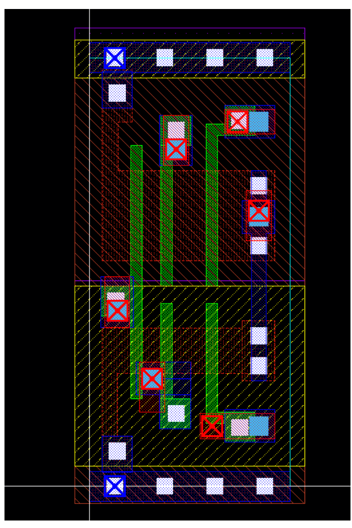
Symbol with Port Names:



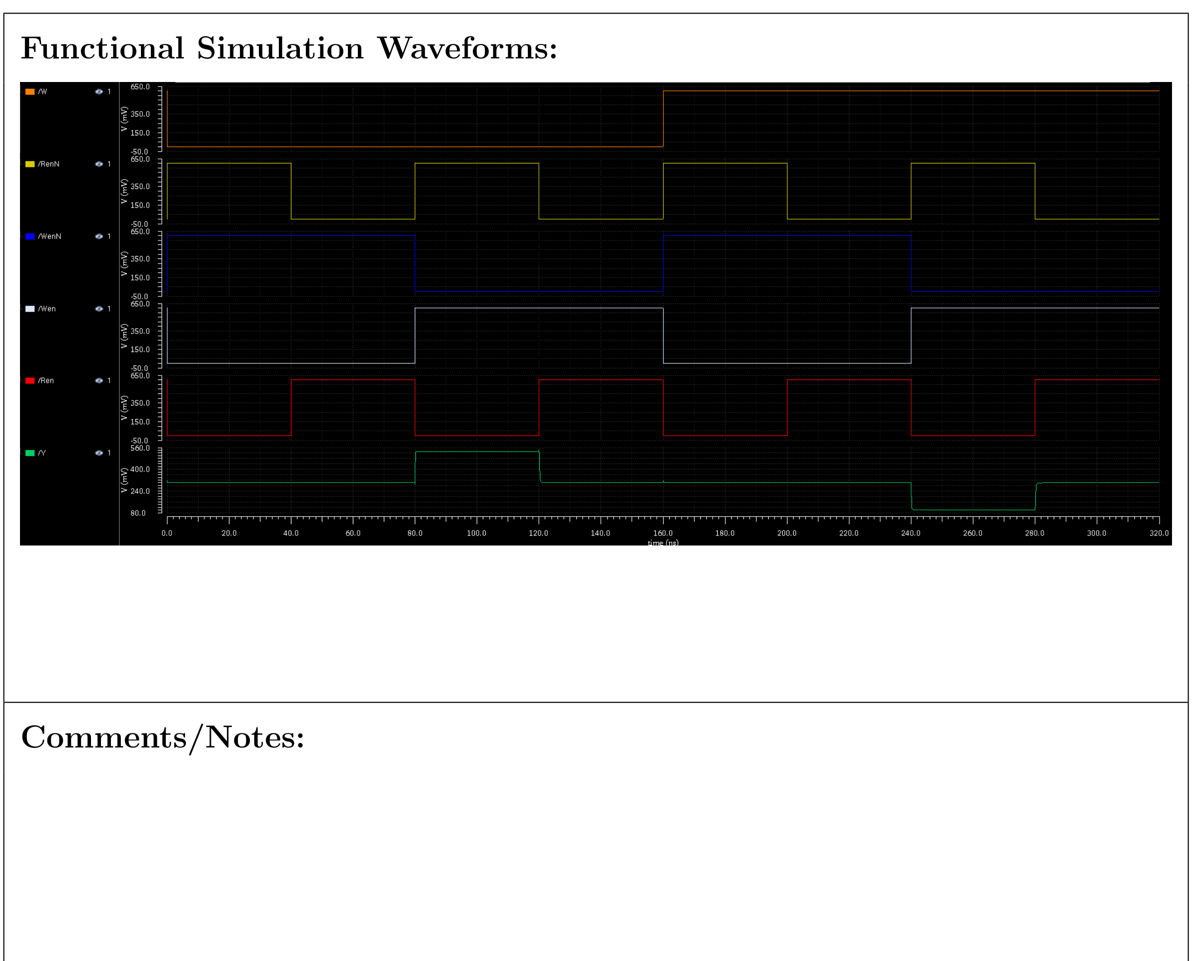
Schematic:



Layout:



Functional Simulation Waveforms:



Comments/Notes:

D.7 SAP_ADDRESS_GND_vcc

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_ADDRESS_GND_vcc

Function/Truth Table:

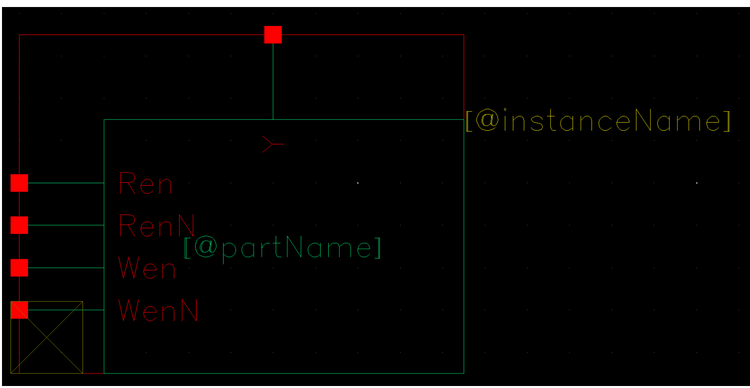
Wen	$WenN$	Ren	$RenN$	Y
0	1	1	0	X
0	1	0	1	VCC
1	0	1	0	X
1	0	0	1	X

Propagation Delay (t_{pdf} and t_{pdr}) and Output Rise/Fall Time (t_{f} and t_{r}):

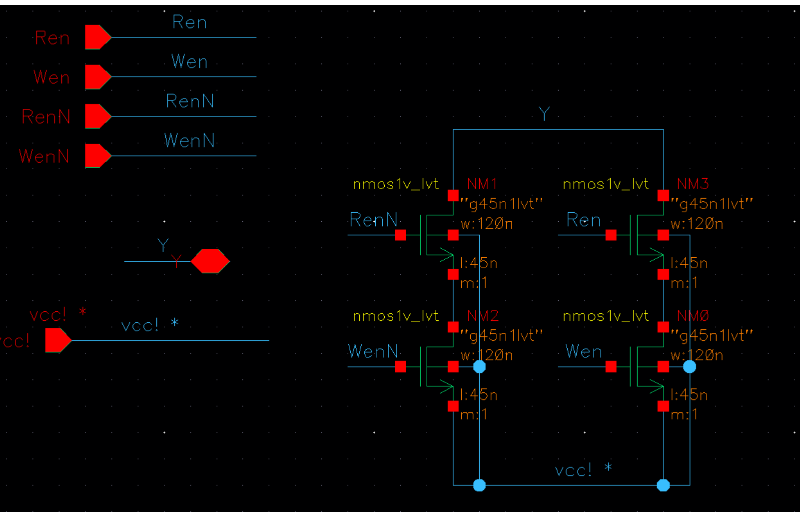
In	Out	t_{pdf}	t_{pdr}	t_{f}	t_{r}
Wen	Y	-	165.0×10^{-12}	-	191.9×10^{-12}
Ren	Y	-	158.4×10^{-12}	-	188.9×10^{-12}

Layout Area: $0.8\mu\text{m} \times 1.71\mu\text{m} = W \times H$

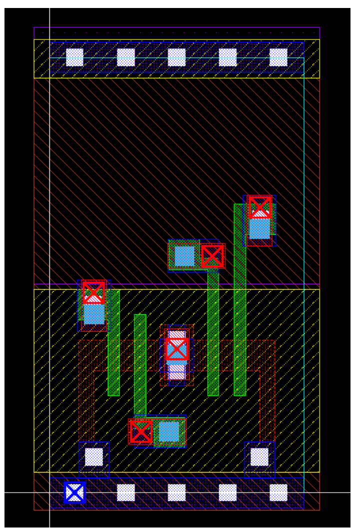
Symbol with Port Names:



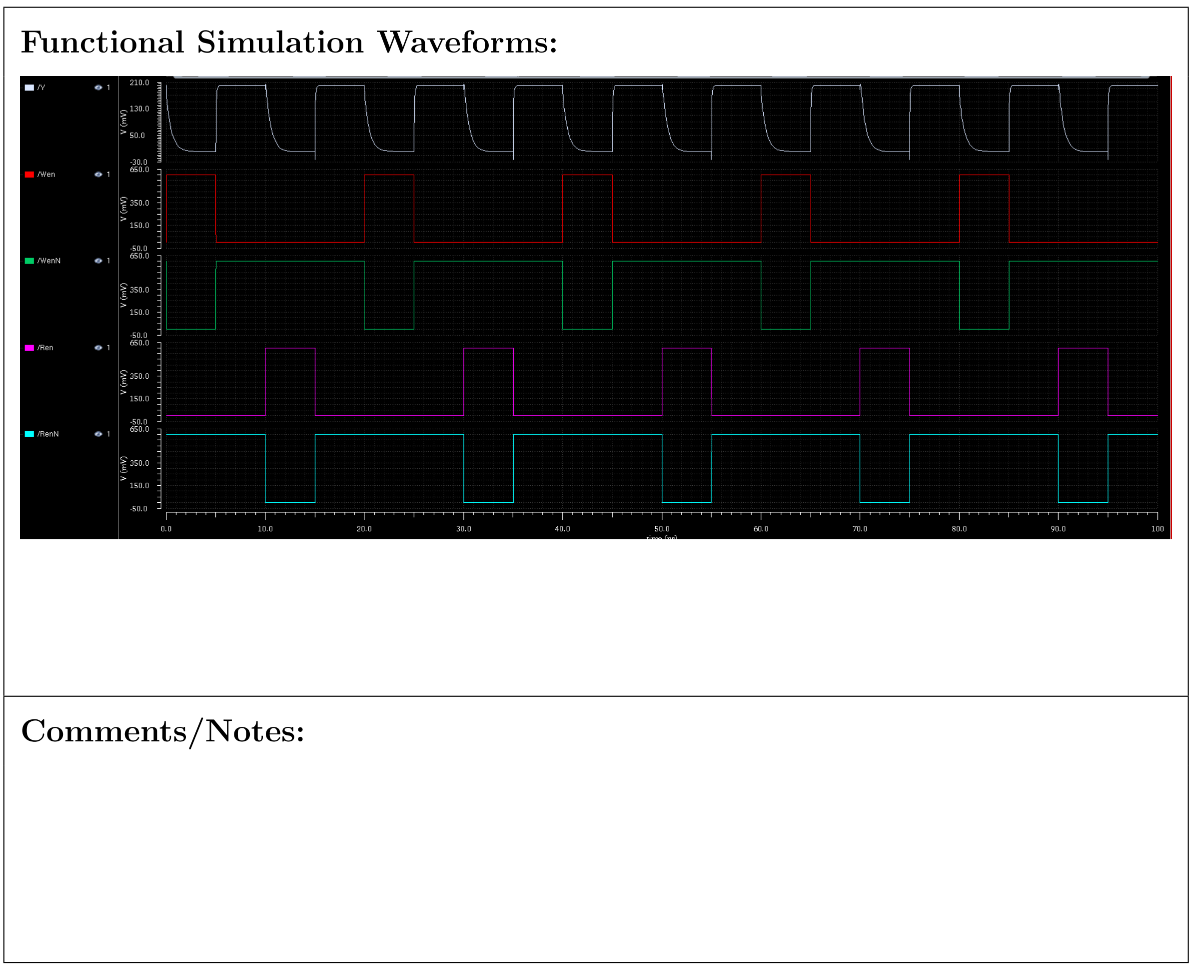
Schematic:



Layout:



Functional Simulation Waveforms:



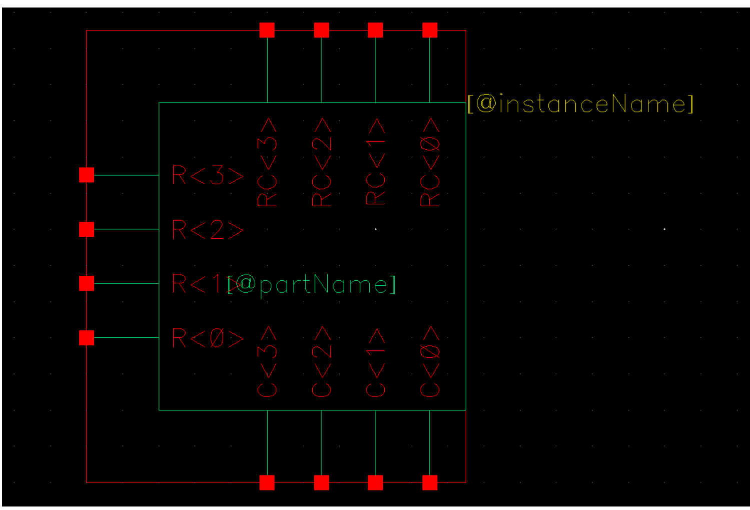
Comments/Notes:

D.8 SAP_FTJ_DIGITAL_LOW_4_x_4

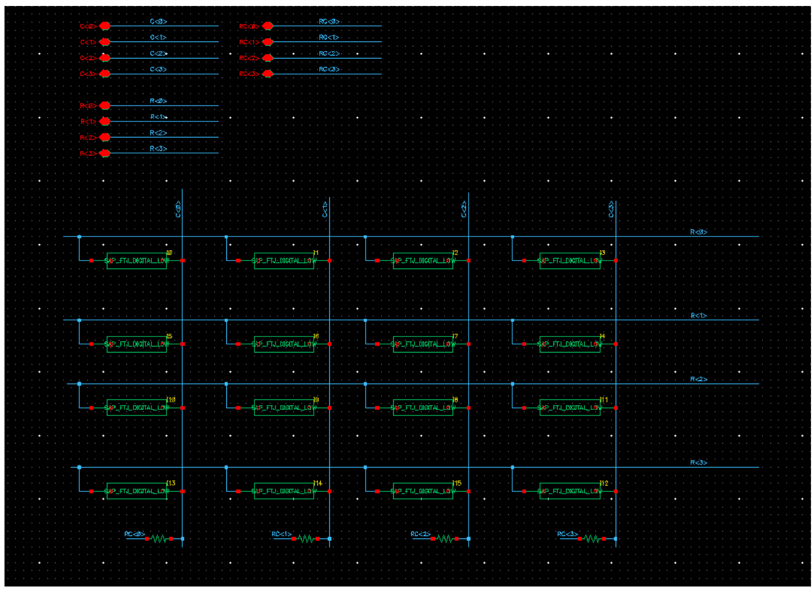
Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_FTJ_DIGITAL_LOW_4_x_4

Layout Area: 2.07µm × 1.985µm = $W \times H$

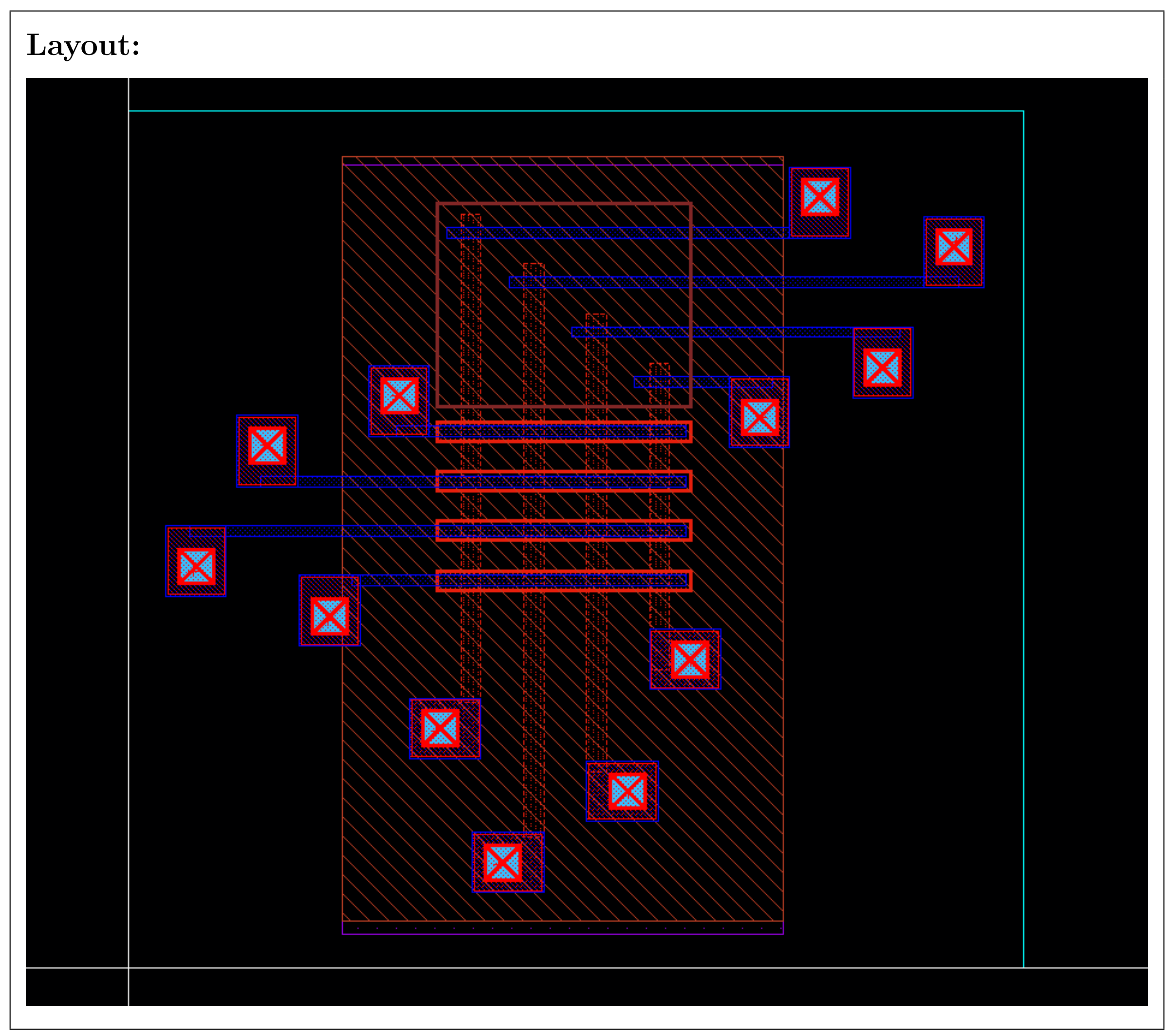
Symbol with Port Names:



Schematic:



Layout:

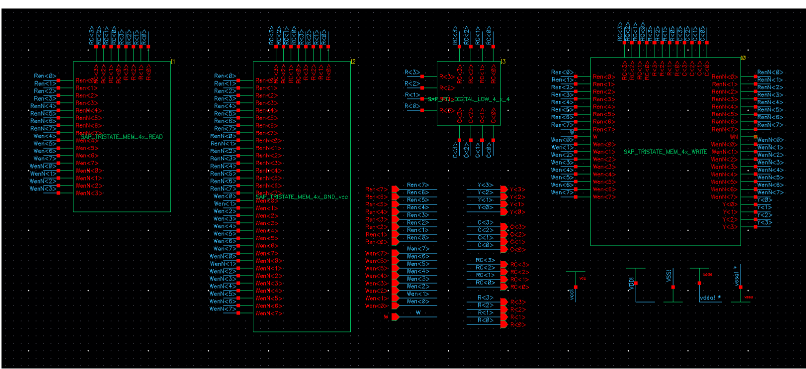


D.9 SAP_TRISTATE_MEM_4x_vcc

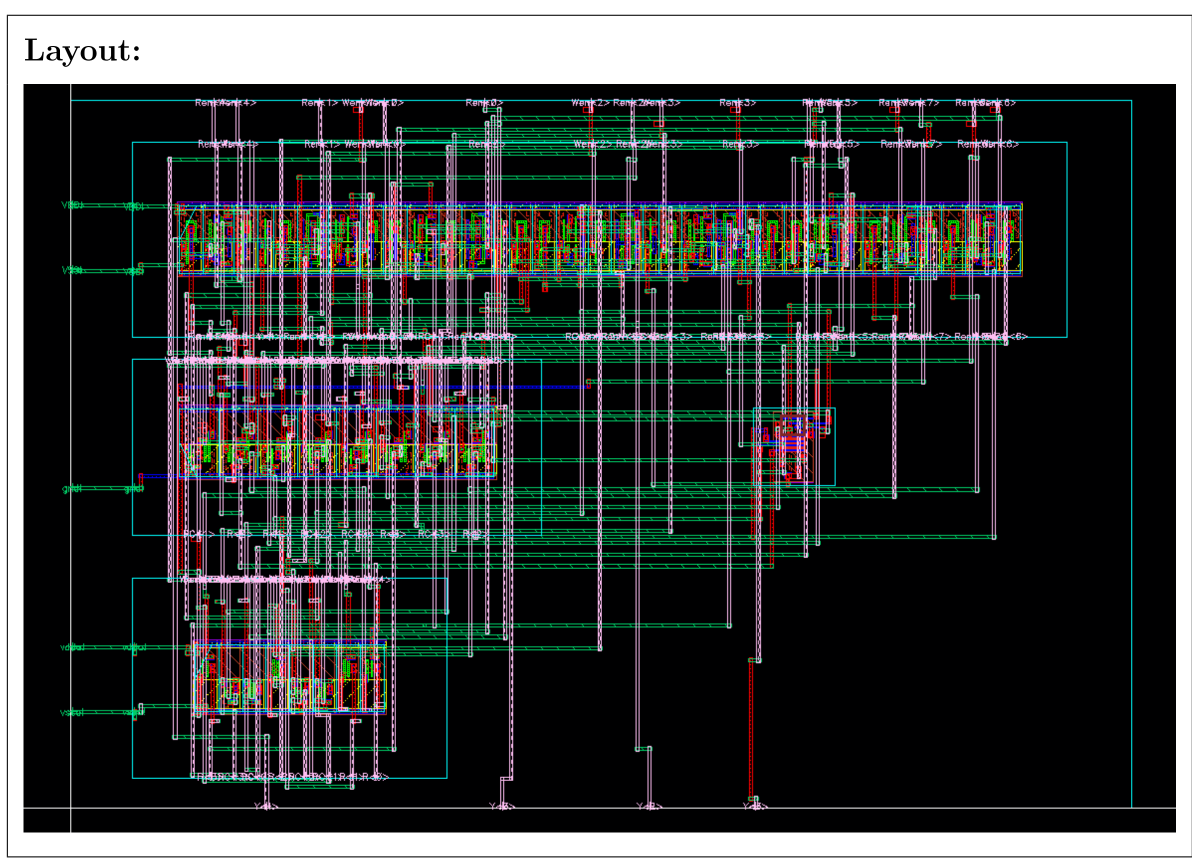
Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_TRISTATE_MEM_4x_vcc
Layout Area: 27 µm × 18 µm = $W \times H$	

Symbol with Port Names:

Schematic:



Layout:



D.10 SAP_TRISTATE_MEM_4x_TESTBENCH

Library Name:	sap1951_FTJ_THESIS_45
Cell Name:	SAP_TRISTATE_MEM_4x_TESTBENCH
Symbol with Port Names:	

D.10.1 Verilog Model

```
1   //Verilog HDL for "sap1951_FTJ_THESIS_45",
      "SAP_TRISTATE_MEM_4x_TESTBENCH" "
      functional"
2   `timescale 10 ns / 1 fs
3   module SAP_TRISTATE_MEM_4x_TESTBENCH(Ren,
      W, Wen, Y, Y_out);
4
5   input [3:0] Y;
6   output [7:0] Ren, W, Wen;
7   output [3:0] Y_out;
8
9   reg [7:0] Ren, W, Wen;
10
11  reg [3:0] val;
12  integer out;
13  integer outnot;
14  reg [3:0] bg;
15
16  integer errors;
17  integer bgerrors;
18  integer disterrors;
19
20  wire [3:0] Y_out = Y ;
21
22  initial
```

```
23                      begin
24                      //Write all High (HRS) for 4us
25                      errors=0;
26                      bgerrors=0;
27                      disterrors=0;
28                      Ren <= 8'b00000000;
29                      W <= 8'b11111111;
30                      Wen <= 8'b11111111;
31                      bg = 4'b1111;
32                      end
33
34                      always
35                      begin
36                      #1;
37                      //10us Guard Time
38                      Ren <= 8'b00000000;
39                      W   <= 8'b00000000;
40                      Wen <= 8'b00000000;
41                      #1;
42                      //Read Mem row 7 (1) for 10us
43                      Ren <= 8'b10001111;
44                      W   <= 8'b00000000;
45                      Wen <= 8'b00000000;
46                      #1;
47                      //10us Guard Time
48                      Ren <= 8'b00000000;
49                      W   <= 8'b00000000;
```

```
50                  Wen  <= 8'b00000000;
51                  #1;
52                  //Read Mem row 7 (1) for 10us
53                  Ren  <= 8'b10001111;
54                  W    <= 8'b00000000;
55                  Wen  <= 8'b00000000;
56                  #1;
57                  //10us Guard Time
58                  Ren  <= 8'b00000000;
59                  W    <= 8'b00000000;
60                  Wen  <= 8'b00000000;
61                  #1;
62                  //for loop through all 15 numbers (2^4-1)
                       and write each one in the first row of
                       the array
63                  for(out=0;out<16;out=out+1)
64                  begin
65                  outnot=15-out;
66                  //write \ac{HRS} for current val
67                  W <= 8'b11111111;
68                  val=out;
69                  Wen  <= {4'b1000, val};
70                  #1;
71                  //guard time 10us
72                  Ren  <= 8'b00000000;
73                  W    <= 8'b00000000;
74                  Wen  <= 8'b00000000;
```

```
75                  #1;
76                  //write LRS for current val
77                  W   <= 8'b00000000;
78                  val=outnot;
79                  Wen <= {4'b1000, val};
80                  #1;
81                  //guard time 10us
82                  Ren <= 8'b00000000;
83                  W   <= 8'b00000000;
84                  Wen <= 8'b00000000;
85                  val=out;
86                  #1;
87                  //read that shit!
88                  Ren <= 8'b10001111;
89                  W   <= 8'b00000000;
90                  Wen <= 8'b00000000;
91                  #1;
92                  if(Y!=val)
93                  begin
94                  errors=errors+1;
95                  end
96                  //guard time 10us
97                  Ren <= 8'b00000000;
98                  W   <= 8'b00000000;
99                  Wen <= 8'b00000000;
100                 #1;
101                 //read the column directly below!
```

```
102                         Ren <= 8'b00101111;
103                         W   <= 8'b00000000;
104                         Wen <= 8'b00000000;
105                         #1;
106                         if(Y!=bg)
107                         begin
108                         bgerrors=bgerrors+1;
109                         end
110                         //guard time 10us
111                         Ren <= 8'b00000000;
112                         W   <= 8'b00000000;
113                         Wen <= 8'b00000000;
114                         #1;
115                         //read that shit!
116                         Ren <= 8'b10001111;
117                         W   <= 8'b00000000;
118                         Wen <= 8'b00000000;
119                         #1;
120                         if(Y!=val)
121                         begin
122                         disterrors=disterrors+1;
123                         end
124                         //guard time 10us
125                         Ren <= 8'b00000000;
126                         W   <= 8'b00000000;
127                         Wen <= 8'b00000000;
128                         #1;
```

```
129                 end
130                 $display("%d␣data␣errors,␣%d␣background␣
                       disturbs,␣and␣%d␣data␣disturbs␣with␣a␣
                       background␣of␣%b.", errors, bgerrors,
                       disterrors, bg);
131                 errors=0;
132                 bgerrors=0;
133                 disterrors=0;
134                 //Write all Low (LRS) for 10us and repeat
                       test!
135                 Ren  <= 8'b00000000;
136                 W    <= 8'b00000000;
137                 Wen  <= 8'b10001111;
138                 bg = 4'b0000;
139                 #1;
140                 Ren  <= 8'b00000000;
141                 W    <= 8'b00000000;
142                 Wen  <= 8'b01001111;
143                 bg = 4'b0000;
144                 #1;
145                 Ren  <= 8'b00000000;
146                 W    <= 8'b00000000;
147                 Wen  <= 8'b00101111;
148                 bg = 4'b0000;
149                 #1;
150                 Ren  <= 8'b00000000;
151                 W    <= 8'b00000000;
```

```
152                 Wen <= 8'b00011111;
153                 bg = 4'b0000;
154                 end
155                 endmodule
```