ELECTROMIGRATION TESTING OF ALUMINUM INTERCONNECTS

David Lam
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

Pure evaporated aluminum interconnects on a flat surface and over topography were subjected to high current densities of 8e5 A/cm2 and measured for Electromigration induced failure times. An electromigration test station was built and used for obtaining Mean Time to Failure, MTTF, data. A rapid statistical approach, where multiple interconnects under the identical conditions could be tested, was utilized to determine that the MTTF was lower for interconnects over topography versus flat surfaces.

INTRODUCTION

The never ending push towards ultra large scale integration has placed a critical concern on the increasing number of metallization failures caused by Electromigration induced voids and subsequent open circuits. It is obvious that the smaller the geometry the smaller the voids necessary to cause electrical failure. Increased current densities, which tend to decrease reliability, will ultimately set a limit on current carrying capabilities of interconnections.

Electromigration is the transport of mass in metal interconnects stressed by high current densities which results in pile up in some regions and void formation in others. The migration of metal ion is likely to occur at grain boundaries, where the interconnect structure is weak due impurity and dislocation defects [1]. Figure 1 depicts metal ion imposed by two forces during current flow. The first is the field force, F1, directed towards the negative terminal. The second force, F2, is the result of the exchange of momentum from the electrons, due to the applied electric field, to the metal ions. The result of F2 is known as the electron wind effect [2]. The region where the metal ions leave acts as the site of void nucleation which can consequently become large enough to sever an interconnect.

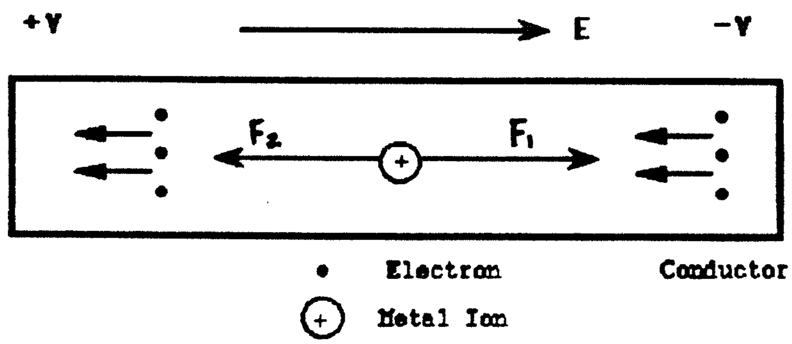

Figure 1: Forces on Metal Ion

Since void accumulation during electromigration typically occurs at grain boundaries, induced failures will preferentially occur at steps over topography or into contacts due to increased number of grain boundaries created by the steps [3]. The average grain size is smaller in and around the vicinity of steps. This may be due to the nature of thin film formation. A metal ion will travel until it is stopped by a corner or a wall. Consequently, corners have high binding energy and thus tend to be the preferred site of nucleation. As the thin film grows on either side of the corner, different orientation usually are produced and grain boundaries are formed. As a result the periphery of the contact will be the region of many boundaries, in other words small grain sizes. The net result is a shorter lifetime for metal interconnects over topography [4].

A typical method of increasing the life time of metal interconnects, used in the industry, is the use of aluminum/copper materials. The amount of .1% copper is sufficient enough to act as a trap for excess vacancies. The bonded copper and vacancy remain fixed at an arbitrary site thereby decreasing the rate of void formation[4]. Deposition conditions also play a role in reducing electromigration. Metals deposited by a high rate magnetron sputtering cathode exhibited a more narrow distribution of grain sizes [5]. Annealing metals can increase lifetimes by causing the agglomeration of grains, which decreases the total number of grain boundaries. The net result is a decrease in resistance and regions of possible void nucleation. Final passivation has also been observed to reduce electromigration induced failures by confining the mobility of vacancy diffusion.

The test station used for the acquisition of electromigration data utilized the hardware interface board developed by Helen Marz [6]. The interface board allows a simple custom test program to execute the necessary functions. The electromigration test station was designed to hold a fixed potential across the probes and extract current versus time data at specified intervals. The test structure used was developed by C.V.Thompson and J.Cho [7]. The technique allows high volume testing of interconnect failure with deviation in time in a single test.

Figure 2 depicts a condensed version of th test structure used. The structure used consists of two contact pads on either side which are connected by 50 parallel, periodically spaced and 1000um long lines. The structure used for this experiment dealt only with 1um lines. The lines were originally patterned for 2um, but the Al wet etch accounted for the 1um undercutting.

Figure 2: Condensed Test Structure

The design of the structure allows the simultaneous testing of identical lines at the same conditions. By placing a constant voltage across the probes each line should experience the exact same flow of current. A current density of 8-10 e5 A/cm2 per line is necessary for electromigration effects to occur[5]. Since the total voltage is constant, the total resistance increases as the lines begin to fail. The total current increment caused by each line failure can be determined by dividing the number of lines into the initial total current monitored. The times at which the failures occur are recorded and used to determine the MTTF and deviation.

The purpose of this investigation was to determine the change of Mean Time to Failure due to Electromigration-induced failures over topography compared to a flat surface. Secondly, the functionality of the data acquisition station will be tested in order to evaluate its reliability.

EXPERIMENT

Four 3" p-type wafers were processed for this experiment. A thermal oxide was grown in dry ambient at 1050C, for 25min, with a resultant thickness off 721.5A. Two of the four wafers were patterned into an array of 10 um wide lines and spaces, to create topography. The photolithography was performed by using the standard Wafertrac KTI 820 coating and developing and exposed on the GCA 4800 stepper. Finally, all four wafers were brought together, sent through the RCA cleaned, coated with 2400A of pure evaporated aluminum and patterned to form the desired test structures.

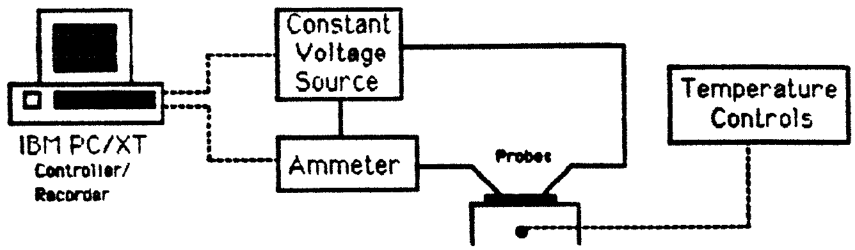

Figure 3a: Test Circuit

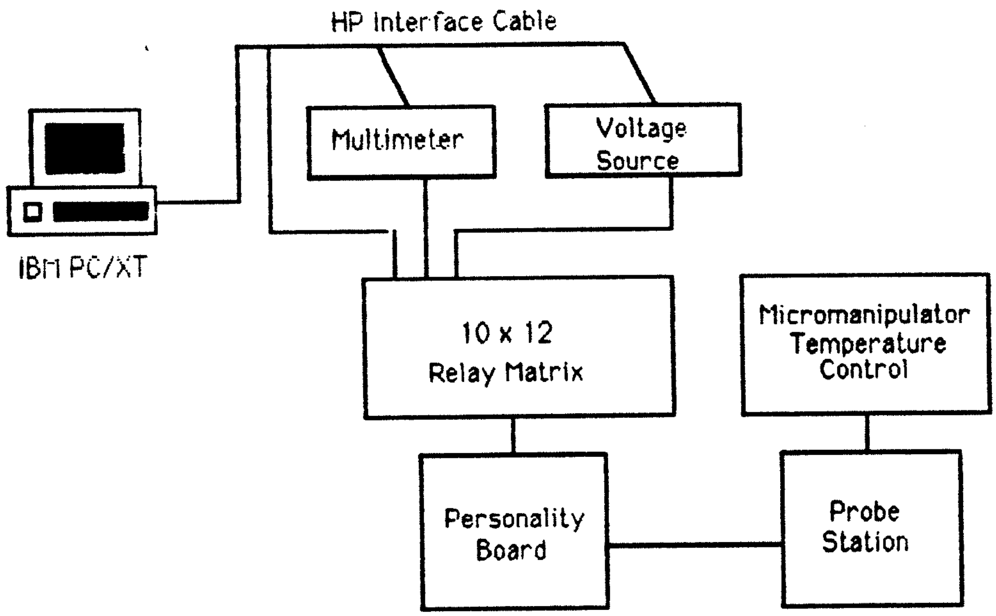

Figure 3b: Test System

Testing was done on the test station shown in Figure 3. The heated stage was manually controlled by the Model 410 high frequency C-V equipment. The functions of the Keithley voltage sources, digital multimeter, and matrix box were controlled by a simple custom program given in Appendix A, that was written for the IBM PC. Communication between the equipment utilized the Hewlett Packard Interface Bus, HPIB. Testing was performed on the heated chuck at 200C, with the voltage held fixed and the current density of 8e5 A/cm2 through the 1um test structures. Current density was determined by dividing number of interconnects into the initial total current along with the individual area, thickness times width.

Current versus time data was acquired and transferred into the Vax system using Kermit where data files and plots were generated. The statistical package RS1 on the Vax, was used to calculate the mean and median times to failure along with the associated deviation. Plots were generated using RS1 and DIS8.

RESULTS/DISCUSSION

Figure 4 and 5 are current versus time graphs plotted from data obtained through the electromigration test station. The testing over topography yielded an expected shorter lifetime for 100% failure. A histogram for the time to failure for the two cases, shown in Figures 6 and 7, presents the frequency of failures per interval of time.

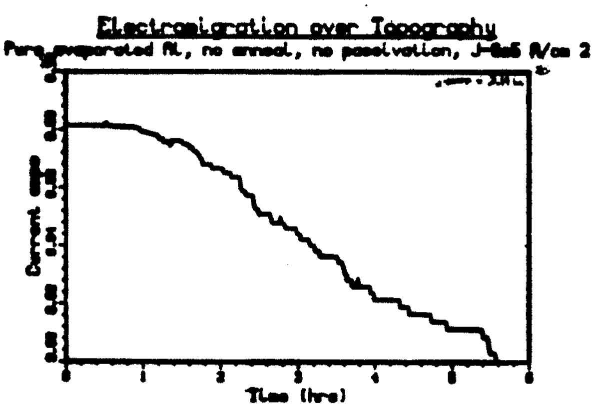

Figure 4

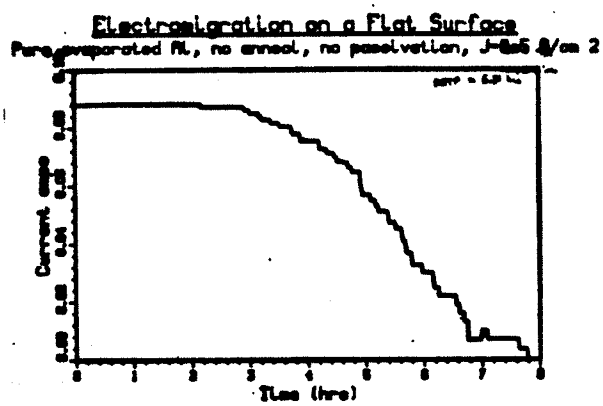

Figure 5

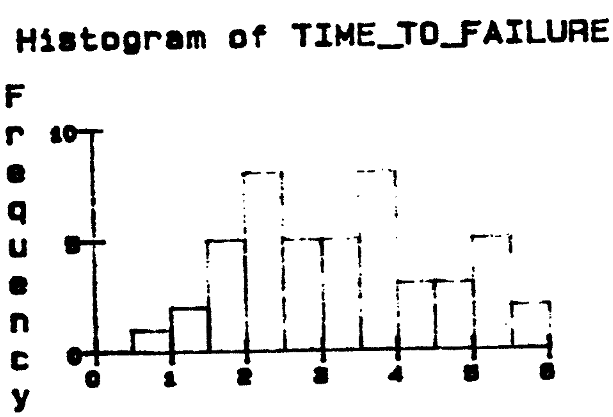

Figure 6: Topography

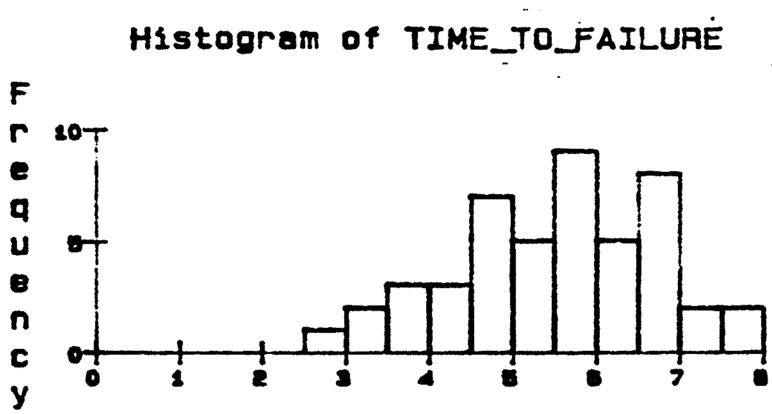

Figure 7: Flat Surface

Variable	Time (hrs)		Diff.
	Flat	Top.	
MTTF	5.31	3.19	2.12
MTF	5.38	3.14	2.24
STDEV	1.11	1.21	0.10

Table 1: Times To Failure

Means, medians, and standard deviations, STDEV, were determined by using the RS1 statistics software. Table 1 is a summary of these values. The Median time to failure, MTF, is the time at which 50% of the testing sites will have failed. The summary shows that the testing done over topography has a MTTF of 3.19 hrs with a STDEV of 1.21 as opposed to the MTTF of 5.31 hrs and STDEV of 1.11 over a flat surface. The MTF over topography was 3.14 hrs compared to the MTF of 5.38 hrs over a flat surface. Under similar testing conditions, the difference of the MTTF and MTF for both cases were 2.12 hrs and 2.24 hrs.

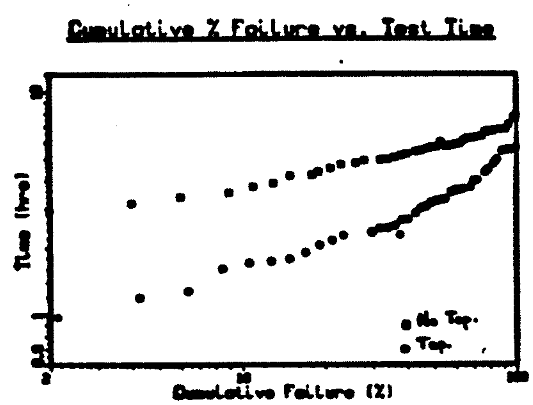

Figure 8: % Failure vs. Test Time

Figure 8 is a plot of cumulative percent failures versus test time for both cases. Failure times for electromigration induced failures for testing on a flat surface and over topography where compared. 40% decrease in MTTF was determined for interconnects over topography

Contact resistance and probe slipping were some major difficulties encountered. One method to insure reproducible results is to eliminate contact difficulties through wire bonding techniques. Contacts can be directly bonded to substrates, that

can be plugged into test sites. Also, for testing large linewidth test structures should be modified by reducing the number of lines tested. The decrease in interconnects will allow testing to be done at a lower voltage setting. Experiments testing the effects of the addition of copper, linewidth variations, testing temperatures, annealing temperature, passivation, and deposition conditions can be easily performed by using the test station developed in this experiment.

CONCLUSION

The experiment has presented data that demonstrates the decrease in MTTF due to electromigration testing over topography versus flat surfaces. A decrease of 2.12 hrs or 40 percent has been determined from the data acquired. The Test station used for acquiring Current vs. Time values has yielded valid data. Future experiments can be performed on the effects of other factors for electromigration lifetimes. Improvements can be made by decreasing contact difficulties through wire bonding techniques.

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