DETERMINATION OF CARRIER LIFETIME FROM MOS CAPACITORS

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ABSTRACT

MOS Capacitors were used to determine minority carrier lifetimes by obtaining capacitance vs time data (C-t). A test system, utilizing an IBM PC as the driver for a Princeton Applied Research model 410 C-V plotter, Kiethley programmable power supply, and HP4145 parameter analyzer, was built to obtain the C-t data. The data can then be down-loaded to the VAX mainframe computer and analyzed by various FORTRAN programs, using analytical techniques developed by people such as, Zerbst, Schroder and Guldberg, Heiman, and others.

INTRODUCTION

The determination of carrier lifetime in the bulk of a semiconductor is often desirable to determine electrical properties in a transistor, and may be influenced by fabrication conditions. Many methods have been investigated to determine recombination/generation lifetimes in semiconductor materials. Several of these techniques include, Photoconductive Decay, Spectral Response, Microwave Reflection, Optical modulation, Electron Beam Induced Current, Open circuit voltage decay, pulsed MOS capacitor, and reversed biased diode [1].

Each technique exhibits advantages and disadvantages relative to the others. Some techniques may require separate test wafers due to their complicated aspects of analysis or destructive nature. These methods however, may yield semiconductor parameters globally, meaning in the interior of the wafer. The more complex techniques often require special sophisticated (and often expensive) equipment. Since we are normally concerned with the properties of the active area of the device, we therefore concern ourself with generation properties in the volume under exterior control (gate control, Depletion width*gate area).

Although other techniques may prove to be more sensitive and non-destructive, pulsed MOS capacitor (MOS-C) methods still dominate generation lifetime measurement techniques in industry. One of several reasons for this popularity is the availability of commercial test equipment and software packages. Another reason is the relatively simple processing required for fabrication of a

MOS-C, which often times can be easily integrated within device fabrication processes. Often times the MOS-C is used as a test structure or "Drop-in" structure in modern I.C fabrication industry.

Lifetimes are determined by pulsing the MOS-C into deep-depletion and monitoring the capacitance as it relaxes back to equilibrium. Initially the capacitor may be biased in accumulation, depletion, or inversion, as long as it is in equilibrium before being pulsed into deep-depletion. Figures 1 and 2 show typical high frequency C-V and C-t plots for a MOS-C.

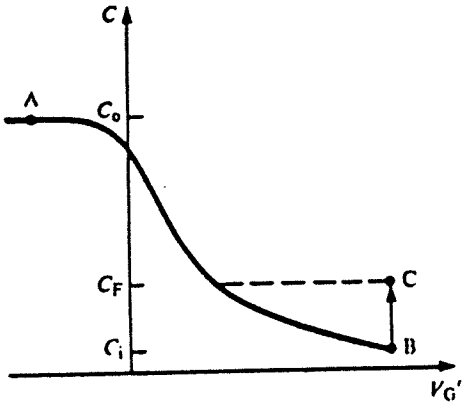

FIGURE 1: C-V Curve

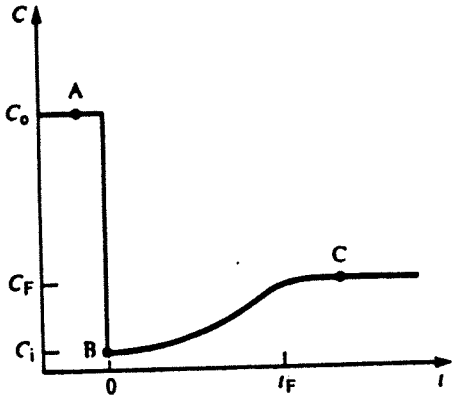

FIGURE 2: C-t Curve

When pulsed from accumulation to deep-depletion the capacitance is driven from point A to B as shown in both Figures 1 and 2. Thermal generation will return the MOS-C back to equilibrium shown in the figures by paths B to C. The recovery time , sometimes referred to as storage time, is determined by the electron/hole pair generation properties of the semiconductor bulk, and by the gate oxide/semiconductor interface.

The minority carriers needed to create the charge in the inversion layer in a MOS-C cannot be provided instantly. The carriers are provided by diffusion through the depletion layer from the quasi-neutral bulk or are generated in the depletion layer. If the gate voltage is sweep at a slow rate, relative to this generation or diffusion time, then the MOS-C will remain in equilibrium (at C(inv)) throughout this change. However if the MOS-C is pulsed into deep-depletion (i.e by a step voltage), minority carriers can not be generated quickly enough to satisfy the demand for inversion layer charge. In this case, the depletion layer width will increase to maintain overall charge neutrality, compensating the gate charge with ionized dopant ions until such time as sufficient minority carriers can be supplied to the area. When carriers are being supplied, the depletion layer width begins to return to it's equilibrium value (C(inv)) [2]. The return back to equilibrium was shown by the paths B to C in Figures 1 and 2.

Zerbst related the change in depletion layer width, as the MOS-C returns back to equilibrium, to a change in inversion layer carrier density, which in turn is related to the carrier lifetimes. An approximation to Zerbst analysis was proposed and studied by Schroder and Guldberg in which they determined generation lifetime by the following equation [3].

Upon obtaining the transient response of the MOS-C (C-t), and transferring the data to the VAX mainframe, the two analysis techniques will be investigated.

EXPERIMENTAL

Figure 3 shows the set-up for obtaining C-t data:

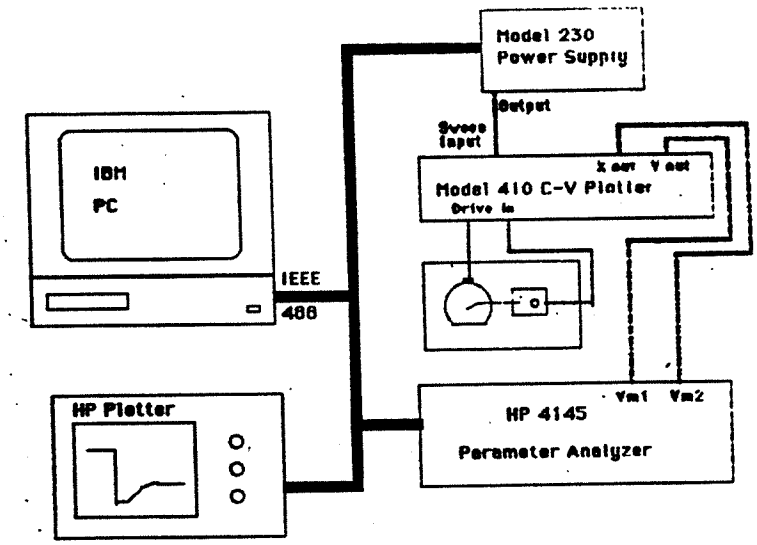

FIGURE 3:
SET-UP for obtaining C-t data.

The Princeton Applied Research model 410 C-V plotter was used in conjunction with a HP4145 parameter analyzer, Keithley model 230 Programmable power supply, and an IBM PC to obtain C-t curves for MOS-C's. Modifications were made the model 410 to allow for external synchronous control of the step voltage applied to the capacitor gate. This is achieved by turning the 'LIFETIME' switch to 'ON' position and selecting the gate 'Start' and 'Stop' limits on the 410. When a step voltage (via the Keithley 230) is applied to the 410 via the rear-panel 'SWEEP INPUT' connector, the MOS-C is pulsed from 'Start' to 'Stop' voltage instantaneously. The sweep input circuitry can be altered to allow control voltages between +1.0 and +1000.0 peak volts. This is achieved by changing an internal resistor according to manufactures specifications (refer to Appendix I). Thus the capacitance transient is monitored, in synchronicity

with the step input, via the HP4145, by connecting the Y-axis output of the model 410 to an input channel on the HP4145.

The IBM PC is used as the remote controller of the HP4145 and the model 230 power supply via the IEEE488 interface bus (Refer to appendix IV). A Microsoft BASIC software routine was written and automatically initializes, and programs these devices to obtain C-t data. The software is written in a menu format in which variables may be altered by the user by choosing the appropriate menu selection. Once a satisfactory C-t curve is obtained on the HP4145's graphics display screen, the software menus allow data to be stored on disk. In this manner the HP4145 is used as an A/D converter. The data file may then be transferred to the VAX mainframe (into users account) by using a software routine called KERMIT (Refer to Appendix II for transfer procedure).

This data transfer will allow the use of the VAX mainframe as the analysis tool. Carrier lifetime can be determined and compared with theoretical results, using Zerbst analysis, Schroder and Guldberg analysis, or any other technique. This system is a very powerful tool for parameter extraction and could be modified to do semi-automatic testing via IEEE488 interfacing.

RESULTS/DISCUSSION

Capacitance .vs. time plots were obtained using the set-up described in the previous section. Figures 4 and 5 show typical C-t plots obtained, and the Zerbst, and Schroder & Guldberg analysis on this data.

The C-t data was transferred to the VAX and analyzed using a FORTRAN program (CAP.FOR, Refer to Appendix III), which analyzed the data and reported the minority carrier lifetimes. The data was also analyzed using Mike Jackson's Zerbst FORTRAN program, and the two techniques were compared.

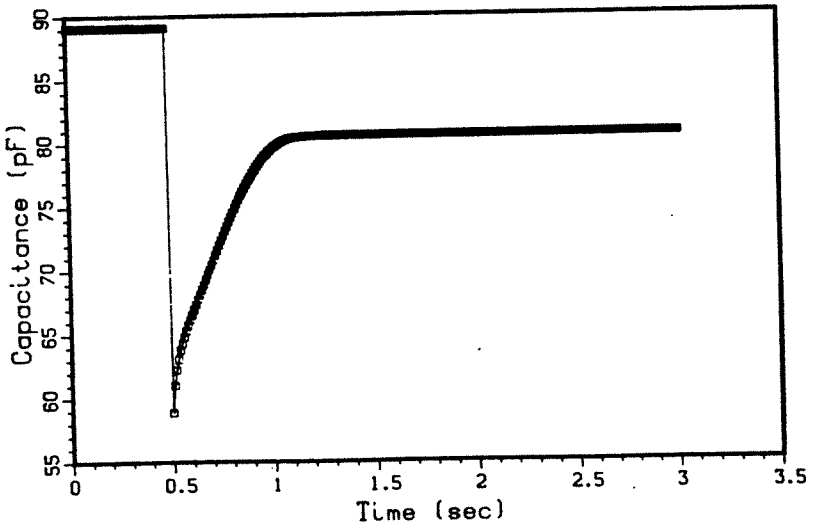

FIGURE 4: Capacitance .vs. Time Data

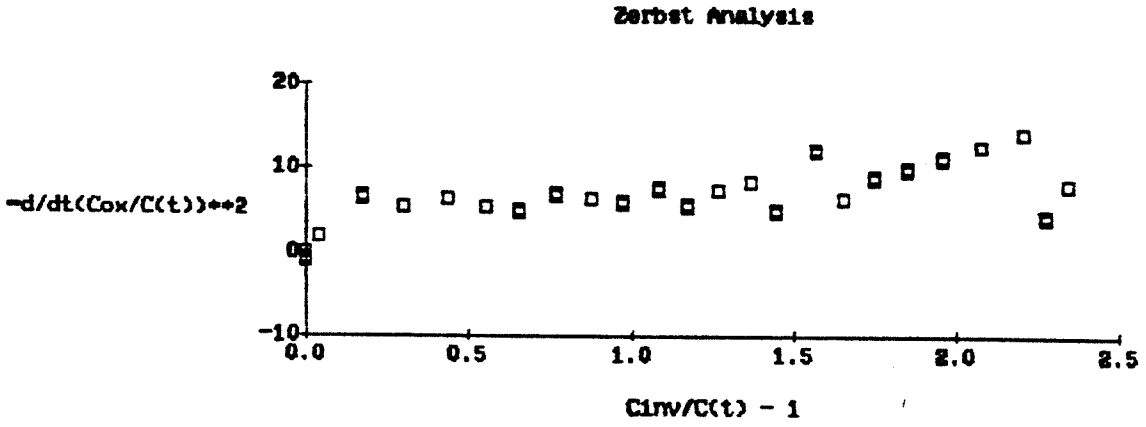

FIGURE 5: Zerbst Analysis

Schroder & Guldberg Analysis:
Minority Carrier Lifetime = 3.17 usec

These two techniques yield very similar lifetimes as shown above (3.51 and 3.17 usec). Further investigation into minority carrier lifetimes using these techniques should be done to determine which is appropriate.

CONCLUSION

In this investigation, a method for determining minority carrier lifetimes was presented using software-driven equipment. This allowed data to be transferred to the VAX for analysis via two techniques. Both techniques proved to be effective and the calculated minority carrier lifetimes were very similar. The capability for determining minority carrier lifetimes now exists at RIT, and this technique can now be implemented in characterizing various future processes, such as CMOS.

ACKNOWLEDGEMENTS

I would like to thank John Connor for his assistance with programming using the IEEE488 interface, and Mike Jackson for his suggestions with this investigation.

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