

TRENCH ISOLATION STUDIES

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ABSTRACT

The Tegal 700 plasma etcher was used to etch trenches into four micron deep p-type diffused resistors to evaluate the quality of the electrical isolation. Etch times of nine and twelve minutes were used to etch trenches approximately 7.8 and 11.5 microns respectively. Current flow was detected in all resistors, despite the fact that the trench should have resulted in open circuits. Therefore, at this time, results are inconclusive.

INTRODUCTION

Silicon trench isolation has become the most favorable method of device isolation in the fabrication of VLSI devices. Prior to the use of trench isolation, devices were separated from one another by diffusing a junction between the devices and reverse-biasing the junction. This technique required large amounts of chip area due to the isotropy of the diffusion and the associated depletion regions [7].

Trench isolation provides a relatively simple method of device isolation which requires minimal "real estate". A deep well, or trench, is etched through the epitaxial layer and into the substrate. If performed by a dry-etching technique, the minimum width of the trench is dictated by the lithographic process used. The trench is then filled with a CVD oxide in order to fill the trench and planarize the wafer surface [1].

One particular gaseous species used to produce a silicon plasma which etch is sulfur hexafluoride (SF_6). The SF_6 will form fluorine radicals upon the creation of a plasma, which will in turn react with silicon atoms at the surface of the wafer. The atoms will react to form SiF_4 , a volatile, non-reactive endproduct which is removed from the etching system. In addition, oxygen is added to the SF_6 in order to tie up the sulfur in the system and form the product SO_2 . Insufficient oxygen addition to the system will cause the formation of $\text{S}(\text{x})\text{F}(\text{2x})$ complexes, which can deposit on the wafer surface, retarding the etch and destroying the wafer.

This experiment was performed to investigate the feasibility of isolating devices by creating trenches using the Tegal 700 plasma etcher. A mask set and process was developed in order to electrically test the quality of the isolation.

EXPERIMENT

The etch rate of silicon masked with KTI-820 photoresist using a 3:1 SF₆/O₂ plasma in the Tegal 700 single wafer plasma etcher was investigated. Flows of 10.0 and 3.3 sccm of sulfur hexafluoride and oxygen, respectively, were used. The etcher was tuned to minimize the reflected power, while yielding approximately 125 Watts of forward power. Etch times ranging from one to six minutes were investigated; however, it was found that the etch rate of the resist mask was very high. The experiment was then repeated on wafers on which 5000 angstroms of thermal oxide was grown to act as an etch stop. Etch times of six, nine, and twelve minutes were used in order to find an average silicon etch rate.

A process was developed with which to evaluate the effectiveness of the trench isolation. First, a test chip was designed on ICE (an internally-developed and maintained CAD tool) with which to perform the photolithographic steps. This mask contains three layers: diffusion, trench, contact cut, and metal. The trenches, ranging from zero to ten microns in length, were designed to completely separate the two ends of the diffusion. Testing would then reveal if the trench in fact did separate the two ends of the diffusion. The cross-sectional view of this structure is shown in Figure 1.

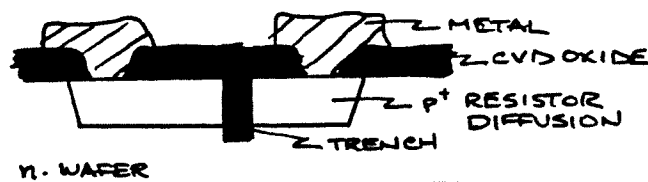


Figure 1. Cross-section of trench etch test structure

Six n-type wafers were obtained and cleaned using a standard RCA clean. Next, an oxide was grown in order to mask the diffusion at 1100 degrees celsius for 45 minutes in a wet oxygen ambient. The first mask was used to image the wafer and etch the oxide in regions which were to be diffused. B150 spin-on dopant was then spun on the wafers, which were then placed in an 1100 degree furnace for 130 minutes in a nitrogen ambient, followed by 20 minutes in a dry oxygen atmosphere to assist in removal of the spin-on dopant layer. The oxide was then stripped.

A drive-in was performed for 120 minutes, also at 1100 degrees. A dry oxygen flow was used for the first 75 minutes, followed by 45 minutes in a wet oxygen ambient. The resulting was used as the etch stop for making the trenches. Windows were transferred into the oxide photolithographically using the second masking level (trench level).

The Tegal plasma etcher was then used to etch the trenches. A 10.0/3.3 sccm SF₆/O₂ mixture was used, with a forward power of 125 Watts. The chamber pressure was 0.550 torr. Etch times of six, nine, and twelve minutes were used. The oxide mask was then removed, and the step heights measured on the Alpha-Step. Finally, following visual inspection with an optical microscope, a HP4145 Semiconductor Parameter Analyzer was used to find the resistance of the test structures.

RESULTS/DISCUSSION

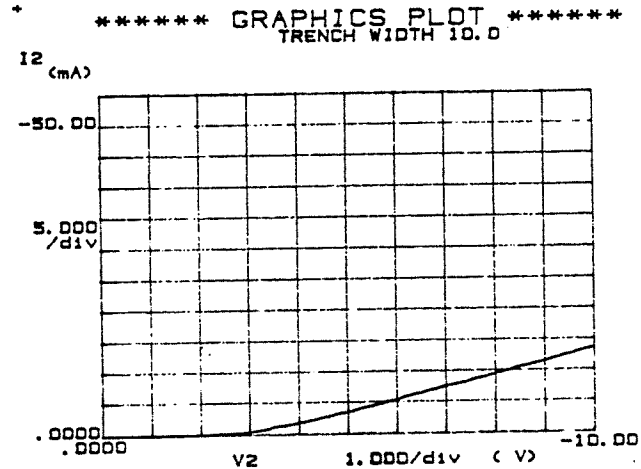
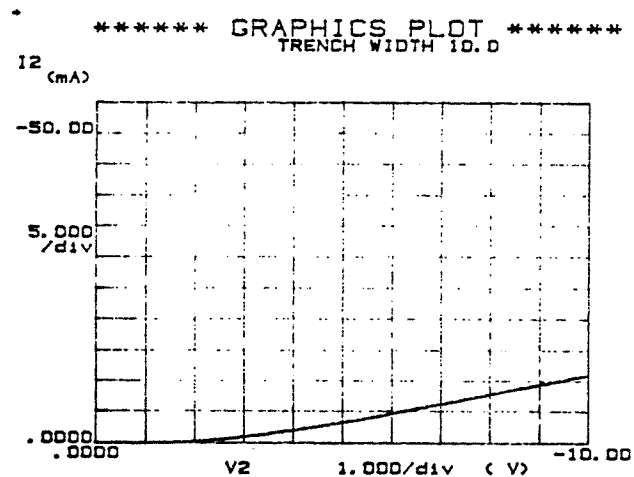
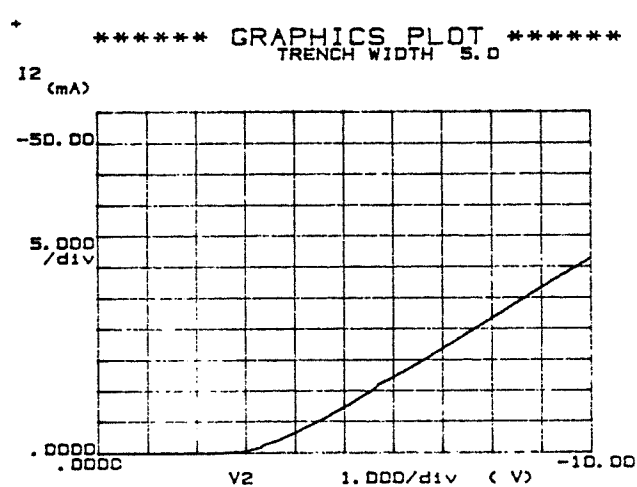
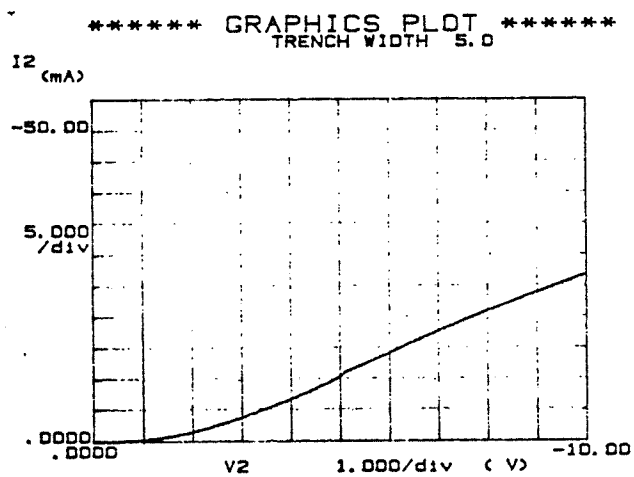
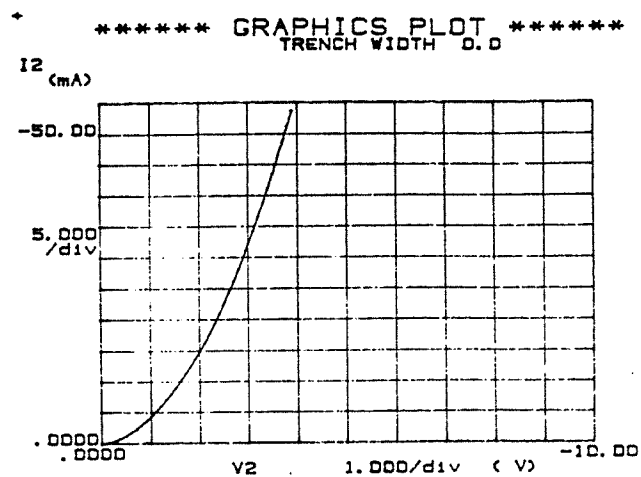
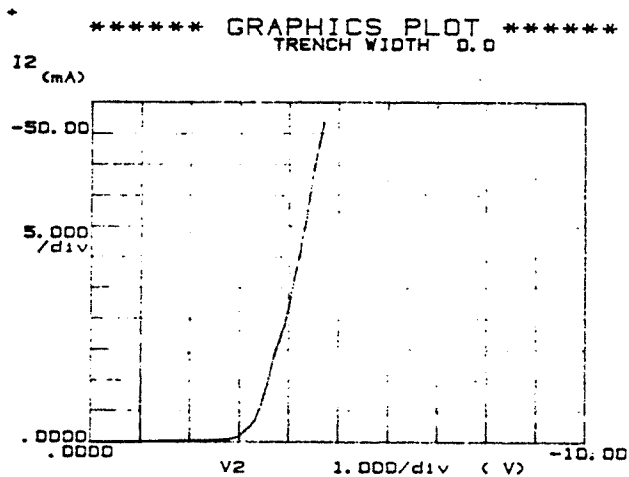
The Alpha-step profilometer was used to measure the depth of the trenches. Results of the initial studies shown in Figure 2 reveal a silicon etch rate of approximately 1.0 micron per minute while using the oxide mask. The oxide mask showed minimal damage from the SF₆/O₂ plasma, but the etch was not very anisotropic--the sidewalls appeared large and dark under dark field illumination. The groove and stain apparatus revealed that the junction depth of the diffusion was 4.04 microns. From this data, etch times of six, nine, and twelve minutes were selected for the experiment.

ID	ETCH DEPTH (microns)	ETCH TIME (minutes)	ETCH RATE (u/min)
TEST2	5.00	6.0	0.8333
D3	6.00	6.0	1.0000
TEST1	7.40	9.0	0.8222
D6	8.00	9.0	0.8888
D4	10.50	12.0	0.8750

Figure 2. Silicon etch rates using SiO₂ mask

The inspection of three of the six wafers revealed that the silicon in the etched areas was extremely discolored and grainy in appearance. The etch rates obtained agreed with those results from the previous study; however, it is apparent that there is a problem with the process. This discoloration appears to be from the deposition of an S(x)F(2x) complex, caused by an insufficient amount of oxygen in the system. It should be noted that only the first three wafers exhibited this problem; this reveals the need to run many "dummy" wafers through the system before performing the etch on product wafers.

The resistors with zero, five, and ten micron trenches were compared using the HP4145 parameter analyzer. From the graphs in Figure 3, it can be seen that the etches did not open-circuit the devices, as significant current flow was measured. It is easily seen, however, that there is an increase in resistance as the



(a) (b)
Figure 3. Resistance of trenches versus trench length
(a) Wafer D6 (9 minute etch); (b) Wafer D4 (12 minute etch)

trench width increases. The trench depth has been measured to be more than twice as deep as the diffusion, meaning that there must be some mechanism which allows for current flow through or around the channel. The high-energy ions created in the etch plasma may cause lattice dislocations at the bottom of the trench, which could allow current to flow around the trench. It would be worthwhile to investigate this possibility; one method of repairing such damage would be a high-temperature anneal following etching of the trench.

Wafer D6, which was etched for nine minutes, shows the same trends as wafer D4, which received a twelve minute etch. This leads to the conclusion that the time of the etch is not much of a factor in the isolation; in other words, for trenches less than ten microns in length, the etch will be limited by the width of the trench. In addition, through a conventional microscope, the etch appeared to be almost totally isotropic.

CONCLUSIONS

There are many areas in which this experiment may be improved. The absolute thicknesses measured on the Alpha-Step profilometer have been shown to be inaccurate in previous work, but no other device is available to measure the trench depths. It would also be possible to perform scanning electron microscopy to evaluate the trench depth, as well as the degree of isotropy, but the SEM in the lab was not in functional order.

Furthermore, a true trench etching process involves the backfilling of the trench with a CVD oxide. When CVD capabilities are implemented at RIT further processing, using the same mask set, can be performed, including the use of metal contacts. It should be noted that the mask set designed on ICE can be used to implement this.

One further enhancement would be the use of a different style plasma etcher. The Tegal 700 is a single wafer, relatively low power etcher, while the use of a triode etcher or high-powered etcher is recommended [1,2].

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