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Investigation of Thermal Stress Degradation in Indium-Gallium-Zinc-Oxide TFTs

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Abstract

The performance of IGZO TFTs has improved significantly in recent years, however device stability still remains a significant issue. Thermal stability of IGZO TFTs becomes very crucial to ensure desired performance of end-product. Both bottom-gate (BG) and double-gate (DG) TFTs were observed to degrade with hotplate treatments under 200°C. Such events are rarely reported in the literature, and thus became the primary focus of this work. The mechanism causing the instability is not completely understood, however experimental results indicate the instability occurs either directly or indirectly due to the influence of H_2O within the passivation oxide above the IGZO channel region. DG TFTs saw more pronounced degradation, which led to the hypothesis that there may be a reaction of the top gate metal with H_2O molecules in the passivation oxide, liberating monatomic hydrogen. Both H_2O and hydrogen behave as donor states in IGZO, thus rendering the channel more conductive. The thermal stability also demonstrated a dependence on channel length, with shorter channel devices showing greater stability. This may be due to the metalized source/drain regions acting as effective getter to water during a 400°C passivation anneal which is performed prior to top-gate metal deposition. This hypothesis led to an investigation on atomic layer deposition (ALD) of capping layers over the passivation oxide of IGZO TFTs to act as an effective barrier to water/hydrogen migrating to the underlying IGZO channel.

Contents

List of Figures

List of Tables

Chapter 1

Introduction to Display and TFT Technology

Flat-panel Displays (FPDs) have evolved over the years to become the most widely used technology for displays in commercial electronic devices. Recently, active-matrix FPDs have dominated the display industry. The active-matrix FPDs use a backplane consisting of Thin-Film Transistors (TFTs) that enable pixel switching to create an image on the front surface of display. This section provides an overview of the display and TFT technologies currently used in the FPD industry.

1.1 Liquid Crystal Displays

Liquid crystal display (LCDs) have widespread applications in several hardware products such as computers, phones and TVs. Most LCDs use a backlight to illuminate the LCD panel. The backlight for the display used to be generated using Cold-Cathode Fluorescent Lamps (CCFLs), but is predominantly generated more recently using Light-Emitting Diodes (LEDs). The glass panel installed over the diffuser consists of various layers. Two polarization filters are present which are oriented at 90° to each other. The first polarization filter polarizes the unpolarized incident light from the source. It creates polarized light with only one polarization plane. The second filter blocks out the light as it is rotated by 90° with respect to the upper filter.

A liquid crystal is used in between the two polarizers to rotate the initially polarized light from the first polarizer by 90° in order to pass through the second polarization filter. LCDs, such as the one depicted in Fig. 1.1, predominantly use a

twisted-nematic liquid crystal structure which twists the molecules 90° upon applying a voltage across the crystal. This enables rotation of the polarization plane, thereby causing the polarized light to pass through the second polarizer to the front surface of the display.

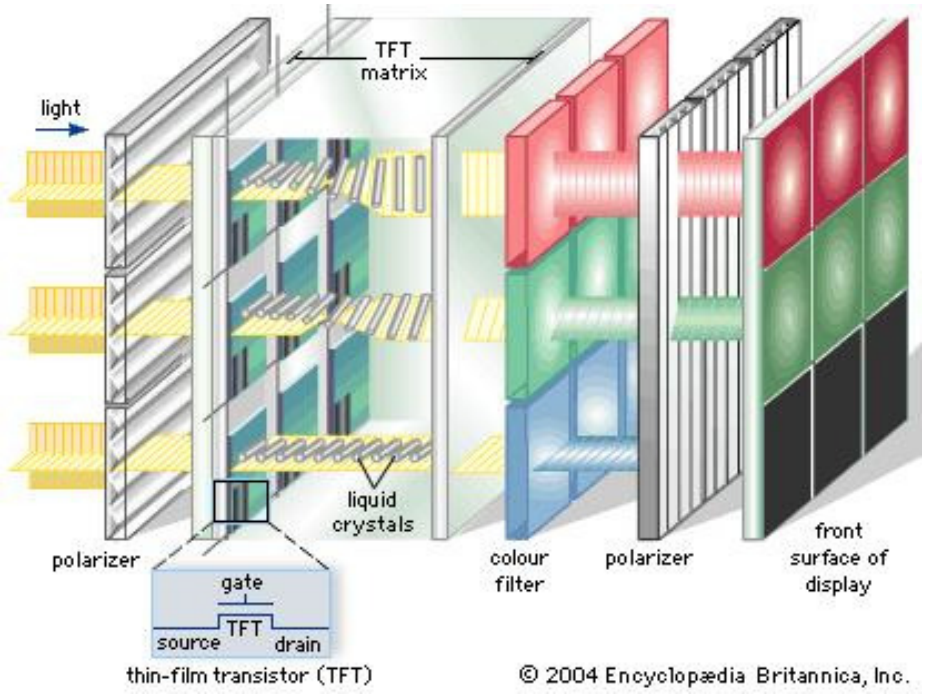


Figure 1.1: Structure of LCD panel with TFT [1].

1.2 Pixel Addressing

There are predominantly two types of display structures for pixel addressing: Passive-matrix and Active-matrix. In the former, a grid is created by using one glass substrate to address the rows and the other substrate to address the columns. The rows and columns are connected to integrated circuits that control the charge to each pixel. To turn on a pixel, the integrated circuit sends voltage to the corresponding column and the corresponding row is grounded to complete the circuit. This type of mechanism involving direct addressing of the pixel is plagued by two main issues: slow response time and poor voltage control. As a result of poor voltage control, adjacent pixels

would also be partially turned on when addressing a particular pixel.

The active-matrix display provides an improved mechanism by using a transistor to address each pixel. Active-matrix displays consist of a switching TFT and a storage capacitor. In order to address a pixel, the voltage is sent to the appropriate transistor controlling the pixel. The capacitor is then able to retain the charge until the next refresh cycle. An example of a simple active-matrix circuit can be seen in Fig. 1.2 which consists of a switching TFT, storage capacitor, and liquid crystal.

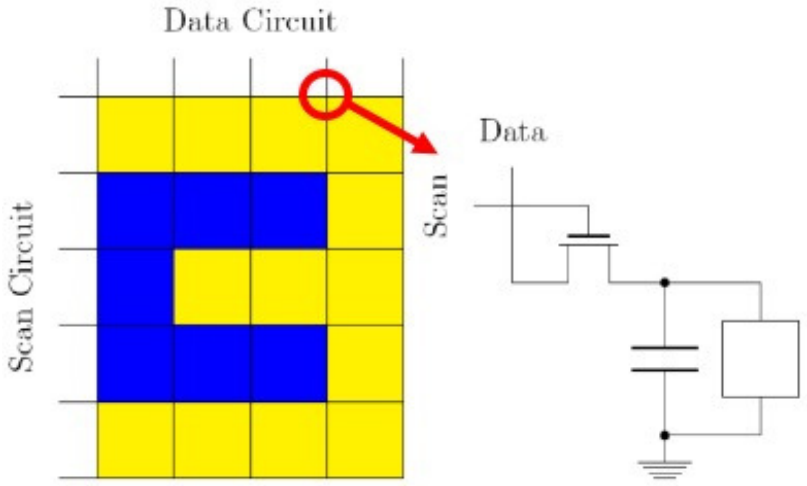


Figure 1.2: Illustration of pixel addressing showing equivalent circuit of active-matrix display. A liquid crystal and storage capacitor are connected in parallel being driven by a TFT that is connected to the scan and data circuits.

1.3 Current TFT Technology and Limitations

With a constant drive towards newer display technology, there is an increasing need to meet the performance and manufacturing requirements of TFTs. One of the common problems faced by the FPD industry is large area uniformity. The FPD industry has been advancing to larger panels due to the increasing demand for larger displays. Fig. 1.3 depicts the trend towards larger display panels in the FPD industry. Since display panels are advancing towards generation 10 (Gen 10), the substrate used is required to be roughly 3 m x 3 m in dimensions. Electrical uniformity is essential

when fabricating TFTs under such circumstances.

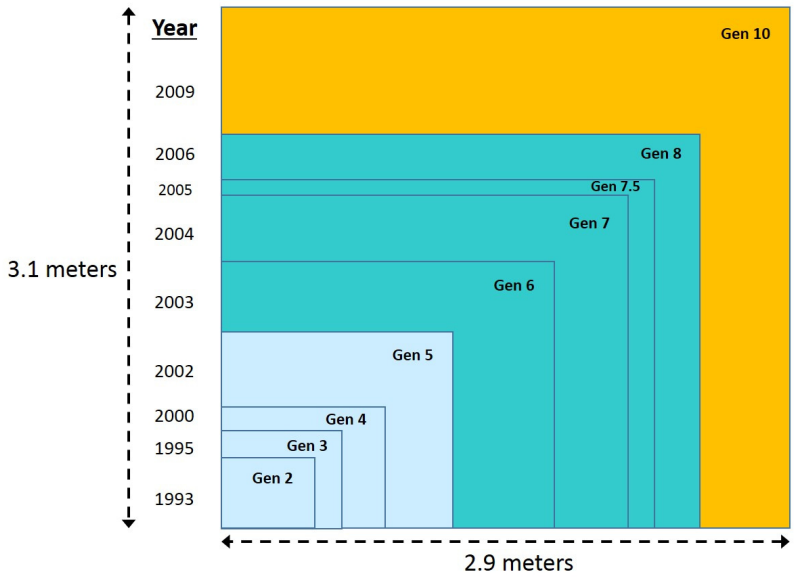


Figure 1.3: Substrate generations of flat-panel display (adapted from [2]).

Another challenge is to ensure the fabrication process used for TFTs manufacturing is low temperature compatible. This is primarily because the TFTs are typically fabricated on glass substrates which have a thermal tolerance of around 600 °C. Additionally, as pixel density increases to offer better resolutions, the aspect ratio between the pixel and the driving TFT becomes lower. In such cases, it helps if the TFT used is also transparent to visible light.

Hydrogenated amorphous silicon (a-Si:H) has been widely used for TFTs and has been the backbone of the display industry for the last decade. Unhydrogenated a-Si has poor conductivity as it contains dangling bonds. Hydrogenation of the a-Si helps saturate the dangling bonds and thereby have a lower defect density and increased conductivity as doping is made possible. Amorphous silicon has become an attractive solution to the TFT material as it ensures excellent large area uniformity due to its amorphous structure. Additionally, it is low-temperature compatible and can be deposited at temperatures under 350 °C using plasma-enhanced chemical-vapor deposition (PECVD). It is also a low cost and a very well understood material to

manufacture and characterize.

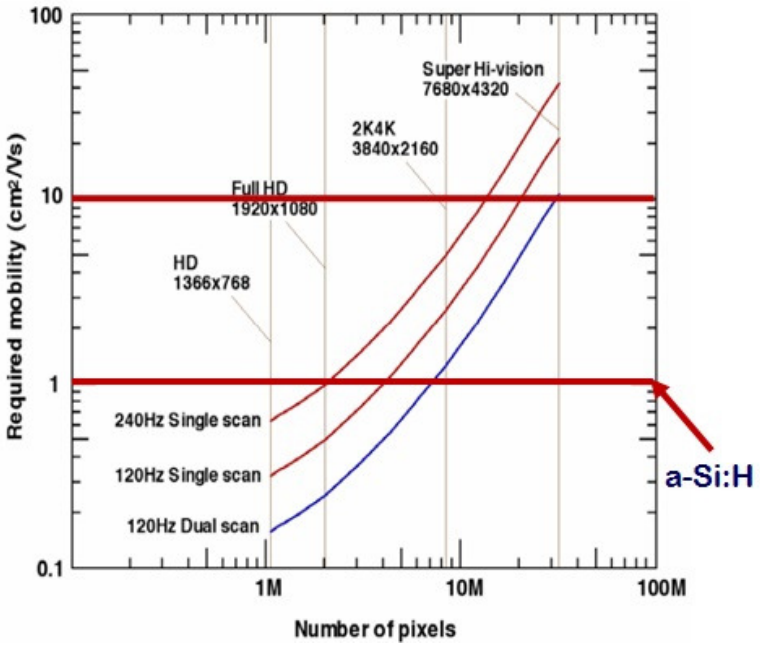


Figure 1.4: Mobility requirements for next-generation displays [3].

With next generation displays, the display industry faced several issues with an increased demand for higher pixel density and faster refresh rates in display devices. This could be resolved by using a TFT channel material with faster electrical mobility, as shown in Fig. 1.4. Due to the limited mobility of a-Si:H, the FPD industry has been looking for alternates to manufacture high-performance TFTs. [15, 17].

1.4 Organic Light Emitting Diodes

While LCD technology is widely used as the display of choice, the industry has been advancing towards Organic Light-Emitting Diode (OLED) based display technology. In OLED displays, there is no requirement of backlighting as there is precise control of current injected into each OLED. Fig. 1.5 describes the structure of an OLED display. The electron-hole recombination in the organic material results in emission of photons. A backplane consisting of TFTs circuits provide current to the OLEDs, thereby controlling their brightness. The simpler structure makes this alternative

thinner and lighter than LCDs.

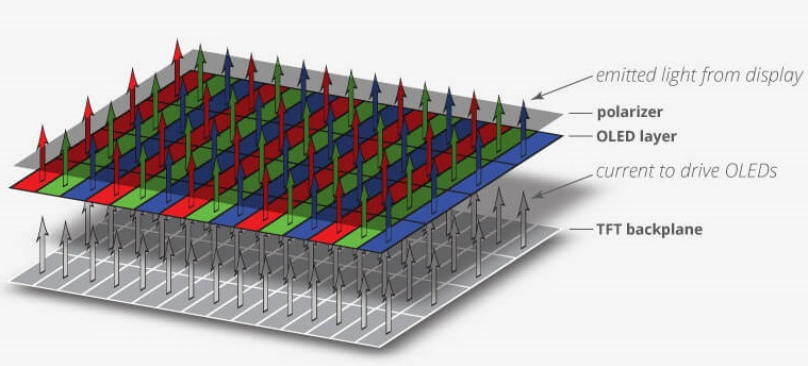


Figure 1.5: Structure of OLED display [4].

There are several advantages to the OLED technology as compared to the LCD technology. OLEDs are generally brighter than LCDs as the latter requires glass for support, causing additional absorption of light by glass. They consume less power than LCDs as the latter uses selective blocking of backlight which is not as power efficient. They provide a higher contrast and a better image quality in comparison to LCDs because there is no light emitted when the pixel is off. OLEDs also have a larger field-of-view as they generate their own light as compared to blocking light in case of LCDs.

Although there are several advantages in adopting OLED technology, the manufacturing process for OLED display is expensive. The OLED technology is even more sensitive to electrical uniformity than LCDs as it requires precise drain current control throughout the entire substrate, which has a high sensitivity towards the screen brightness.

1.5 TFT Materials for Next-generation displays

The limitations in a-Si:H has led the display industry to look for alternative channel materials to make high performance TFTs in support of the next-generation display requirements. Currently, there are two materials being widely researched to replace

a-Si:H and improve TFT performance, as seen in Table 1.1. The first alternate is a silicon-based Low-temperature polycrystalline silicon (LTPS) which involves depositing a-Si:H on glass and then crystallizing it using excimer laser annealing (ELA) technique to form polycrystalline silicon. This material yields a very high channel mobility and can be used to make CMOS TFTs. However, this is an expensive technique due to high cost laser annealing and process complexity. Additionally, the random, polycrystalline structure of LTPS leads to problems with large-scale uniformity issues.

Amorphous-oxide semiconductors (AOSs) are the other choice of TFT channel material for next-generation displays. They have been preferred over polycrystalline materials from the viewpoint of uniformity in device characteristics. More recently, Indium Gallium Zinc Oxide (IGZO) has been a popular choice amongst the group of AOSs. IGZO is compatible with the current hydrogenated amorphous silicon (a-Si:H) manufacturing lines, thereby making it attractive for its low cost. It offers very good large scale uniformity as it is amorphous in structure, making it an appealing option for manufacturing on larger glass substrates such as the Gen 10 panels.

Table 1.1: Comparison of properties between different TFT channel materials [15, 16].

Semiconductor	Electron Mobility (cm^2/Vs)	Off-state Leakage	Large Scale Uniformity	Transistor Type
a-Si:H	< 1	Moderate	Good	NMOS
LTPS	$30 - 100$	High	Poor	CMOS
IGZO	$10 - 20$	Low	Good	NMOS

Fig. 1.6 shows the typical I-V characteristics of a L/W = 24/100 µm IGZO TFT. It can be observed that the IGZO TFT shows very steep subthreshold slope along with an excellent on-off ratio. It also has a high electron mobility that supports better TFT performance and a very low off-state noise level. Additionally, it is low-temperature compatible as it can be deposited at temperatures under 200 °C. These attractive properties make IGZO a front-runner to replace the current a-Si:H technology.

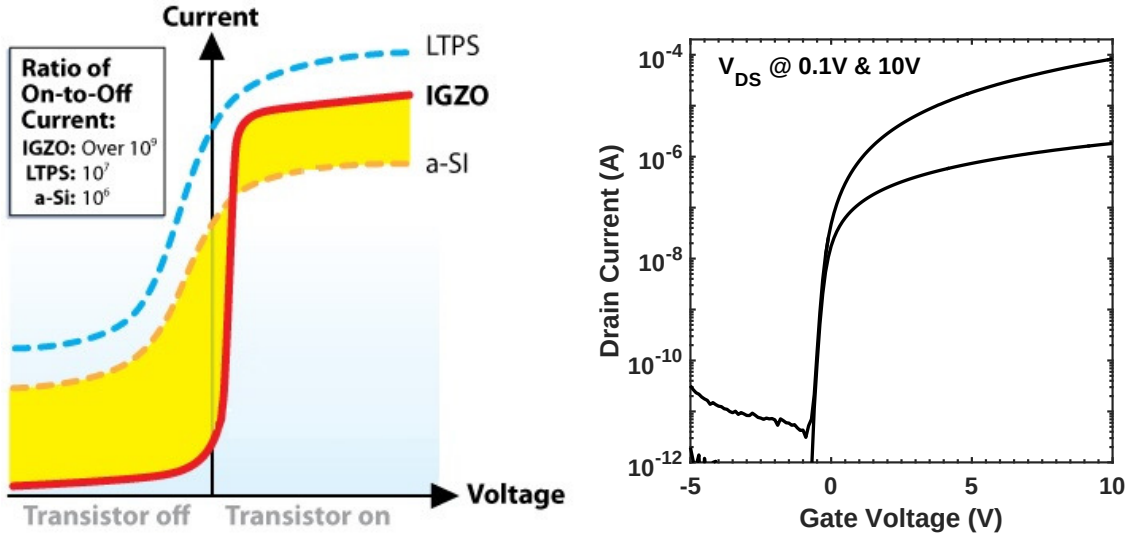


Figure 1.6: (a) Comparison of *I-V* characteristics between different channel materials [18] (b) *I-V* characteristics of a L/W = 24/100 µm IGZO TFT [13].

1.6 Challenges and Motivation

Although IGZO has yielded desirable TFT characteristics (as explained in Section 1.5), there are some challenges that still need to be addressed before it is adopted for high-volume manufacturing.

IGZO is not a chemically robust material and therefore requires lift-off processing for the layers that follow. It also degrades in performance when subjected to plasma processes as the material is ambient sensitive. Therefore, wet chemistry is used to etch in order to prevent plasma-induced damages.

Presently, the primary challenge is in regard to the instability of IGZO TFTs when subjected to electrical and thermal stress. It has been observed that the electrical properties of IGZO change when subjected to a thermal treatment. This is an area of concern when it comes to manufacturing IGZO TFTs as the transistors might get subjected to elevated temperatures during back-end processes.

This thesis primarily focusses on understanding the mechanism behind instabilities displayed by IGZO TFTs when subjected to thermal stress. Chapter 1 provides a

quick background to TFT technology and outlines few important challenges faced by the display industry and research groups. Chapter 2 would discuss the motivation for IGZO as a suitable TFT material and explore its material and electrical properties in detail. This would also cover requirements of passivation materials in order to improve electrical stability of IGZO. Chapter 3 will provide an overview of the fabrication and operation of TFT structures used for investigation. This chapter will also briefly discuss challenges of electrical bias-stress stability commonly observed in IGZO TFTs.

Chapter 4 discusses the thermal instability results and presents a hypothesis to explain the observations. A mechanism that relates thermal instability shown by IGZO TFTs to silicon MOSCAP sinter would help understand and bolster the proposed hypothesis. Chapter 5 provides process modifications to address thermal instability issues. It would also briefly discuss an investigation of channel length dependence of IGZO TFTs on thermal stress. Finally, chapter 6 would provide a summary of learnings and conclusions based on the observed results, and discuss relevant areas that would require further research to characterize the behavior.

Chapter 2

Introduction to Indium-Gallium-Zinc-Oxide

This chapter will provide a brief introduction to amorphous oxide semiconductors, more specifically IGZO. The conduction mechanism and characteristics of IGZO will be discussed. The influence of ambient interactions on the electrical properties of IGZO will be investigated.

2.1 History of amorphous oxide semiconductors

The first AOS-based TFTs gained recognition after the development of CdS TFTs in 1962 [15]. Zinc oxide (ZnO) was the first AOS material that was explored with the first ZnO based TFT fabricated in 1968 [19]. However, the ZnO research was put on hold shortly after. It was in 2003 that the interest in ZnO TFTs was revitalized, becoming the primary material of interest for several research groups. ZnO was considered to be a promising candidate to replace a-Si:H due to its electron mobility being greater than a-Si:H by an order of magnitude. It was considered primarily as it can be deposited at temperatures below 300 °C. It also has an amorphous structure giving uniform electrical properties across large substrates. Fig. 2.1 shows the *I-V* characteristics and electron mobility of a PE-ALD deposited ZnO TFT.

However, ZnO material showed instability and non-uniformity at higher temperatures as it easily crystallized into a polycrystalline material leading to formation of grain boundaries. In such situations, obtaining large area uniformity becomes a

challenge as device characteristics vary across the grain boundaries. Several other alternate binary AOS materials have been considered since the development of ZnO TFTs. However, some of these alternatives form oxides that have poor conductivity and others contain cations that are highly toxic (e.g., Pb, Cd, Hg). Ternary and quartenary AOSs materials were widely researched to address the uniformity issues faced by ZnO due to crystallization. Using AOSs with multiple cations would effectively inhibit film crystallization and maintain the amorphous structure of the film at higher temperatures.

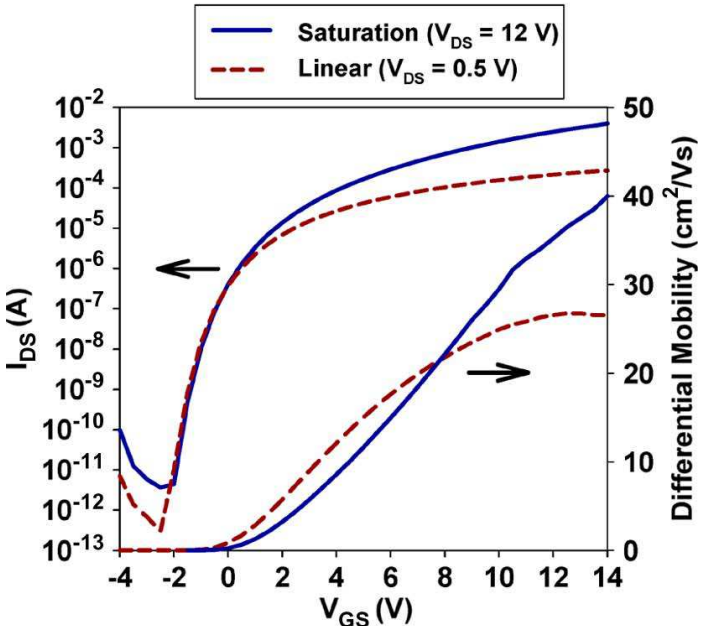


Figure 2.1: I-V measurements and differential mobility extraction of a PE-ALD deposited ZnO TFT [6].

2.2 Conduction mechanism in AOSs

Hosono et al. provides a thorough discussion of the conduction mechanism in amorphous oxide semiconductors [7]. AOS materials were developed to make transparent and conductive active layers in TFTs. In the case of covalent semiconductors, which includes silicon, the conduction path is formed by overlapping sp^3 orbitals and is very

sensitive to variations in bond angles. Therefore, the amorphous structure of covalent semiconductors leads to mobility issues. For crystalline materials, these orbitals are aligned and thereby result in a better channel mobility.

Ionic semiconductors such as AOSs, on the other hand, have their conduction path formed by overlapping metal s-orbitals which do not possess spatial directivity due to their isotropic structure. The amount of overlap between the orbitals is also high as they have larger ionic radii. Therefore, band conduction is made possible, preventing degradation of electron mobility. Fig. 2.2 illustrates the conduction mechanism operative in covalent and ionic semiconductors. It can be noted that the amorphous form of covalent semiconductors is inferior as a TFT active layer due to the directional nature of sp^3 orbitals. On the contrary, the amorphous form of ionic semiconductors remains unchanged and therefore becomes an excellent candidate as an active layer material. Fig. 2.3 illustrates the difference in bonding arrangements between covalent and ionic semiconductors.

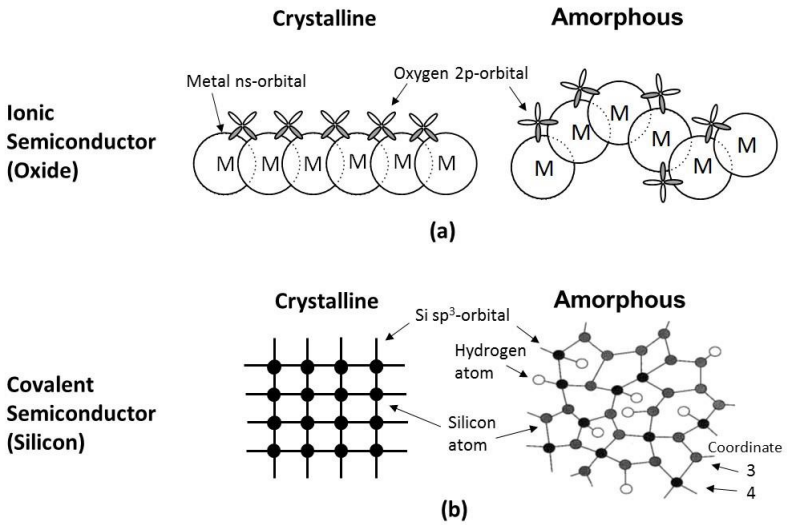


Figure 2.2: Orbital structures of (a) ionic and (b) covalent semiconductors showing conduction mechanism in crystalline and amorphous structures [20].

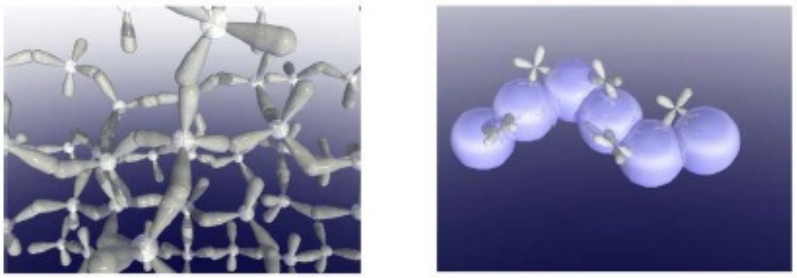


Figure 2.3: Illustration of (a) sp^3 and (b) s-orbitals bonding in an amorphous structure showing the directional nature of sp^3 orbital as opposed to the s orbital [7].

2.3 Characteristics of IGZO

IGZO is a promising material that has gained interest in the FPD industry. It is a ternary metal oxide material that is comprised of three known metal oxides: In_2O_3, Ga_2O_3 and ZnO. As mentioned earlier, this composition impedes the crystallization of the compound material at higher temperatures. Therefore, the amorphous structure that is required for large area uniformity is achieved in IGZO. IGZO is also a wide band-gap semiconductor with its energy band-gap estimated to be around 3.2 eV. Due to the wide band-gap, the IGZO material remains transparent in the visible range and is therefore a suitable candidate as a TFT active layer material.

IGZO, like other AOS materials, is an inherently n-type semiconductor material. It does not utilize dopants to alter the electronic properties to create transistors as silicon technology. In IGZO, oxygen vacancies are commonly present throughout the material. These oxygen vacancies act as intrinsic donors and their effective concentration controls the conductivity of the material. Oxygen vacancies are created due to imperfections in amorphous structure of the material. Since the material conductivity primarily depends on the concentration of oxygen vacancies, the material is understood to be devoid of p-type carriers.

Kamiya *et al.* proposed the following correlation between the cations and the electronic properties of IGZO. Each metal cation in the IGZO compound material –In,

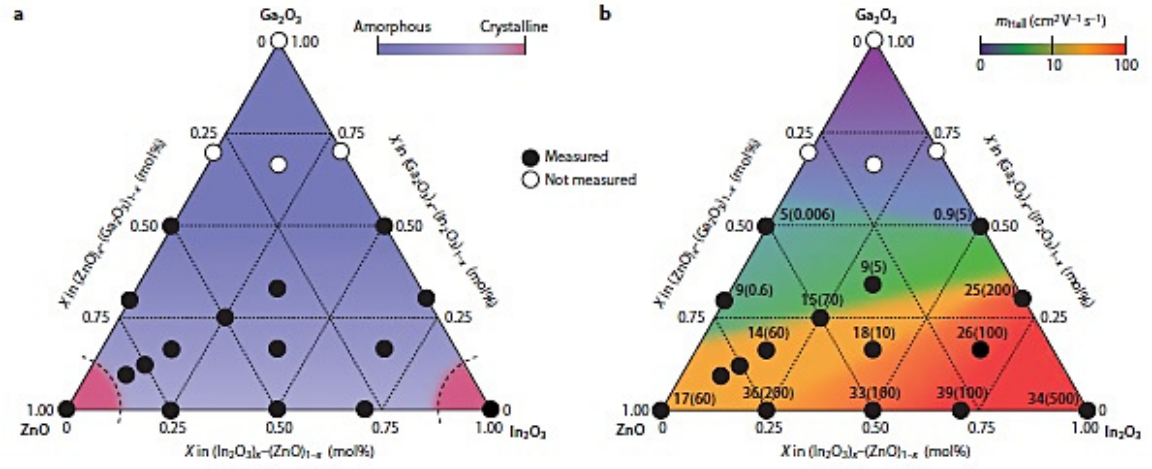


Figure 2.4: (a) Structure of IGZO material for varying compositions of IGZO (b) Electron mobilities and concentrations for varying compositions of IGZO material. The number in parenthesis denotes the carrier concentration (x 10^{18} cm^{-3}) [8].

Ga and Zn– has its unique significance in establishing the material properties of IGZO. Fig. 2.4 shows a study conducted by Kamiya *et al.* to understand the contributions of the cations. In^{+3} provides the electron conduction path due to its large spherical 5s-orbitals leading to greater overlap between adjacent orbitals. This is because In^{+3} is the only cation that meets the criterion for electronic configuration of heavy post-transition metal cation that helps conduction in AOS materials to be similar to their crystalline form. This was also verified by varying the fraction of indium in the composition of IGZO, where the samples containing maximum fraction of indium had the highest carrier concentration [8]. However, In_2O_3 is very conductive by itself and would not yield good transistor characteristics. Zn^{+2} ions provide stability to the structure and also promote a greater mobility. This is attributed to the small inter-atomic distance which provides a smaller electron effective mass [21]. The effect of Ga^{+3} was investigated by comparing the carrier concentration between Indium-Zinc-Oxide and IGZO. It was observed that the enhanced concentration of oxygen vacancies due to In^{+3} gets suppressed by the addition of Ga^{+3} ions. This was understood to be due to the ability of Ga to form stronger bonds with oxygen as compared to Zn and In ions as it has a higher ionic potential [7, 22]. The ratio of the three metal cations must

be maintained in such a way that the resulting structure always remains amorphous in order to ensure large-area uniformity. Fig. 2.4a shows the study conducted by Kamiya *et al.* to investigate a suitable ratio of elements to ensure an amorphous IGZO film is formed. It was noted that an elemental ratio of 1:1:1 would result in an effective amorphous structure of IGZO that would ensure uniformity in characteristics over larger substrates, while maintaining a good mobility and electron concentration.

2.4 Ambient Interactions

IGZO is very sensitive to ambient interactions. The electrical properties of the material can be easily engineered by subjecting IGZO to different ambients. This section briefly compares the changes in electrical characteristics of IGZO when subjected to different ambients.

2.4.1 Annealing Conditions

Deposition and annealing conditions define the electronic properties of IGZO. As-deposited IGZO TFTs, without anneal, showed extremely poor electrical characteristics. Therefore, annealing is crucial to control defect states in the IGZO material. Performance of IGZO TFTs with respect to different annealing conditions and ambient interactions was investigated in this study.

Samples annealed at 400°C under vacuum resulted in highly conductive I-V characteristics. It is theorized that this occurs due to the increase in free electron concentration from the increased oxygen vacancies in IGZO under vacuum. Another sample was annealed at 400°C in N_2 ambient. The resulting TFTs showed no gate modulation and exhibited resistor-like characteristics (see Fig. 2.5a). This confirmed the need for an oxidizing ambient in order to reduce oxygen vacancies and establish an appropriate free-electron concentration in IGZO. Upon subjecting the IGZO device to a 400°C aggressive oxidation treatment in air ambient, the I-V characteristics

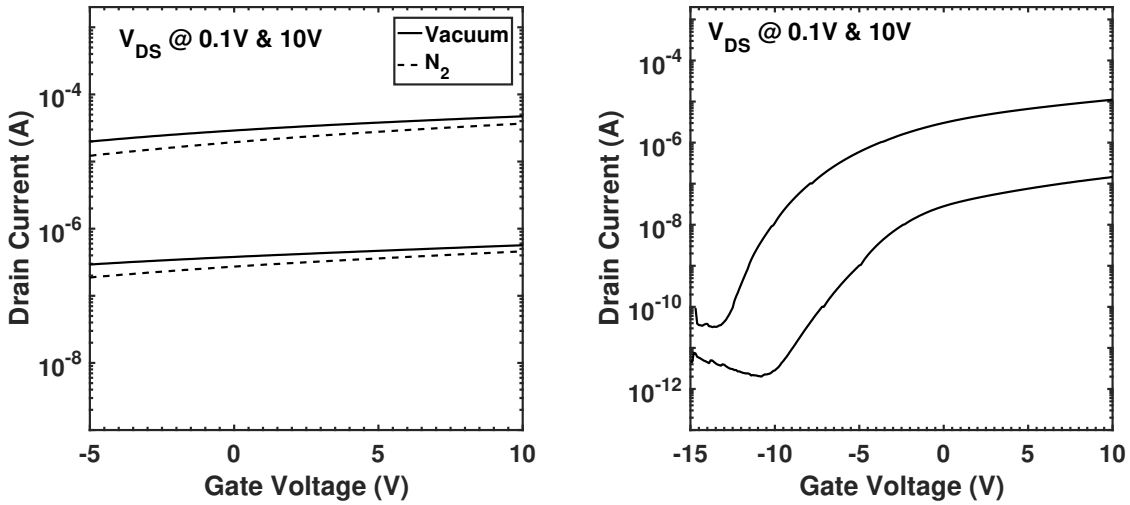


Figure 2.5: (a) *I-V* transfer characteristics of a L/W = 24/100 µm TFT after vacuum and N_2 anneal at 400°C (b) *I-V* transfer characteristics of a L/W = 24/100 µm TFT after air anneal at 400°C [9]

significantly shifted left, showing depletion-mode operation with loss of gate control (see Fig. 2.5b). However, annealing the sample in air ambient at 350 °C resulted in enhancement-mode devices with good gate modulation. Annealing in forming gas (H_2/N_2) showed improved characteristics in comparison to the air anneal, with a steep subthreshold slope and high on-state current. In contrast, annealing in O_2 demonstrated a slight degradation in performance when compared to the forming gas ambient (see Fig. 2.6).

Annealing in forming gas with an air ramp-down was then investigated. This anneal yielded good device characteristics. However, the devices stored in air ambient shifted slightly to the left over time. Fig. 2.7a shows the transfer characteristics after an anneal in H_2/N_2 with an air ramp-down. The presence of the H_2 did not appear to offer any significant benefit and therefore anneal in N_2 ambient with an air ramp-down was investigated significance of H_2. This anneal condition resulted in superior device performance and improved the device stability over time, indicating that the reason for instability with H_2/N_2 anneals might be attributed to the presence of H_2. It was observed that annealing in N_2 ambient at 400°C followed by an air ramp-down

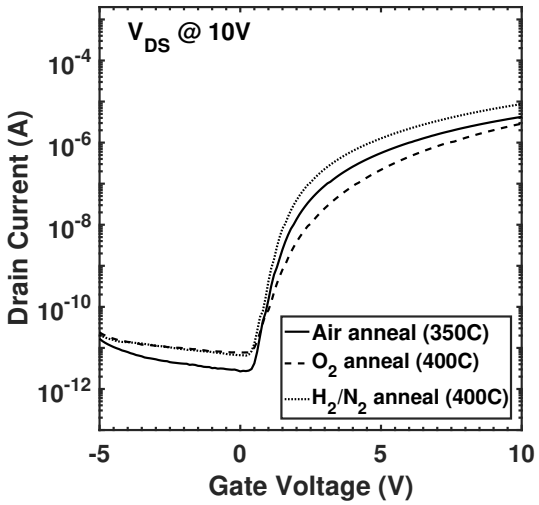


Figure 2.6: Comparison of *I-V* transfer characteristics between air, O_2 and H_2/N_2 anneals [9].

gave desirable device characteristics and better stability (as shown in Fig. 2.7b).

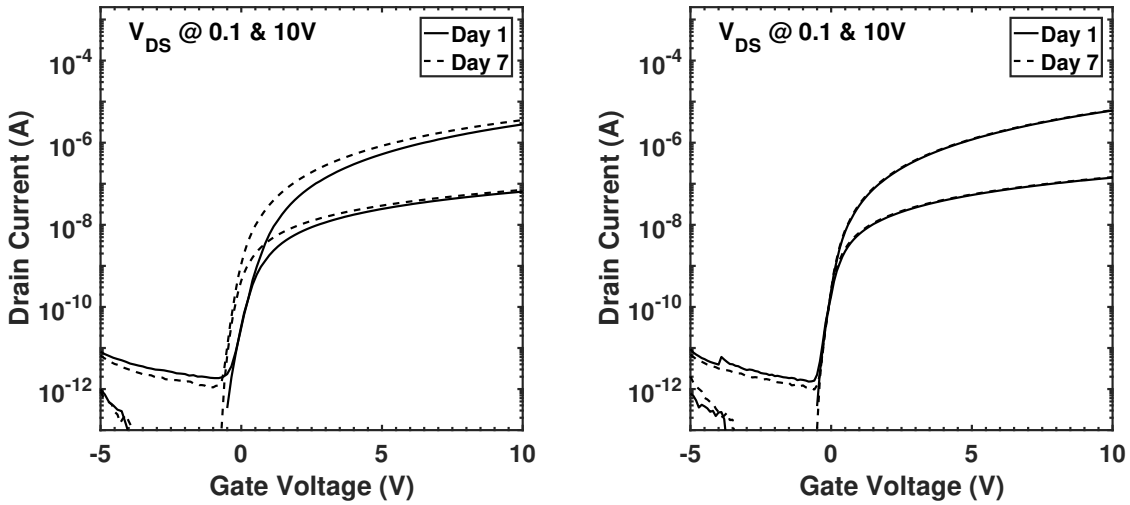


Figure 2.7: *I-V* transfer characteristics after anneals in (a) H_2/N_2 with an air ramp-down and (b) N_2 with an air ramp-down [9].

2.4.2 Interactions with hydrogen and water

IGZO is also sensitive to an O/H–containing ambient. Therefore, it is crucial to understand the influence of oxygen and hydrogen on the electrical properties of IGZO. Oxygen helps reduce the oxygen vacancies in the IGZO material, thereby reducing the

free electron concentration. The role of an oxidizing ambient has been established in Section 2.4.1. Hydrogen, on the other hand, forms -OH bonds which ionize to generate H^+ and a free electron. Kamiya *et al.* studied that the formation energy of H^+ ions from -OH bonds was small ($\sim$ 0.45 eV) [23]. This leads to an increased generation of free electrons during a hydrogen anneal or in the presence of hydrogen ambient, thereby increasing the conductivity of IGZO.

Exposure to water and high humidity also affects the electrical properties of IGZO. Park *et al.* reported that water absorption significantly influenced the electrical parameters of the IGZO TFT. The adsorbed water molecules are believed to form an accumulation layer in the IGZO surface, thereby increasing conductivity of the IGZO material [10].

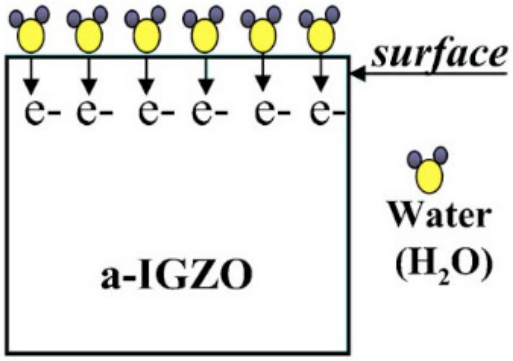


Figure 2.8: Illustration of water forming an accumulation layer on the IGZO surface [10].

2.5 Materials for Passivation of IGZO

In order to suppress ambient interactions and improve stability of IGZO TFTs, the IGZO is protected by a passivation material. Various dielectrics were investigated as candidates for passivation material. Some of the candidates were PECVD TEOS oxide, e-beam deposited quartz and e-beam deposited alumina (AlO_x). It was noted that deposition of passivation material on the IGZO back-channel rendered it conductive due to increase in interface states. Therefore, a more aggressive oxidation

anneal was required post-passivation to yield desired semiconductive behavior.

E-beam quartz did not yield working TFTs even after an aggresive anneal. However, both TEOS passivated and e-beam AlO_x showed improved stability and suppressed hysterisis after an aggresive anneal in oxygen. Fig. 2.9 shows a comparison between the *I-V* characteristics of quartz, e-beam alumina and PECVD SiO_2 (with TEOS precursor). From the figure, it is evident that quartz is not a good passivation material that could yield stable TFT characteristics [11].

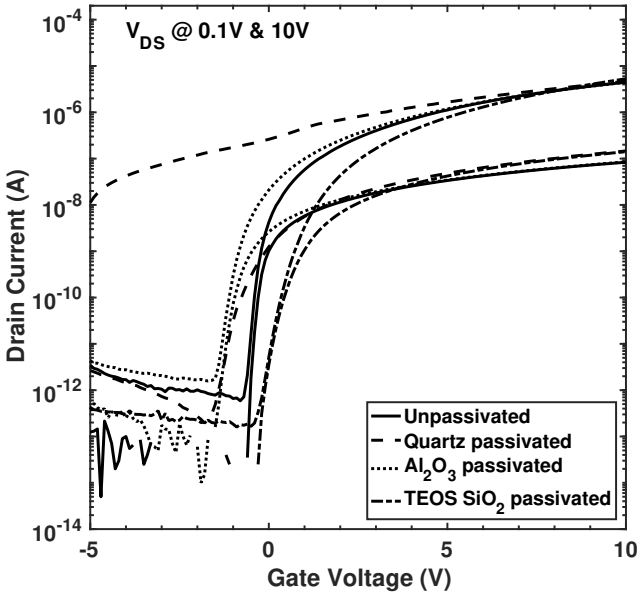


Figure 2.9: I-V characteristics of quartz, alumina and TEOS SiO_2 passivated TFTs [11].

Although e-beam alumina showed promise as a good passivation material, it had to use a lift-off process for deposition due to problems with etch selectivity. Therefore, TEOS SiO_2 was preferred as the baseline passivation material due to ease of process integration and benefits as a dielectric for double gate TFTs.

2.6 Density of States Distribution of IGZO

In order to gain a better understanding of the operation of the IGZO TFTs, it is essential to understand the density of states distribution in IGZO. In IGZO, the acceptor

level subgap density of states distribution [$g_{\mathrm{A}}(E)$] primarily consists of acceptor-like tail states [$g_{\mathrm{TA}}(E)$]. The donor level density of states [$g_{\mathrm{D}}(E)$] includes the donor-like tail states [$g_{\mathrm{TD}}(E)$] and density of oxygen vacancies in the material. The amorphous nature of the material contains structural disorders that induce electron scattering, leading to localized wave functions. This leads to the formation of localized tail state distributions of $g_{\mathrm{TA}}(E)$ and $g_{\mathrm{TD}}(E)$. The acceptor-like tail states ($g_{\mathrm{TA}}(E)$) near the conduction band minimum are thought to originate due to disorders of metal ns-bands whereas the donor-like band tail states ($g_{\mathrm{TD}}(E)$), located near the valence band minimum, originate mainly due to the oxygen p-band disorders [12]. The tail states seem to fit an exponential distribution whereas the distribution of oxygen vacancies has a tighter fit to a gaussian distribution. Mathematically, the density of state distribution can effectively be modelled as,

$$g_{\mathrm{A}}(E) = N_{\mathrm{TA}} \times exp\left(\frac{E - E_{\mathrm{C}}}{W_{\mathrm{TA}}}\right) \tag{2.1a}$$

$$g_{\mathrm{D}}(E) = N_{\mathrm{TD}} \times exp\left(\frac{E_{\mathrm{V}} - E}{W_{\mathrm{TD}}}\right) + N_{\mathrm{OV}} \times exp\left(-\left(\frac{E - E_{\mathrm{OV}}}{W_{\mathrm{OV}}}\right)^2\right) \tag{2.1b}$$

where N_{TA} represents the density of acceptor-like trap states near at the conduction band edge, N_{TD} represents the density of donor-like trap states at the valence band edge and N_{OV} represents the concentration of oxygen vacancies present in the material. Fig. 2.10 shows a pictorial representation of the DOS distribution in IGZO as proposed by Fung et al.

The donor-like oxygen vacancy distribution is considered to be located closer to the conduction band minimum as the structure becomes highly relaxed after a thermal anneal. The thermal anneal step is considered to improve the interface quality. On the other hand, without a thermal anneal, the energy distribution is located near the mid-band or closer to the valence band minimum [12]. Therefore, the electrical properties of the IGZO material are enhanced after a thermal anneal. This study provided a

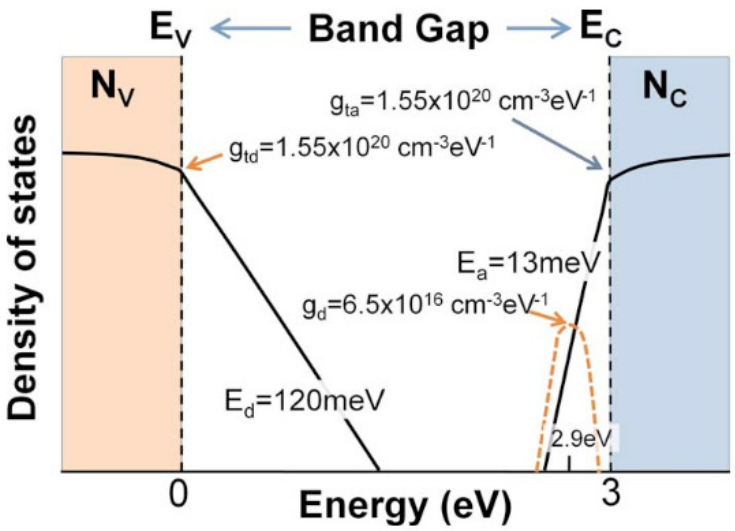


Figure 2.10: Proposed DOS distribution in IGZO [12].

qualitative distribution of the density of states in the IGZO structure. Quantitative analysis providing energy levels and concentration gradients of the illustrated model would require further investigation.

2.7 Summary

Earlier sections of this chapter discussed material and electrical characteristics that make IGZO a suitable channel material for TFTs. It also briefly demonstrated the ambient sensitivity of IGZO and established the need for a good passivation material to improve electrical stability. The following chapter would discuss in detail the fabrication and operation of IGZO TFTs with a back-channel passivation material.

Chapter 3

Fabrication and Operation of IGZO TFTs

This chapter will provide an overview of the TFT structures used for investigation. The fabrication process for the different structures will be detailed along with discussions of the electrical characteristics. Preliminary results concerning bias-stress response of IGZO TFTs will be introduced.

3.1 Bottom-Gate TFT

Bottom-gate TFTs are fabricated as a staggered TFT structure. This structure is used as the baseline process to investigate electrical characteristics and performance of Bottom-Gate (BG) TFTs.

3.1.1 Fabrication Process Overview

A 150 mm Si wafer with a 650 nm thermal oxide is used to emulate a glass subtrate. A 50 nm molybdenum gate electrode is DC-sputter deposited and patterned using a quartz reticle by a subtractive etch process. A 100 nm silicon dioxide (SiO_2) layer is deposited as the gate dielectric using low temperature Plasma-Enhanced Chemical Vapor Depositon (PECVD) mechanism with tetraethyl orthosilicate (TEOS) as a precursor. The SiO_2 is then densified at 600 °C for 2 hours in N_2 ambient. After densification of gate dielectric, a 50 nm layer of IGZO material is RF-sputter deposited at 200°C using an IGZO target with In:Ga:Zn:O in the atomic ratio of 1:1:1:4 in a sputter ambient containing 7 % oxygen. The IGZO layer is then patterned by subtractive

etch in 6:1 dilute HCl solution. Gate pads are patterned to etch gate dielectric using 10:1 Buffered-Oxide-Etch (BOE) solution to provide contact openings to the underlying gate electrode. Mo/Al bilayer, used for source and drain electrodes, is then deposited by a lift-off process as the IGZO is not chemically robust. A passivation material can be deposited to protect the underlying IGZO from room ambient. The passivation material used for this process is a 100 nm PECVD SiO_2 layer with TEOS as a precursor. A final anneal is then performed to reduce conductivity of IGZO and enable it to have good TFT characteristics. If the structure is unpassivated, the anneal is performed at 400 °C in N_2 ambient followed by an air ramp down. The anneal in N_2 ambient helps reduce the number of oxygen vacancies present in the IGZO material, leading to a lower electron concentration. On the other hand, if the structure is passivated, the anneal is performed at 400 °C for 4 hours in O_2 ambient followed by a 5 hour ramp-down in air. This is a more aggressive oxidation anneal as the IGZO is protected by SiO_2. An additional level of lithography would be required in this case to pattern and etch contacts to source and drain electrodes.

A top-down micrograph and cross-sectional illustration of the resulting structure may be seen in Fig. 3.1.

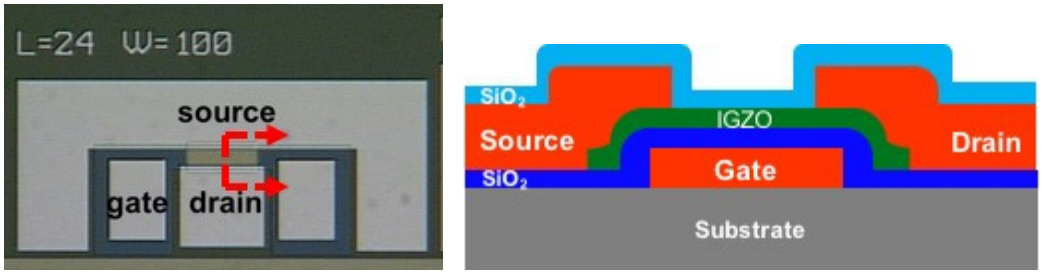


Figure 3.1: (a) Top-down and (b) cross-sectional view of a SiO_2 passivated staggered bottom-gate TFT.

3.1.2 Electrical Characteristics

The structure of an unpassivated staggered BG TFT structure is depicted in Fig. 3.2a. Staggered BG TFTs are investigated as a baseline treatment for further studies,

fabricated according to Section 3.1.1. I-V transfer characteristics can be seen in Fig. 3.2b. The V_T is $-0.25\,\mathrm{V}$ with a μ_{eff} of 11.19 $\mathrm{cm}^2/\mathrm{Vs}$ and a subthreshold swing (SS) of 124 mV/dec [13]. This device was annealed in a nitrogen ambient at 400 °C for 30 min with an air ramp-down.

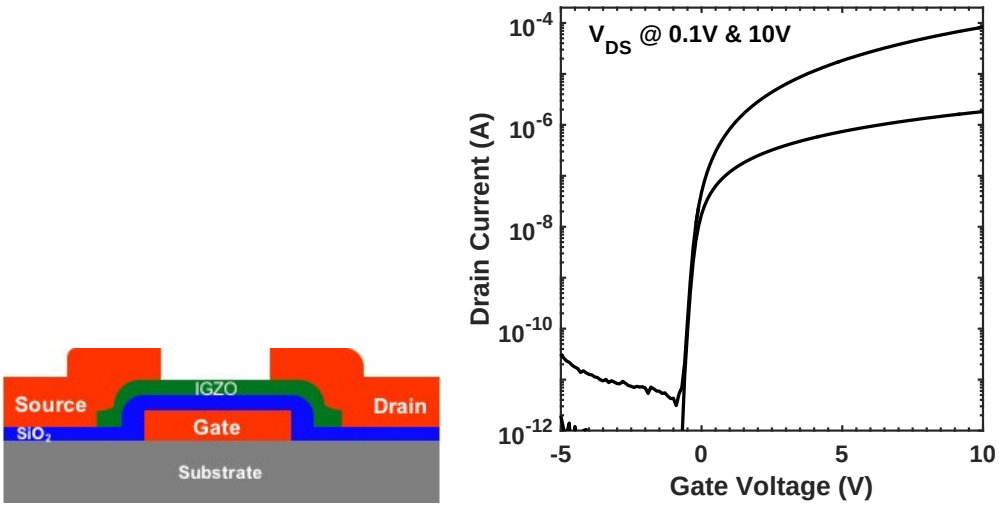


Figure 3.2: (a) Cross-sectional view of a staggered bottom-gate IGZO TFTs without a back-channel passivation material (b) I-V transfer characteristics of a L/W = 24/100 µm TFT with $\mathrm{V_{DS}} = 0.1\,\mathrm{V}$ and 10 V [13].

3.2 Double-Gate TFT

Double-gate TFTs are derived out of the BG TFT structure by adding an additional top gate electrode over the passivation layer. This is done to offer an enhanced channel control, and thereby improving the I-V characteristics of the TFTs.

3.2.1 Fabrication Process Overview

The fabrication steps followed to design Double-Gate (DG) TFTs follows the same procedure as described in Section 3.1.1 till the final passivation anneal. Following the final anneal, 250 nm of evaporated aluminum is patterned through a lift-off process to become the top gate electrode. Fig. 3.3a shows a cross-sectional view of the DG

TFT structure.

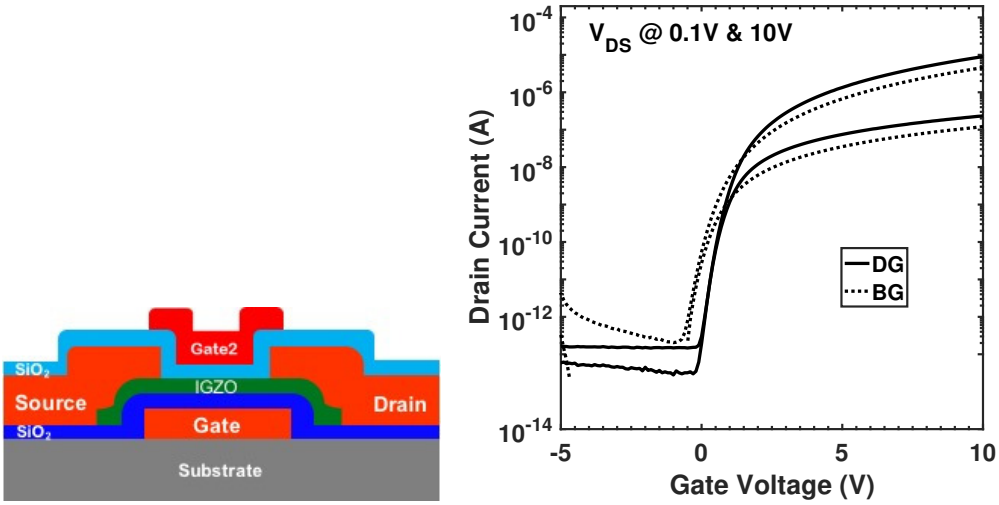


Figure 3.3: (a) Cross-sectional view of a double-gate IGZO TFTs (b) Comparsion of *I-V* transfer characteristics between a L/W = 24/100 µm double-gate and SiO_2 passivated bottom-gate TFT with $V_{DS} = 0.1\,\mathrm{V}$ and $10\,\mathrm{V}$

3.2.2 Electrical Characteristics

Fig. 3.3b shows the comparison of *I-V* characteristics between a double-gate and bottom-gate TFT structures. As illustrated, the presence of an additional top gate enhances the on-off ratio and the subthreshold swing of the TFT. *SS* of the DG TFT improved from 260 mV/dec to 180 mV/dec whereas the mobility μ_{eff} doubled with an additional gate electrode on top.

3.3 Capacitance-Voltage Characteristics

In TFTs, the gate metal-dielectric-IGZO structure acts as a capacitor. The structure becomes capacitively coupled when voltage is applied. Electrically, it behaves as two capacitors connected in series: one capacitor formed by gate dielectric and the other being formed by the IGZO material.

Traditionally, Si based MOS capacitors have three regions of operation: accumulation, depletion and inversion. Accumulation region is formed when the majority carriers form the surface channel in the semiconductor. Depletion region occurs when the surface is depleted of majority charge carriers. This results in discharge of the gained capacitance during accumulation. This is followed by inversion region where the applied voltage is sufficient to attract minority charge carriers to the surface, thereby enabling charging of capacitance due to channel inversion.

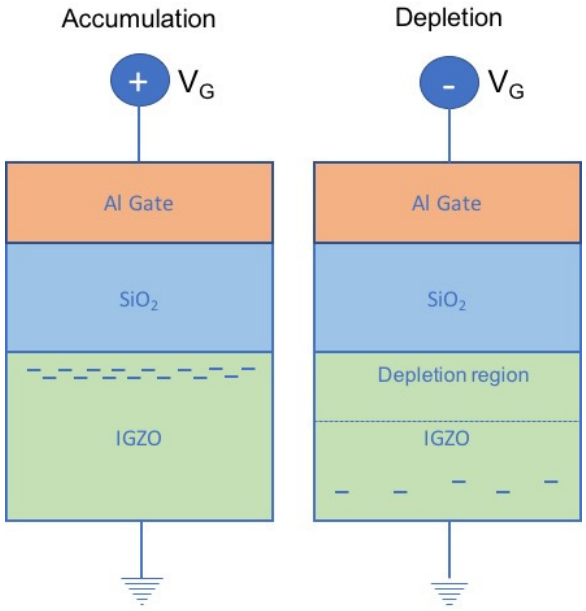


Figure 3.4: Working of an IGZO MOS capacitor in (a) accumulation and (b) depletion modes

However, IGZO consists of only electrons as charge carriers as it is an inherently n-type material. Therefore, it operates only in accumulation and depletion modes. Fig. 3.4 offers a schematic representation of the capacitor operation in the two operating modes. When the applied gate voltage (V_G) is positive, electrons present in the IGZO material are pulled towards the surface, resulting in charging of capacitor in accumulation mode. On the contrary, as V_G becomes increasingly negative, electrons are repelled by the negative gate voltage, depleting the IGZO surface of electrons and causing the capacitor to get discharged. Due to absence of hole carriers, inversion

does not occur. Fig. 3.5a illustrates the C-V characteristics exhibited by a typical IGZO TFT. This was measured on an inter-digitated capacitor, therefore the remaining capacitance in depletion region is due to the overlapping electrodes (gate over channel-contact-metal). Fig. 3.5b represents the structure of a typical inter-digitated capacitor.

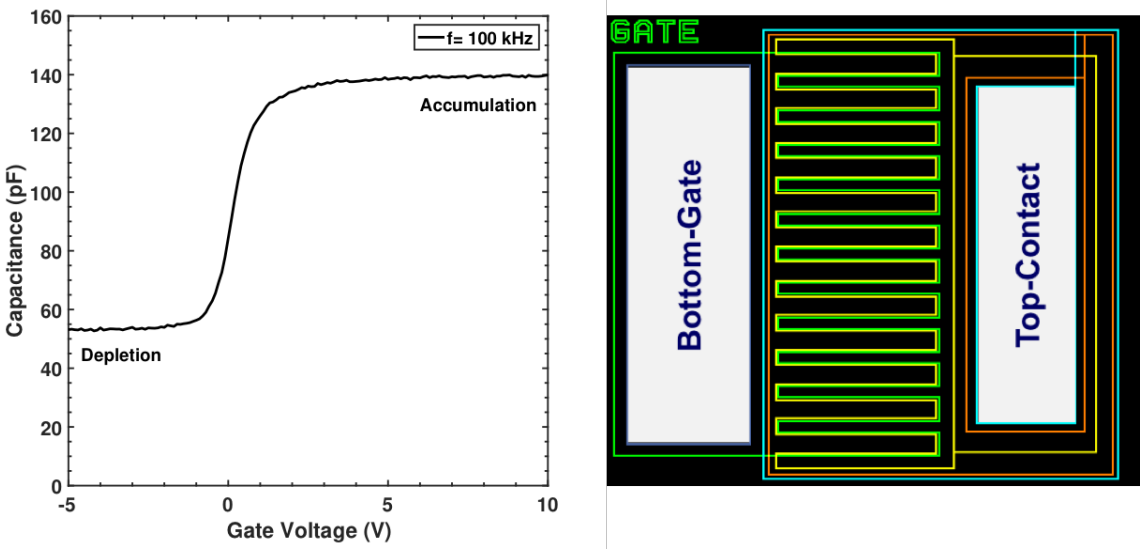


Figure 3.5: (a)C-V characteristics of a typical IGZO MOS capacitor (b) Structure of a typical inter-digitated capacitor

3.4 Investigation of Bias-Stress Instability

This section presents a preliminary analysis on the bias-stress instabilities involved in BG and DG TFTs. Electrical stress or bias-stress stability is an important performance indicator for TFTs, considering it has a direct impact on the lifetime of the display.

This can be investigated by prolonged application of voltage on one or more terminals of the TFTs. On application of bias-stress for a long time, TFTs may show a decaying performance with threshold voltage (V_T) shifts and degradation of SS. This affects the display brightness as it causes imprecise switching of pixels.

Table 3.1: Summary of Bias-stress conditions

Stress Type	V_{GS} (V)	V_{DS} (V)
PBS	+10	0
NBS	-10	0

Predominantly, there are two conditions for bias-stress testing on TFTs. Positive-Bias Stress (PBS) involves application of a positive voltage on the gate electrode for a prolonged duration, whereas Negative-Bias Stress (NBS) involves holding the gate electrode at a negative voltage, keeping the source and drain electrodes grounded. A short summary of the bias-stress conditions has been outlined in Table 3.1.

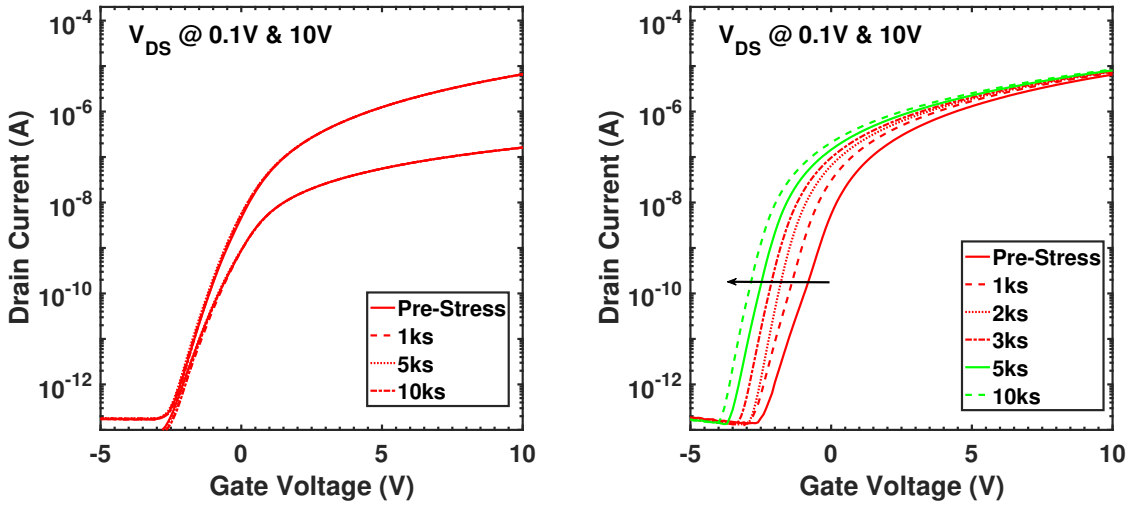


Figure 3.6: (a) PBS on a L/W = 24/100 µm SiO_2 passivated BG TFT (b) NBS on a L/W = 24/100 µm BG TFT [13].

Fig. 3.6 depicts the influence of PBS and NBS stress on BG TFTs. The stress was perfomed for 10,000 seconds (roughly 2.5 hours) for both PBS and NBS. As observed, PBS stress does not seem to have much of an influence on BG TFTs. On the other hand, there is a left shift in V_T observed after NBS stress. This shift seems to occur due to the ionized donor states behaving as fixed charges rather than interface traps.

Fig. 3.7 illustrates the influence of PBS and NBS stress on DG TFTs. In contrast to BG TFTs, DG TFTs show a significant right shift in V_T with a PBS stress. This

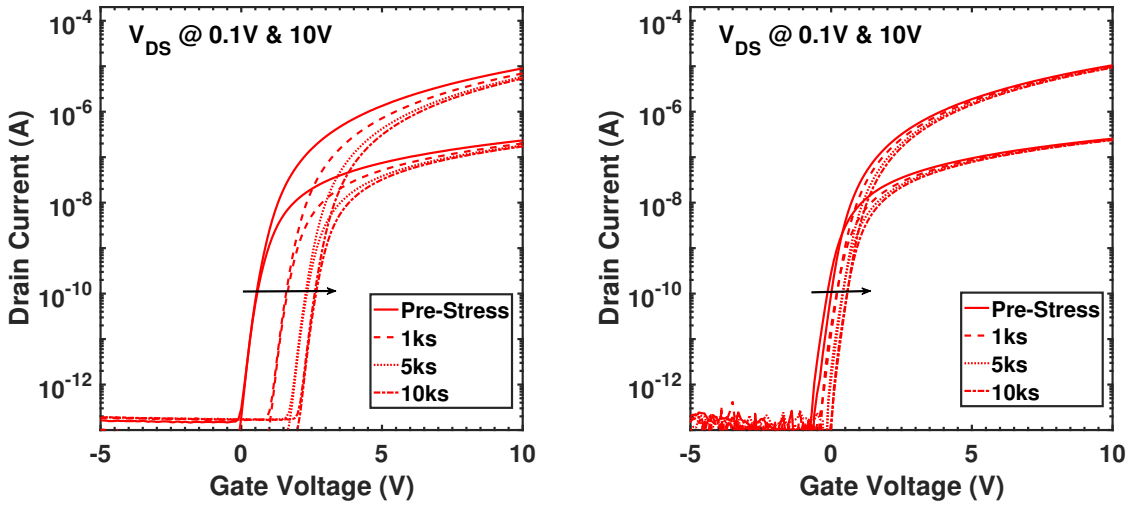


Figure 3.7: (a) PBS on a L/W = 24/100 µm DG TFT (b) NBS on a L/W = 24/100 µm DG TFT [13].

instability is attributed to the oxide charge present in the overlapped regions between the gate electrode and source/drain electrodes, which arises due to electron injection and trapping [13].

3.5 Summary

In this chapter, a detailed overview of the fabrication process for BG and DG IGZO TFTs was described. A quick background to the C-V behavior of IGZO MOSCAPs was provided, followed by discussion of preliminary bias-stress results of IGZO TFTs.

The sensitivity of IGZO to bias-stress created the motivation to verify if it was possible to recover the characteristics by performing a hot-plate anneal. The anneal caused the characteristics to drastically left-shift, thereby becoming very conductive. The results of this experiment became the primary motivation to further investigate the thermal instability of IGZO TFTs, which is introduced in the next chapter.

Chapter 4

Investigation of Thermal Instability

This chapter primarily focusses on detailing the investigations of thermal instability in IGZO TFTs. A proposed hypothesis explaining the reason for this behavior is presented. Possible process modifications to control the instability will be investigated.

4.1 Introduction to Thermal Instability

Thermal stability of the TFT is important as the transistors may need to undergo processes even after completion which use a higher temperature. Chip-on-glass bonding would be one such process that may require heat in order to improve bonding. Even though the characteristics might have been stable upon completion, the performance might deteriorate upon subjecting the devices to an additional process at a higher temperature. In order to investigate the thermal stability of IGZO TFTs, the devices were subjected to elevated temperatures (up to 200 °C). The devices demonstrated erratic behavior with the I-V characteristics varying significantly.

Fig. 4.1 shows the effect of a 20 minute hot-plate bake at 200 °C on BG and DG TFTs. In the case of BG devices (see Fig. 3.7a), a significant left shift in I-V characteristics was observed. On the other hand, DG devices showed resistor-like characteristics following the hot-plate bake (see Fig. 3.7b). This observation was surprising since the devices showed stable characteristics after the final passivation anneal at 400 °C.

In order to investigate recovery of the devices, an additional furnace anneal at 400

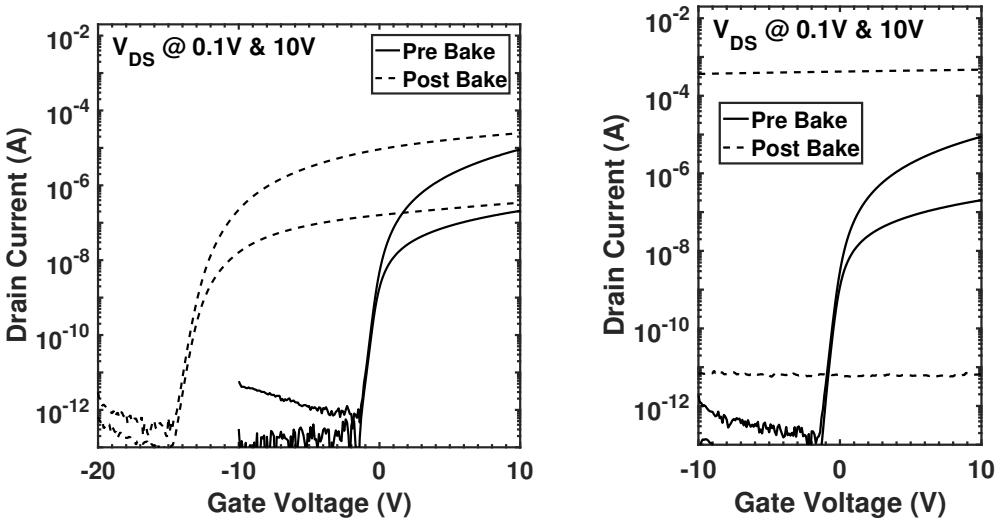
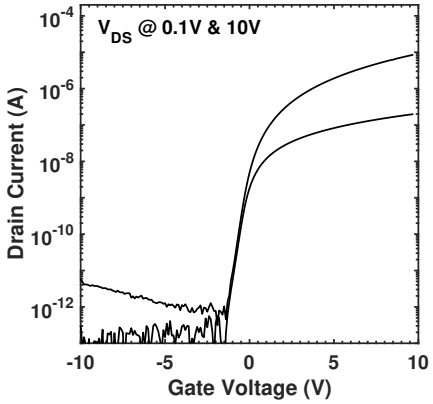


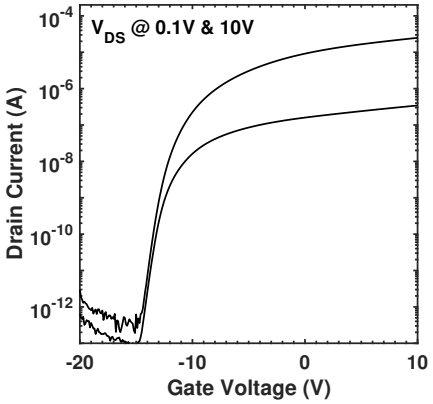
Figure 4.1: Effect of a 20 minute hot-plate bake at 200 °C on a L/W = 24/100 µm SiO_2 passivated (a) BG TFT and (b) DG TFT

°C was performed in O_2 ambient. The furnace anneal did not have any impact on DG TFTs but had an influence on BG TFTs. Fig. 4.2 highlights the results of the additional anneal. As observed previously, BG devices have a significant left-shift in I-V characteristics when subjected to a hot-plate bake. The additional furnace anneal helped the characteristics to shift back to its initial V_T. However, the characteristics were distorted and did not improve with time (see Fig. 4.2c). The characteristics observed after the additional anneal was similar to "over-oxidation" observed in earlier experiments. In previous research, the IGZO TFTs have shown improvements in electrical characteristics when stored in room ambient after 3 days following the passivation anneal. This was explained to be due to a phenomenon referred to as ripening [24]. However, there were no improvements in characteristics noted when tested after 3 days (see Fig. 4.2d). It is therefore believed that a hot-plate bake results in permanent distortion of electrical characteristics.

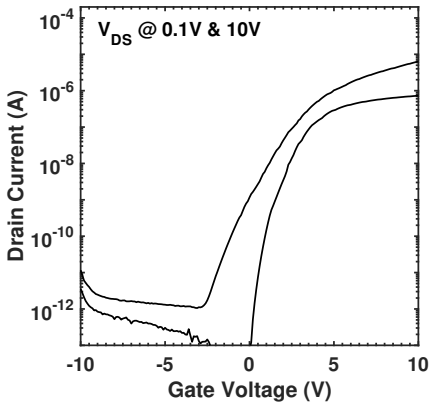
Since the attempt to recover these devices was not successful, further investigation was carried out to understand the temperature-time response in order to identify the point at which the devices begin showing instability. DG TFTs were investigated for



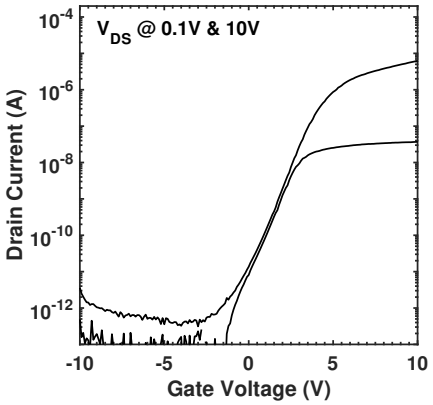
(a) Before 200°C hot-plate bake



(b) After 200°C hot-plate bake



(c) After additional 400°C O_2 furnace anneal



(d) 3 days after furnace anneal

Figure 4.2: Event sequence investigating recovery of a 200°C hot-plate baked L/W = 24/100 µm BG TFT by additional furnace anneal in O_2

this experiment. All the devices received a standard 400 °C O_2 anneal before the hot-plate bake experiments.

The DG TFTs were subjected to temperature increments of 10 °C on the hot-plate in room ambient. The hot-plate bake time was also increased at certain temperatures. As the temperature on the hot-plate was increased, the characteristics started to show a left-shift. The devices were stable until a temperature of 90 °C, with the instability beginning to occur around a temperature of 100 °C. Fig. 4.3 illustrates the time-temperature response of DG TFTs to a hot-plate bake. This shift in characteristics was observed to be dependent on the accumulated combinations of temperature and

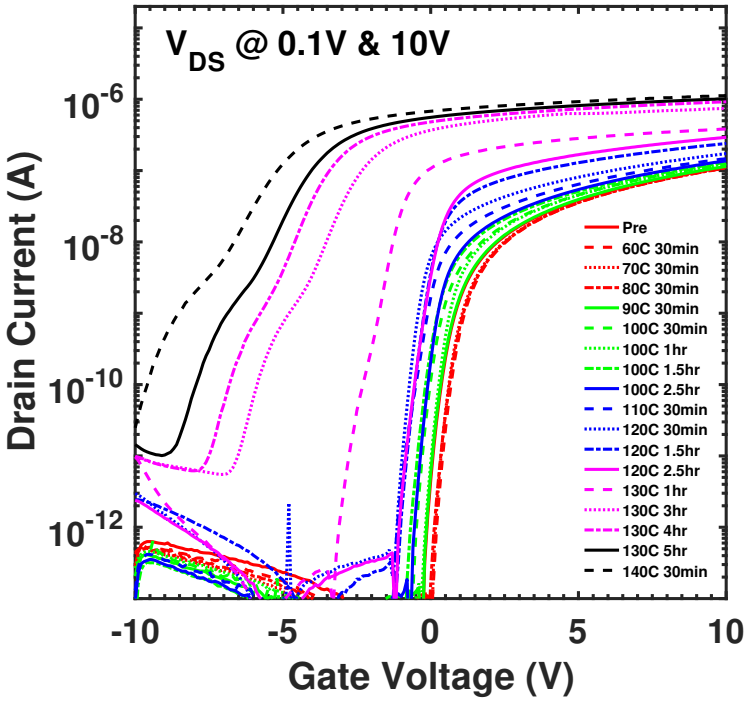


Figure 4.3: Effect of hot-plate bake from 60 °C to 140 °C on a L/W = 48/100 µm DG TFT

time.

4.2 Hypothesis behind Thermal Instability

It is hypothesized that the IGZO TFTs show thermal instability due to the presence of water in the SiO_2 passivation layer, absorbed by the oxide after deposition. Wager *et al.* demonstrated donor behavior in IGZO and as a source of instability in unpassivated devices [25]. Water is also readily absorbed by PECVD SiO_2. Upon performing a hot-plate bake on DG devices, the water present on the surface and bulk regions of the oxide layer reacts with the Al gate on top to form aluminum oxide and liberate monatomic hydrogen [26].The released hydrogen diffuses through the oxide layer to the SiO_2-IGZO interface and reacts with the IGZO surface/bulk. This reaction effectively increases the electron concentration in the IGZO as hydrogen has a donor effect [27], causing a left shift in *I-V* characteristics. Fig. 4.4 illustrates the proposed

mechanism depicting liberation of monatomic hydrogen from the water molecule with the presence of a top gate Al electrode.

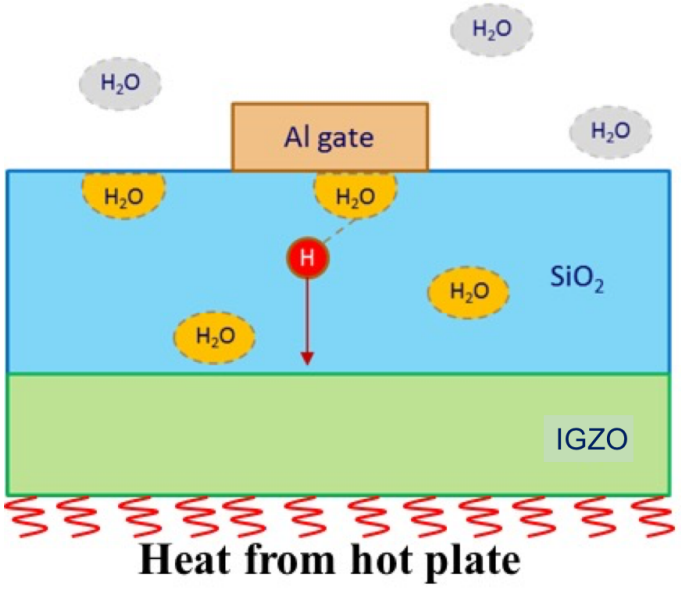


Figure 4.4: Generation of monatomic hydrogen upon application of heat due to the presence of top gate aluminum in DG TFTs

It is understood that a minute amount of water gets readily absorbed by the oxide in room ambient. This is due to the porous nature of the undensified oxide. A stress relaxation study conducted on standard PECVD TEOS oxide corroborates this investigation [14].

Fig. 4.5 depicts the study that compared relaxation of stress with time after oxide deposition between two wafers A12 and A13 obtained from the same process lot. The study demonstrated stress in TEOS oxide changing from tensile to compressive over a week, which is characteristic of a porous film. Upon an 8 hr 600C furnace anneal, the stress reverts back to initial state, strongly suggesting a structural change occuring within the oxide. The study also verifies that the stress is from TEOS by measuring zero stress after removing the deposited oxide.It can be inferred that the structural changes within the oxide mainly occur as a result of water molecules getting desorbed during the anneal.

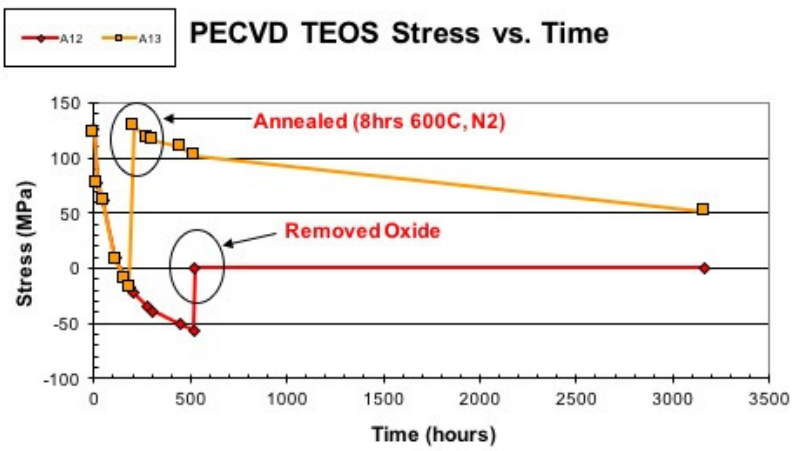


Figure 4.5: Stress relaxation study of PECVD TEOS indicating water absorption over time [14].

There is an increased need to further understand the phenomenon and effectively address the instability in IGZO TFTs. Further analysis supporting the role of monatomic hydrogen in IGZO TFTs would be necessary to verify the hypothesis of thermal instability. Additional capping layers could possibly suppress the influence of hydrogen on the IGZO material.

Different ALD materials were explored for the capping layer, aluminum oxide and hafnium dioxide being the preferred due to process limitations. ALD alumina and hafnium dioxide were understood to be good barriers to water due to their high chemical resistance as a result of the strong bond [28].

4.3 Verification of hypothesis using MOS capacitors

A part of the proposed operative mechanism in the working hypothesis involves the availability of hydrogen. An investigation on silicon MOSCAPs was done since interface traps are readily passivated by hydrogen during the sintering process.

Sintering is the process of annealing MOS capacitors at elevated temperatures so that the adsorbed water in the oxide reacts with the metal gate. This reaction creates a metal oxide interface which effectively releases monatomic hydrogen. The

monatomic hydrogen species migrate to Si-SiO_2 and helps passivate interface traps. As a result, the total number of surface states rapidly reduce lowering effective contact resistance. Therefore, the sinter process is essential to make ohmic contacts.

However, the process that proves to be beneficial for MOS capacitors can be detrimental for IGZO TFTs. The monatomic hydrogen generated in the process penetrates through the oxide layer to the IGZO surface. The hydrogen is understood to have a donor effect upon interaction with IGZO [10, 27]. As a result, there is a rapid increase in electron concentration due to the hydrogen acting as a catalyst. This causes the rapid shift in I-V characteristics that is observed upon subjecting IGZO TFTs to elevated temperature treatments.

MOS capacitors (MOSCAPs) with a similar stack can be studied to further understand and verify the mechanism. By introducing an additional capping layer over the oxide dielectric (TEOS precursor), the water absorbed by dielectric, causing diffusion of generated monatomic hydrogen to the IGZO surface, can be effectively suppressed. For MOSCAPs, this means that the sintering process is impeded, causing them to exhibit poor C-V characteristics. Fig. 4.6 depicts the MOSCAP structure with a capping layer to prevent migration of hydrogen to the semiconductor material.

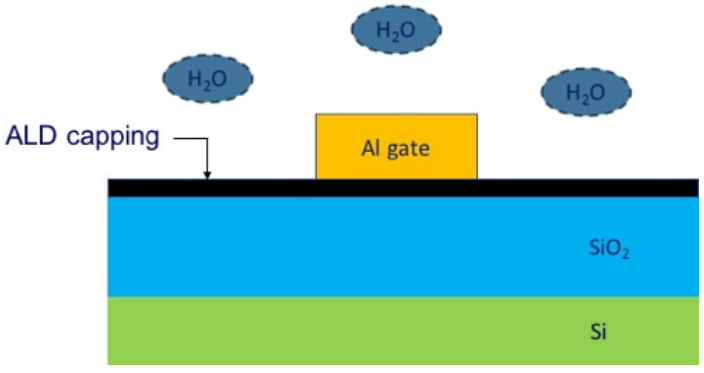


Figure 4.6: Cross-sectional depiction of MOSCAP structure with ALD capping layer

There were two sets of capacitors: one set went through a standard sinter at 450°C. The other set was not sintered and was retained for hotplate experiments.

4.3.1 Discussion of TEOS-based sintered MOSCAP results

This experiment used n-type Si MOSCAPs with passivation TEOS oxide. The TEOS oxide was annealed for 8hr in 400°C with O_2 ambient in order to replicate conditions seen in IGZO TFTs. After anneal, it either received ALD hafnia, ALD alumina or no capping layer. This was followed by evaporation of aluminum for the gate electrode.

Fig. 4.7 shows a comparison between the normalized capacitance values with and without an ALD capping layer following a 30 minute sinter at 450°C in N_2 ambient.

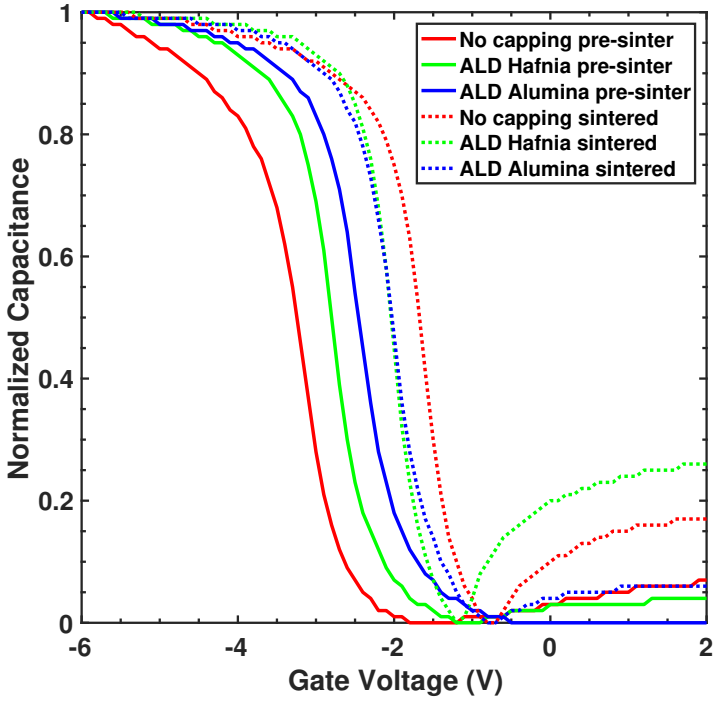


Figure 4.7: Comparison between normalized capacitances of TEOS only, ALD Hafnia and ALD Alumina capping layers following a 450°C N_2 sinter

The capacitance is normalized in order to make comparisons between capacitors with different dielectrics easier. From Fig. 4.7, it can be observed that the MOSCAPs without ALD seems to improve the most after a sinter anneal is performed as a result of hydrogen passivation. On the contrary, the ALD capping layers seem to curtail the sinter process of MOSCAPs. Although ALD hafnia and alumina show some difference

in pre-sinter, they end up with the almost the same V_{FB} post-sinter. This indicates that ALD layers may offer some suppression of interface trap passivation at 450°C. ALD capping treatments post-sinter are left-shifted from the no capping sample by an amount, presumably due to suppression of sintering with an ALD capping layer.

The mechanism behind the MOSCAPs with the ALD capping layer showing lesser impact of the anneal supports the hypothesis explaining the influence of water trapped in the TEOS oxide.

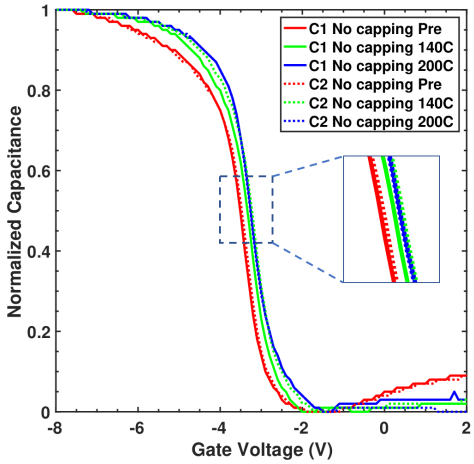
4.3.2 Impact of hotplate bake on unsintered TEOS-based MOSCAPs

Unsintered MOSCAPs were subjected to a hotplate anneal after metal deposition to replicate the conditions seen for thermal experiments on IGZO TFTs. The purpose of this experiment was to see if there is a possibility of Si/SiO_2 interface passivation at 140-200°C. This range of interest was selected for the following reason: 140°C being the temperature at which dehydration bake is done on resist track for all wafers, and 200°C being the ALD process temperature. Also, this experiment would check effectiveness of the ALD capping materials and possibly recommend best candidate to act as a strong water/hydrogen barrier in IGZO TFTs.

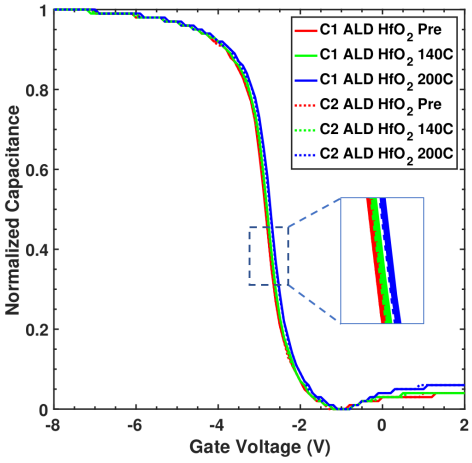
Table 4.1: Summary of shift in characteristics of unsintered MOSCAPs with hotplate bake.

Capping	Device	ΔV_{FB} Pre-140 (V)	ΔV_{FB} 140-200 (V)	ΔV_{FB} Pre-200 (V)
No capping	1	0.23	0.13	0.36
	2	0.32	-0.01	0.32
ALD Hafnia	1	0.04	0.08	0.12
	2	0.02	0.08	0.10
ALD Alumina	1	-0.01	0	-0.01
	2	-0.08	0.02	-0.06

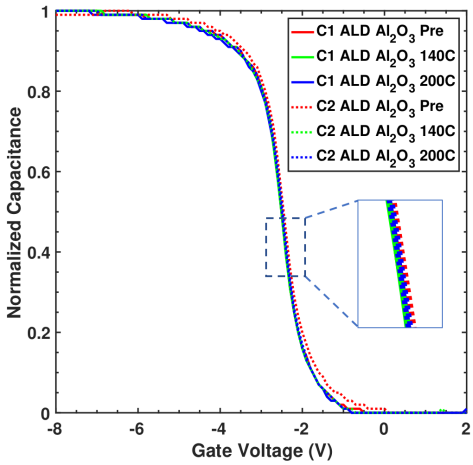
It was seen that there was a relatively small shift in characteristics without a capping layer (see fig. 4.8a). With an ALD hafnia capping, the shift is even more slight and ALD alumina shows almost zero shift after a 200°C hotplate bake. The



(a) Without capping layer



(b) With ALD Hafnia capping



(c) With ALD Alumina capping

Figure 4.8: Influence of a 1 hr hotplate bake on unsintered capacitors w/ and w/o ALD capping layer

replicates are well behaved, indicating a real difference. Fig. 4.8c depicts the influence on hotplate bake on capacitors with an ALD alumina capping layer.

Table 4.1 provides a summary of the flat-band voltage shifts with 140°C and 200°C anneals for capacitors with and without ALD capping layer. The flat-band voltages for the capacitors are extracted by the parametric analyzer based as shown in table.

Results suggest that there is some passivation of interface traps with hydrogen during the hotplate treatments on samples without ALD. Based on the change in flat-band voltages with respect to hotplate bakes, it can be inferred that ALD alumina can

be a very effective capping layer to prevent diffusion of water through TEOS to the active region of the TFT formed by IGZO. The following chapter would present the thermal stability improvements as seen in TFTs after integration of an ALD capping layer.

4.4 Summary

Detailed discussion of thermal stress results was presented to gain understanding of the mechanism causing the increased conductivity of IGZO. It was believed to be occuring due to migration of water /monatomic hydrogen to the IGZO surface upon a thermal anneal, causing an increase in effective electron concentration. A hypothesis was proposed to explain IGZO TFT results using the sintering mechanism in Si MOSCAPs.

The capacitor results strongly indicated that a similar mechanism which improved capacitor characteristics plagued the performance of IGZO TFTs. Additionally, based on the capacitor results, it was noted that ALD alumina could be a potential solution as a capping layer to suppress migration of water to IGZO. The following chapter would discuss results after process integration of the capping layer in IGZO TFTs.

Chapter 5

Process Modifications to Address Thermal Instability

A study of the possible process modifications and additional capping layers was necessary in order to address the thermal instability issues as outlined in the previous chapter.

5.1 Process Integration of capping layer in TFTs

In order to support the understanding from MOSCAP experiments, ALD Alumina and hafnia were integrated into the TFT structure as capping layers over the TEOS passivation layer. This was done in order to reduce amount of water that the TEOS passivation would otherwise absorb. Section 5.1.1 would describe process details involved in the integration of capping layer, followed by the discussion of results from thermal experiments in Section 5.1.2.

5.1.1 Experimental Details

Two BG and two DG device wafers received 1000 Å of passivation oxide on top of 50 nm of IGZO sputtered at Corning Inc. All four wafers were then annealed at 400°C for 10 hours in a pure oxygen ambient to drive out any water that adsorbed into the oxide previously. Immediately after the anneal, one BG and one DG wafer received 15 nm of ALD HfO_2. The remaining pair of BG/DG wafers did not receive any capping layer. Fig. 5.1 depicts the structures of BG and DG TFTs after the integration of a capping layer.

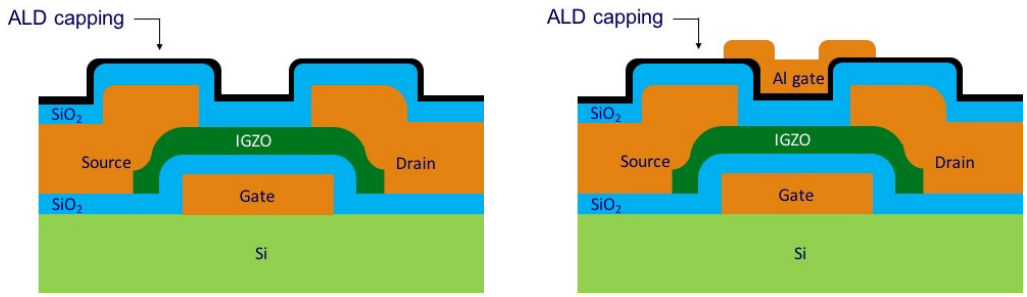


Figure 5.1: Cross-sectional view of (a) bottom-gate and (b) double-gate IGZO TFT structures with a capping layer to improve thermal stability

5.1.2 Results and Discussion

Once the devices were fabricated, two thermal experiments were conducted. For the first experiment, several devices from each wafer were subjected to a hot-plate anneal of 140°C for a total of 120 minutes. For the second experiment, all devices were subjected to a hot-plate anneal for 200°C for a total of 60 minutes. All devices in both experiments were electrically tested before and after the hot-plate treatments.

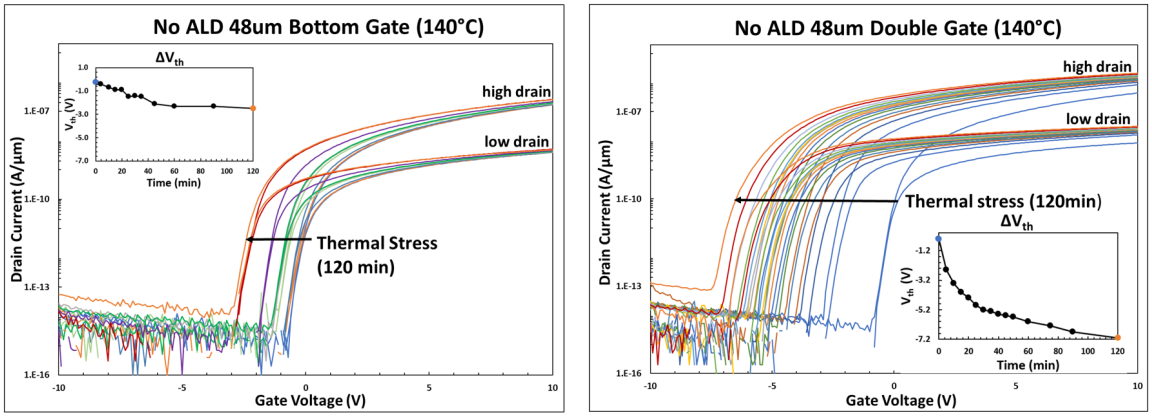


Figure 5.2: (a) BG TFTs without a capping layer have a voltage shift of about 2 V over 120 minutes at 140°C. (b) DG TFTs see an even greater voltage shift of 7 V.

Fig. 5.2 shows the instability when IGZO TFTs without ALD capping layer was subjected to a hot-plate bake. It can be noted that the amount of shift is much greater for the double-gate structure as a result of reaction between water and top gate metal causing increased carriers.

The devices with ALD hafnia showed good stability with a 140°C hot-plate bake

for both BG and DG TFTs. Fig. 5.3 shows an improved thermal stability of BG and DG TFTs at 140°C with an additional ALD hafnia capping layer. Although ALD hafnia showed promise at 140°C, the devices were not stable enough when temperature was increased to 200°C. Fig. 5.4 illustrates the failure of ALD hafnia as a stable capping layer at 200°C.

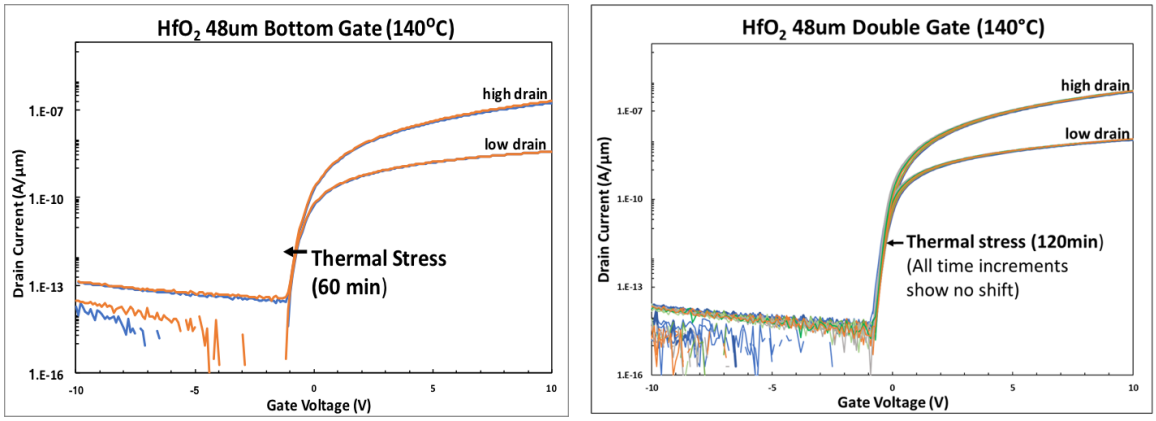


Figure 5.3: (a) BG TFTs with ALD hafnia show excellent thermal stability at 140°C (b) DG TFTs almost see no shift with 2 hours of hot-plate bake at 140°C

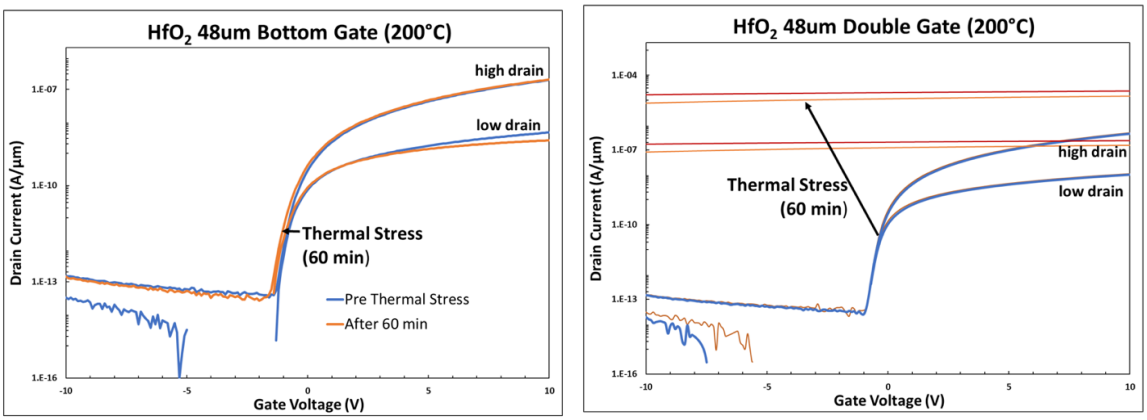


Figure 5.4: (a) BG TFTs with ALD hafnia appear to be very unstable at 200°C(b) DG TFTs break at 200°C

With an ALD alumina capping layer, thermal stability of the IGZO TFTs improves even at 200°C. The TFTs received three cycles of treatments at 140°C for one hour each and two tcycles at 200°C also for an hour each. Fig. 5.5 illustrates the response of 24µm BG and DG devices to the thermal stress treatments. Based on the

results, it can be noted that ALD alumina capping proves to be a good candidate to provide thermal stability for IGZO TFTs.

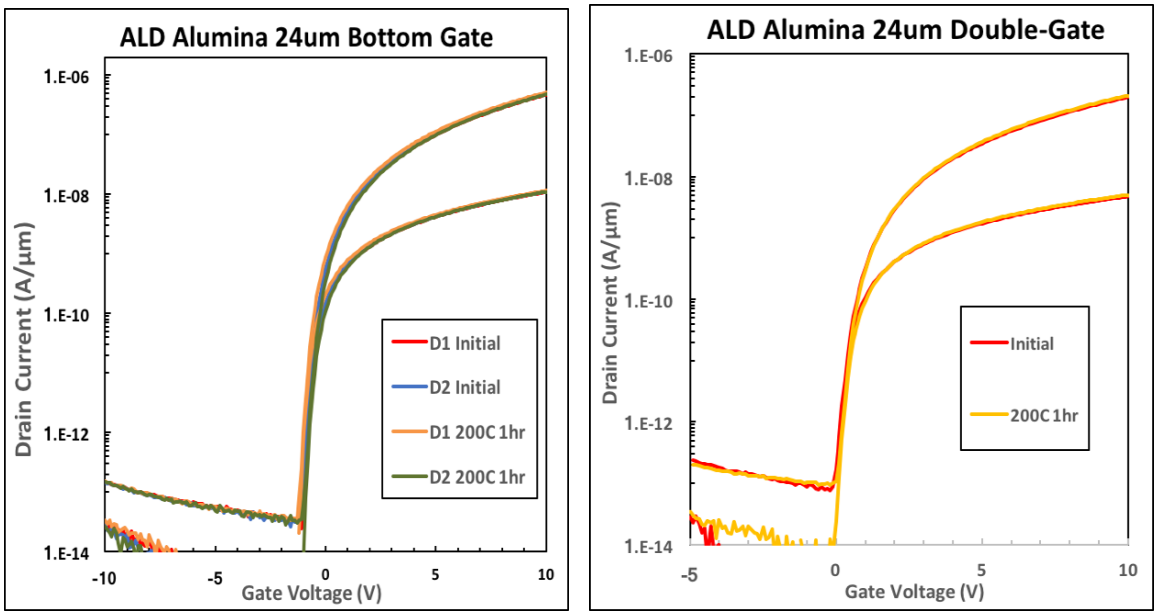


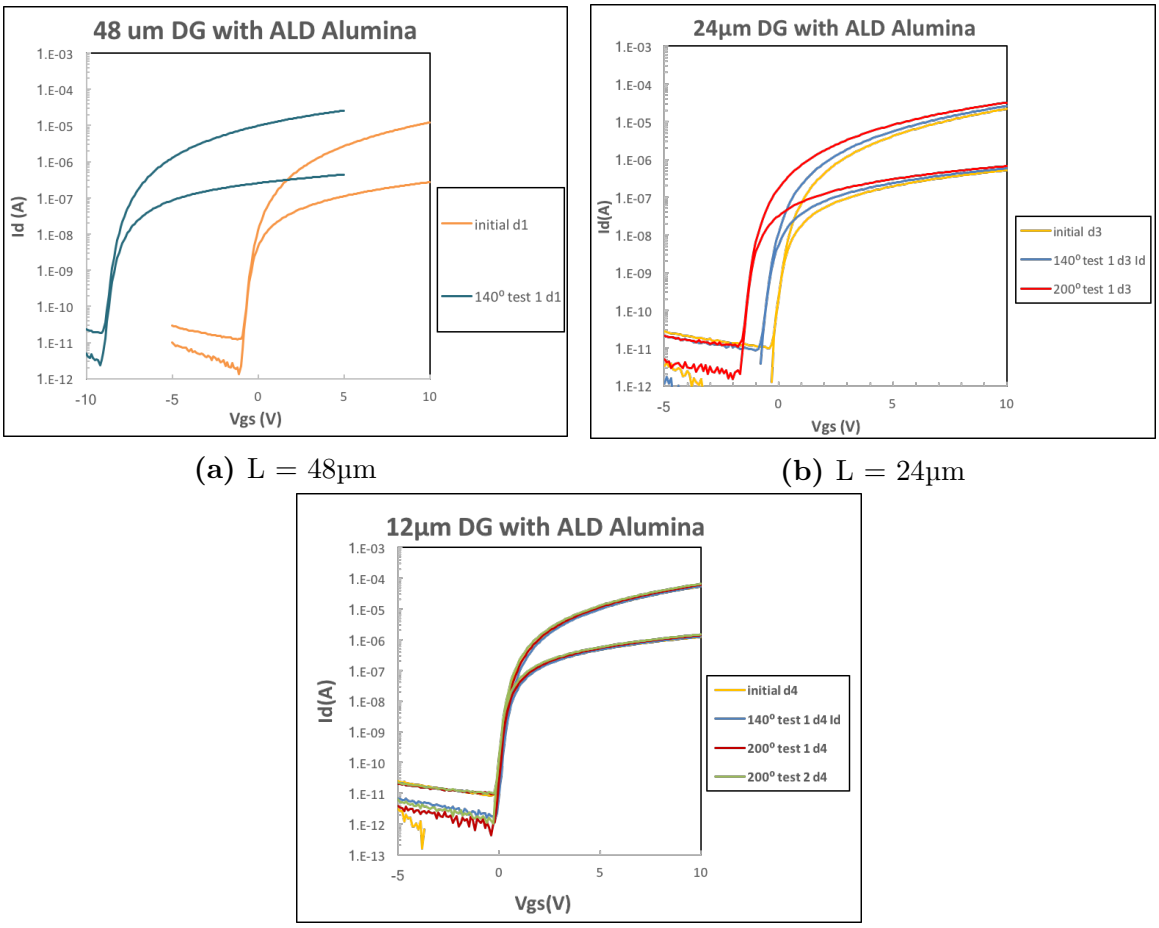
Figure 5.5: (a) BG TFTs with ALD alumina show excellent stability at 200°C (b) DG TFTs with ALD alumina also show excellent stability at 200°C

5.2 Working hypothesis for channel length dependence on thermal stress

Upon performing thermal experiments on multiple devices, it was observed that failure of TFTs due to thermal treatments was statistical, with some devices being able to withstand more thermal cycles than the rest. Additionally, the amount of shift caused due to the thermal stress decreased as channel length reduced. No channel width (and thus area) dependence was observed. Fig. 5.6 shows the channel length dependence observed on DG TFTs with thermal treatments.

The data shows that the suppression is more effective on devices with shorter lengths. There seemed to be a probability for the likelihood of device to fail, with more devices failing the longer their channels were. Fig. 5.6 shows representative results that demonstrate the dependence of thermal stability on channel length. Long

channel IGZO TFTs (L $\geq$ 48µm) with ALD alumina capping layer appear to fail consistently when subjected to thermal hotplate treatments (1-2 hours) at or above 140°C. Some short channel devices (L $\leq$ 24µm) can fail, but in general were able to withstand more thermal cycles at elevated temperature before (if) they fail (see Fig. 5.6c).



(a) L = 48µm

(b) L = 24µm

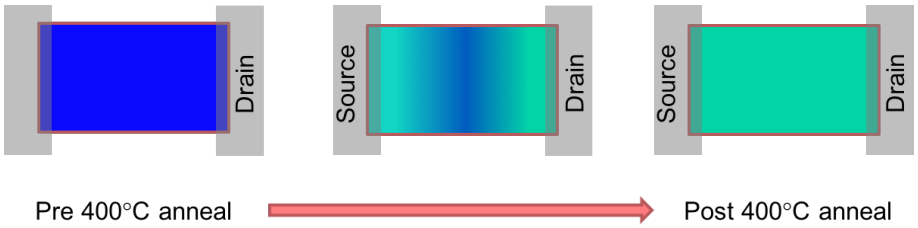
(c) L = 12µm

Figure 5.6: Representative results of channel length dependence in DG TFTs (with ALD alumina capping) on thermal stress

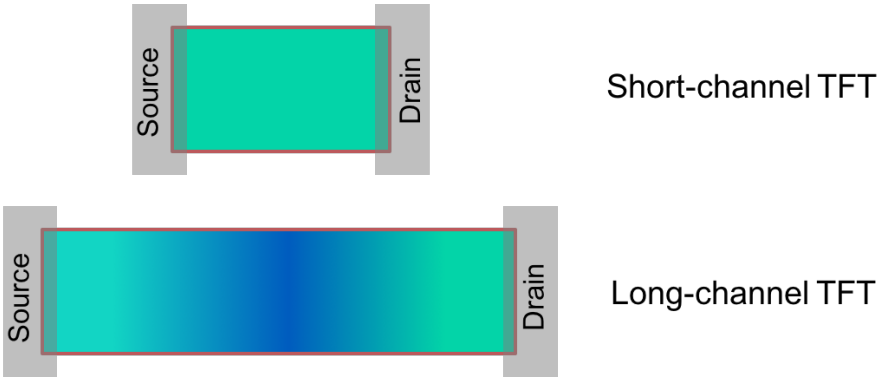
Adding an ALD capping layer following the oxygen anneal reduces the effects of thermal stress put on IGZO TFTs. However, the longer channel length DG devices consistently fail when subjected to thermal stress. Results suggest that water is either directly or indirectly responsible for this degradation process. Both water and hydrogen have been shown to have donor-like behavior in IGZO, thus supporting a

higher level of electron channel charge [10, 27, 29].

The source-drain metal is proposed to act as a getter to water during the 400°C 8hr anneal, thus removing water molecules from within the back-channel passivation oxide nearby these regions. Fig. 5.7a shows a cartoon illustration of the said phenomenon. In shorter channel devices (L $\leq$ 24µm), water segregates to the metal regions and is effectively removed from the system. In longer channel devices, the water molecules level that are not in the immediate vicinity of these regions remains significant, and therefore are not gettered during the 8hr 400°C anneal.



(a) Water segration from channel due to source/drain electrodes acting as a getter



(b) Comparison of water remaining in the system after the passivation anneal - Long vs short-channel TFTs

Figure 5.7: Cartoon illustration of source/drain acting as getter to water in IGZO TFTs

During subsequent thermal stress at 140-200°C, any remaining water molecules can migrate and may be above the gas-phase solubility limit. These molecules may segregate to the back-channel interface. In DG devices, a reaction of water with the top gate metal may liberate monoatomic hydrogen atoms (similar mechanism as the getter process) which may influence the entire back-channel region. Liberation of

hydrogen that may be occuring during the 400°C anneal and during the 200°C ALD process following the anneal does not appear to have a negative impact on device operation.

5.3 Summary

Without ALD capping, both BG and DG TFTs shift degrade with thermal treatments at 140°C and 200°C. Integration of an ALD Alumina capping layer over the TEOS passivation oxide improves thermal stability of IGZO TFTs. The results strongly indicate water having an impact, directly or indirectly, on the degradation process of both BG and DG TFTs. Frequency of device failures due to thermal hotplate treatments are statistical. A working hypothesis to explain the channel length dependence on the thermal response has been detailed.

The 200°C ALD processes may liberate hydrogen for a short time period at the beginning of the deposition because of the surface chemistry involving water. However, this may be short-lived once the thickness is a few nanometers, and thus does not degrade the IGZO TFT operation. This short time is apparently enough time for silicon interface trap passivation.

Chapter 6

Final Remarks

6.1 Summary of Work

The main objective of this work was to develop a mechanism to understand and address the thermal instability seen in IGZO TFTs. It is proposed to be occuring due to a negative impact caused due by water directly or indirectly.

A multi-point hypothesis was developed through the interpretation of thermal degradation behavior in SiO2 passivated IGZO TFTs. Water was hypothesized to be the primarily candidate responsible for thermal instability in BG TFTs. The monatomic hydrogen generated by reaction of additional top gate with water was believed to cause a more pronounced instability in case of DG TFTs. Integration of an additional capping layer was explored in order to suppress the influence of water on IGZO channel. ALD capping layers were seen to improve thermal stability. These capping layers, apart from being good diffusion barriers to water, were also able to suppress liberation of monatomic hydrogen in IGZO TFTs. Based on the results obtained, ALD alumina was established to be a suitable candidate as a capping layer.

Water was believed to be gettered by the source/drain metal contact regions during the oxygen annealing process. It was hypothesized to be a two-dimensional process limited by the diffusivity of water, which results in channel length dependence. Short-channel devices were observed to be superior in thermal stability.

6.2 Future Work

Current process integration strategy with ALD Alumina capping improved thermal stability of IGZO TFTs, but is not sufficient to prevent long-channel device degradation. Alternative S/D metal options are being investigated to improve long-channel stability. Further investigation to integrate sacrificial getter features in actively being studied. This would require S/D layout modification. The study would focus primarily on comparing long and narrow TFTs. Additional investigations would be needed to understand if the metal needs to be in contact with IGZO feature in order to act as an effective getter to water.

Investigation of alternative ALD layers and process schemes to eliminate water more effectively is under research. Integration of alternating layers of different ALD films to form a nano-laminate capping layer could be more effective than ALD alumina alone as it could, arguably, be a much better barrier to water/hydrogen.

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