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# Development of a Self Aligned CMOS Process for Flash Lamp Annealed Polycrystalline Silicon TFTs

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# ABSTRACT

The emerging active matrix liquid crystal display (AMLCD) market requires a high performing semiconductor material to meet rising standards of operation. Currently amorphous silicon (a-Si) dominates the market but it does not have the required carrier mobility for use in next-generation AMLCD manufacturing. Other materials have been developed including crystallizing a-Si into poly-silicon. A new approach to crystallization through the use of flash lamp annealing (FLA) decreases manufacturing time and greatly improves carrier mobility. Previous work on FLA silicon for the use in CMOS transistors revealed significant lateral dopant diffusion into the channel, greatly increasing the minimum channel length required for a working device. This was issue was further magnified by the required gate overlap due to potential misalignment during lithography patterning steps. Through the use of furnace dopant activation instead of FLA dopant activation, and application of a self-aligned gate, the minimum size transistor can be greatly reduced. A new lithographic layout and process flow were developed to accommodate these modifications. Fabrication of the self-aligned devices resulted in oxidation of a molybdenum self-aligned gate; further development is needed to successfully manufacture these devices. However non-self-aligned transistors were made simultaneously with self-aligned devices and used a furnace activation process. These devices showed an increase in sheet resistance, a decrease in electron and hole channel mobility, and a shallow subthreshold slope due to carrier trap states; all attributed to inferior activation and defect annihilation compared to the FLA method. However the minimum transistor size realized was reduced from $L \sim 20\ \mu m$ to $L < 5\ \mu m$. Noted improvements in dopant activation and defect passivation are necessary for high performance self-aligned devices.

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# CHAPTER 1 INTRODUCTION

## 1.1 Displays

Flat panel displays have been in development since 1971 [1]. Large scale manufacturing of the displays began in the 1980s as an alternative to CRTs. Initially they were considered inferior due to poor resolution and other problems but since then technology has improved. CRT displays now represent a miniscule fraction of the display market. Flat panel displays now have a widespread use from cell phones to TVs. Flat panel displays can be made in a variety of different ways. All pictures are based on an array of red, blue, and green pixels with an adjustable brightness to get the desired image. The main display technologies in order to produce the pixel arrays include liquid crystal display (LCD), plasma, and organic light emitting diode (OLED).

Most of the displays in today's market are currently being made with LCD technology [2]. The essential components of a LCD include the backlight, liquid crystal, and switching matrix. The backlight is made from a fluorescent tube or LED and provides the light for the pixels. The liquid crystal controls the amount of light that passes through each pixel. When a voltage is applied to the liquid crystal it blocks the light turning the pixel off. The voltage can be varied to allow for grayscale control over the pixel. Finally a RGB color filter is used. A diagram showing the various components can be seen in Figure 1. The switching matrix can be passive or active. The passive matrix uses a series of row and column electrodes to turn the liquid crystal on or off. The main disadvantage of this switching matrix is its slow response and it can result in smearing of

the image. Active matrix displays use thin film transistors (TFT) to control each pixel. This dramatically increases the response time of each pixel.

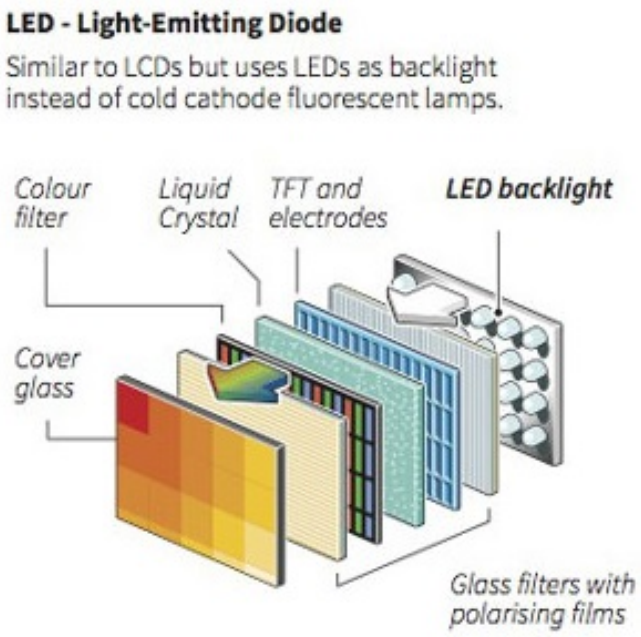


Figure 1: LCD component layout. [3]

Plasma displays are an alternative to LCDs but represent a small part of the market. They operate using a series of gas filled capacitors. When a voltage is applied to the capacitor plasma is struck emitting UV light. This light is absorbed by a phosphor and re-emitted as red, blue, or green light. The components of a plasma displays are shown in Figure 2. The pulse widths of the voltage applied to the capacitor are controlled to determine the brightness of each pixel. In order for fast enough switching to occur with each pixel the plasma is kept on at a low voltage. This limits the possible contrast of the display. Each pixel is controlled through electrodes similar to the passive matrix for LCDs.

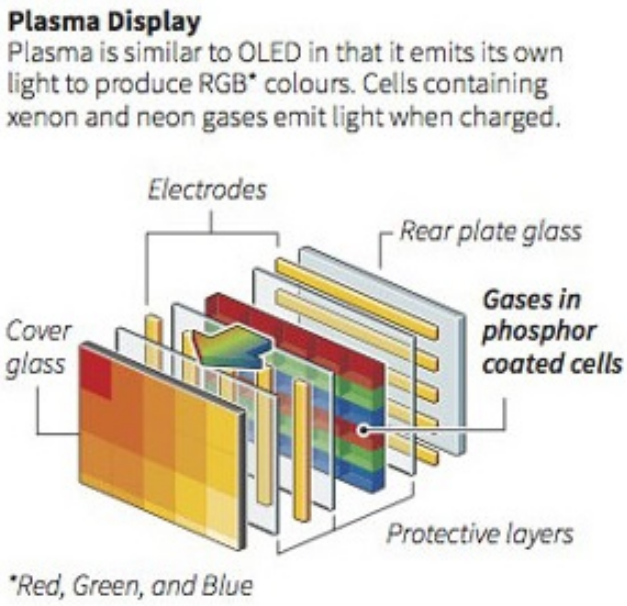


Figure 2: Plasma display layout. [3]

OLED are an emerging display technology. Each pixel is made with an organic semiconductor that emits light when a current is passed through it. The semiconductor stack includes an electron transport, emitter, and a hole injection layer. The layout of the OLED display is shown in Figure 3. Each of the pixels can be addressed through either a passive or active matrix similar to LCDs in order to provide the current necessary for light emission.

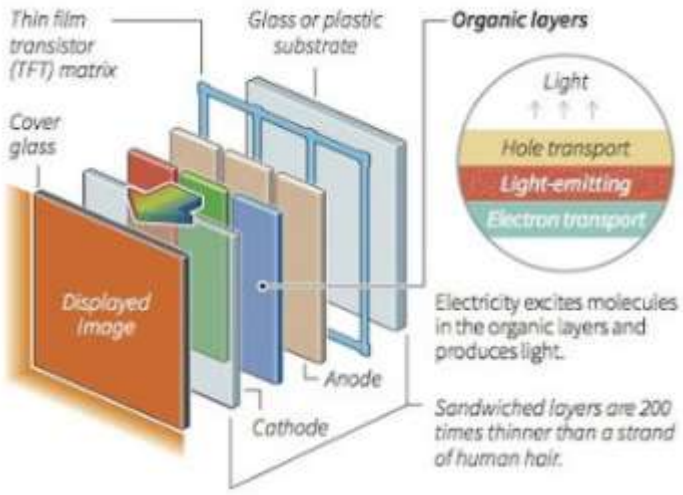


Figure 3: OLED component layout. [3]

## 1.2 Thin Film Transistor

The active matrix arrays mentioned in the previous section rely on TFTs in order to have such fast responses to changing pictures. TFTs have been in development since 1968 [1]. They were initially investigated as an alternative to bipolar junction transistors alongside metal oxide semiconductor transistors. Development of the TFT went into a recession until flat panel displays found a use for them. They were used for their low leakage current and transparency. Most of the TFTs are used in front of the light source in the active matrix displays. TFTs are defined as semiconductors on an insulating substrate. The thin film refers to the semiconducting film that is grown on the insulating substrate that has a thickness much less than its lateral dimensions. In displays this is an amorphous or polycrystalline film that is deposited on a glass substrate.

## 1.3 Semiconducting Materials

The semiconducting layer can be made with a variety of materials. One of the most important properties of the semiconductor is its ability to be deposited with plasma enhanced chemical vapor deposition (PECVD) at low temperatures around 400 °C. If the temperature is too high this can cause dimensional change in the glass or even melt it. One of the materials that can be deposited at low temperatures is amorphous silicon (a-Si) and is the most widely used semiconductor for TFTs as seen in Figure 4 [1]. Its biggest advantages include the high degree of uniformity across large substrates [4]. This is important for the construction of large TV screens. It is also inexpensive compared to other materials. The disadvantage to using a-Si is the low mobility. The mobility typically ranges between 0.5 and 1 $cm^2/(Vs)$ because of the dangling bonds inherent in amorphous materials. The bonds can be terminated with hydrogen increasing the mobility of the material [4]. The a-Si is typically deposited by PECVD because of its uniformity and low temperature required for deposition.


Figure 4: Percentage of material use on the display market. [2]

Other amorphous semiconductors have been investigated. The amorphous nature of these semiconductors allows the material to be deposited at low temperatures using a process such as sputtering. These materials however tend to have lower mobilities than poly-crystalline materials. The material that has shown the best electrical characteristics for use in displays is Indium Gallium Zinc Oxide (IGZO) This material has a high mobility of ~10 $cm^2/(Vs)$ and a high on/off ratio of ~$10^6$ [5] that is significantly higher than what can be achieved with a-Si.

## 1.4 Low Temperature Poly-Silicon

One of the ways to increase the mobility of the a-Si is to crystallize it. The improvement comes from the shift in defects. The a-Si was limited by dangling bonds and poly-crystalline silicon (poly-Si) is limited by crystal defects and grain boundaries. A much higher mobility of ~100 $cm^2/(Vs)$ is possible with poly-Si [6,7,8]. This vastly improved performance allows for much faster switching, pixel density, and drive current. The uniformity of poly-Si is worse than a-Si. In the short range crystal boundaries are random and change electrical performance. In the long range the uniformity of the crystallization comes into effect. For example the edges may have smaller crystals or even be only partially crystallized.

Just like the amorphous deposition the crystallization has to remain below the strain point of the glass. This prevents single crystal epitaxy from being used because it is grown at higher temperatures. There is a method of getting crystalline silicon (c-Si) on glass [9]. A crystalline silicon substrate is bonded to the glass substrate. Then through chemical mechanical planarization the silicon is thinned to within a micron in thickness.

This process is costly and the limitation in substrate size prevents this process from being manufacturable at large scale.

One of the methods to achieve low temperature crystallization is furnace solid phase crystallization (SPC). Substrates with a-Si are exposed to temperatures ranging from 500-600 °C for multiple hours. Crystal sizes are typically around 10 nm in size and the mobility can get up to 20 $cm^2/(Vs)$ with an anneal in water vapor [6]. This process has an improved mobility over IGZO and a-Si. The anneal times can reach up to 100 hours severely decreasing throughput. The anneal times can be reduced but at a cost of the crystal size.

In order to get large crystal sizes the silicon needs to be melted. The method commonly used is through excimer laser annealing (ELA). The silicon absorbs the radiation from the laser while the glass is transparent. This prevents the glass from heating during the crystallization process. Any heat transferred to the surface of the glass is negligible when considering any damage to the glass due to the vast difference in thicknesses. The absorption of the radiation by the silicon is enough for it to melt and then crystallize into grain sizes of 100 nm or more [7,8]. The mobility of this poly-Si can then reach up to 100 $cm^2/(Vs)$ [7,8]. Due to the spot size of the excimer laser the substrate has to be scanned creating a lengthy process that restricts the maximum display size due to throughput restrictions.

Another process that crystallizes the silicon is joule heating [10]. This process can heat the entire silicon film at once. A series of molybdenum electrodes either above or below the film heat the silicon to a-Si melting temperatures. The grain sizes resulted from this were up to 100 nm in size similar to ELA.

The method focused on in this thesis is flash lamp annealing (FLA). This method operates similarly to ELA. The light radiation comes from a pair of xenon arc lamps. The FLA setup can be seen in Figure 5. The light radiated from the lamps is not in the wavelength range that is absorbed by the glass but is absorbed by the silicon. The primary difference between FLA and ELA is the exposure area. While ELA is limited to the laser spot size the xenon bulbs can be scaled to sizes that cover the entire substrate area. This allows the crystallization to occur in the time of a single pulse that lasts less than a second. This also removes the limit of the area in which the crystallization can occur during exposure. Because of this crystal sizes of 1 μm or greater have been found [11].

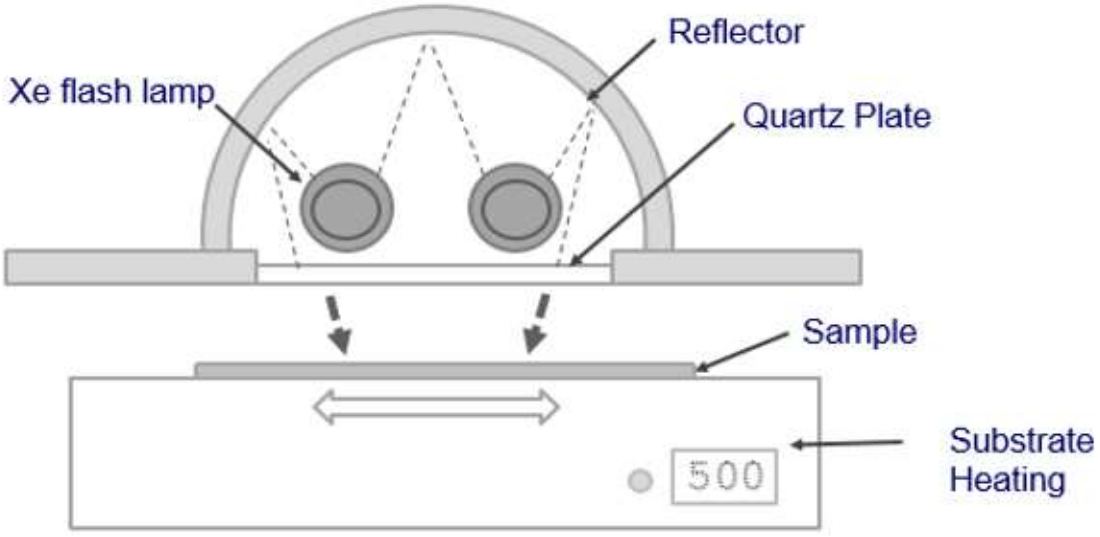


Figure 5: FLA tool layout. [11]

# Chapter 2 Sample Construction

## 2.1 Sample Preparation

To create a sample for exposure with FLA it starts with corning glass wafers. Typically the Eagle or Lotus formulation of glass is used for its high strain point. The substrates are cut into 6" wafers for easy handling in manufacturing tools. The glass substrates simulate the display backplane used in the display industry. The high strain point of Lotus glass allows for extended anneals at 630 °C without any dimensional change with the glass. A PECVD oxide barrier layer is deposited on the glass. This barrier layer prevents diffusion of any glass materials into the semiconductor. Without it boron can diffuse into the silicon causing it to become degenerately doped. Then the a-Si is deposited by PECVD using $SiH_4$ and $H_2$ at 400 °C, 1 Torr pressure with RF power at 100 mW/cm$^2$ [12]. During deposition hydrogen is incorporated into the film. Because of this a dehydrogenation anneal is needed in order to remove hydrogen from the film. If left in the film during the FLA process the hydrogen during the melt will collect and form bubbles that can ablate the film. The a-Si is then patterned and etched using $SF_6$ to form mesa structures. These mesa structures serve to control the crystal direction and reduce the exposure required to crystallize. The edges formed with the structure absorb more light because the light is not collimated. Another transparent dielectric is then deposited on top of the silicon. This serves as an anti-reflective coating and thermal barrier [11,13]. This further reduces the amount of exposure needed to melt the silicon.

## 2.2 Flash Lamp Annealing Exposure

Once the sample has been made it can then be exposed. During the exposure the sample is heated at around 500 °C. While this temperature is hot enough to cause SPC the sample is not heated long enough to begin nucleation [14]. The sample is typically heated for only a few minutes at most. The heating slows the cooling of the film during exposure allowing the crystallization to occur over a longer period of time. By having the substrate at a temperature closer to that of the film during exposure the thermal stress on the sample is reduced. A high enough difference in temperature can cause enough thermal stress on the film to cause it to ablate. This can also occur if the film is cooled to quickly after exposure. The substrate heating also provides additional thermal energy to the film further reducing the exposure required for crystallization.

To heat the substrate an enclosed hot plate is used as pictured in Figure 6. The enclosure prevents any outside air from entering the area with the sample preventing contamination. Any particles on the surface of the capping layer can block light preventing or slowing crystal growth in localized sites. This can cause crystal growth to happen in unwanted directions. The enclosed hotplate also provides a more uniform thermal gradient. With an open hotplate system the top of the sample is left at atmosphere. The large thermal gradient across the sample creates a large amount of tensile stress on the sample. A glass substrate can cup or break due to the stress.

Figure 6: Enclosed hotplate used in FLA exposure.

Various parameters of the exposure can be adjusted to change the amount of power delivered to the sample. The parameters involved include the exposure time, voltage applied to the bulbs, distance from the bulbs, and substrate temperature. Exposure times are kept around 200 μs to give a consistent crystallization time. With this exposure time the Nova Centrix Pulse Forge used for this experiment could deliver ~40 kW/cm$^2$. The voltage applied to the bulbs is often changed to keep the energy of exposure constant. A bolometer is used to measure the amount of power delivered per area. The desired energy of exposure is 5 J/cm$^2$. The voltage is then adjusted to give a consistent energy. The distance from the bulbs can have a dramatic effect on the exposure because the light is not collimated due to the reflector on the exposure tool used. A parabolic reflector has been investigated but is not used in this experiment [15]. The sample is always kept at a particular distance from the bulbs.

The wavelengths of light emitted by the bulbs are only absorbed by the silicon. The output spectra of the xenon lamps can be seen in Figure 7. The shortest wavelength emitted from the bulbs is around 300 nm, which is well above the wavelength at which absorption occurs by the glass. Silicon however absorbs at 700 nm or less so it will absorb the light emitted by the tool. The n and k values of the various materials can be seen in Figure 8. Since the glass and silicon oxide do not absorb at these wavelengths they will only be heated at the interface with the silicon. The bulk of the glass substrate remains cool preventing dimensional change.

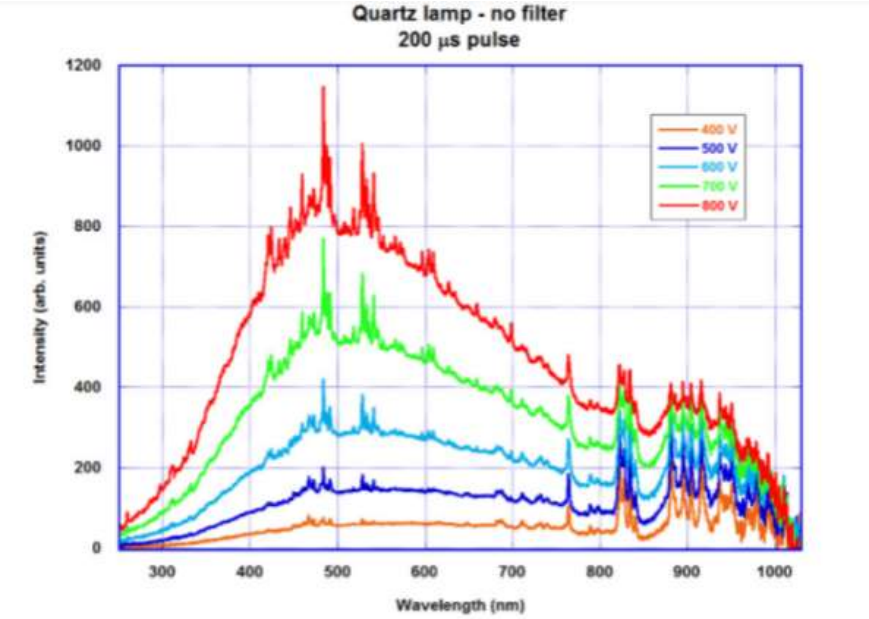


Figure 7: FLA lamp emission spectra.

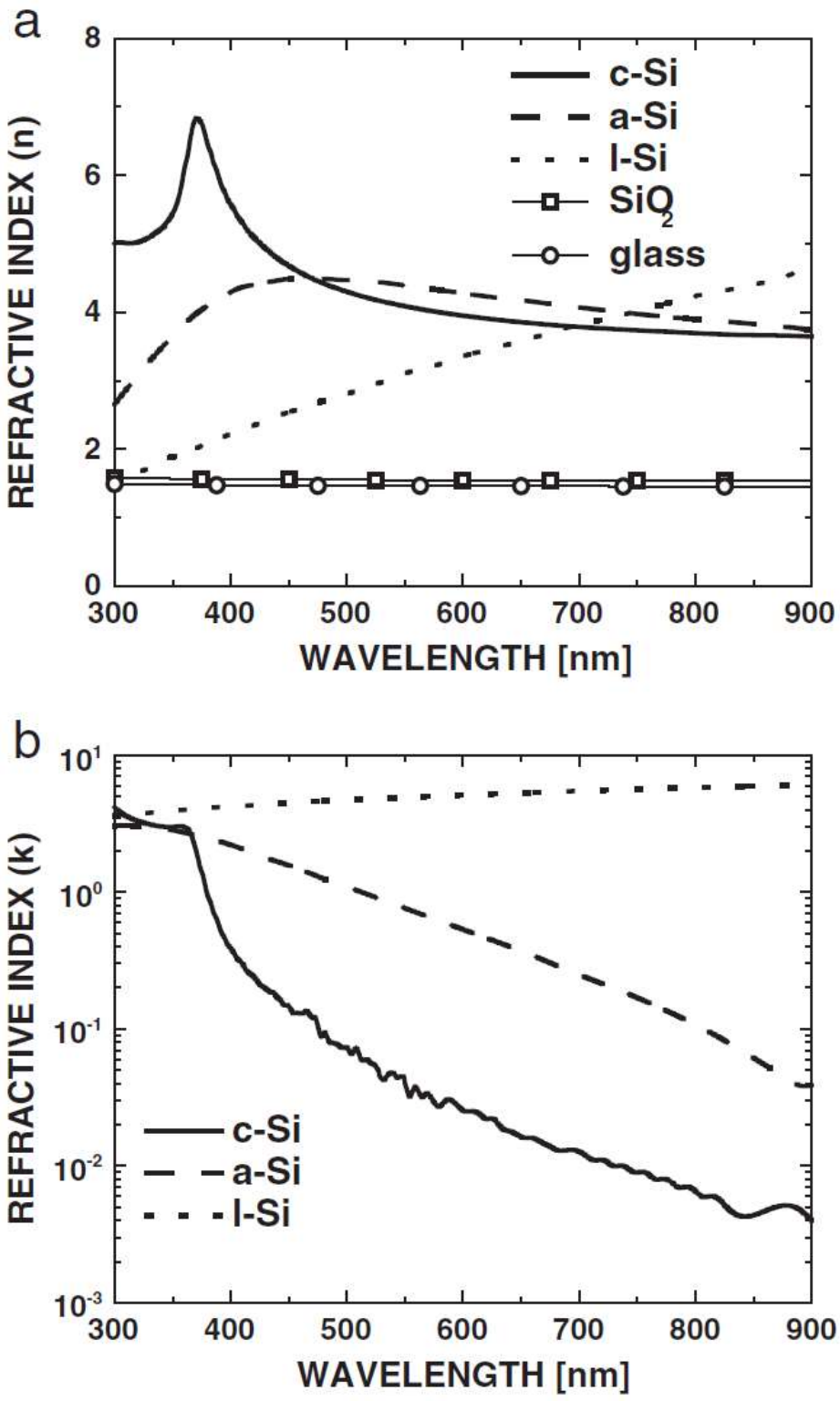


Figure 8: Real and imaginary refractive indices for materials used in FLA. [15]

# Chapter 3 Silicon Crystallization

After absorbing the light radiation the silicon heats beyond furnace annealing temperatures. At these temperatures the silicon can crystallize during the flash pulse. With an amorphous layer the silicon can crystallize in one of two ways, either SPC or liquid phase crystallization (LPC). During SPC the silicon does not heat enough to melt and the film remains a solid throughout the process. With LPC the film melts into a liquid then crystallizes.

## 3.1 Solid Phase Crystallization

For SPC to occur the film needs to remain below the melting point of amorphous silicon at 1145 °C so the film remains solid [14]. The silicon atoms have enough energy to form bonds and rearrange into a crystalline structure. Crystals grown in this manner are limited to 10 nm in size and have a random crystal orientation [16-19]. This limitation on crystal size limits performance of this growth method. The film also remains flat with no surface topography caused by crystallization. In order for SPC crystallization to happen an existing seed crystal structure needs to exist. This is provided during the PECVD process where small c-Si structures will form at the substrate interface [14]. This growth can often be seen at lower exposures or at the edges of the sample where the film did not receive enough energy to melt. This growth is not desired for FLA samples because of its limited mobility.

## 3.2 Liquid Phase Crystallization

As opposed to SPC where the silicon crystallizes as a solid, during LPC the silicon atoms form a solid crystal from the melted material. The silicon atoms will crystallize under two different temperature conditions, super cooled and thermal equilibrium. Super cooling of the silicon happens when the film is heated to a point above the melting point of a-Si and below the melting point of c-Si at 1414 °C [19]. After the amorphous silicon melts the atoms will then want to form c-Si due to the lower Gibbs free energy of the material. Thus the silicon is super cooled at this temperature.

The speed of crystallization is limited first by nucleation, and then by how fast the atoms form the crystal. Nucleation of the crystal is dominated by heterogeneous nucleation at the interfaces of the silicon film and silicon oxide layers. Homogeneous nucleation in the bulk of the film is insignificant [14]. The heterogeneous nucleation occurs first at the edges of the mesa. From the nucleation point the crystal will grow in all directions. The growth stops when it encounters the edge of the film or another crystal growth front. When two of the growth fronts meet the crystal forms protrusions from the surface [20-22]. Due to this form of growth horizontal columnar structures will form starting from the edges of the mesa moving towards the center. The columnar growth can be seen in Figure 9. Often this will result in the protrusions forming an envelope pattern on a rectangular mesa. With increased exposure energy nucleation will begin to occur randomly in the film. This can also be seen with samples that are not patterned. Due to the increased amount of energy in the film the silicon nucleation can occur randomly in the film before growth from the edges reaches the center of the film. This growth results in 100 nm or larger grain sizes [18]. The crystals are asymmetric in shape with the length

being in the direction of growth [19]. A comparison of asymmetric LPC and SPC growth in a thick film can be seen in Figure 10. Fine SPC grains are seen in (c) and large asymmetric grains in (d) that are consistent with the grains found in Figure 9. The crystals will grow with orientation dependence. Silicon grows in the <100> and <110> directions much faster than the <111> direction. Thus the crystal surface will often be {111} [8]. A KOH etch was used to help determine the orientation of the crystal grains because it etch along the {111}. The etch results can be seen in Figure 10. Most of the grains remained intact after the etch showing the grain surface had a {111} orientation.


Figure 9: Columnar structure can be seen growing from the edges inward resulting in an envelope shape.

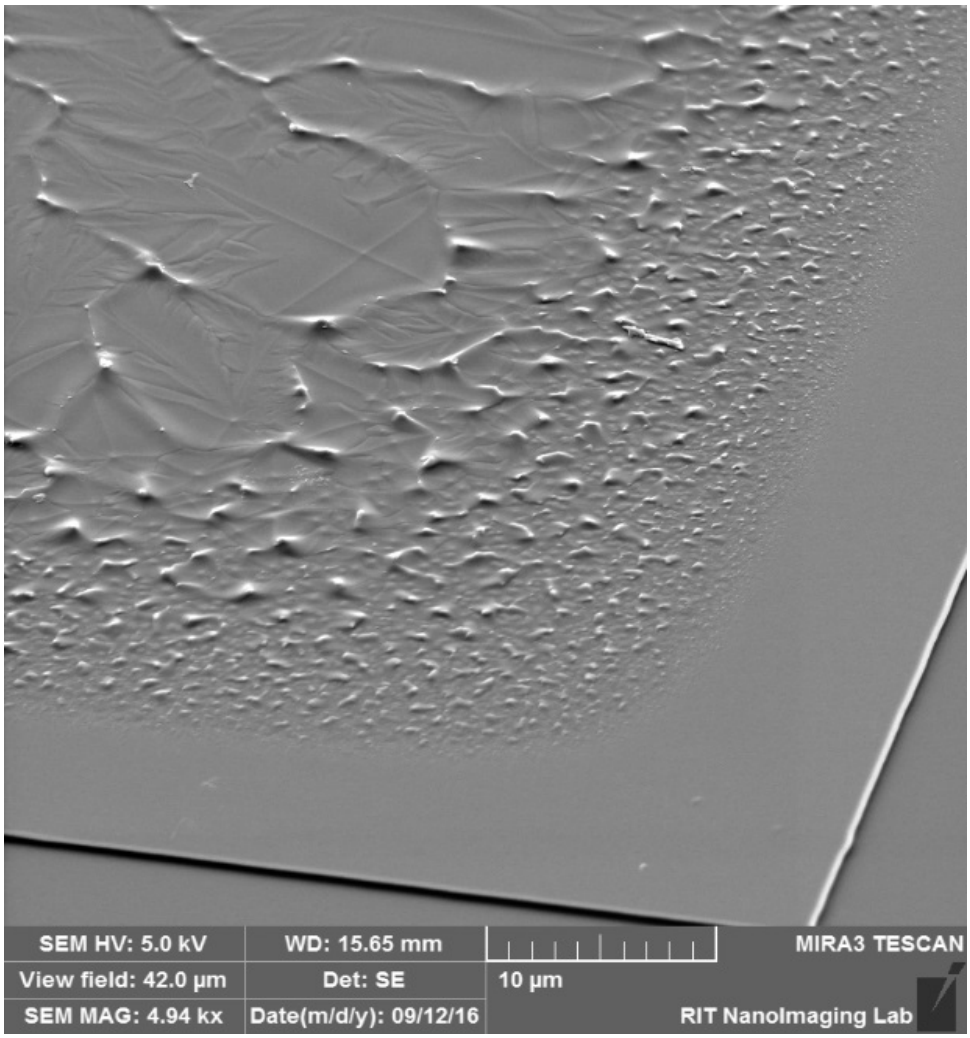


Figure 10: SEM of mesa structure such as the one in Figure 9 after a KOH etch

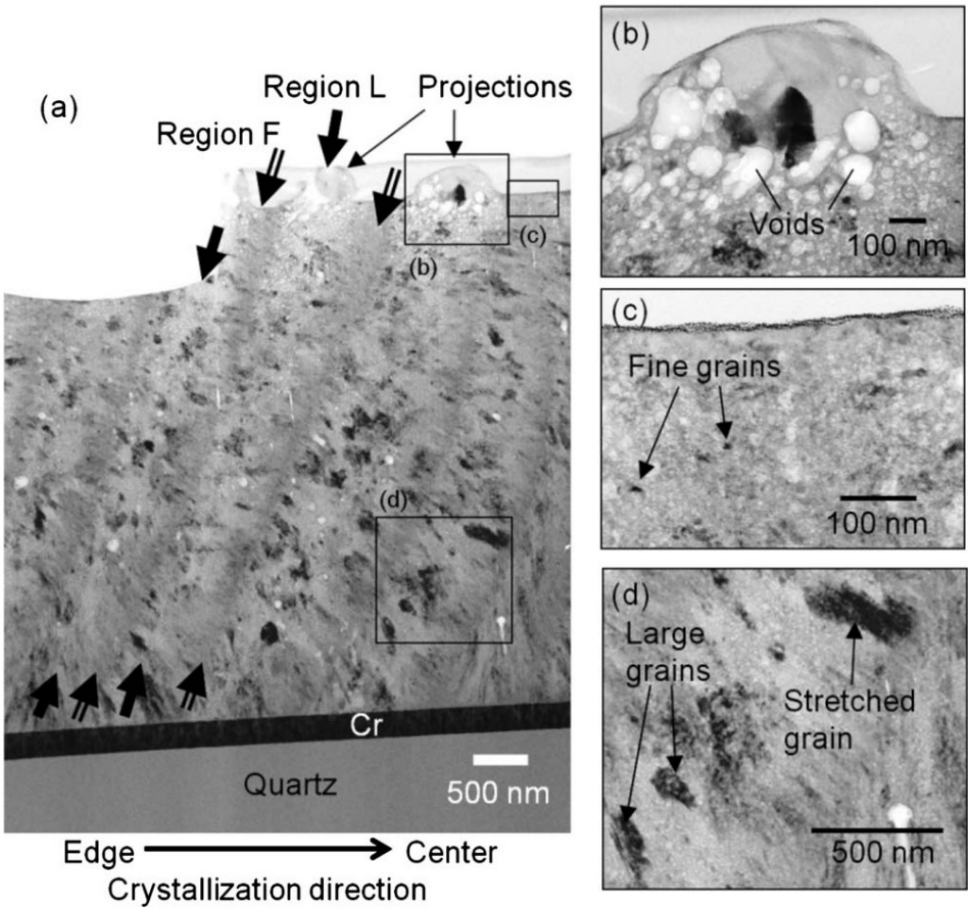


Figure 10: Cross-sectional TEM image of the poly-Si film formed by FLA. There exist 1 μm pitch projections on the surface. One can also observe region L containing large stretched grains and region F consisting of 100 nm sized fine grains, which are indicated using single- and double-line arrows, respectively. [19]

The speed of crystallization can also be aided with explosive crystallization. As the silicon crystallizes heat is released [15]. The crystallization speed has been found to be faster than what is expected with heat from the exposure alone [16]. The faster crystallization speed is due to the released energy during crystallization. The crystallization velocity was found to be ~15m/s. This was measured by pulsing the film with a specified frequency then measuring the distance between growth fronts. Explosive crystallization in combination with edge nucleation creates a controllable crystal growth.

## 3.3 Electron Backscatter Diffraction

Electron backscatter diffraction (EBSD) analysis is used to determine the size of the crystals grown and their orientation. To perform EBSD analysis samples are loaded into a SEM with an attached module. In the module a phosphor screen or CCD imager is used to capture backscattered electrons from the angled electron beam. The backscattered electrons undergo Bragg diffraction from the silicon crystal. The electrons will form a distinct pattern known as a Kikuchi diffraction pattern. This pattern will change based on the atomic makeup and orientation of the crystal [23]. The pattern formed is then compared to known diffraction patterns. The analysis can be done quickly enough so that the beam can be scanned across the sample. Then a map is constructed of the polycrystalline film showing where the crystals are and their orientation.

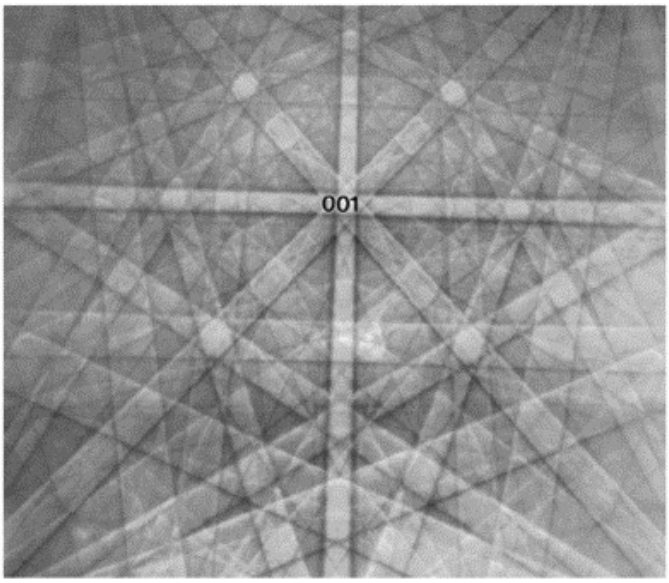


Figure 11: A ZnS crystal showing the Kikuchi diffraction pattern. The [001] zone axis is marked. [24]

LPC growth has been shown previously in FLA samples [11]. EBSD analysis of FLA silicon can be seen in Figure 12. The analysis revealed that grain sizes of 3 μm and greater were grown with FLA as seen in Figure 13. Typically these grains had a top surface orientation of {111} seen in Figure 14. With grains of this size a transistor could be designed to be fabricated on a single crystal. The transistor would be able to operate as if the channel were fully crystalline.

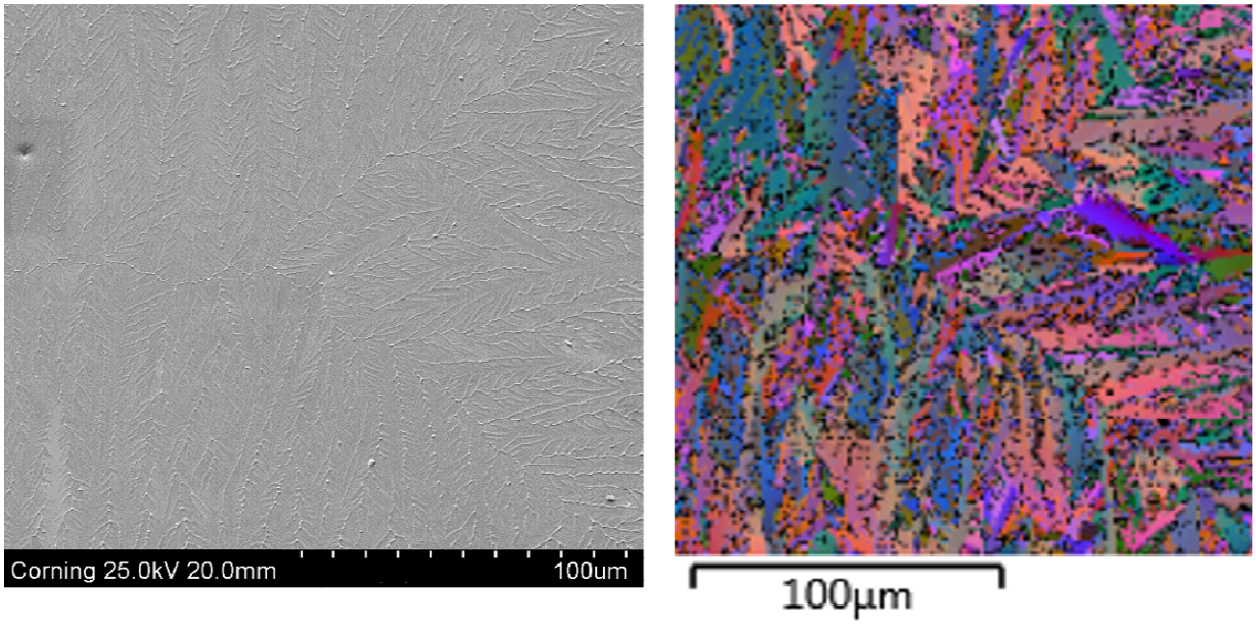


Figure 12: SEM and EBSD of the same area. Each color represents a different crystal orientation. [11]

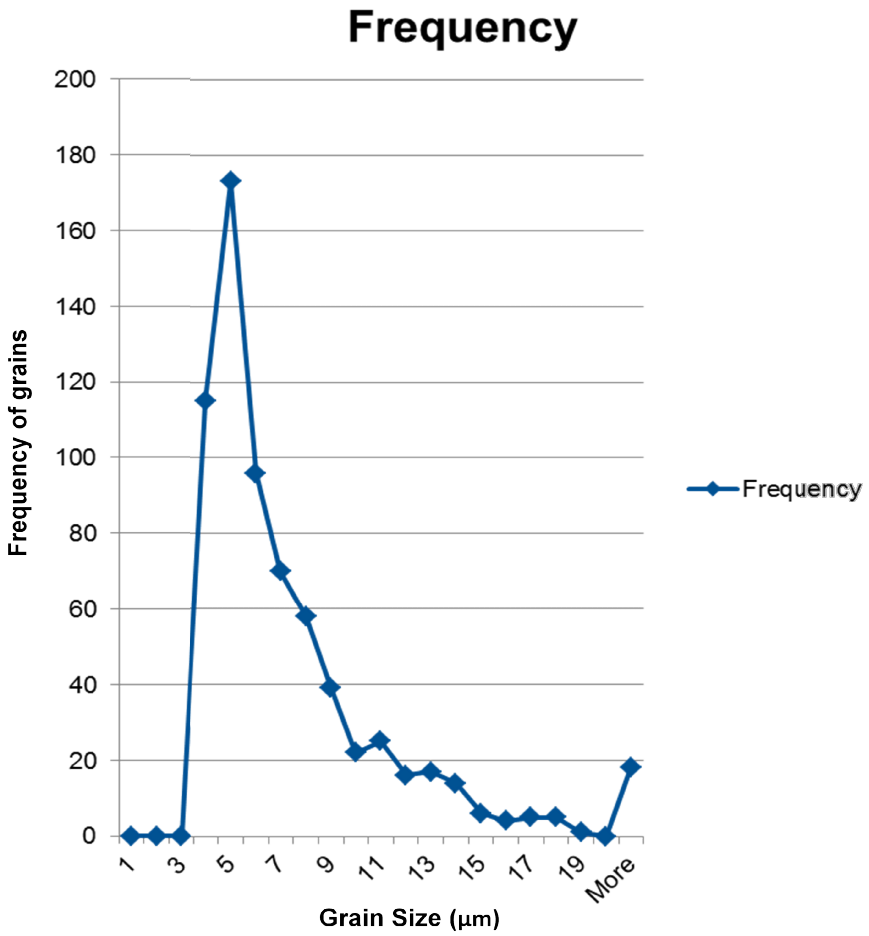


Figure 13: Frequency of each grain size pictured in Figure 12.

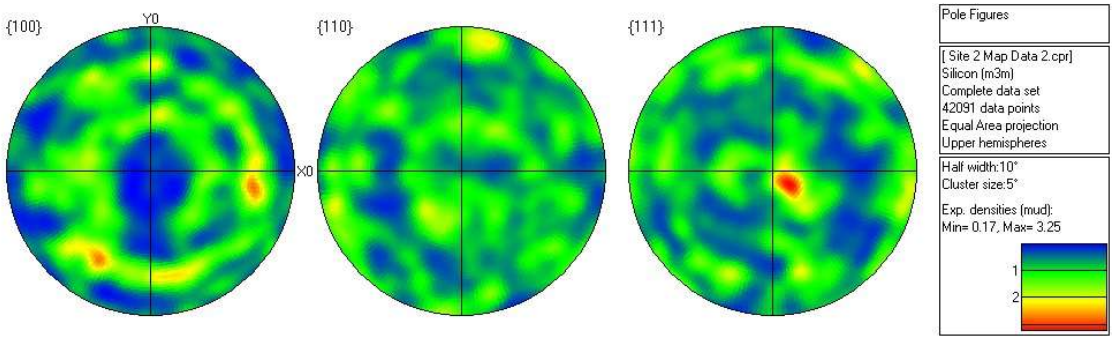


Figure 14: Heat map of grain crystal orientation. Red represents higher frequency.

## 3.4 Thermal Equilibrium

The other method of LPC is thermal equilibrium cooling. With this growth the temperature of the film exceeds the melting point of silicon. The film then must cool below the melting point for crystallization to occur. The rate of crystallization is determined by the film cooling [25].

At higher exposure energies the silicon film has been shown to ball up [21]. This is due to the surface tension at the interface. Due to larger islands having a lower Gibbs free energy small islands will tend to combine into the larger islands known as Ostwald ripening [25]. The balling up of the films and Ostwald ripening has led to different film morphology than that of large crystal growth with LPC. At higher exposures voids begin to form. These voids can be seen in Figure 15. These voids will grow with increasing energy due to Ostwald ripening. Eventually this can lead to breaks in the silicon film. In some devices this will cause a break in the conductive path as can be seen in Figure 16. The ripened material also shows an increase in thickness showing that material migrates away from the voids. In Figure 17 the film was originally 60 nm in thickness and after FLA it has increased to 600 nm as seen in Figure 18 due to the ripening. Recent films that have been made have shown de-wetting instead of the large crystal growth. The ripening has shown to be quicker with doped silicon. The implanted source drain regions of the device ripened faster than the channel region. This can be seen in Figure 18 where the source drain regions are the top and bottom regions with the channel in the center. The degree at which the ripening occurs can be measured. Due to not being able to replicate the large crystal growth the ripened material is what is used for this thesis. EBSD analysis

has shown that crystals do form with this growth. The topography is too rough for accurate EBSD measurement but crystals can be seen in Figure 19.

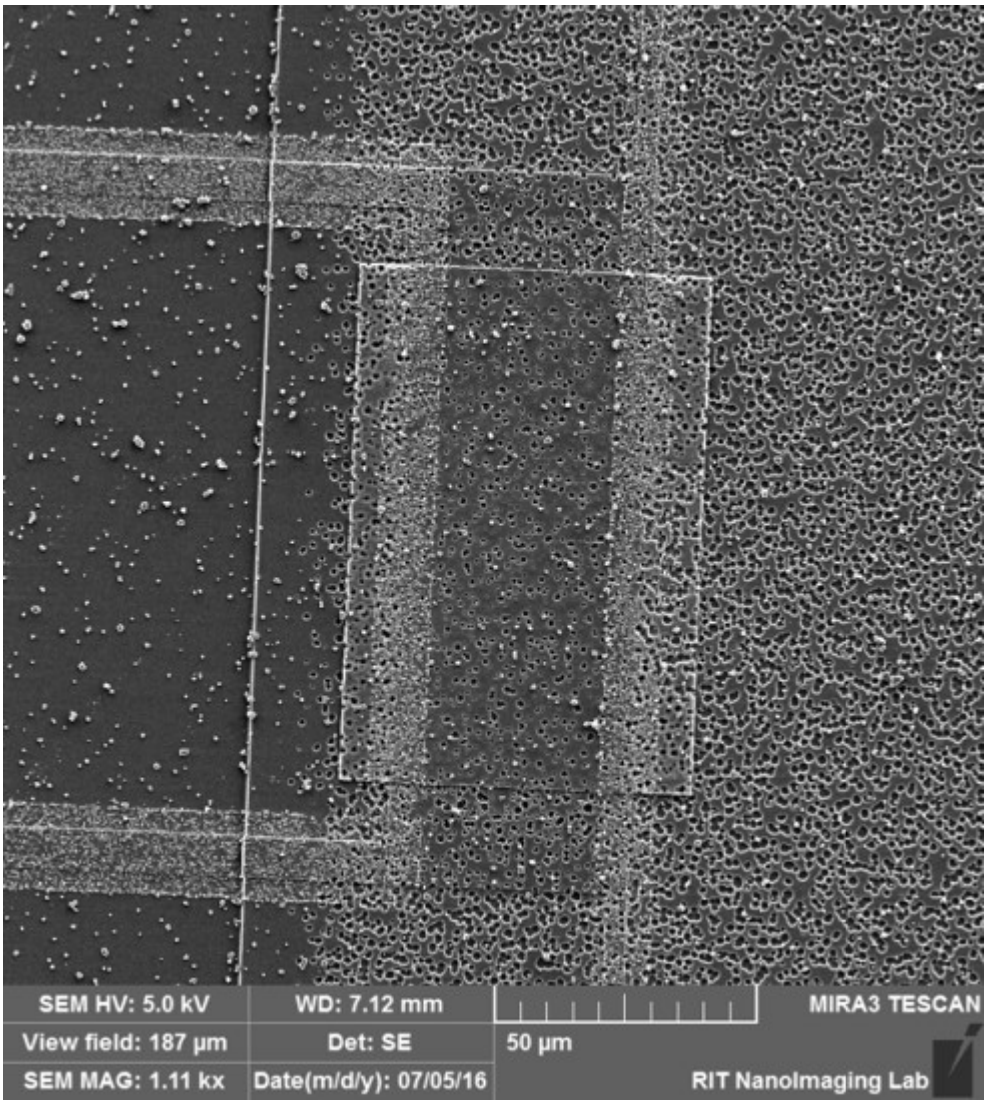


Figure 15: Void formation in the silicon mesa.

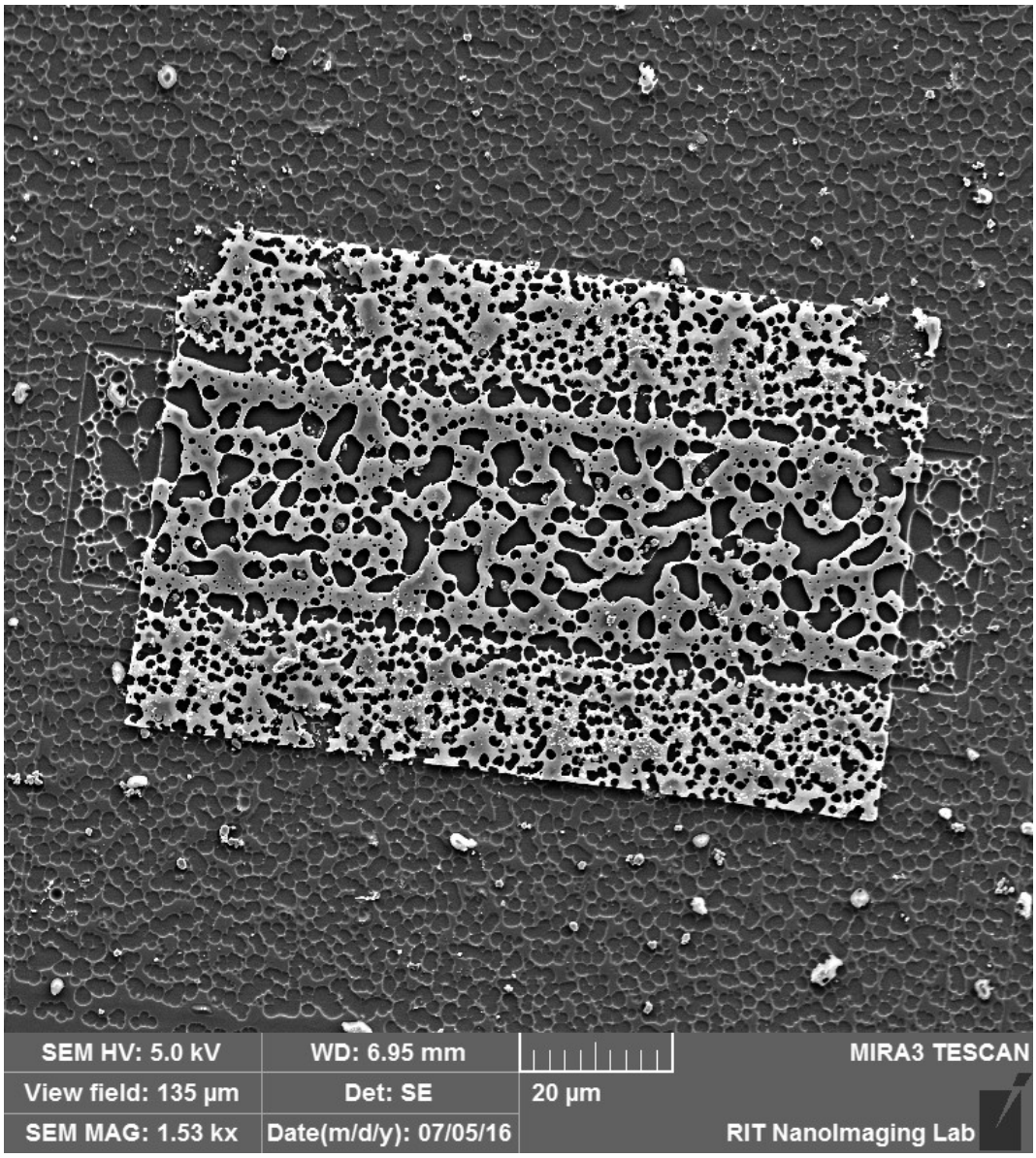


Figure 16: SEM of a dewetted silicon mesa used for a transistor. Breaks in the mesa can be seen between the source and channel regions.

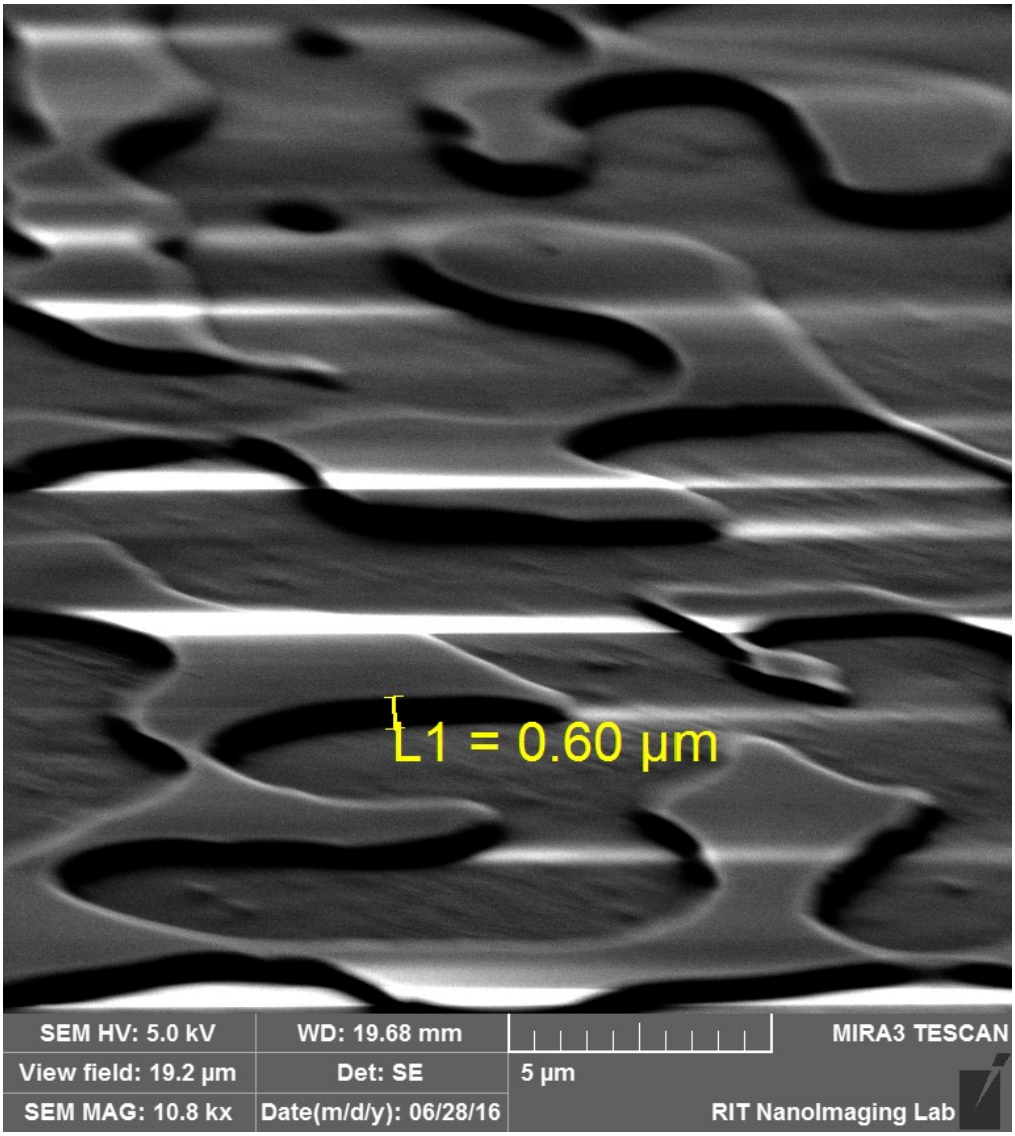


Figure 17: Height measurement of de-wetted film. Sample image taken at 55° angle

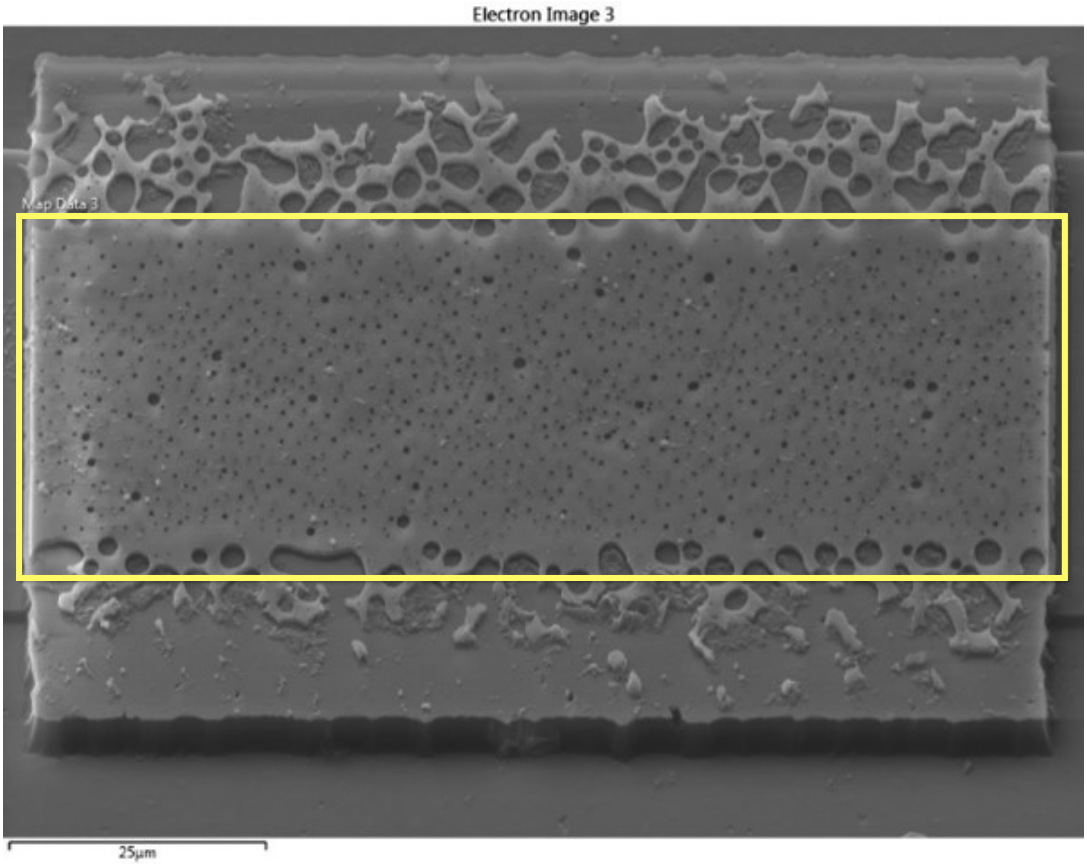


Figure 18: SEM of working device mesa. Box outlines area where EBSD analysis was done.

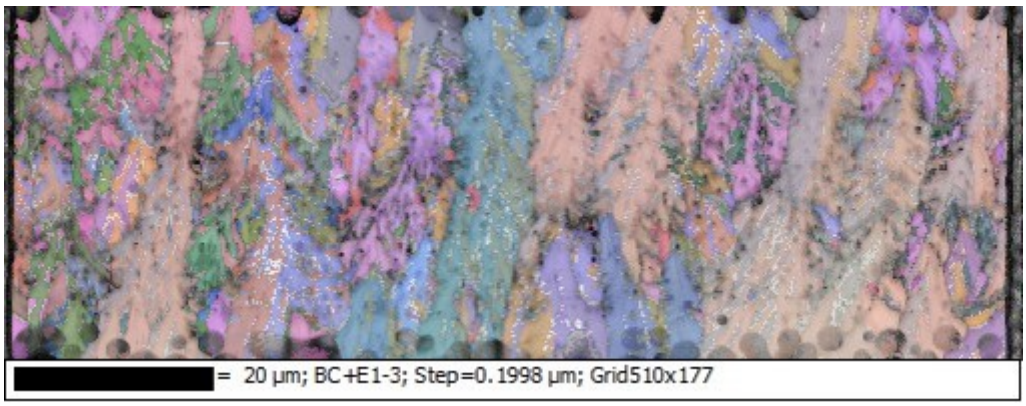


Figure 19: EBSD of area outlined in Figure 16.

# Chapter 4 Previous Work

Without the ability to replicate large grain silicon, devices were made with the de-wetted material. In the past devices were fabricated with the large grain material but there was no barrier layer to prevent diffusion of boron from the glass substrate into the amorphous silicon layer. The transistors made without the substrate barrier layer behaved as resistors due to degenerate doping of the silicon from the boron. For the de-wetted devices both Boron and Phosphorus were implanted for the source and drain regions before the FLA. This way the FLA served as dopant activation. After this the capping oxide was stripped and a gate oxide was deposited. Contacts cuts were made and a single aluminum layer was used for source, drain, and gate.

After the devices were fabricated they were tested. Both the NMOS and PMOS transistors showed good characteristics. The sub threshold slope and mobility were found to be 140 and 118 mV/decade, 380 and 143 $cm^2/(Vs)$ for NMOS and PMOS respectively [11]. The $I_D$-$V_{GS}$ transfer curves can be seen in Figure 20. After testing the devices had aluminum and oxide stripped for imaging under an SEM. This is where the dopant enhanced de-wetting was discovered and breaks between the source drain regions and channel causing an open circuit were discovered. After testing Terada-Muta analysis was performed. Only two transistor lengths were usable for the analysis due to devices with a channel length smaller than 20 μm being unable to work. It was found that the transistors had effective channel length reductions due to lateral dopant diffusion of 6.3 μm and 13.4 μm for NMOS and PMOS, respectively [11]. Microscopic images of the devices confirmed the lateral dopant diffusion. Figure 21 is a microscopic picture of a PMOS

device. A visible change in color can be seen between the doped and un-doped regions. The values for lateral dopant diffusion do not perfectly correspond with the diffusion distance. This dramatic reduction in channel length is likely due to diffusion during the FLA process. The minimum transistor size is further challenged by a 4 µm designed gate overlap of the implanted source/drain regions to allow for potential image misalignment on the projection stepper used for patterning the implant and aluminum layers.

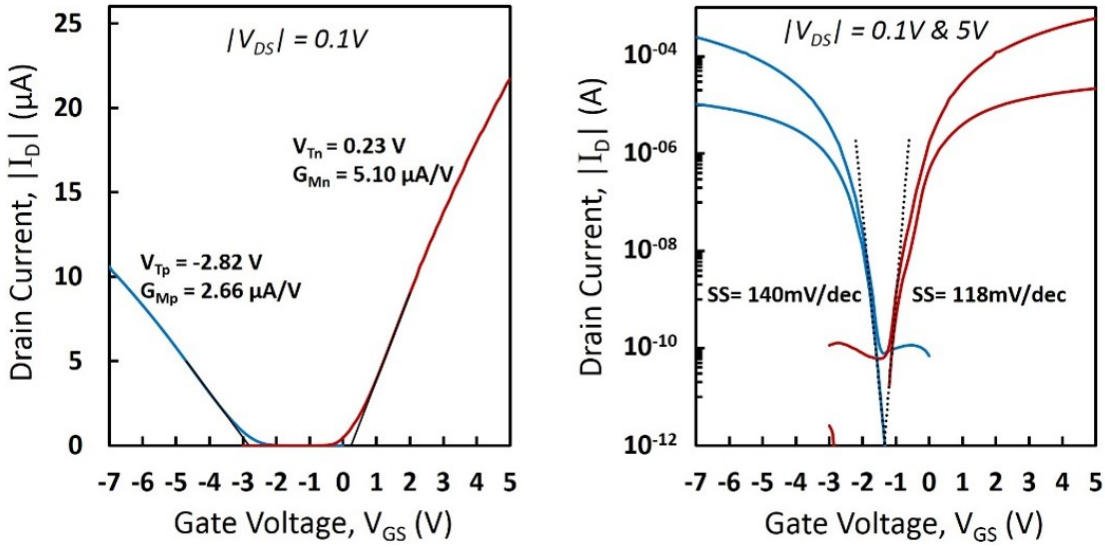


Figure 20: $I_D$-$V_{GS}$ transfer curves of the best devices. [11]

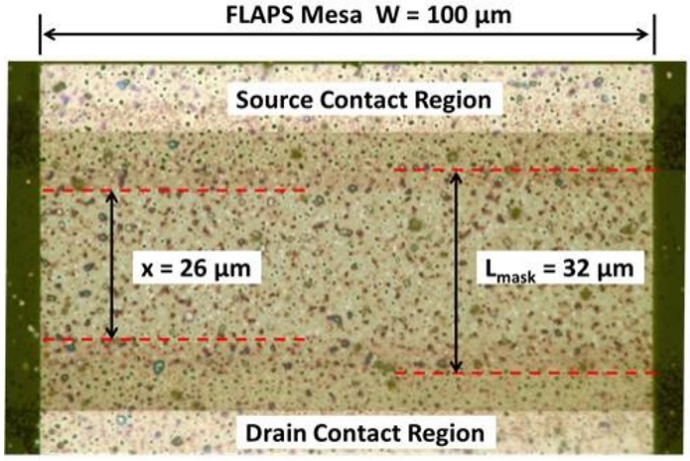


Figure 21: Microscopic image of a silicon mesa in a NMOS transistor. The designed channel length and actual channel length are marked. [11]

# Chapter 5 Self Aligned Processes

To reduce the significant lateral dopant diffusion a new mask and process flow was developed. The self aligned transistors work by having the metal gate present before the implant. This eliminates the need for a photoresist mask. The tolerance included in the design to account for possible misalignment between the metal gate and implant layers can therefore be removed. The metal gate for self alignment must be added after the FLA. This is because the metal gate will block light from reaching the silicon preventing the desired crystallization in the channel region. Also the metal gate may melt or even vaporize due to the large amounts of energy. The metal gate was made with molybdenum due to its high melting point to prevent it from liquefying during annealing. Since the implant must follow the metal gate deposition the implant must also be after FLA. In order to activate the dopants furnace annealing is used. This will reduce the diffusion of dopants but may not activate the dopants as well as the FLA. Some diffusion of the dopants will be seen due to the activation anneal.

In addition to the new process a new mask set was developed. The metal gate layer was added. Larger sized transistors of up to 64 μm length and 96 μm width were added to better characterize lateral dopant diffusion. In addition to larger devices smaller channel length devices were added down to 1 μm to determine the minimum channel length possible for these devices. New test structures were added. The Van der Pauw structures were kept for sheet resistance calculations. This would help determine the change in gate capacitance with the thinner gate oxide in the self aligned flow. CMOS device capability was added with the addition of separate NMOS and PMOS masks once

they were shown to be possible with working NMOS and PMOS devices. Non-self aligned devices shown in Figure 22 were included in the new mask design to serve as a comparison in performance and lateral dopant diffusion.

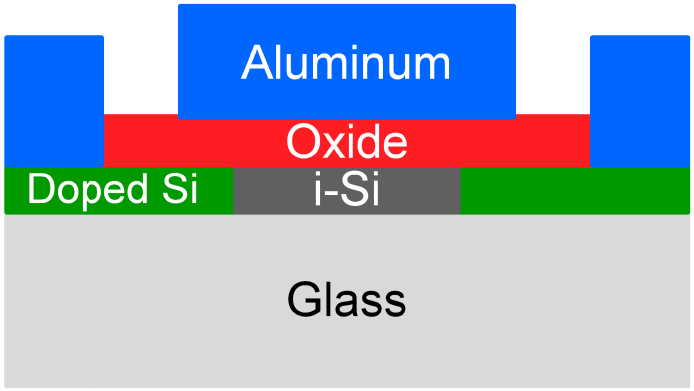


Figure 22: Diagram of the non-self aligned device structure.

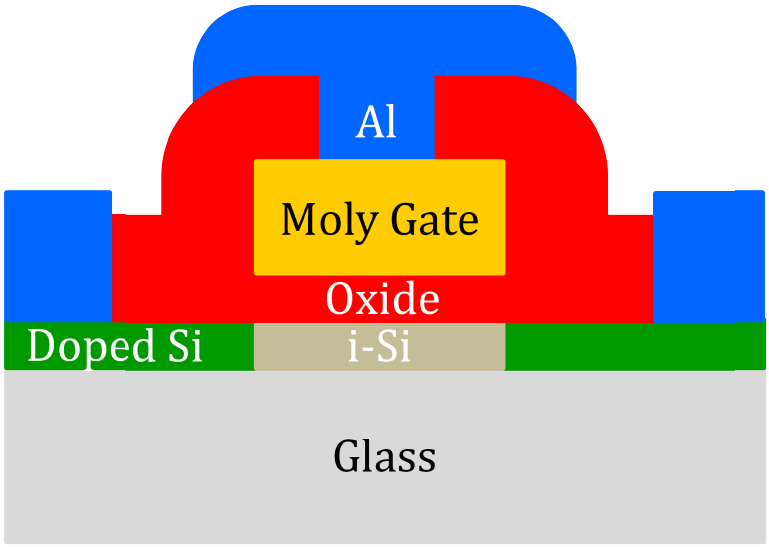


Figure 23: Diagram of the self aligned device structure.

One of the features of the new mask is the grain orientation with respect to the channel length and width. The goal of the large grain sizes is to create a transistor on a single crystal to reduce the number of grain boundaries. By changing the orientation of the grains the number of grain boundaries along the channel would change influencing

the electrical characteristics of the device. An example of a channel length oriented grain can be seen in Figure 24. The new mask provides different ways of making FLA transistors including a wide range of sizes, self-aligned gates, and different grain orientations. The different combinations of transistors can be seen in Figure 25.

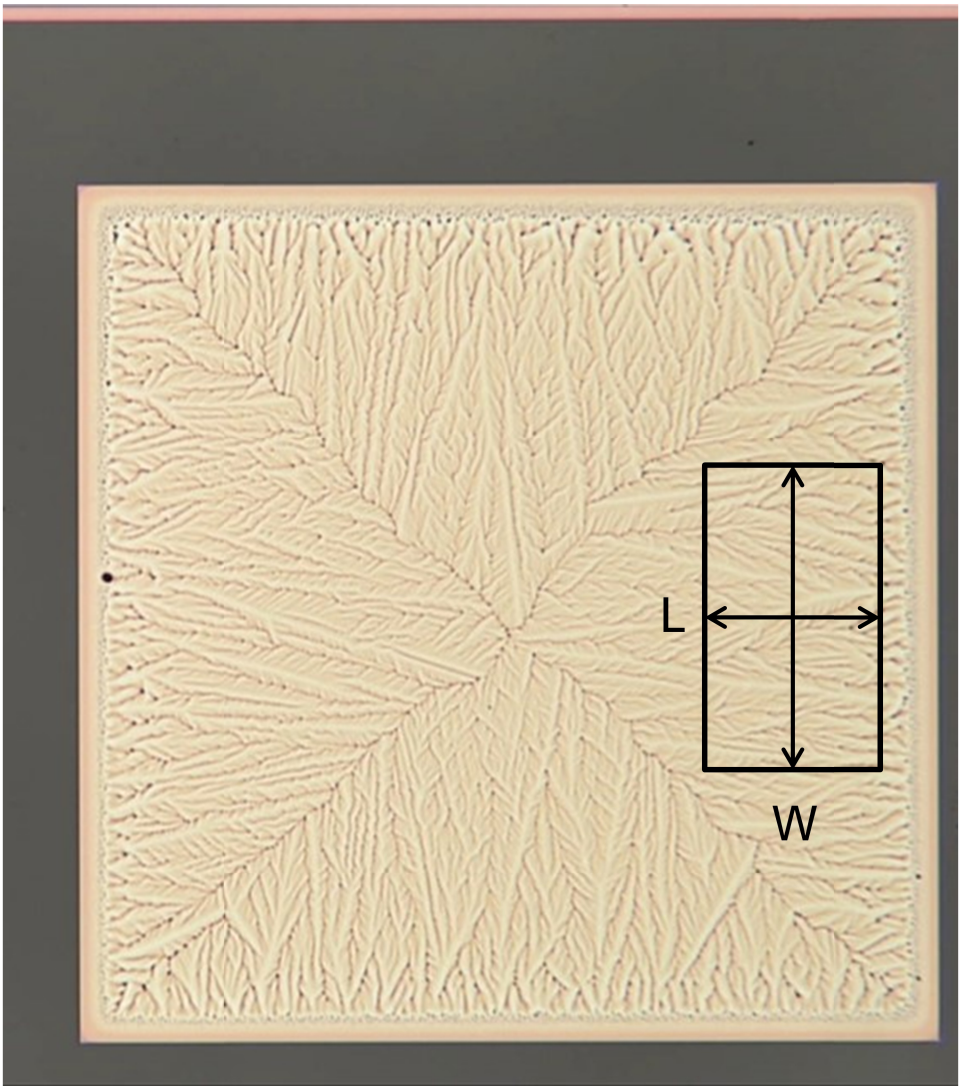


Figure 24: Picture of mesa structure taken from Figure 9. The black box represents the channel of a transistor. The grains are oriented along the length of the transistor.

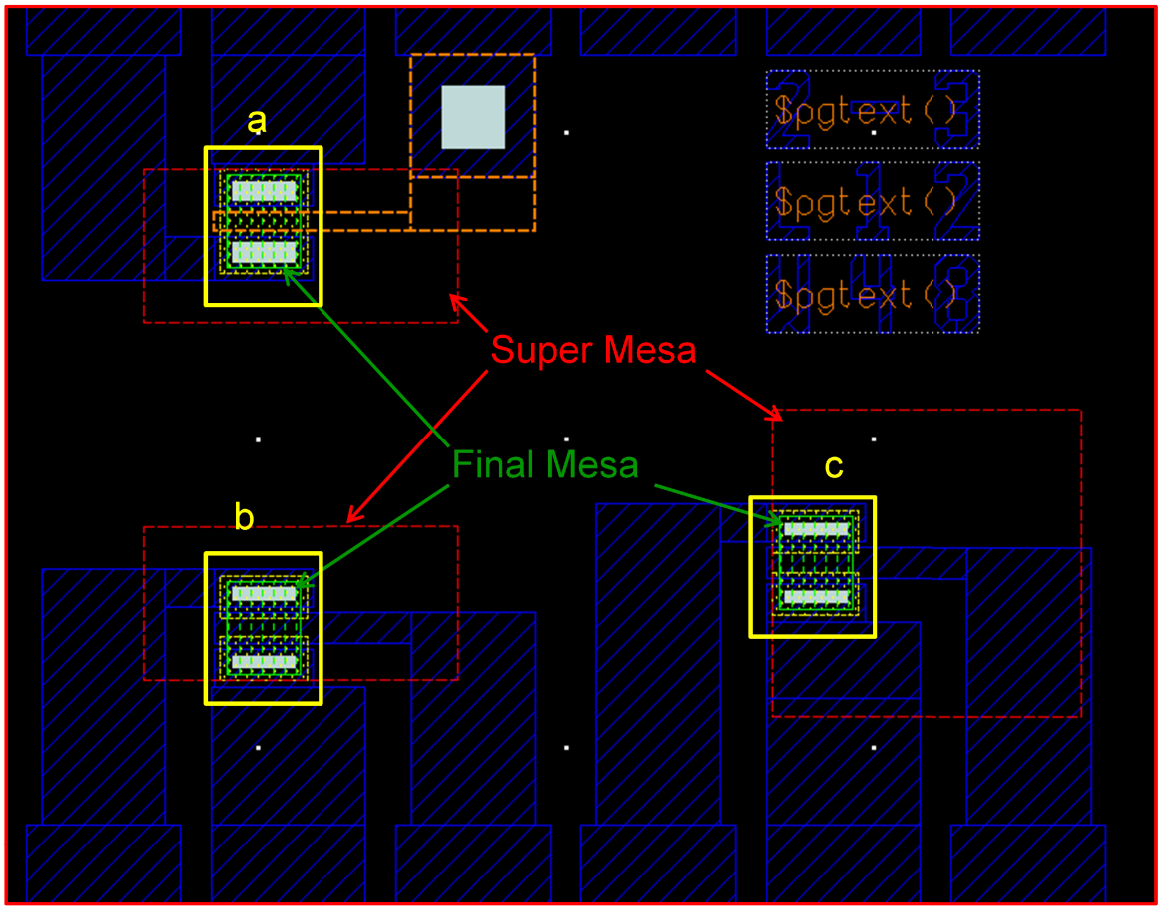


Figure 25: Layout of transistors in the new mask design. Transistor a) has the self aligned structure and the grains are oriented along the channel length. Transistor b) is a non-self aligned device oriented in the same direction as a). Transistor c) is a non-self aligned device with the grains oriented in the direction of the width.

# Chapter 6 Results

## 6.1 Self Aligned Results

A group of wafers were fabricated to test the new process flow. The new mask had not been made yet so there was no self aligned metal gate. The aluminum gate non-self aligned structures were fabricated. With the implant being after the FLA the phosphorus implant has the possibility of amorphization of the silicon after it has been crystallized. This group of wafers then had the implant after FLA to test whether the dopants would activate. After the wafers were fabricated they were tested. The sheet resistance was measured using a Van der Pauw. It showed that the dopants did activate with sheet resistances of 1.4k to 2.3k Ω/sq for P type and 600 to 1.4k Ω/sq for N type. Activation with the FLA resulted in sheet resistances of 250 Ω/sq. The silicon was implanted with a dose of $4x10^{15}$ $cm^{-2}$.

Testing of the transistors revealed leaky gates. The gate current dominating the drain current can be seen in Figure 26. The cause of the gate current is likely from the 100 nm gate oxide being implanted. Normally the screen oxide is stripped from the wafer after the implant and replaced with a gate oxide but it was not done in this case. Because of the non-self aligned gate overlap there was implanted gate oxide underneath the aluminum gate. This implanted oxide would break down much easier. The gate oxide during operation would experience an electric field of 0.1 to 1 MV/cm.

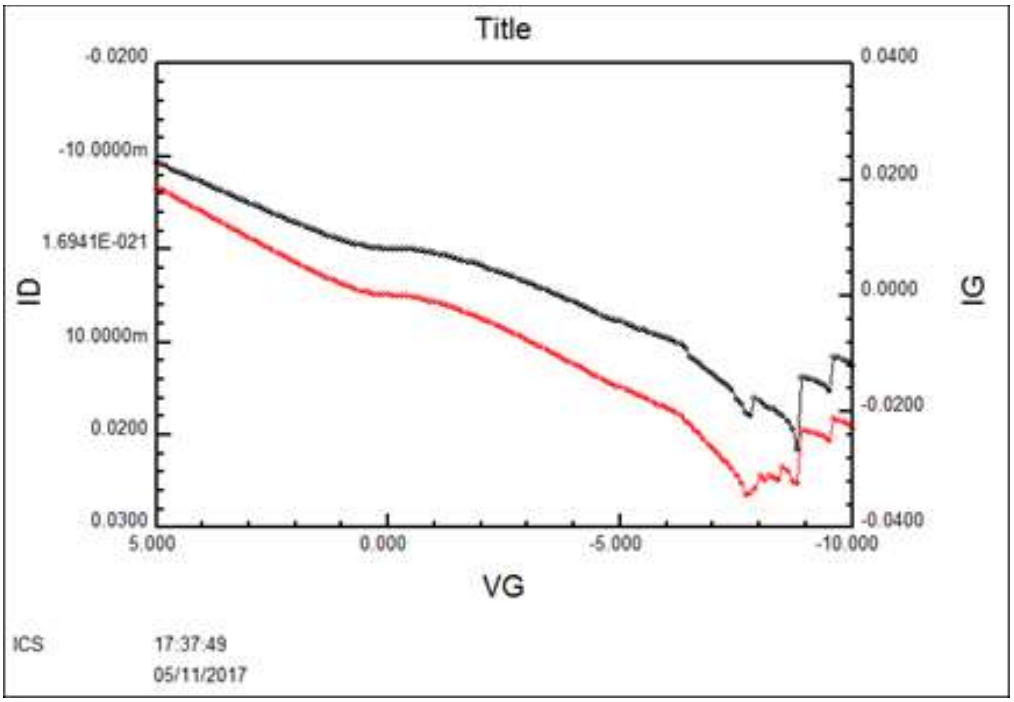


Figure 26: Voltage transfer curve of implanted gate oxide devices. Gate current is in red and drain current in black. Note characteristic offsets are due to plot auto-scaling.

Once the implant activation was verified and the new mask was created self aligned devices were started for fabrication. Issues with the processing were found. The molybdenum that was deposited for the self aligned gate caused a large amount of stress on the wafer. The stress of the film was noticeable by the film flaking off the samples. This resulted in all of the wafers forming cracks in the glass at the center of the wafers. If the wafers continued with processing eventually the substrates would break in half. Some of the wafers did not show cracks until later in processing. These wafers were then implanted and activated. After the activation anneal some of the molybdenum showed oxidation when the film turned clear under the microscope. The activation anneal is carried out with a nitrogen gas flow to make the atmosphere inert but it is still carried out in atmospheric pressure so some oxygen may have been present during the anneal. The

metal gate turning clear on the edges can be seen in Figure 27. Because the wafers cracked during the implant only a thin oxide was protecting the molybdenum. This thin oxide was made by depositing a 100 nm oxide then etching in 10:1 DI:HF to reduce the oxide thickness to 30 nm. Restrictions in the minimum film thickness that can be deposited with the PECVD process used prevented a deposition below 60 nm. The etched back film had a standard deviation of 25% over the mean showing significant non-uniformity. Due to the non-uniformity of the oxide the molybdenum may not have been sufficiently protected during the activation anneal.

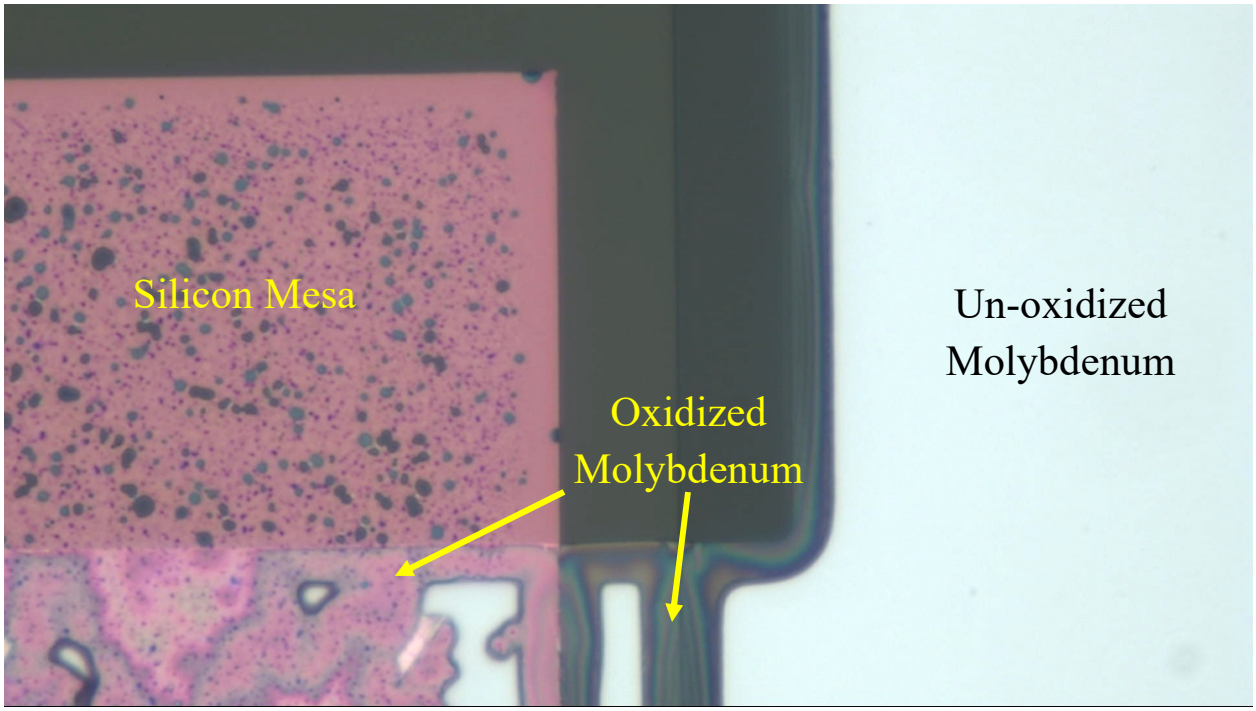


Figure 27: The silicon mesa is in pink, un-oxidized molybdenum in white, and oxidized molybdenum is semi-transparent.

## 6.2 Non-Self Aligned Electrical Results

For the next round of experiments, non-self aligned devices utilizing an aluminum gate were fabricated. The implant was not done through the gate oxide to prevent the leaky gates seen previously. FLA exposure energy of 5 J/cm$^2$ was used. This gave the largest area where the silicon crystallized and gave low sheet resistance while still not de-wetting to the point of breaking connections. The implanted dopants were activated using a 630 °C 12hr furnace anneal in $N_2$. The silicon was processed with the molybdenum gate and the new mask. The use of a thinner molybdenum layer as well as a lower processing temperature prevented the molybdenum from peeling off.

Problems were still found with the molybdenum oxidizing. During the implant, resist is still used for patterning to enable CMOS devices. After implanting the resist was difficult to remove and required multiple ashings in $O_2$ plasma and solvent strip removals. During this processing the molybdenum oxidized and became transparent similar to before. The protective oxide again wasn't enough to prevent molybdenum oxidation. This also prevented any working self aligned transistors. However the process did produce working non-self aligned transistors that were made on the same die as the self aligned devices.

The first round of testing was on the Van der Pauw structures to determine the sheet resistance. Due to the square geometry of the testing structures Equation 1 was used to calculate the resistance. $R_s$ is the sheet resistance, $V_1$ and $V_2$ are the applied voltages, and I the measured current.

$$R_S = \frac{(V_1 - V_2) * \pi}{I * ln(2)}$$

(1)

The sheet resistance was found to be 972 Ω/sq and 2800 Ω/sq for N-type and P-type, respectively. Both sheet resistance values were similar to what was found in the preliminary results. The high resistance values, especially for the PMOS, indicate poor activation of the dopants or not enough dopants being incorporated to the silicon during implant.

To determine the best transistor such as the one shown in Figure 28 a range of transistor length devices was measured. It was found the best characteristics came from a 64 μm length 96 μm width transistor for NMOS and a 24 μm length 48 μm width device for PMOS. The measurements were taken with a drain voltage of 1 V and -1 V for NMOS and PMOS respectively. The sub threshold slope can be seen in Table 1. This is comparable to the results found previously of 118 and 140 mV/dec. The mobility for the devices was then calculated using equation 2, where μ is the mobility, $g_m$ is the transconductance, $C_{ox}$ the capacitance of the oxide and $V_{DS}$ is the drain to source voltage. The peak transconductance for the NMOS and PMOS devices was taken.

$$\mu = \frac{g_m}{\frac{W}{L} * C_{OX} * V_{DS}}$$

(2)

The mobility calculated is in table 1. This is an order of magnitude less than what was found previously. The measured mobility is still higher than what is typically achieved with amorphous silicon at ~1 $cm^2/(Vs)$. While the mobility is less than previously the devices still show that the self aligned process flow is capable of forming functional devices. The performance of the NMOS transistors was not limited to a single device as seen in Figure 30. These devices were replicated over multiple die in a single wafer showing that the channel material can be optimized to work in several devices.

The threshold voltage was calculated from the linear characterization shown in Figure 29. The extracted threshold voltages are in Table 1. These values are quite high but can be improved through a higher concentration of activated dopants.

The low mobility and sub threshold slope compared to previous devices is likely due to an increased number of traps in the device. The different sources of traps include interface traps between the channel and gate oxide or substrate, traps along the poly-silicon grain boundaries, and traps caused by the implant. The deposition of the gate oxide was the same between the FLA activated device and the furnace annealed device. Both were deposited with PECVD tetra-ethyl ortho-silicate (TEOS) after FLA and the implant. They later saw the same processing steps as the molybdenum gate step was skipped for the non-self aligned devices tested. The channel material for the furnace annealed devices was matched to the FLA annealed devices. Because of this the grain boundary density is expected to be the same across devices. Each of the devices received the same $4x10^{15}$ $cm^{-2}$ dose implant. The furnace annealed devices did not activate the same as shown with $R_S$. Because of this more traps are expected within the silicon. With

the interfaces and grain boundaries remaining similar but the implant activations being different it is expected that the traps generated by implant damage are the cause of the devices performing worse than previously.

Once the devices were testing the lateral dopant diffusion was investigated. Initially Terada-Muta analysis was performed to determine the diffusion as was previously done. The analysis however was difficult to analyze as can be seen in Figure 31 and Figure 32. The measured resistance ($R_M$) does not trend downward as would be expected. Because there is no trend no value could be determined for the change in channel length. Due to having multiple channel length devices the smallest working device could be determined. The smallest channel length for a working transistor was 4 and 2 μm for NMOS and PMOS respectively. The transistor transfer curve can be seen in Figure 33. Devices with smaller channel lengths were not able to turn off. The lateral dopant diffusion then could be interpreted as being slightly less than these channel lengths. For both NMOS and PMOS this is significantly less than the 6.3 and 13.4 μm found previously with the FLA dopant activation.

Table 1: Comparison of furnace-activation electrical characteristics to previously fabricated FLA-activated devices

| | **Furnace activation** | | **FLA activation** | |
|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS |
| **RS (Ω)** | 800 | 2800 | 250 | 250 |
| **L/W (μm)** | 64/96 | 24/48 | 32/100 | 32/100 |
| **μ ($cm^2$/(Vs))** | 40.2 | 12.3 | 380 | 143 |
| **SS (V/dec)** | 2 | 1.1 | 0.118 | 0.14 |
| **VT (V)** | 4.22 | -15 | 0.23 | -2.82 |
| **Min L (μm)** | 4 | 2 | 20 | 20 |

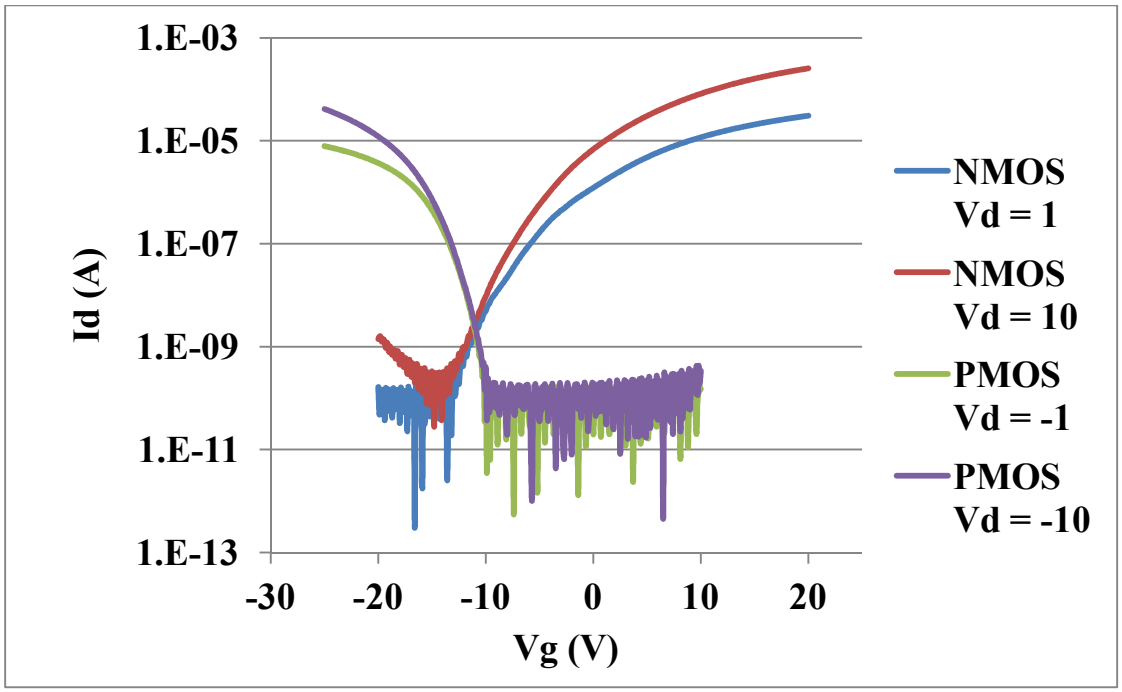


Figure 28: Logarithmic $I_D/V_G$ transfer curve of best performing transistors.
NMOS L = 64 µm, W = 46 µm; PMOS L = 24 µm, W = 48 µm

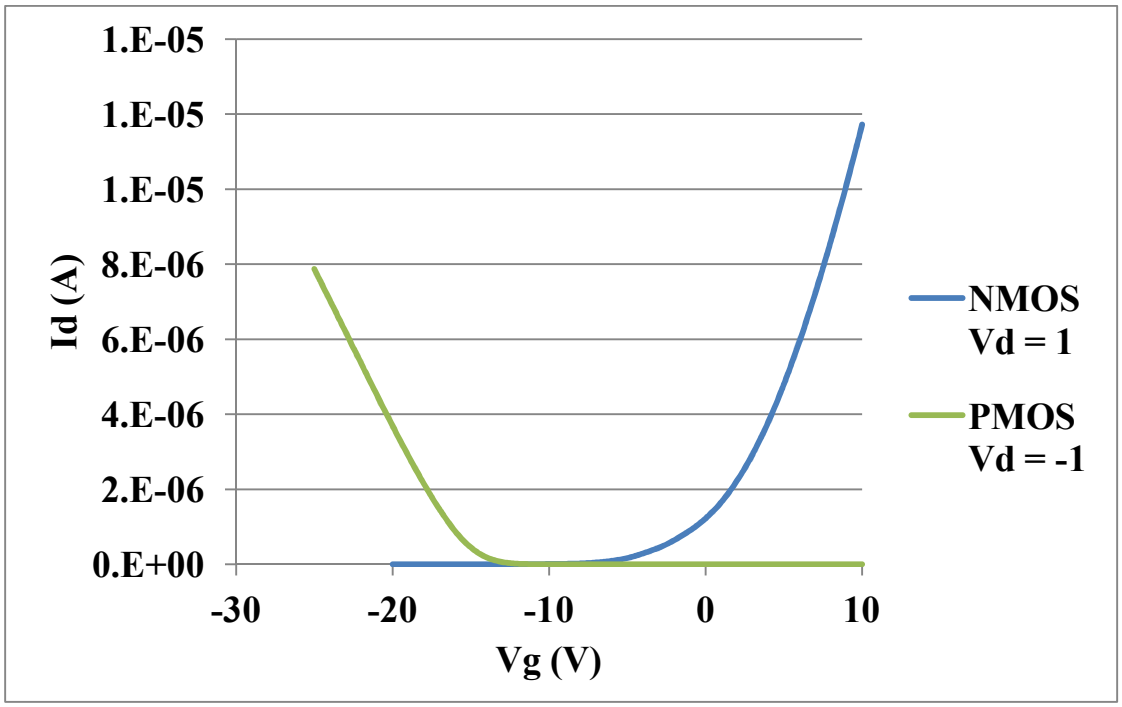


Figure 29: Linear $I_D/V_G$ transfer curve of best performing transistors
NMOS L = 64 µm, W = 46 µm; PMOS L = 24 µm, W = 48 µm

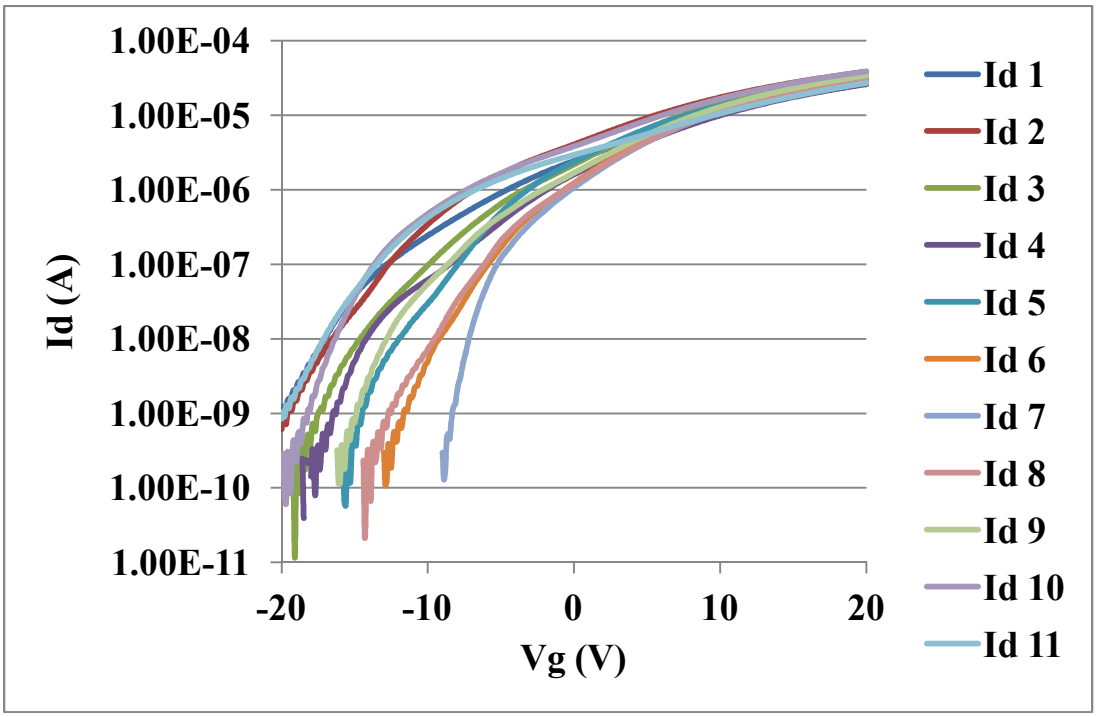


Figure 30: Overlay of multiple 64 µm length 96 µm width NMOS transistors

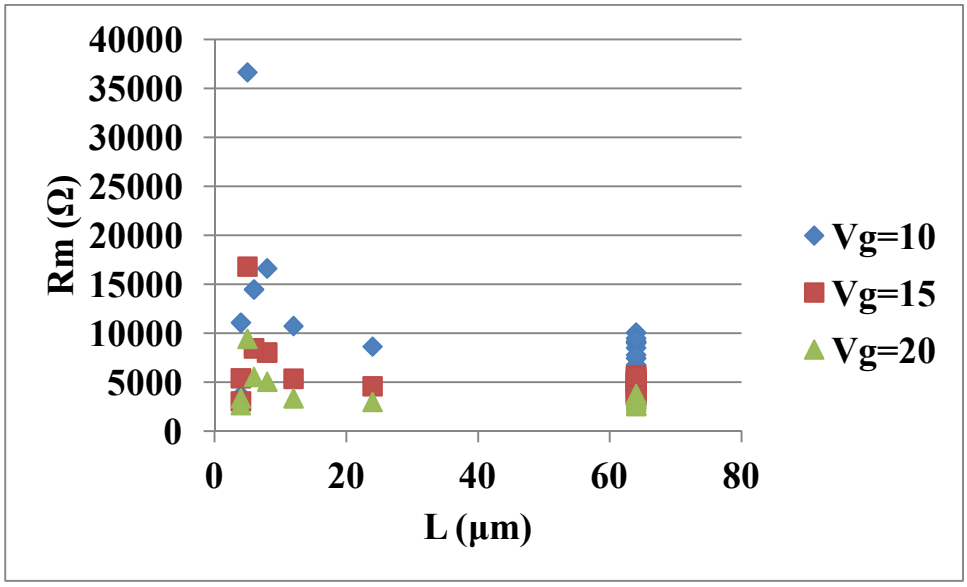


Figure 31: NMOS Terada-Muta analysis

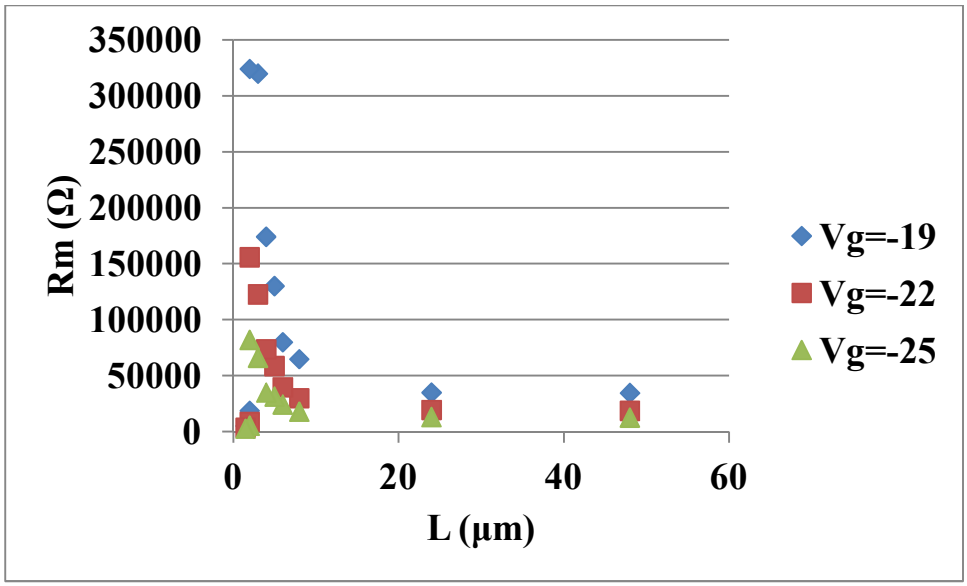


Figure 32: PMOS Terada-Muta analysis

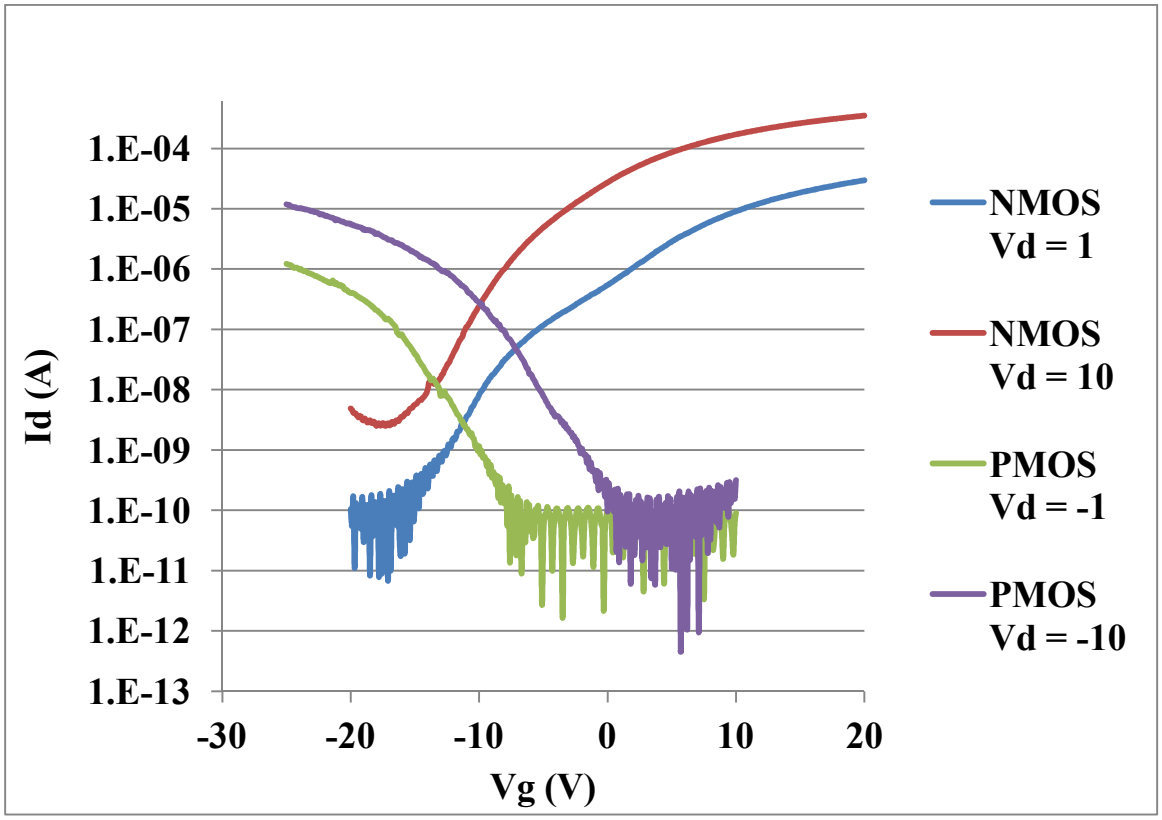


Figure 33: Logarithmic $I_D/V_G$ transfer curve of smallest working transistors
NMOS L = 4 µm, W = 8 µm; PMOS L = 2 µm, W = 4 µm

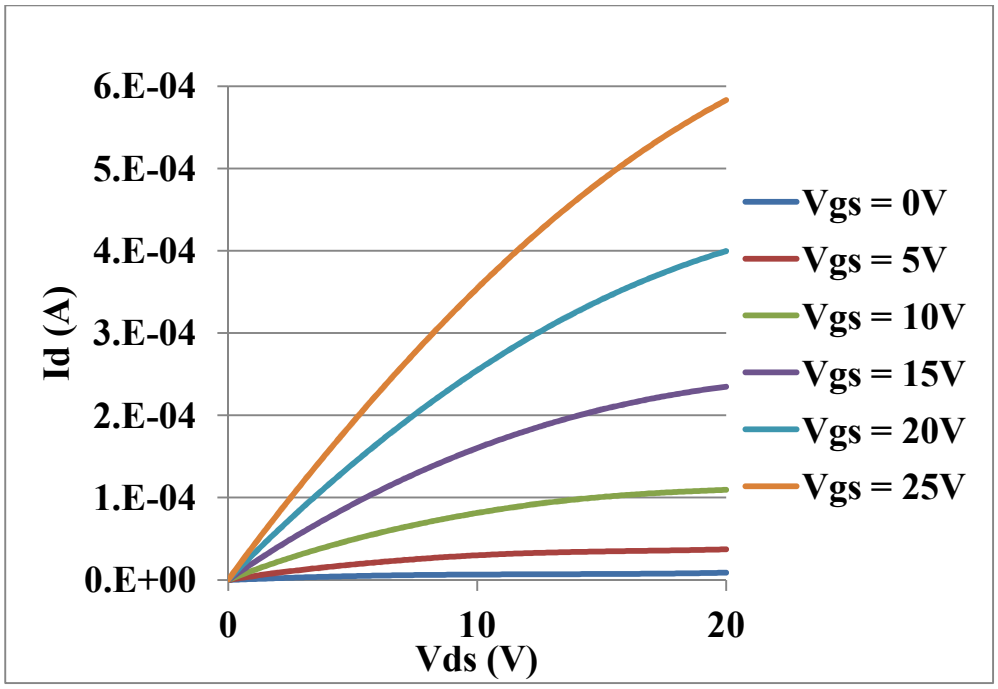


Figure 34: NMOS family of curves for smallest working device
NMOS L = 4 µm, W = 8 µm; PMOS L = 2 µm, W = 4 µm

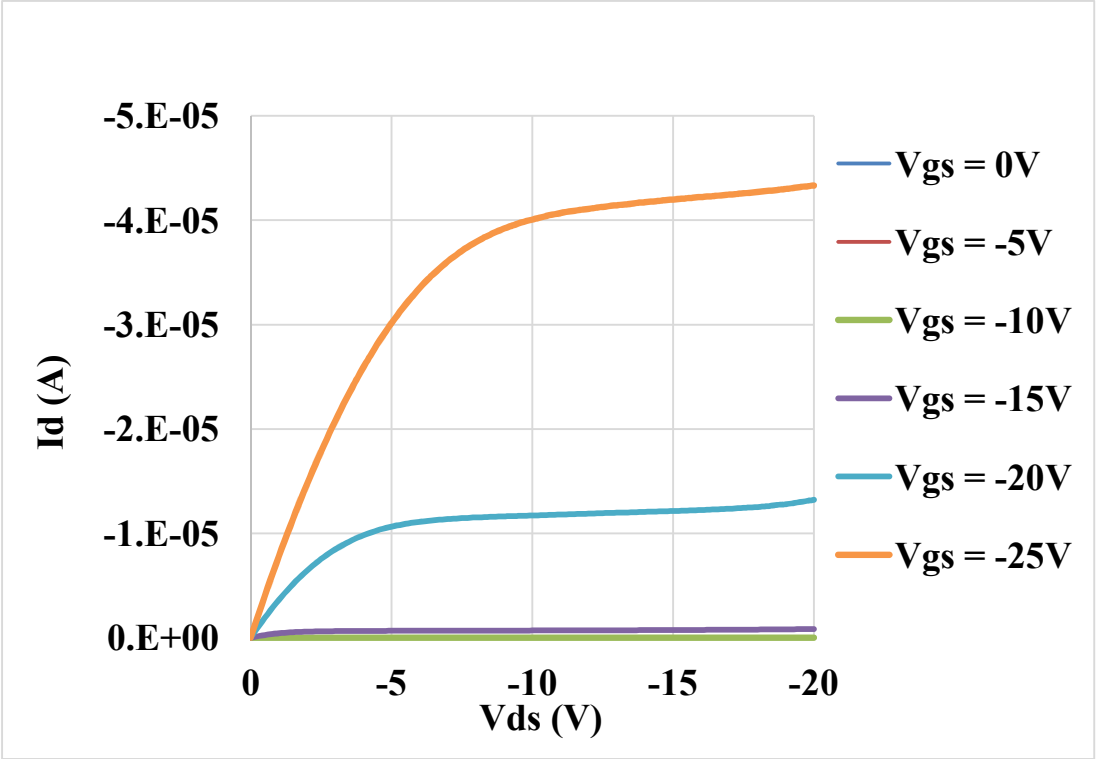


Figure 35: PMOS family of curves for smallest working device
NMOS L = 4 µm, W = 8 µm; PMOS L = 2 µm, W = 4 µm

# Chapter 7 Fin

## 7.1 Conclusion

AMLCD technology requires a low cost polycrystalline material to be manufacturable. FLA poly silicon is able to provide the needed requirements with an improved mobility over amorphous silicon and large scale manufacturability. Through the use of a Nova Centrix Pulse Forge low temperature poly silicon CMOS devices have been realized.

The disadvantage to previously made devices was the lateral dopant diffusion during the FLA activation of implanted dopants. The lateral dopant diffusion limits the minimum transistor size. In order to improve this process a self aligned gate and furnace dopant activation were investigated. The use of a self aligned gate eliminates the need for any gate overlap due to lithography misalignment. The molybdenum protection layer used to protect the gate during processing was too thin and the difficulties in removing resist resulted in the molybdenum being oxidized. An improved molybdenum protection layer and a different implant mask material are needed to successfully create a self aligned gate.

The furnace activation was investigated because the previous process flow activated dopants using FLA. With the silicon liquefying the dopant diffusion is greatly accelerated even over the extremely short exposure time. By switching to a longer, lower temperature furnace anneal the diffusion of dopants and lateral dopant diffusion was greatly reduced. This difference in activation processes did affect some of the other electrical characteristics. The threshold voltages were increased by an order of magnitude

and the mobility was reduced by an order of magnitude. This is due to the traps caused by the implant damage not repairing to the same extent as the FLA dopant activation. The mobility was still higher than what is seen with a-Si transistors making this material superior. With the addition of a self aligned gate and improvements in dopant activation and defect passivation these transistors may be candidates for next-generation AMLCD technology.

## 7.2 Future Work

The next step in developing better performing transistors is making a working self aligned gate and improving the doping profile of the source and drain. In order to prevent molybdenum oxidation during the furnace anneal or resist stripping steps, a more robust protection layer for the molybdenum is needed. The limiting factor in oxide thickness is the deposition. The tool used for PECVD of the oxide is limited to 60 nm. Anything below this deposition thickness becomes uncontrollable. By depositing both the gate oxide and oxide protection layer at 60 nm the implant masking layer would only increase by 20 nm while also significantly increasing the thickness of the protection layer. Depositing the protection layer and using a dry etch back would be more controllable compared to a wet etch back.

The other issue that resulted in molybdenum oxidation was the resist stripping. The molybdenum protection layer did not prevent oxygen plasma from reaching the molybdenum and oxidizing it. A way to prevent this is through the use of an aluminum hard mask during implanting. Since the resist would only be used to pattern the hard mask and be removed before the implant step it would be much easier to remove. A

solvent strip alone would suffice in removing the resist preventing any oxygen plasma from reaching the molybdenum.

The other process change needed for improved transistor characteristics is the P-type implant. Previous experiments have shown a fluorine implant before boron improves the activation of the boron during the furnace step. This amorphization of the silicon allowed for better boron activation and higher concentration of implanted boron in the silicon. Using $BF_2$ as the implanted ion could also increase the amount of boron implanted into the silicon layer. The amorphization of the silicon would have to remain controlled during the implant to still allow the furnace annealing to repair the silicon lattice.

Another factor that greatly influenced the electrical characteristics was the traps present in the device. The amount of traps needs to be characterized through the use of I-V and C-V characteristics. Interdigitated capacitors already exist on the device allowing for this characterization to be done. Additional experiments can be done with plasma or chemical surface treatments in order to passivate the surface. Additionally the grain orientation in the channel can be investigated. Width oriented grains would be expected to have worse performance due to the increased number of traps with the additional grain boundaries. With these improvements in the process better performing transistors can be realized.

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