IMPURITY CONCENTRATION PROFILE DETERMINATION BY CAPACITANCE-VOLTAGE MEASUREMENTS

David J. Cheskis
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

A FORTRAN program has been written to manipulate the data obtained from 1 MHz C-V measurements. This program utilizes the data to compute information on the impurity profile of capacitors. Capacitors were fabricated with varying doping profiles and tested. The doping proifles obtained using this program were consistent with SUPREM models.

INTRODUCTION

Capacitance-voltage (C-V) measurements have many applications in the characterization of semiconductors, among the most popular are techniques used to study the Metal-Oxide-Semiconductor (MOS) system. Using the basic high frequency (1 MHz) C-V test, information can be gathered about the quality of the oxide with respect to both the electrical performance and the processing involved in fabrication of the MOS device. With further manipulation of the C-V data, more information can be gathered,such as the doping profile of the semiconducting substrate.

The typical n-type C-V curve shown in Figure 1 depicts the regions of operation of the MOS capacitor. With a large voltage applied opposite of the polarity of the substrate (positive voltage), the majority carriers build up at the Si-SiO2 interface due to the applied voltage. When the voltage is decreased toward zero volts, the majority carriers relax and the donors at the surface start to become depleted of their carriers. This results in the ionization of the donors to maintain charge neutrality in the semiconductor. Finally, as the voltage in increased with the same polarity of the bulk (negative), the depletion region width reaches a maximum value and majority carriers are then attracted to the surface to compensate for the excess charge applied to the gate.

In both the accumulation and inversion regions of the typical C-V plot the ionized impurity density is only weakly proportional to the applied voltage since the free carriers in the bulk comprise the majority of the charge accumulation under these biasing conditions.

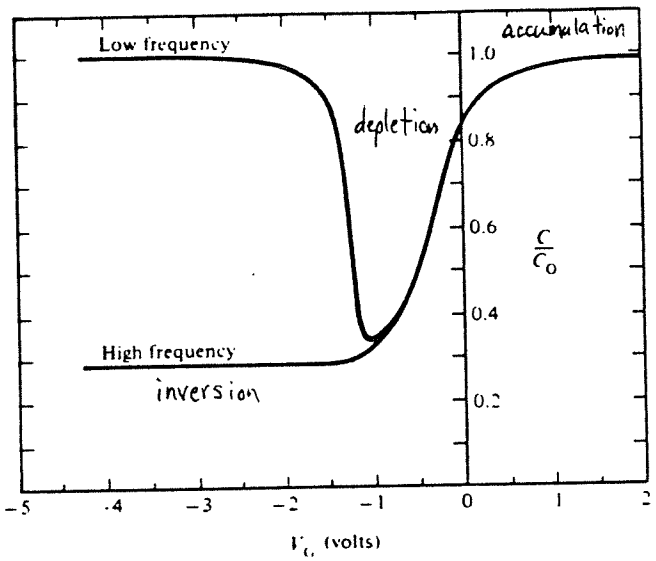


Figure 1: N-type capacitor C-V plot.

Therefore, using the abrupt space-charge approximation for the capacitor in the depletion region, and assuming that interface traps have negligible influence, the amount of charge depleted in the semiconductor is proportional to the charge on the metal by a factor of q, the charge of an electron. The depletion region width then varies as a function of applied voltage, Va, by

$$W = \{(2\ s/qN(x))[Vbi - Va]\}^{**}1/2 \qquad (1)$$

where s is the permittivity of Silicon, N(x) is the impurity concentration, and Vbi is the built-in potential of p-n junction. The total charge per area in the depleted region is then given by Equation 2.

$$Q = qN(x)W \qquad (2)$$

Since the capacitance is the differential of the charge with respect to the voltage, the capacitance at any given applied voltage is determined by

$$C = dQ/dV = A\{(q\ sN(x)/2[Vbi - Va])\}^{**}1/2 \qquad (3)$$

which can then be used to fit data from C-V analysis by rearranging Equation 3 to be

$$C = A\ s/W. \qquad (4)$$

To determine the doping profile at a given depth into the substrate, the amount of the change in the depletion region width due to additional applied voltage is necessary. The Mott-Schottky [1] relation allows the doping density to be determined by the slope of the inverse square data of the C-V plot. A plot of 1/C**2 as a function of the applied voltage yields a constant slope for a uniformly doped substrate. A typical 1/C**2 curve is shown in Figure 2 for an undoped substrate in the depletion region of the C-V curve.

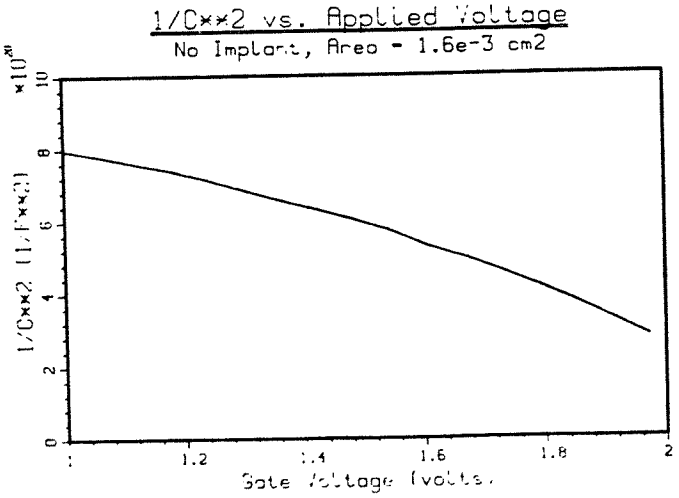


Figure 2: A typical 1/C**2 vs voltage curve.

If the substrate is non-uniformly doped (i.e. ion implanted, diffused concentration gradient), the Mott-Schottky plot will, in turn, be nonlinear. The slope of the Mott-Schottky plot is given in Equation 5.

$$m = \text{slope} = (1/C^{**}2)/\ V = 2/(Aq\ sN(x)) \qquad (5)$$

Rearranging Equation 5 provides the impurity concentration as below

$$Nd = 2/(Aq\ sm), \qquad (6)$$

which then is plotted as a function of position into the substrate, by determining the position, W, from the capacitance using Equation (4).

In addition, the maximum dept.. to which the doping profile can be determined is limited by the onset of the inversion region in the C-V curve [2]. The profiles vary, therefore depending upon the C-V charactersitics of the particular device.

A FORTRAN program was developed and implemented to determine the slope of the Mott-Schottky curve. From the C-V data gathered with a 1 MHz test set-up, the Mott-Schottky curve and the doping profile of the sample were generated with the program. MOS capacitors have been fabricated and tested which have varying doping profiles as a result of ion implantation.

EXPERIMENT

A FORTRAN program was developed and implemented to determine the slope of the Mott-Schottky curve. Data acquisition was performed using the method developed by Dale Webb using the HP4145 as an analog to digital converter [3]. The data is then passed to the IBM PC and uploaded to the VAX mainframe using KERMIT protocol.

The FORTRAN program CVND.FOR uses the central difference method to calculate the slope of the Mott-Schottky curve. The space charge width is on the order of a Debye length [2] when the capacitor is biased in the accumulation mode, thus the doping profile cannot be determined accurately until near the depletion mode of operation. Since the data in the accumulation region is not as important as that in the depletion region, more attention was paid to the detail of the curve there when digitizing the data.

With the slope of the Mott-Schottky curve, the ionized impurity concentration is calculated using Equation (6) above. The depth into the substrate at which this impurity concentration occurs is then calculated by rearranging Equation (4) and solving for W.

MOS Capacitors were fabricated and obtained from Matt Wickham. In addition, Schottky diodes were fabricated to test and compare with the MOS capacitors to determine the effects of the 1 hour 1100 C capacitor oxide growth process on the impurity profile. Three p-type wafers were implanted with Boron at 80 keV with a dose of 8e12 cm-2 ions. These three wafers and two bare wafers received a 900 C anneal for 30 minutes in N2 at 6 slpm to remove the damage of the implant and activate the impurities.

Aluminum was then deposited onto the backside of all of the wafers and sintered at 450 C for 15 minutes to achieve an ohmic contact to the backside. Three wafers were then patterned with capacitors on the front side, two of which were implanted with one was non-implanted wafer.

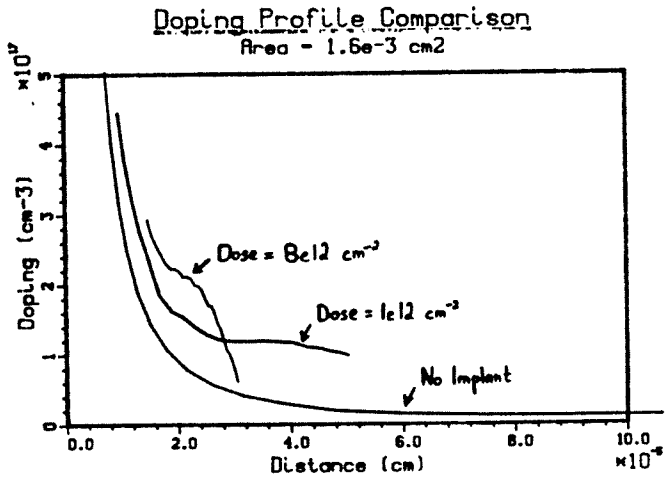
The fabricated deviecs were then tested and along with the wafers fabricated by Matt Wickham, were analyzed using the CVND.FOR program to determine their impurity profiles. SUPREM was used to model the implant and oxidation steps performed in the fabrication.

RESULTS/DISCUSSION

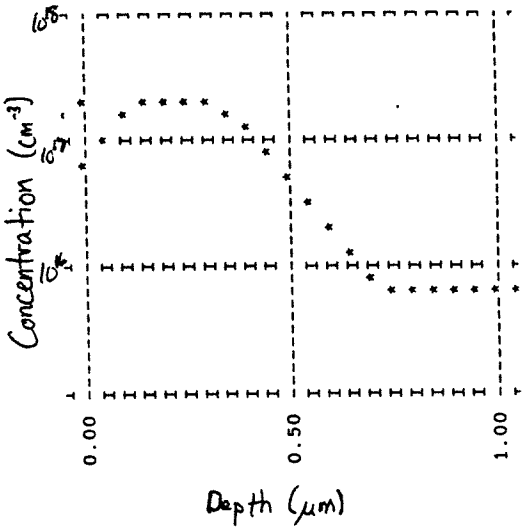
After the fabrication of the Schottky diodes, electrical testing indicated that each capacitor was shorted, most probably due to the ohmic contact on the backside. In addition, the Aluminum deposited on the front side could have been annealed to some extent during the ashing of the photoresist used to pattern the contacts, creating an ohmic contact as well. Therefore, the results described were only gathered on the capacitors fabricated by Matt Wickham, which received doses of 1, 2, 4 and 8e12 cm-2 ions of Boron at 80 keV. At 80 keV, the projected range of the implant is approximately 2500 A and produces a profile of about 2e17 atoms/cm3 according to the Pearson IV distribution utilized in SUPREM II.

Various capacitors were tested, and using the digitized data, the number crunching was performed on the VAX/VMS system. The program CVND.FOR also allows for the data to be analyzed on the VAX as the program not only outputs the doping profile as a function of position in a file called NDDATA.DAT, but also the C-V data (in a file called CVOUT.DAT) and the Mott-Schottky plot of 1/C**2 vs applied voltage (in a file called MOTT.DAT).

The impurity profiles correlated well with the results of simple SURPEM models. Shown in Figure 3a is a comparison of two different implant dose profiles and a non-implanted profile, while in Figure 3b, the SUPREM model of the highest implant dose is depicted.



(a)



(b)

Figure 3: (a) Impurity profiles for no implant, 1e12 cm-2 dose and 8e12 cm-2 dose. (b) SUPREM II model of 8e12 cm-2 implant with thermal oxidation.

As mentioned above, the impurity profile is calculated for a much larger portion of the bulk in the undoped capacitor as compared to the implanted capacitors. In addtion, it can be noticed that the impurity profile extends upward in the region closest to the surface of the substrate. This is due to the interface proximity limitation [2] in which the profile begins to increase exponentially as the interface is approached. This affect of the impurity profile is caused by the Si-SiO2 interface within a few Debye lengths of the interface.

Additionally, the profile in the very closest region to the interface is unable to be determined as the carriers in this region are also depleted either by interface traps or other charge in the oxide.

SUMMARY

A program has been developed which will allow for simple determination of impurity profiles of capacitors fabricated at RIT. The program CVND.FOR (attached in the Appendix) is used to calculate these profiles and output C-V and 1/C**2 curves. A capacitor was profiled and had a maximum impurity concentration of about 2e17 /cm3 approximately 2100 A into the substrate, which correlates well with a SUPREM simulation.

REFERENCES

[1] R.K. Ahrenkiel, Microelectronic Manufacturing and Testing 11 (13), 13-14 (1988).

[2] E.H. Nicollian and J.R. Brews, MOS Physics and Technology, pp. 380-408.

[3] Webb, Dale, RIT Senior Project, Automated Capacitance-Voltage Measurements , 1987.