ECL CIRCUITS

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ABSTRACT

Emitter Coupled Logic (ECL) gates were fabricated on a n-epi layer. SUPREM was used to simulate the fabrication including junction depth and sheet resistance. The Integrated Circuit Editor was used to layout the design based on SUPREM parameters. SPICE was also used to confirm the proper operation of the devices. Testing was limited due to a lack of a probe card for the logic analyzer. But, an npn transistor was tested with a gain of one indicating a working device was present. A subcollector implant was not performed due to the time constrains placed on the project.

INTRODUCTION

Emitter Coupled Logic operates all transistors in their forward active region or in their cutoff region, avoiding saturation and the accompanying stored charge [1]. Thus, ECL gates are faster than those in any other logic family. ECL gates operate with a supply voltage of -5.2 volts. The logic levels are therefore negative, being approximately -.75 (high) and -1.6 volts (low). Complementary outputs are also available which avoids the necessity of adding gates simply as inverters. A fanout as large as 25 is allowed, but with noise margins on the order of .2 volts [2]. Other disadvantages associated with ECL gates include a small difference between the two logic levels (approximately .8 volts), larger chip area occupied due to the transistor isolation regions, and a high power dissipation relative to other logic families.

A typical ECL transistor is shown in Figure 1. The isolation regions are necessary to obtain devices which are electrically separate. The p-type substrate must always be held at a negative potential with respect to the isolation islands in order that the pn junctions be reverse biased.

Figure 1: Cross section of a typical npn transistor

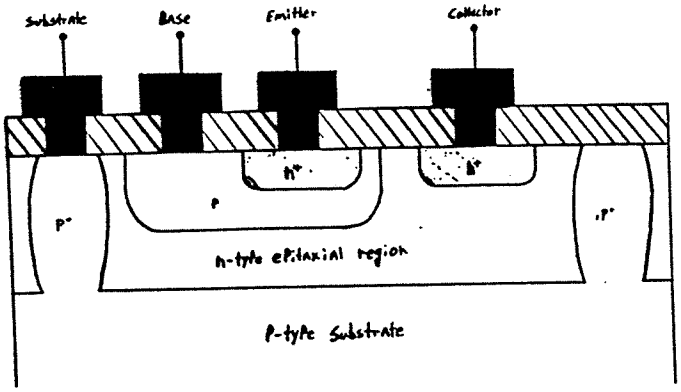
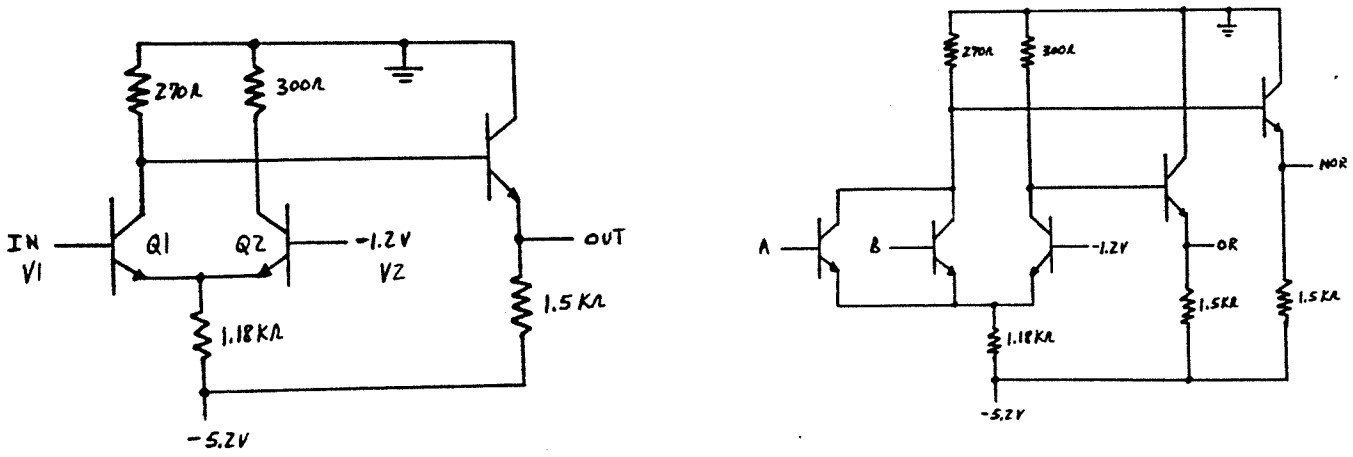


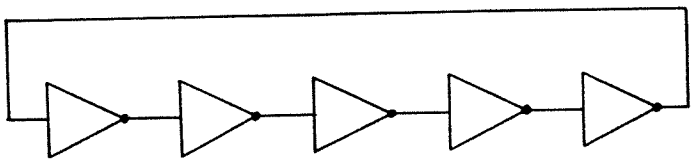
Figure 2: (a) Inverter (b) OR/NOR gate



This project involved the simulation, design, fabrication, and testing of ECL devices. The devices designed and built include an inverter, OR/NOR gate, ring oscillator, transistor, and base and emitter resistors. The ECL inverter design shown in Figure 2(a) is called a difference amplifier because of the output is proportional to the difference between the two input voltages V1 and V2, which is fixed at -1.2 volts. When V1 increases above -1.1 volts, the transistor Q1 turns ON and Q2 is off which causes the output to go LOW. Also, if V1 decreases to -1.3 volts, Q1 is off and Q2 is ON which causes the output to go HIGH. Except for a very narrow range of input voltages V1, the output takes on only one of two possible values and, hence, behaves as a digital circuit [3].

The OR/NOR gate designed is shown in Figure 2(b). The OR/NOR gate consists of three transistors plus another two transistors to correct for DC level shift. Note if Figure 2(b) that either the OR or NOR function can be utilized depending on where the output is taken from.

Figure 3: Ring Oscillator



The ring oscillator designed is shown in Figure 3. The ring oscillator is simply an odd number of inverters arranged with the input of one going into the output of another. The purpose of including a ring oscillator in the design was to determine the speed at which the ECL circuit operates.

EXPERIMENT

The wafers used for processing were p-type wafers with a 5um, 10 ohm/square epi layer. The Integrated Circuit Editor (ICE), an in house CAD tool, was used to design the layout of the devices. The layout of the design is shown in Figure 4. Reticles were made using the MANN Pattern Generator. Masks were generated on the MANN photorepeater.

The process consisted of five masking levels. The levels were for isolation diffusion, base diffusion, emitter diffusion, contact cuts, and metalization. Spin on dopants were used for all diffusion steps. The Kasper contact mask aligner was used with Kodak 820 as the photoresist.

The layout was designed based on a SUPREM simulation. In addition to information about junction depth and sheet resistance, SUPREM provided a base from which the fabrication process was developed. The wafers had 5300 angstroms of oxide grown on before isolation to mask the long boron diffusion step necessary for the complete isolation of the 5 micron epi layer. After the isolation regions were defined, the base regions were diffused using boron dopant as modeled by SUPREM. The emitter regions were then diffused using phosphorous dopant. The contact cuts were then made followed by aluminum evaporation and patterning. A final sinter step was performed for 30 minutes at 450 degrees celsius in a nitrogen environment to provide ohmic contacts. SPICE was used to model the logic devices designed. Because logic circuits were used, SPICE was used only to confirm the correct logic levels of the gates. The devices were tested on the HP 4145 semiconductor parameter analyzer.

RESULTS/DISCUSSION

The critical parameters obtained from SUPREM included junction depth and sheet resistance. The junction depth and sheet resistance after each hot process step are summarized in Table 1. The simulated junction depth was an important parameter to have when designing the circuit on ICE. The spacing between lines had to be large enough to compensate for lateral diffusion. Since the isolation diffusion went down 6 microns, it can be concluded that it will probably diffuse 3 microns laterally on each side of the lines.

The HP 4145 semiconductor parameter analyzer was used to test the devices with limited success. The large and small base resistors were determined to have resistances of 220 ohms (Figure 5) and 415 ohms (Figure 6) respectively. The emitter resistors were not isolated from the n-type epi layer so the values

Figure 4: ICE layout

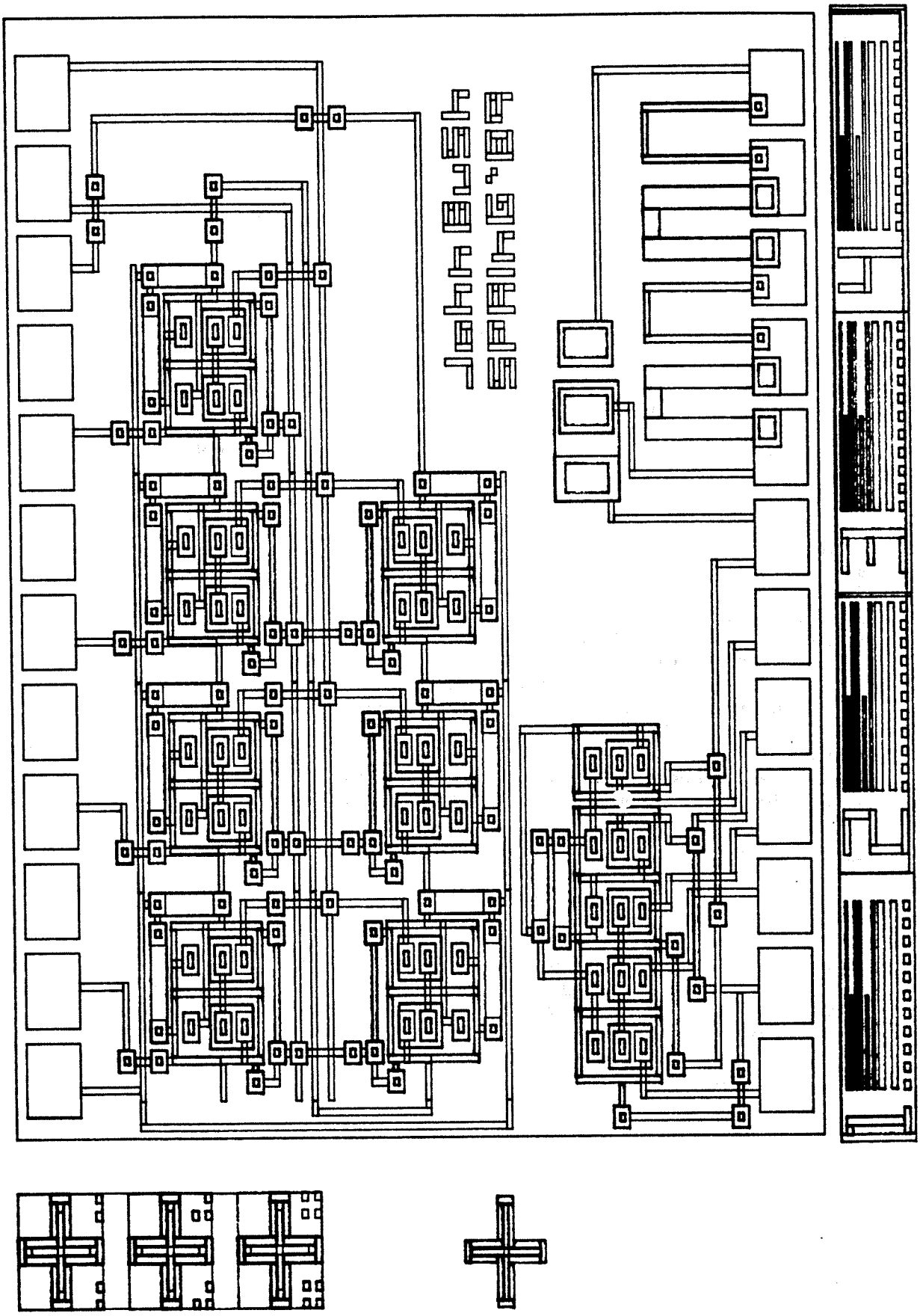
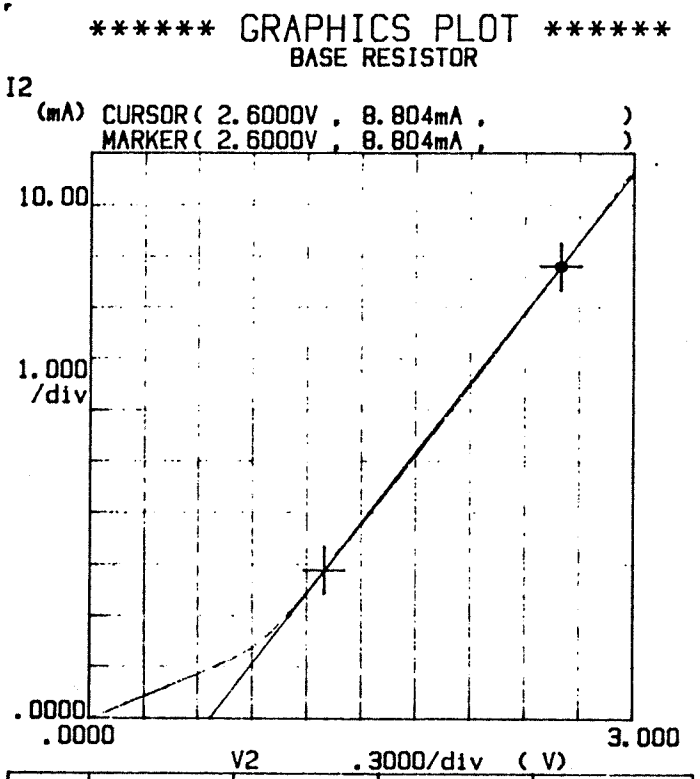
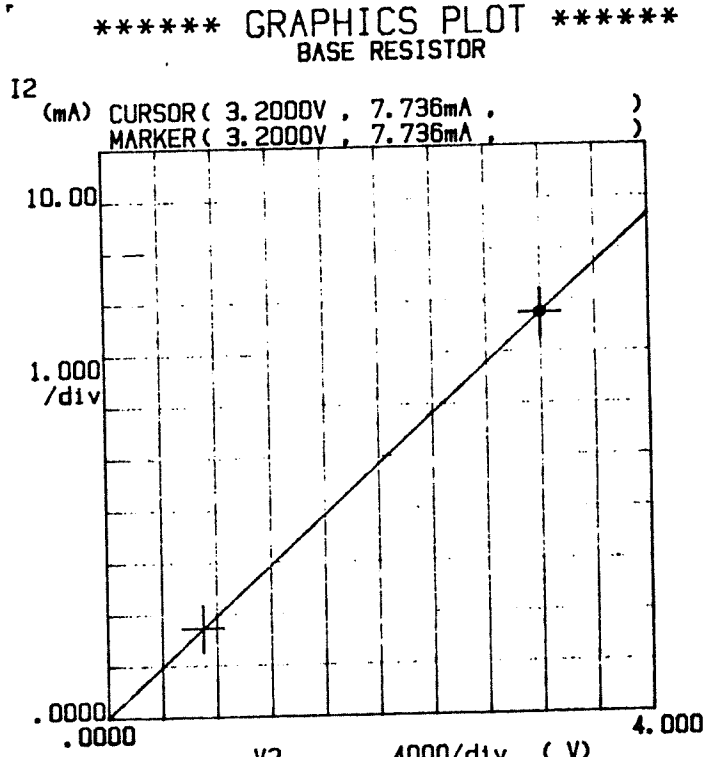


Figure 5: Large Base Resistor



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	4.55E-03	220E+00	665E-03	-3.03E-03
LINE2				

Figure 6: Small Base Resistor



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	2.41E-03	415E+00	-11.0E-03	26.5E-06
LINE2				

Table 1: SUPREM values for junction depth and sheet resistance

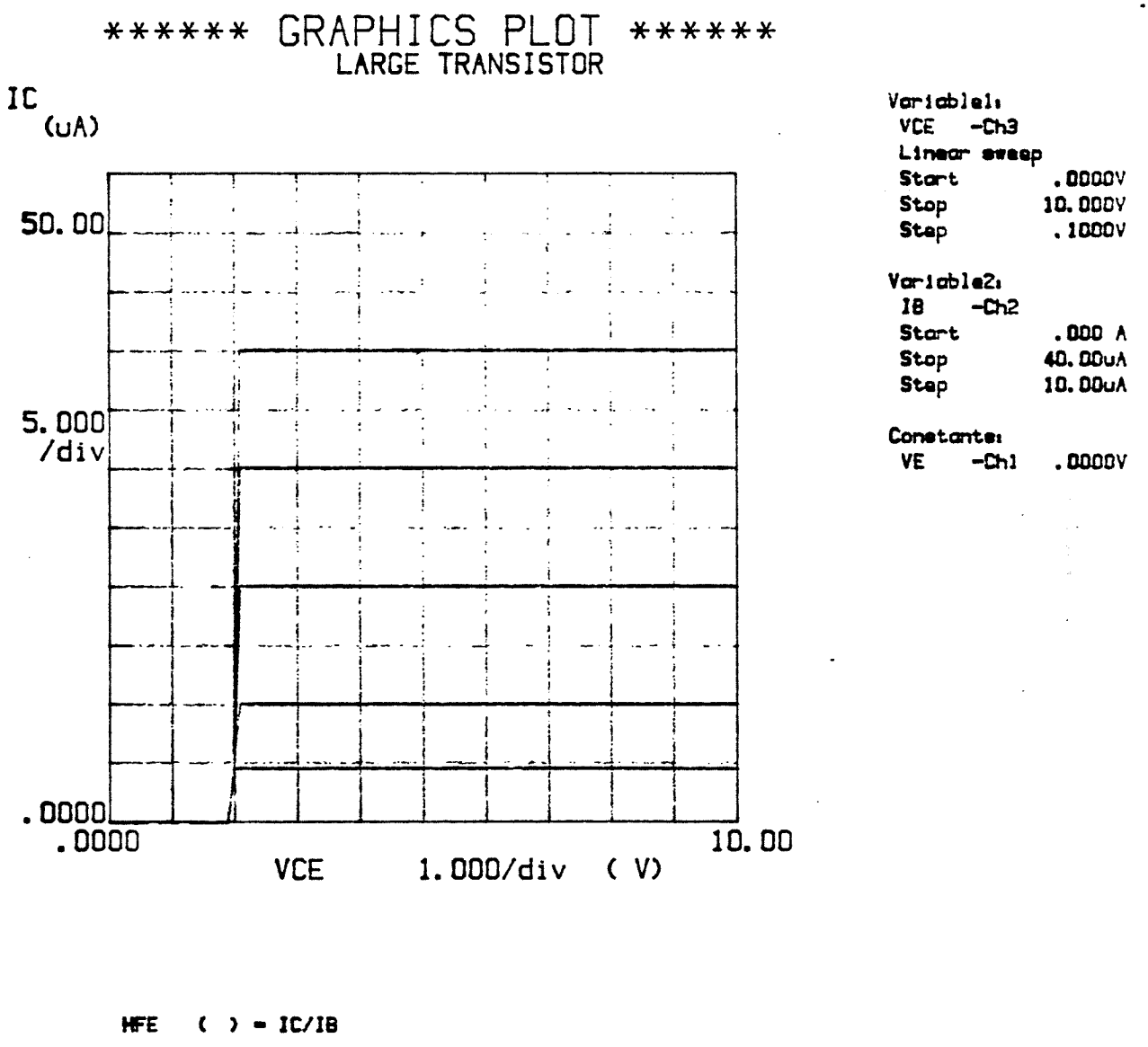
Hot Process Step	Isolation Xj Xj/PHO	Base Xj Xj/PHO	Emitter Xj Xj/PHO
Isolation Diffusion	5.25 1.31	---- ----	---- ----
Base Oxide	5.52 1.50	---- ----	---- ----
Base Diffusion	5.52 1.60	1.02 16.7	---- ----
Emitter Oxide	5.79 1.77	1.94 28.0	---- ----
Emitter Diffusion	5.77 1.86	2.98 154.2	0.95 17.6
Contact Cut Oxide	6.02 2.02	3.73 2081	2.23 11.32

obtained did not correspond to those for which they were designed. A large npn transistor was tested and determined to have a gain of one. The characteristic for the npn is shown in Figure 7. The low gain from the transistor may indicate a problem with the quality of the diffusion steps. Spin on dopants were used in the fabrication process because of the time factor involved in using solid sources. The use of solid sources is recommended in the future to obtain more pure and uniform diffusions. Another reason for the low gain is that a subcollector implant was not performed. A subcollector implant would have lowered the collector resistance and thus increased the gain. The testing of the ECL gates was attempted but with no success. However, it was not concluded that gates lacked the potential to work. Because a probe card was not available, the logic analyzer could not be used. The use of the logic analyzer is almost a necessity when testing ECL gates because of the power supplies needed. Perhaps further testing on the logic analyzer would produce working gates. The quality of the diffusions was again in doubt when testing the ECL gates. Future ECL work should include designs with more test devices so that it could be determined if the circuits would work without actually testing them. The area needed for the additional test structures could be obtained by increasing the size of the chip used.

CONCLUSIONS

The project produced working resistors and a working bipolar npn transistor with a gain of one. The low gain was concluded to be the result of a problem with the quality of the diffusions.

Figure 7: Transistor Characteristic



Also, it was noted that a subcollector implant was not performed. A subcollector implant would have lowered the collector resistance and thus increase the gain of the transistor. The ECL gates were unable to be properly tested due to a lack of a probe card for the logic analyzer. Suggestions for future work include using a pad configuration which corresponds to an existing probe card and performing a subcollector implant.

ACKNOWLEDGMENTS

Mike Jackson for his ideas on the project and for his help in presenting the work, and Scott Blondell for his efforts keeping the equipment operating.

REFERENCES

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