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Development of High Efficiency III/V Photovoltaic Devices

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Development of High Efficiency III/V Photovoltaic Devices

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

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Development of High Efficiency III/V Photovoltaic Devices
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Committee Approval:

We, the undersigned committee members, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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ABSTRACT

Kate Gleason College of Engineering
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Degree: Doctor of Philosophy **Program**: Microsystems Engineering

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Dissertation Title: Development of High Efficiency III/V Photovoltaic Devices

Developments of photovoltaic (PV) devices are driven by increasing needs for economically competitive renewable energy conversion. To improve the efficiency of PV devices for outdoor applications, the concept of intermediate band solar cell (IBSC) has been proposed to boost the conversation efficiency to 63% under concentrated suns illumination, which requires two-step photon absorption (TSPA) dominates among other competing processes: carrier thermal escape, tunneling and recombination. To optimize the design of III-V QD-IBSCs, first, the effect of electric field on band structure and carrier dynamics and device performances were quantitative investigated via simulation and experiments. Second, to experimentally increase TSPA at room temperature, novel QD systems related QD-IBSCs were designed, fabricated and characterized. The InAs/$Al_{0.3}$GaAs QD-IBSC shows high TSPA working temperature towards 110K, promising for a room temperature IBSC under concentrated sunlight. Alternative QD systems including GaSb/GaAs and type II InP/InGaP were also investigated via band structure simulations. Meanwhile, developments of PV devices under indoor low intensity light (0.1 $\mu W/cm^2$-1 mW/cm^2) illumination not only enable long lifetime radio-isotope based batteries, but also, more important for the daily life, have the potential to promote an emerging market of internet of things by efficiently powering wireless sensors. Single junction InGaP PV devices were optimized for low intensity light sources using via simulations and statistical control. To reduce the dark current and increase the absorption at longer wavelengths (>550 nm), several parameters including doping and thickness were evaluated. The experimental results on the devices show higher conversion efficiencies than other commercial PVs under varied indoor light sources: 29% under 1$\mu W/cm^2$ phosphor spectrum and over 30% efficiency under LEDs illumination. In addition, the work includes developments of InAs nanowires epi-growth for PV applications. Several marks for selective area growth were successfully made.

DEDICATION

To my family

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I have hesitated in writing these acknowledgements towards the end of the wonderful trip in the RIT nano-PV group, for the difficulty in adequately expressing what should be said and inevitability of forgetting someone or some contributions. I must apologize in advance then, for anyone I have left out. You are not forgotten, merely out of mind for a short moment.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 Quantum dot intermediate band solar cell

The development of photovoltaic (PV) devices is driven by the increasing need for economically competitive renewable energy conversion. Back to 1961, based on the detailed balance calculations, Shockley and Queisser found a power conversion efficiency limit of 30% in a single junction solar cell [1] under one sun illumination. Nowadays, under one-sun air-mass 1.5 (global) (AM1.5G) spectrum (a standard reference of the sun spectrum filtered by the earth's atmosphere [2]), the laboratory record efficiencies for Si is 26.7% [3], while the highest efficiency record is 28.8% with a GaAs single junction solar cell [4]. Figure 1.1 shows a modified efficiency versus cost plot (original by Martin Green UNSW [5]). The commercial PV is still dominated by Si based solar modules, while the next generation PV technologies, including nanostructured solar cells, are required to further promote PV terrestrial and space applications.

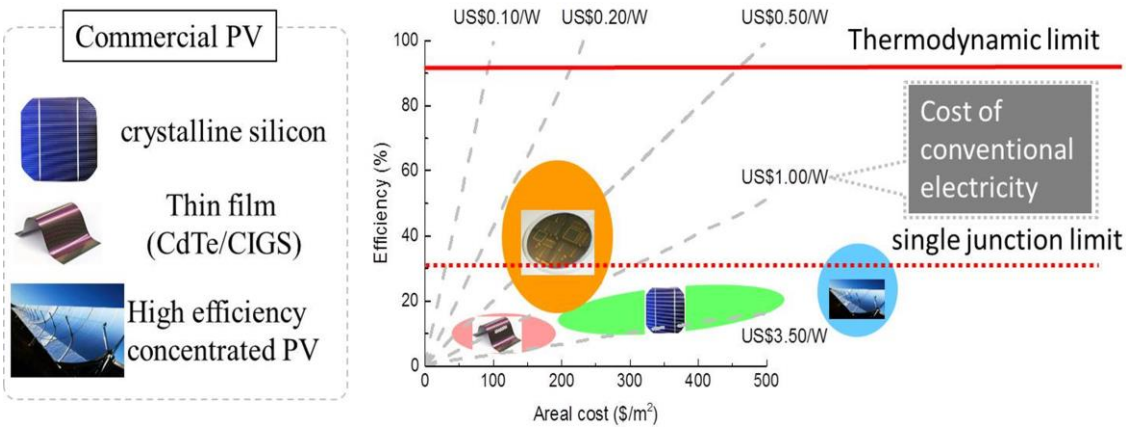

Figure 1.1 Relationship between power conversion efficiency and module area cost. The red dotted horizontal line is the Shockley–Queisser limit for single-junction devices. Orange circle shows that RIT PV group is mainly working on the next generation PV devices.

Commercially feasible method to exceed a single junction PV device detailed balance limit is to stack several different semiconductor materials with increasing bandgap to reduce losses from transmission and themalization [6], which refers a multi-junction PV device [7]. So far, the most common multi-junction PV devices are three-junction devices made from InGaP/(In)GaP/Ge with a record efficiency of 34.5% [3] under one sun AM1.5G illumination. Figure 1.2 shows a simplified triple junction PV device diagram and its equivalent circuit. The highest energy photons, shown in purple and blue, are absorbed in the top junction with the largest bandgap (E_{g1}), while lower energy photons, shown in green and yellow, are absorbed in the middle junction with a lower bandgap (E_{g2}), and so on. However, those photons with energy lower than the bottom junction bandgap (E_{g3}) cannot be collected because of transmission loss. The PV device is a set of three diodes in series, so the short-circuit current is limited to the junction with smallest current, while the open circuit voltage correlates the sum of each junction's bandgap.

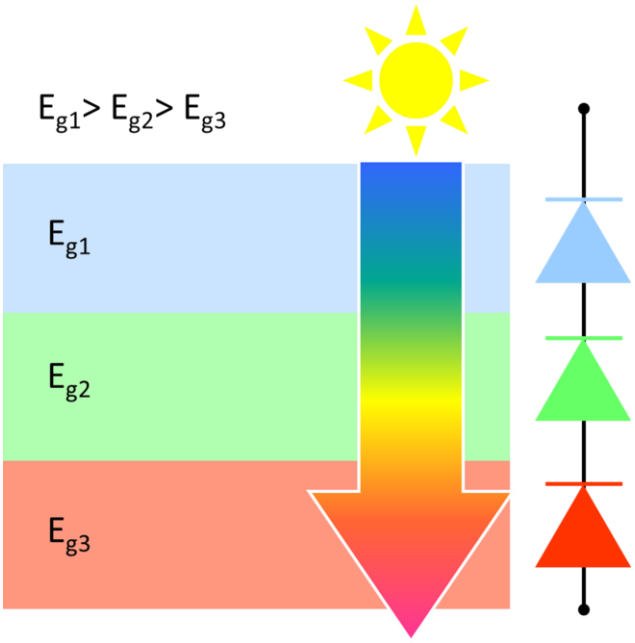

Figure 1.2 Simplified diagram of a triple junction solar cell and its equivalent circuit.

However, in order to improve the efficiency of PV devices within a single junction for outdoor applications, a concept of intermediate band solar cells (IBSCs) has been proposed to boost the solar cell efficiency to 63% under concentrated illuminations by two-step-photon absorption (TSPA) [8]. Figure 1.3(a) shows a simplified band structure of an ideal IBSC. By inserting a third quasi-Fermi level IB between the original conduction band (CB) and valence band (VB), the solar cell is essentially like a set of diodes in series (VB-IB, IB-CB) with a parallel diode (VB-CB), as shown in Figure 1.3(b), which increases current output while preserving the voltage from the bandgap of the host bulk semiconductor. III-V quantum dot (QD), as one of the materials to form an IB, has been extensively studied recently [9]–[14], due to their discrete density of states that reduce thermal coupling and less angular dependent absorption than the quantum well IBSC [15], [16].

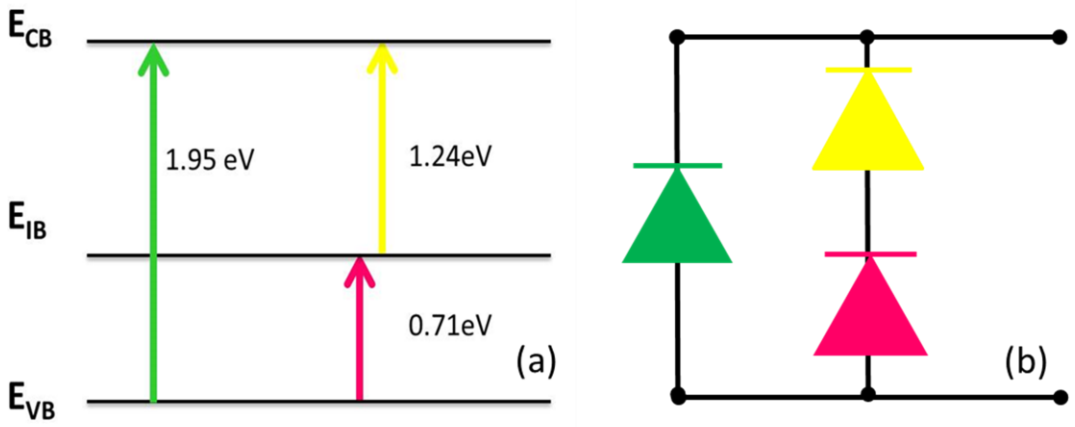

Figure 1.3 (a) Simplified band structure of an ideal intermediate band material under illumination, the bulk band-gap photon absorption process is green arrow (Band-gap is 1.95 eV to maximize the efficiency). The sub-band-gap optical transitions of VB-IB (0.71 eV) and IB-CB (1.24 eV) are in pink and yellow arrows, respectively. (b) Simplified equivalent circuit of the IBSC.

The main challenge of room temperature IBSC is to enable TSPA to dominate from an IB among other competing processes including thermal escape, tunneling and recombination as shown in Figure 1.4. An increased short circuit current from the VB-IB transition via thermal escape or tunneling will result in voltage degradation [17], while recombination process fundamentally reduces photon to carrier conversion efficiency. To enhance the TSPA in QD-IBSCs at room temperature, it is important to study the parameters (including electric field, barrier height and etc.) that affect the TSPA. Furthermore, updated designs of QD-IBSCs should be proposed, fabricated and tested to towards realization of this high efficiency IBSC concept at room temperature.

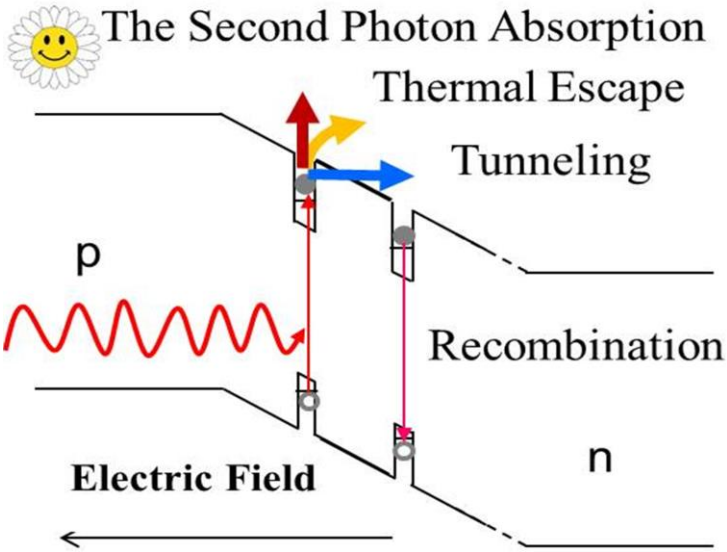

Figure 1.4 Simplified band diagram of a *p-i-n* solar cell under illumination with several competing processes: TSPA, tunneling, thermal escape, and recombination) in an IB formed in QDs layer and its barrier.

1.1.2 Low intensity light energy harvesters

Figure 1.5 shows PV devices as low light energy harvesters have drawn attention because of an increasing need for constant powering indoor wireless systems/sensors, which enable the data collection and exchange for internet of things applications [18]. The typical spectrum for indoor low power light sources, including LED and fluorescent tubes, is between 400-700 nm. Due to a wide and direct band gap introduced strong absorption, InGaP PV devices have been theatrically predicted as the best indoor light power converters (an efficiency towards 60% for a white LED combined with red, green and blue LEDs [19]). However, it still requires experimental investigation on the parameters (carrier lifetime, doping, thickness and etc.) to optimize design for high efficiency InGaP energy harvesters under low power illumination (1μW-10 mW) [20].

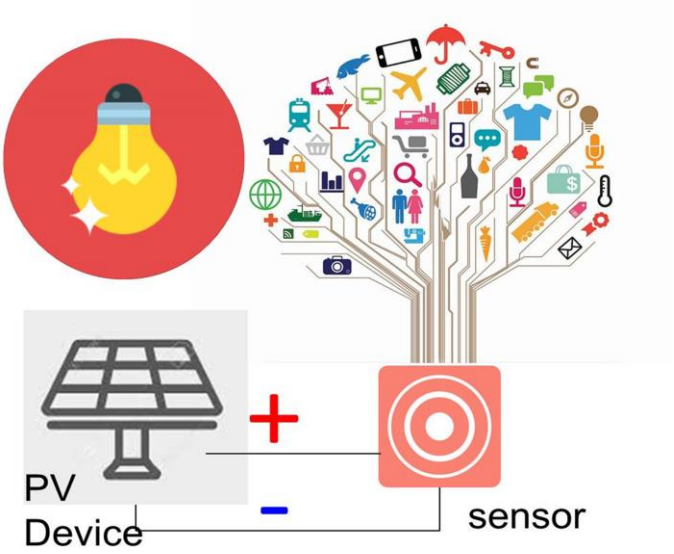

Figure 1.5 Sketch of using PV devices to power wireless systems and sensors for internet of things applications

1.1.3 Nanowire epitaxy via for PV application

Additionally, InAs nanowires for PV devices applications are promising to enhance light absorption by light trapping [21]. Furthermore, the cost of the substrate is 84% [22] in a GaAs solar cell without reusing substrate, which dominates over Metal-Organic Chemical Vapor Deposition (MOCVD) and device processing. Due to the volume strain relaxation [23], InAs nanowires can be grown different substrates including silicon [24]–[26], which reduces the cost of the PV devices substrate. Moreover, similar to the III-V QDs, when the diameter of nanowire reduces to 25 nm [27], the absorption edge extends below the band gap of the host material because of the quantum confinement. To finally incorporate nanowires into PV devices or any optoelectronic devices, it is important to optimize InAs nanowire epi-growth via MOCVD.

1.2 Objectives

The specific objectives of this thesis include:

- Investigate the effect of electric field on carrier dynamics of the InAs/GaAs QD-IBSC.
- Update the design of the QD-IBSC to increase the probability of TSPA by using barrier modification. Fabricate and characterize the devices with updated design.
- Update design of InGaP PV devices for low intensity light applications by adjusting parameters, including doping, thickness, antireflection coating.
- Fabricate the updated InGaP PV devices, evaluate the performance and demonstrate pathways for a higher efficiency.
- Design masks for the InAs nanowire selective area growth.
- Characterize MOCVD InAs nanowires growth results

1.3 Approaches

1.3.1 Test

To realize the listed research objectives, Figure 1.6 shows a cycle chart of research approaches, involving test, analysis, update design and fabrication. Each research project starts with existing testing PV devices or structures in the nanopower research lab, in order to be familiar with instruments for measurements and collect relevant data for further analysis. The test also associates design of experiments (DOE) and testing stage built-up. The experimental set-up details are discussed in Chapter 2. Here, in general, the performances of PV devices are evaluated via external quantum efficiency (EQE) measurements, dark and light current and voltage (I-V) characteristics. Capacitance-voltage (C-V) measurements are conducted for detect the doping profile in the PV

devices. Electroluminescence (EL) is used to characterize the optical transition in devices, while photoluminescence (PL) can be applied with both devices and test structures to determine the band-gap or sub-band-gap confined energy level. Hall measurements are used to detect doping calibration material quality (including mobility and doping concentration) grown by MOCVD.

More specifically, for QD-IBSC related projects, temperature dependent external quantum efficiency (TDEQE) or photoluminescence are involved to calculate the activation energy from the QD confinement. Time-resolved photoluminescence (TRPL) measurements are used to extract the lifetime of the radiative recombination process. Two photon absorption photocurrent experiments with two light sources are used to detect the optical transition from an IB. For low intensity light PV InGaP devices, reflection test are used to evaluate the performance of front surface anti-reflection coating. Light I-V measurements under low intensity artificial light (~$\mu W/cm^2$-mW/cm^2) are used to demonstrate the device performance for low power light application. For InAs nanowires MOCVD growth optimization, scanning electron microscopy (SEM) is employed to check the morphology. Transmission electron microscopy (TEM) is used to further examine the nanowires crystal quality.

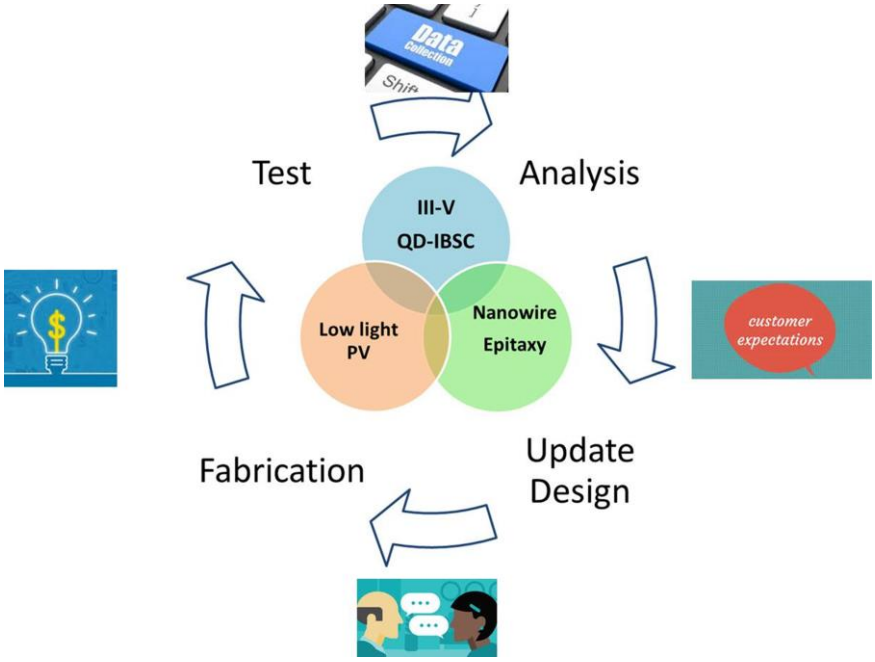

Figure 1.6 Cycle chart of summary of research and approach

1.3.2 Analysis

After data collecting from the test, data analysis is completed by two steps: first, compare the experimental results to related state-of-the-art literatures, which provides background information and helps to assess performance of the measured devices. Second, compare the experimental results to the theoretic predictions to understand device physics before adjusting parameters that influence performance of the. The PV devices' performance, including short circuit current, open circuit voltage, fill factor and efficiency, can be estimated via simulations from Sentaurus TCAD [28]. The Sentaurus software device simulation is physics based by solving Poisson equation and drift-diffusion equation across a PV device length, which is used to generate the initial simulation through customized list of input parameters. Band structure of varied III-V QDs can be calculated via the eight-band ***k·p*** calculations from either homemade C^{++} code or commercial software (Nextnano [29]). The detail of the eight-band ***k·p***

calculations is discussed in Chapter 3. Dark and light IV experimental curves can be fitted with a double diode equation to extract the reverse saturation current and ideality factor, which associate different recombination processes under different operation regions. Growth results of QD or nanowire should follow the diffusion and nucleation processes that depend on III/V ratio, temperature, precursor and etc.

1.3.3 Update design

Based on the test results analysis, as an engineer and researcher, an updated design should be proposed to meet research expectations and goals within certain time frame and cost to improve device performance. Generally, because of dealing with photons and minority carriers, PV devices design is an optimization between absorption and recombination within limited resources (material selection, epi-growth tool and etc.). Specifically, the design of III-V QD-IBSCs is via barrier modification method [30] and adjusting the electric field around QD layers to increase TSPA working temperature. Different from QD-IBSCs illuminated under sun spectrum, as shown in Figure 1.7, the various indoor spectrum on low light PV devices are usually between visible region (400-700 nm) [31], so the design of InGaP PV devices is to reduce front surface reflection, as well as, based on the Epi-growth capability related material selection and quality, to maximize the efficiency within varied indoor spectrum intensity (power limited to 1 $\mu W/cm^2$-10 mW/cm^2). The optimization of InAs nanowires growth is to grow uniform nanowire (with or without a mask) on a large area (> 1×1 mm^2) on a (111) GaAs substrate.

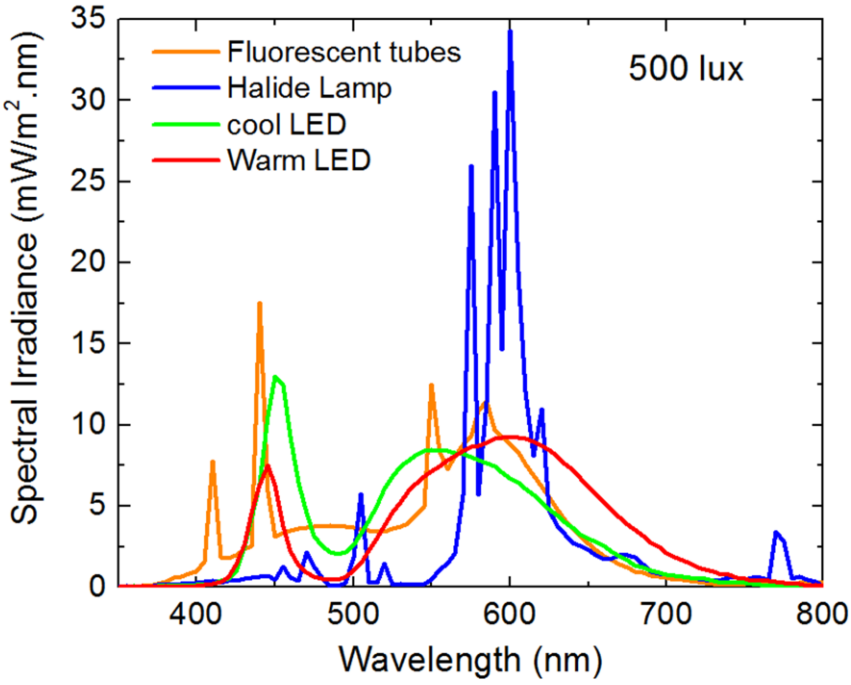

Figure 1.7 The spectral irradiance E(λ) of various indoor illuminants scaled to 500 lux.

1.3.4 Fabrication

It is well known that fabrication is critical to transform ideas to reality in semiconductor research. However, updated III-V designs are stacked with semiconductor materials grown by MOCVD. As mentioned, material quality determined minority carrier lifetime and diffusion length are crucial to the PV devices performance, so before device fabrication, good communications or discussions with experts on MOCVD benefit to the final products.

Once the epi-growth is completed, the PV devices were fabricated with designed mask, metal contact, and anti-reflection coating at RIT semiconductor & microsystems fabrication laboratory (SMFL). Figure 1.8 shows details of a standard fabrication procedure of III-V *p-i-n* PV devices and a two inch GaAs wafer after fabrication. Acetone and isopropyl alcohol (IPA) were used for wafer clean. Microchem lift-off resist

(LOR) 10A and Microposit S1813 photoresist were applied to wafers front side before baking. Followed exposure process was completed via Suss MA 56 contact mask aligner. Dipeptidyl peptidase-4 (CD26) was used to develop the photoresist. A p-type doped GaAs Ohmic contact was achieved with Lesker Nano38 physical vapor deposition (PVD), while n-type doped GaAs Ohmic contact was completed via Lesker PVD 75C. MicroChem Remover PG was used for a metal lift-off process of the front size. Chemicals for mesa etch and contact etch were varied in different device structures. Electron patterns on SiO_2 layer for the InAs nanowire selective area MOCVD growth were completed in Cornell Nanoscale Science and Technology Facility. Finally, all the updated designs are re-evaluated with test and analysis into a new loop to further push the research products efficiency or performance forward.

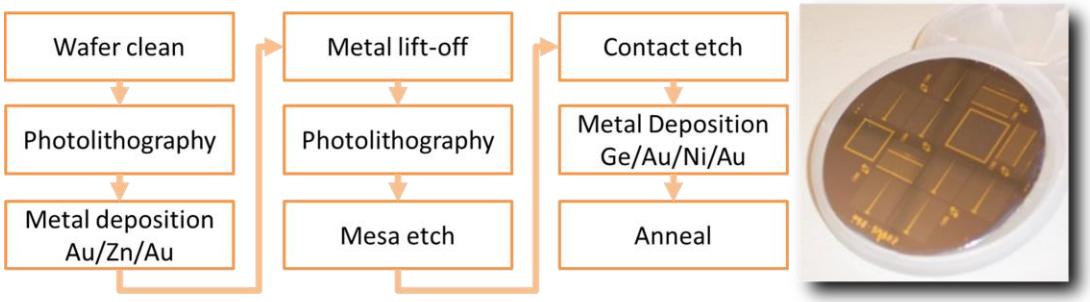

Figure 1.8 (left) The simplified fabrication process flow chart of *p-i-n* PV devices. (Right) A picture of a two-inch wafer consisted of thirteen PV devices with varied

1.4 Research works accomplished

1.4.1 Development of QD-IBSC

❖ **Carrier dynamics study in QD-IBSC**

Multiple InAs/GaAs QDSCs with varied layer structure were fabricated and characterized. The effect of electric field on carrier dynamics including escape, radiative recombination and TSPA were investigated. Results showed that increasing the electric

field enhances carrier escape by lowering the effective barrier height and accelerating tunneling, while increasing the electric field also extends the radiative recombination lifetime in the ground state of the QDs as a consequence of the reduced wave-function overlap between the electrons and holes. The balance of carrier escape and recombination determines the probability of TSPA.

- **Barrier modification for high working TSPA temperature**

Furthermore, simulated, designed, fabricated, characterized and analyzed novel QD-IBSCs with barrier modifications, mainly involving InAs/$In_{0.5}GaP$ and InAs/Al_xGaAs systems, for higher conversion efficiency and working temperature of TSPA. Based on the simulations and experimental results, three areas for improvement can be addressed. First, the first step of two-step photon absorption (between the deep confined levels) should be enhanced to improve TSPA by increasing carrier concentrations in an IB. The increment of carrier concentration in an IB can be achieved by increasing incident light intensity, improving QD surface density, the number of QD layers, and photon recycling [32]. Second, the QD capture process affects carrier collection and distribution in a given QD layer. Novel QD systems like InP/$In_{0.5}GaP$ [33] or GaSb/Al_xGaAs could be used to reduce the hole or electron capture and recombination in the QDs, respectively, by careful QD growth optimization and device design. Third, efficient TSPA requires a reduced recombination rate and escape rate. To balance the effect of electric field and finally achieve a high efficiency room temperature IBSC, it is important to investigate the magnitude of the electric field required at P_{max} condition for a specific design in order to achieve a photon ratchet for a given IBSC design [34], [35].

❖ **Development of fabrication process (1-dimensional patterning)**

Additionally, to improve QD absorption within a limited number of layers and surface density, a lithography and wet etching process for one dimensional (Al)GaAs back surface patterning was developed. Characterizations show the patterned structure enhanced light trapping by switching directly reflection to diffusive reflection from the patterned surface.

1.4.2 Development of InGaP low light PV devices:

Single junction InGaP PV devices for low intensity light applications were simulated, designed, fabricated and characterized. Doping, thickness, layer sequences were modified based on the RIT MOCVD growth capability and the required working spectra. Statistical analysis was applied to evaluate different parameters effects on device efficiency. The final experimental results show reduced front surface reflection (below 1% between 450-700 nm) using MgF_2/ZnS as anti-reflection coating. The experimental efficiency under required 523 nm centered green phosphor (~1 $\mu W/cm^2$) is consistent with simulation (efficiency of 29%). Under the order of 1$\mu W/cm^2$ incident lights intensity, the designed InGaP devices are with an open circuit voltage toward 1 V. Also the designed InGaP PV devices also show high conversion efficiencies under indoor light illumination (efficiency under cold/warm LED > 30%). Side wall passivation during the fabrication and epi-growth related crystal quality can be further optimized to improve the InGaP devices performance for low intensity light energy harvesters.

1.4.3 Development of InAs nanowire epi-growth on GaAs

InAs nanowires grown by MOCVD on (111)B GaAs substrates were characterized and analyzed. Different masks (electron-beam and anodic aluminum oxide) for Au

nanoparticle patterning and nanowire selective area growth were successfully developed. The growth results of InAs nanowires with the masks are also demonstrated, indicating that a finer tuning of growth temperature, III-V ratio during the growth for a specific mask design are required for InAs nanowire growth optimization. In additional, selective area-MOCVD of InAs nanowires using a PS-b-PMMA diblock copolymer nano-patterning technique were evaluated via TEM measurements [36]. The TEM measurements indicate that fully strain-relaxed catalyst-free InAs nanowires were achieved with interfacial misfit dislocations near the growth interface, but otherwise appear to be threading dislocation-free while exhibiting twin defects in a primary zinc blend crystal structure.

1.5 Organization of Dissertation

Chapter 1 is an introduction to this dissertation, which briefly discusses on the importance and challenges in the research works including QD-IBSCs, low light InGaP PV devices, and InAs nanowire epi-growth optimization. Chapter 1 also clarifies the motivation, objectives and research approach for each project. The completed research works are also listed in Chapter 1.

Chapter 2 demonstrates the investigation of electric field effect on carrier dynamics in InAs/GaAs QD-IBSCs. The importance to investigate the effect of electric field on the InAs QD-IBSCs is addressed by literature review. In order to optimize the TPSA for future designs of the QD-IBSC, results of simulations and experiments were combined to quantify the effect of electric field on the barrier height and the carrier escape from QDs in the investigated five-layer InAs/GaAs QDSCs. The electric field dependent effective barrier heights for ground state electrons were calculated using eight band ***k•p*** theory at

short circuit conditions. TDEQE measurements were performed to verify that the increasing electric field decreases the effective barrier height. Additionally, the electric field dependent radiative lifetimes of the ground state were characterized with TRPL experiments. The increasing electric field extended the radiative recombination lifetime in the ground state of the QDs as a consequence of the electric field reduced wave-function overlap between the electrons and holes. TSPA intensity has a maximum at 0.5 V bias (QD local E-field ~7 kV/cm) in the investigated InAs/GaAs QDSC.

Chapter 3 focuses on the development of QD-IBSCs via barrier modification in order to improve the high temperature TSPA and efficiency. Methods to enhance TSPA in the QD-IBSCs are presented. Barrier modifications with various QD systems were discussed with band structure simulation. Experimentally, the performance of InAs/InGaP QDSCs is examined via external quantum efficiency measurements with varied external bias condition and temperature. The temperature-dependent and voltage bias-dependent two-step photon absorption processes were investigated in the MOCVD-grown InAs/GaAs/$Al_{0.3}$GaAs Dot in a well (Dwell)-IBSC. TSPA is sensitive to the incident photon density because of varied optical extraction rate. Due to the limited QD ground state absorption resulting from low QD surface density, QD ground state TSPA was not observed at low incident photon density, though could be improved by increasing incident photon density (sun concentration). Instead, TSPA was observed from shallow confined levels formed by the $Al_{0.3}$GaAs/GaAs wells, which is mainly due to the combination of enhanced absorption and charge separation. The enhanced absorption of the wells introduces higher carrier concentrations in the shallow confined levels, and the charge separation results in longer radiative lifetimes.

Chapter 4 shows the design and development of single junction InGaP PV devices for low intensity light applications. The fabricated single junction InGaP photovoltaic devices show overall 30% conversion efficiency under 1.27 $\mu W/cm^2$ illuminations. The development not only enables long lifetime radio-isotope based batteries but also, more important for the daily life, has the potential to promote the concept of the internet of things by efficiently powering indoor wireless sensors. To reduce the dark current and increase the absorption at longer wavelengths (>550 nm), several parameters including doping and thickness are optimized for the device design. Additional current-voltage characteristics under dark conditions and external quantum efficiency were also performed in order to evaluate the performance of the InGaP photovoltaic cells.

Chapter 5 states the development of InAs nanowire growth via MOCVD for PV applications. It firstly introduces the benefits to utilize InAs nanowire in PV devices. The growth details of InAs nanowire with/ without Au seed are demonstrated. SEM was used to characterize the pattern and InAs nanowire growth results. The anodic aluminum oxide membranes (AAO) [37] were used to pattern Au seed and the InAs nanowire. The AAO mask was successfully pattern the Au seed on the GaAs surface. Due to the fast growth rate of the MOCVD, it is required a finer tuning on the nucleation and growth of the InAs. As an alternative method to complete selective area growth of the InAs nanowires, the details of the E-beam mask design and the fabrication process of the pattern are described. The evaluations on the growth results of InAs nanowire surface morphology via E-beam the patterning are also included. Additionally, Chapter 5 discusses crystal structures of catalyst-free MOCVD grown InAs via di-block copolymer patterning.

Chapter 6 summarizes conclusions of the research on III-V PV devices and provides the future outlook of development of III-V nanostructured IBSCs and PV devices towards commercial applications.

Chapter 2

Effect of electric field on InAs/GaAs QD-IBSC

2.1 Introduction

The concept of intermediate band solar cells (IBSC)[38], [39] has been proposed as a method of achieving a conversion efficiency of 63% with maximum concentrated light illumination using detailed balance calculations. Between the conduction band (CB) and the valence band (VB), the ideal intermediate band IB is a band that is partially filled with electron in quasi-thermal equilibrium to support sequential optical absorption.[10] The IBSC enables two-step photon absorption (TSPA), as shown in Figure 1.3, first an optical transition from the VB to the IB followed by an optical transition from the IB to the CB, so the IBSC increases output current by extending the absorption to sub-band-gap photons. Consequently, the IBSC operates as three current sources: two in series (VB-IB transition and IB-CB transition) are in parallel with the original bulk diode (VB-CB transition). This allows the IBSC to maintain the voltage output of the bulk host material. So far, quantum dots QDs have been considered as one of few materials systems to form an IB for the realization of IBSC concepts.[10] The confined levels of QDs can be tuned by varying QD size, or through selection of QD or barrier material. A zero density of states between the confined states of electrons reduces the thermal coupling, helping to facilitate the two-photon-absorption process. Due to mature growth techniques in metalorganic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE), GaAs solar cells with embedded InAs-GaAs quantum dots (QDs) in the intrinsic region have been widely studied.[17], [40]–[42]

Many studies have shown enhanced sub-band-gap carrier collection in InAs/GaAs QDSCs.[17], [42], [43] However, if the increase in current from the VB to IB transition occurs by either thermal escape or tunneling, the open-circuit voltage of the host material is sacrificed because of coupling between the IB and CB. To maintain the voltage of the bulk material (also known as a voltage preservation), the IB should be completely separated from the CB and the second photon absorption (transition from the IB to CB) should be the dominant process of the carriers in the IB.[17] To enable quasi-Fermi level splitting between IB and CB, thermal escape should be suppressed. Therefore, although experimental observation of the second photon absorption has been observed at both low temperature[44]–[46] and room temperature[9], [47], [48], the voltage preservation so far has only been shown at low temperature.[49], [50]. To increase the sub-band-gap carrier collection via the second photon absorption, other competing process including thermal escape, tunneling and recombination must be reduced.

Because the QDs are usually embedded in the intrinsic regions of the diode, they exist within an electric field formed by the built-in potential that is then affected by external bias. It is important, therefore, to investigate the effect of electric field on carrier escape and radiative recombination. Many published studies have investigated the effect of electric field on the QD-IBSC. Antolin *et al.* demonstrated that an electric field (>100 kV/cm) enhanced tunneling escape of carriers and demonstrated suppressed tunneling through application of a thick GaAs spacer layer between QDs in InAs/GaAs QDSCs.[17] Because the thick spacer layer limited the number of QD that could be grown in the intrinsic region, Ramiro *et al.* further improved the spacer layer design by inserting a field damping layer to reduce the electric field to 47.5 kV/cm and observed

that voltage preservation toward GaAs bandedge can be achieved even if tunneling exists at short circuit conditions.[50] Elborg *et al.* experimentally revealed that a maximum in TSPA occurred at a reverse bias of -0.3 V in GaAs/AlGaAs QDSCs.[51] Creti *et al.* demonstrated that the effect of electric field on electron-hole separation along the growth direction can be used to preserve TSPA up to room temperature.[45] Kasamatsu *et al.* has shown that a strong internal electric field of 193 kV/cm severely reduces the radiative lifetime of the ground state carriers thereby quenching TSPA in InAs/GaAs QD-IBSC, but internal electric fields on the order of 10 kV/cm reduces tunneling-assisted electron escape rate. The interval electric fields on the order of 10 kV/cm also maintains QD electronic coupling (wave-functions overlap between different stacking layers of QD along the epi-growth directions)[52], which enable to form superlattice minibands [53] with enhanced TSPA towards 60K in a close stacking InAs/GaAs QD-IBSC [54].

Obviously, the electric field significantly affects TSPA efficiency and the performances of QD-IBSCs. However, the effect of electric field on the other more dominant mechanisms of carrier escape and recombination has not yet been fully understood and published, especially with regard to the barrier height and the radiative lifetime. In this work, quantitative analysis of the effect of electric field on thermal escape and tunneling escape in five-layer QDSC structures is presented. The simulations of the QD band structures using the eight-band $k \cdot p$ theory is corroborated with temperature dependent external quantum efficiency (TDEQE) measurements to characterize carrier escape from the QDs. Time-resolved photoluminescence (TRPL) experiments were also applied to detect the electric field dependent radiative recombination dynamics.

2.2 Sample and experiment

Three QD embedded *p-i-n* GaAs solar cell samples with a varied local electric field of QDs were prepared and studied. The structures were grown on a 350 μm thick Si-doped GaAs (100) substrate misoriented 2° toward to the [110] direction, using a low-pressure rotating disk metal organic vapor phase epitaxy (MOVPE) reactor (Veeco D125LDM) [55]. After growth of a low temperature GaAs capping layer, temperature was ramped to 585ºC for the growth of the GaAs spacer layers and a thin (1.1-1.4 nm) GaP strain compensation layer. The average size of hemisphere-shaped QDs, measured via atomic force microscopy (AFM), is 3-4 nm in height and 20-25 nm in diameter [56]. As shown in Figure 2.1, three separate devices with a five-layer superlattice of QDs were grown in the 600 nm (unintentionally n-type doped 1×10^{16} cm^{-3}) intrinsic region of a pin GaAs solar cell, each with the QDs in different locations, emitter shifted (33 nm towards the p-emitter), at the center or near the base (33 nm towards the n-base). Thin (50 nm) InGaP front and back window layers are employed to reduce surface and interface recombination. The emitter consisted of 500 nm of Zn-doped GaAs with a doping density of 2.2×10^{18} cm^{-3}. Finally, a heavily doped GaAs contact layer was used for ohmic contact formation, which was etched after self-aligned to the metallization to eliminate parasitic absorption effects. Solar cells were then fabricated using standard III–V processing and microlithography techniques as shown in Figure 1.8. Individual cells were isolated using wet chemical etching techniques. Anti-reflective coatings were not used. Measurements were performed on 1×1 cm^2 cells on the three investigated samples.

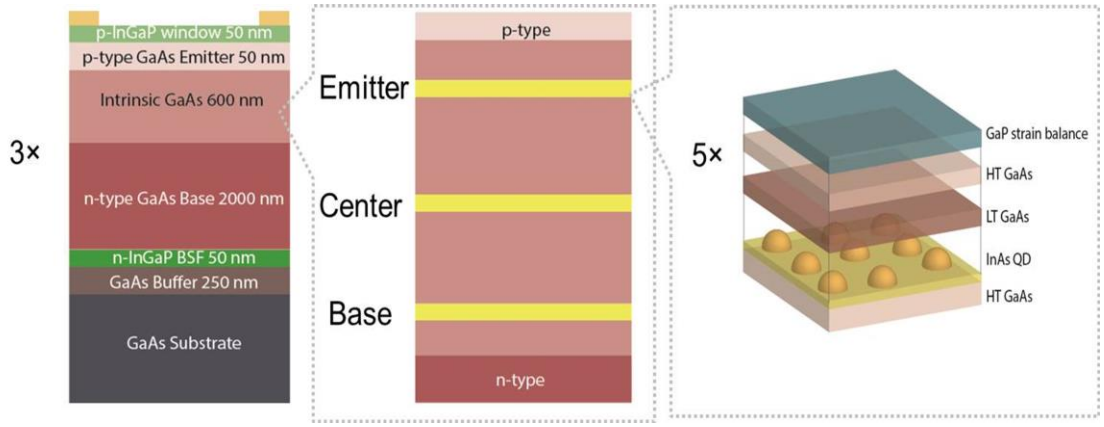

Figure 2.1 Schematic drawing of structural layer layout for 5-layer QD embedded GaAs *p-i-n* solar cell devices.

Room temperature External Quantum Efficiency (EQE) measurements were taken with a Newport IQE-200 Spectroradiometric Measurement system using Standford Research SR570 preamplifier and SR830 lock-in amplifier. EQE is the number of carriers collected from per incident photon at a particular wavelength. EQE cannot be measured directly, but it can be derived from spectral response (SR) that is a ratio between the current generated by a PV device to the power incident on the PV device. Therefore, the EQE can be converted from the SR by replacing the power of the light at a particular wavelength with the photon flux for that wavelength, as shown in Equation 2.1

$$EQE(\lambda) = \frac{hc}{q\lambda} SR(\lambda) \qquad 2.1$$

Where λ is wavelength of incident light, h is Planck constant, q is electron charge, and c is light speed. Figure 2.2 shows an experimental set-up for the EQE measurements. A continuous monochromatic light generated by a Tungsten lamp with a chopper positioned in the front to generate an AC signal. The photocurrent was measured and normalized to a calibration file from a reference detector to get SR and convert to EQE using equation

2.1. Temperature dependent EQE measurements were analyzed using OL750 spectroradiometric measurement system in a Cryoindustries 10K M-22 cryo-system.

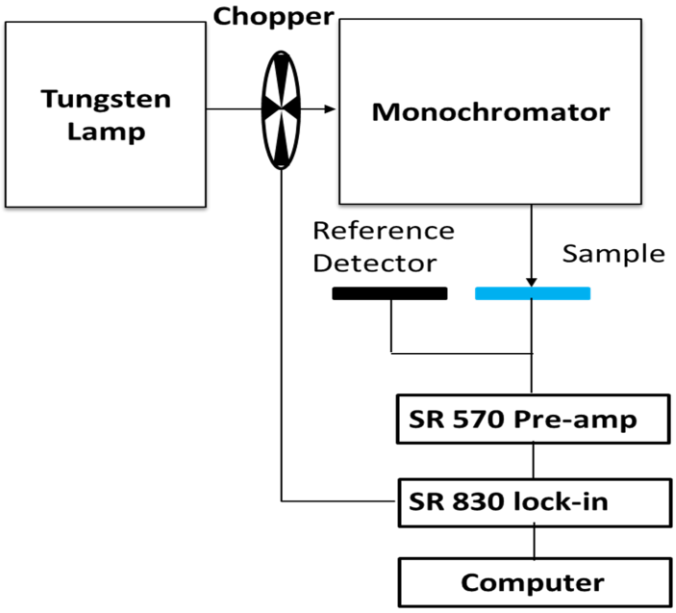

Figure 2.2 Schematic drawing of the experimental set-up for EQE measurements

Figure 2.3 shows the experiment set-up for TRPL measurement in order to estimate carrier lifetime in the investigated devcies. TRPL was measured by a Becker & Hickel single photon counting module and a Hamamatsu near infrared photomultiplier tube, with a temporal resolution of 20 ps. TRPL excitation wavelength was provided by a Fianium supercontinuum white laser source (SC400-2) with an Acusto-Optical Tuning Filter set to 800 nm with a repetition rate of 10MHz (flux of 8.8×10^{11} photon/cm^2·s). TRPL measurements were held at 15K by an Advanced Research System 10K DE-202 closed loop helium cryostat.

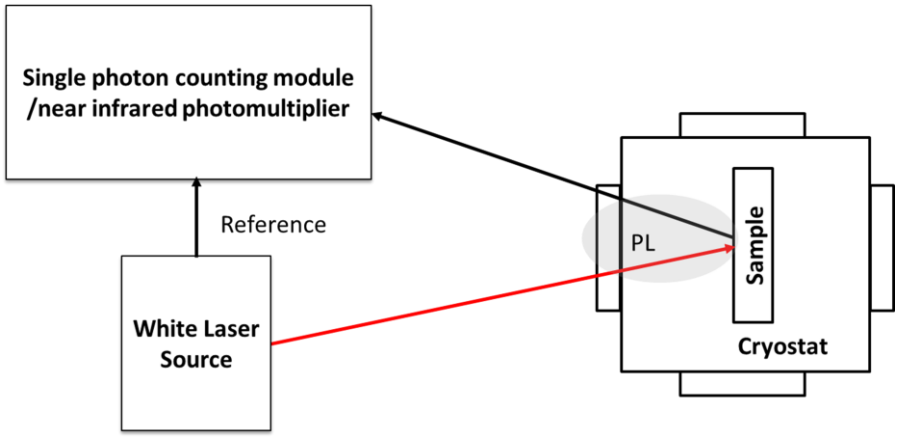

Figure 2.3 Schematic drawing of the TRPL experimental set-up

2.3 Theory

2.3.1 Band structure simulation with varied electric field

Because of non-negligible n-type background doping (1×10^{16} cm^{-3}) in the 600 nm unintentionally doped (uid) "intrinsic" region of the *p-i-n* diodes, the electric field is maximized near the p-type emitter and decreases towards the position close to the n-type base. The details of simulation of the electric field can be found in a previous publication[40]. Therefore, the electric field around the QDs varies with the depth across the intrinsic region under short circuit conditions. In order to theoretically investigate the effect of electric field in the QDSCs within the three designs, the band structures of InAs/GaAs quantum dots embedded in the intrinsic region of a *p-i-n* solar cell were simulated using a finite-difference discretization method of the eight-band ***k·p*** Hamiltonian.[57]. The eight-band refers eight Bloch functions, which include two spin-orbit coupled s-orbital symmetry electrons, and each two spin coupled p-orbital symmetry of heavy holes, light holes, and split-off band. The strain from lattice-mismatch was considered in the Hamiltonian [58]. A Poisson-Schrodinger solver was written in C++ program with material parameters from the most cited literature [59]. The

temperature was set at 300K. Based on the AFM results shown in prior work [56], the average height, radius, and the wetting layer thickness of a single hemispherical quantum dot were set at 3 nm, 10 nm, and 0.5 nm, respectively. In addition, 1.3 nm GaP as a strain compensation layer was inserted between the dots, so the total dot-dot distance was set at 14 nm.

Figure 2.4(a), 2.4(b), 2.4(c) show the simulated band structures at 300K under open circuit conditions of the five-layer-QD super-lattice with local electric field of 5 kV/cm (Base-Shifted, 33 nm from the n-base), 15 kV/cm (Centered), and 50 kV/cm (Emitter-Shifted, 33 nm from the p-emitter), respectively. Due to the increasing local electric field around the QDs, the band bending experienced by the QDs at the three positions is illustrated. The blue line refers to the conduction band. Two localized energy levels of electrons are shown in each QD. The energy difference between each of the localized energy levels and the edge of the conduction band is referred to as the barrier height of the electron. The red line represents the valence band and the ground state of holes. Due to the multiple states (heavy, light, split off) of the holes, there are too many excited states to be shown.

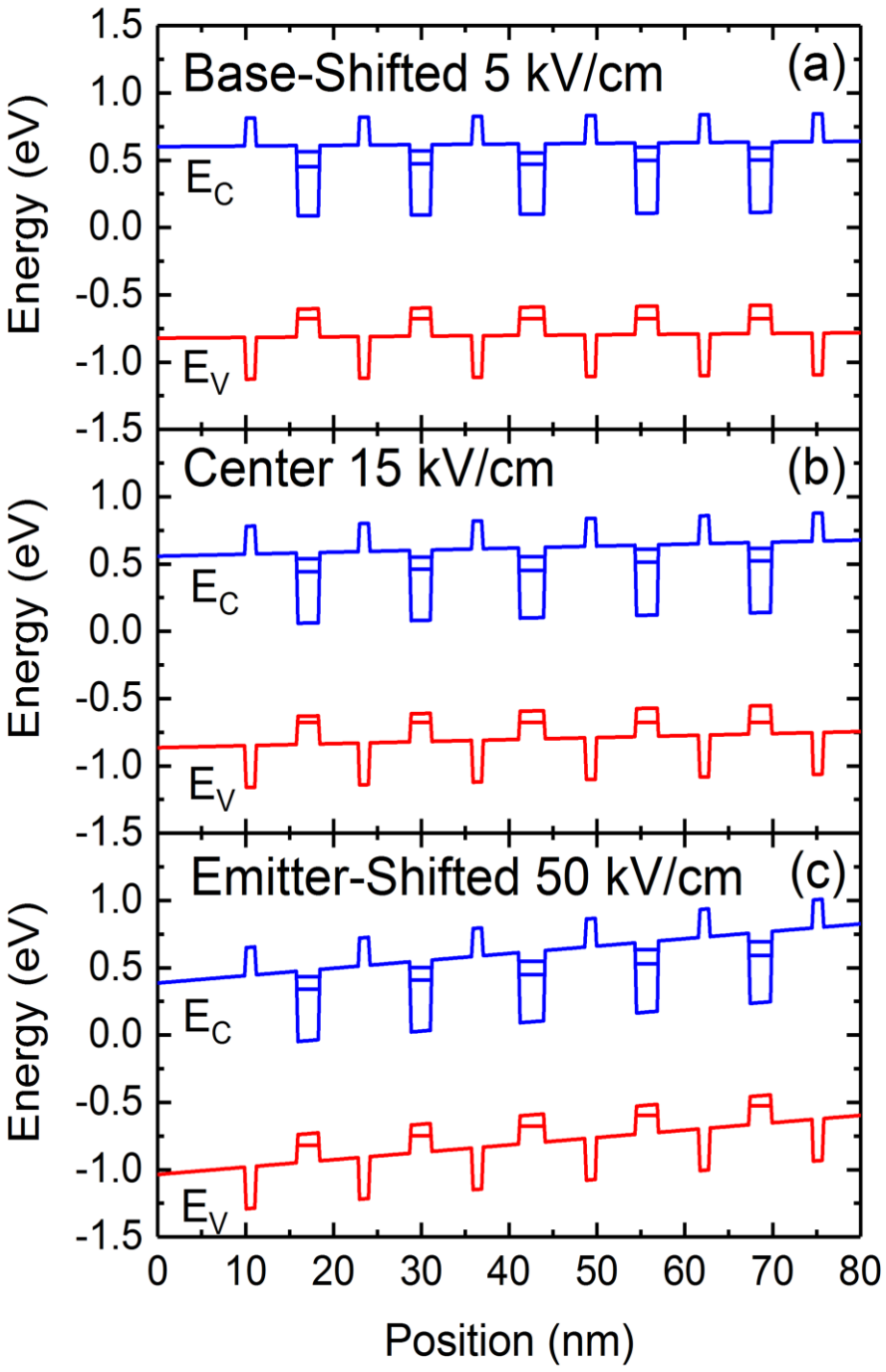

Figure 2.4 Calculated band structure of different QD local electric field under short circuit conditions: (a) The Base-Shifted QDs with local electric field of 5 kV/cm, (b) The Centered QDs with local electric field of 15 kV/cm, and (c) The Emitter –Shifted QDs with local electric field of 50 kV/cm.

2.3.2 Estimation of escape rates

Figure 2.5(a) shows the extracted average electron barrier heights. Because the electric field acts as another perturbation to the Hamiltonian that changes the wave-functions of the electrons, the electric field lowers the confined level of the electrons and extends the conduction band edge. The barrier height of both ground state and excited state electrons decreases slightly with increasing electric field. At a local electric field of 5 kV/cm, the barrier height of the electron ground state and the excited state is 147 meV and 68 meV, respectively. Increasing QD local electric field to 15 kV/cm decreases the barrier height to 141 meV from the ground state and 64 eV from the excited state. When the local electric field is 50 kV/cm, the barrier height of the electron from the ground state and excited state is 136 meV and 60 meV, respectively. Similar to the electrons barrier heights, the average barrier height of the ground state holes is 137 meV, 130 meV and 117 meV for the increasing electric field of 5 kV/cm, 15 kV/cm and 50 kV/cm, respectively. Due to shifting of the confined levels of electrons and holes under an electric field, the state becomes affected by the quantum confined stark effect (QCSE)[60]. Using the subtraction between the band-edge of the GaAs and the barrier height of the ground state electron and hole, the calculated transition energy between the ground state electron and holes (H1-E1) red shifts from 1.13 eV (1097 nm) under the electric field of 5 kV/cm to 1.12 eV (1107 nm) under the electric field of 50 kV/cm at 300K. However, because of the limited absorption from the five layer ground state QD [61], carrier collection from photon energies below 1.1 eV (> 1100 nm) is negligible.

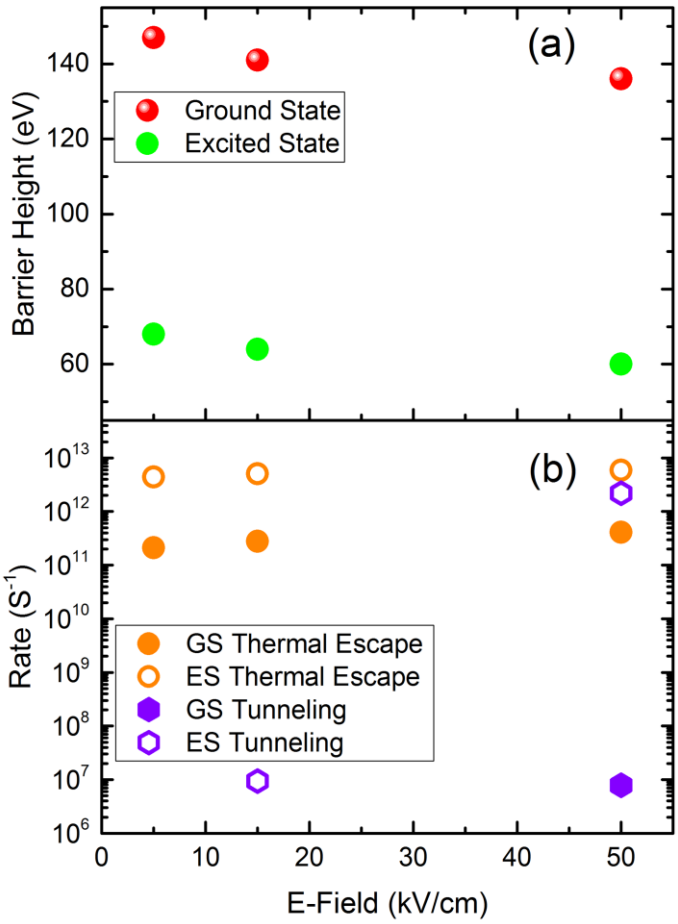

Figure 2.5 Parameters extracted from the band structure simulation at 300K (a) average barrier height, (b) Thermal escape rate and tunneling rate.

Using the extracted barrier height, the thermal escape rate from different energy level can be estimated using Equation 2.2. Due to the small height to diameter aspect ratio, the confinement is mainly along the QD layer growth axis, which is similar to a quantum well structure. For simplification, the thermal escape rate exponentially decreases with the ratio of field dependent barrier height and the temperature [62] [63] as shown in Equation 2.2.

$$\frac{1}{\tau_{th}} = \frac{1}{L_z}\sqrt{\frac{kT}{2\pi m_Q}}\exp\left(-\frac{E_b}{kT}\right) \qquad 2.2$$

Here, m_Q is the carrier's effective mass in the quantum confinement, L_z is the height of the quantum dots (3 nm), E_b is the barrier height, k is Boltzmann's constant and T is temperature. Equation 2.3 is the inverse of tunneling probability per unit time. The tunneling probability was originally estimated using a transfer matrix technique in the effective mass approximation [64]. In order to highlight the basic physical trends in the tunneling rate, Equation 2.3 is simplified by assuming transmission through a single barrier [65][66]. As can be observed in Equation 2.3, the tunneling rate depends on barrier height, tunneling length, and electric field.

$$\frac{1}{\tau_{tun}} = \frac{1}{L_z^2}\frac{n\pi\hbar}{2m_Q}\exp\left(-\frac{2}{\hbar}\int_0^b \sqrt{2m_b(E_b - qFz)}\,dz\right) \qquad 2.3$$

Here, $\hbar$ is Planck's constant, b is the thickness of the barrier, F is the strength of the electric field, and m_b is the carrier effective mass in the barrier. By assuming an electron mass in InAs of $0.023m_0$ and in GaAs of $0.063m_0$ [67], Figure 2.5.3(b) shows the calculated thermal escape rate ($1/\tau_{th}$) and tunneling rate ($1/\tau_{tun}$) of electrons for different confined energy level. First, regardless of electric field at 300K, thermal escape dominates electron escape from the ground state, with a rate on the order of 10^{11} s^{-1}. For ground state electrons, the tunneling rate is too slow ($<10^{-12}$ s^{-1}) to show in Figure 2.5(b) under low electric field conditions ($\leq$ 15 kV/cm). The ground state tunneling rate increases near 10^7 s^{-1} at 50 kV/cm. For the electrons in the excited states, thermal escape dominates in the QDSCs with lower electric field around the QDs (5 kV/cm and 15 kV/cm). However, when the electric field around the QD layer reaches 50 kV/cm, the tunneling rate (2×10^{12} s^{-1}) is comparable with the thermal escape rate (6×10^{12} s^{-1}). Second, increasing electric field around QDs decreases the effective barrier height, so the increased local electric field enhances both tunneling and thermal escape, albeit with a

much more obvious effect on tunneling. The tunneling rate increases exponentially with increasing electric field magnitude according to Equation 2.3.

The dynamics of the ground state electron also need to be considered when evaluating the physics of the IBSC. Along with carrier escape (tunneling and thermal escape), there are other three processes that happen to electrons in the ground state of QDs, including non-radiative recombination, radiative recombination and TSPA. The lifetime (τ_{total}) of the ground state carriers consists of the five rate components shown in Equation 2.4.

$$\frac{1}{\tau_{\text{total}}} = \frac{1}{\tau_{nr}} + \frac{1}{\tau_r} + \frac{1}{\tau_{th}} + \frac{1}{\tau_{tun}} + \frac{1}{\tau_{TSPA}} \qquad 2.4$$

Here τ_{nr} is the non-radiative recombination component which is usually negligible inside high quality QDs because few defects are formed during volumetric strain relaxation.[68], [69] τ_r is the radiative recombination lifetime which depends on wave-function overlap[70] and carrier distribution[71]. The typical values of τ_r from the ground state carrier in InAs/GaAs QD is usually between 0.5~5 ns, depending on the size and the number of repeat layers of QDs [72]–[74]. The optical generation rate from the ground state to the conduction band, $1/\tau_{TSPA}$, depends on the product of incident photon flux and optical capture cross section,[75], [76] and has been shown to be on the order of 1×10^8 seconds^{-1} under 1×10^4 sun concentration.[2] Thus, for the InAs/GaAs QD-IBSC at 300K, although the ground state tunneling rate reaches 8×10^6 s^{-1} at 50 kV/cm, the thermal escape (10^{11} s^{-1}) will limit TSPA under concentrated illumination. In order to enable TSPA to be dominant at room temperature, barrier modifications with wide band gap material including InGaP[30], [77] or AlGaAs[14], [78] are being considered for the IBSC design to suppress the thermal coupling between the IB and CB at the room temperature. The radiative recombination (10^8-10^9 s^{-1}) also reduces the efficiency of

TSPA in InAs/GaAs QD. Because the radiative recombination is the inverse process of optical absorption, to increase TSPA by increasing ground state radiative recombination lifetime, the QD-IBSC design should optimize the trade-off between absorption and recombination. Photon recycling [79] is one option that could be considered to relieve loss due to radiative recombination.

2.4 Results and discussion

2.4.1 Room temperature EQE

In order to experimentally assess the electric field dependent carrier escape from QD absorption (VB-IB), Figure 2.6(a) shows the 300K EQE in semi-log scale of the three investigated QDSCs. There are five peaks in total, including EQE from the wetting layer (WL, around 910 nm), three transitions between excited states of holes and the excited state electrons (ES, 920 nm ~1020 nm), and the ground state (GS, around 1060 nm). The ground state refers the transition from excited states of holes to the ground state of the electrons. The ground state transition (H1 to E1) above 1100 nm is too weak to detect from the five-layer-QD absorption as mentioned in the simulation section. With increasing local electric field intensity of the QDs from 5kV/cm to 50 kV/cm, the overall sub-GaAs band-gap EQE increases. The integrated sub-band-gap AM0 short circuit current (J_{sc} for $\lambda > 880$ nm) is 108 μA/cm^2, 117 μA/cm^2, and 119 μA/cm^2 for the QDSC with 5 kV/cm, 15 kV/cm and 50 kV/cm, respectively. The electric field enhanced sub-band-gap carrier collection is caused by the increased rate of the tunneling and thermal escape, which correlates with the calculations in Figure 2.5(b). The absorption edge is red shifted with the increasing electric field around the QDs, which is due the QCSE.

Figure 2.6(b) shows the electric field dependent sub-band-gap EQE normalized to 50 kV/cm. The carrier collection from the WL shows a slight increase with increasing

electric field, which indicates that almost all carriers can be collected from the wetting layer at 300K even at 5 kV/cm. This is because even though the thermal escape dominates the shallow WL levels, higher electric fields may provide a slight increase in escape due to both barrier lowering and carrier tunneling. When the electric field increases from 5 kV/cm to 50 kV/cm, the carrier collection from ES2 increased 60%, while the carrier collection from GS increased 70%. Based on the low tunneling rates calculated in Figure 2.5(b), this large increase was not expected except perhaps in ES at fields over 50 kV/cm. There may be three possible reasons for this:

(1) The QCSE separates the electron and hole wavefunction, which causes a red shifted [80] and broadened [81] sub-bandgap absorption spectra. Fry *et al.* found that an increasing tail of GaAs (Franz-Keldysh effects) and wetting layer photocurrent affects the QD region with greater reverse bias in a single layer InAs/GaAs QD pin structure.[82] Therefore, the enhanced ground state carrier collection with increasing electric field may be due to the electric field introduced boarding of the optical transitions between higher energy states.

(2) After carriers escape from QD, the carriers may be recaptured and recombine in the wetting layer and QDs.[83] Increased electric field improves the charge separation[45] and reduces the number of carriers around the QD region, so the carrier collection increases with increasing electric field.

(3) Although the QCSE reduces the absorption rate in the QD ground state[81] due to spatial separation of electron and hole wave-function, the associated increasing radiative recombination lifetime of the ground state carriers may contribute to enhanced carrier collection.

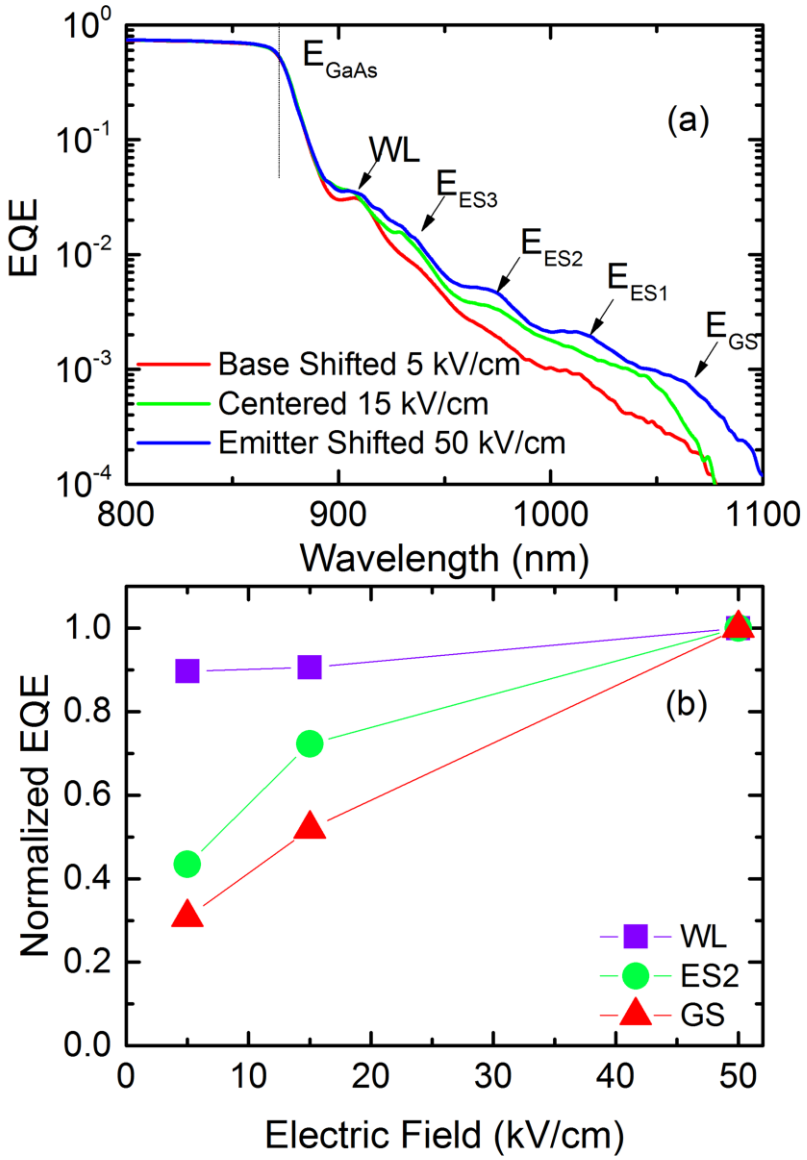

Figure 2.6 (a) 300K EQE of the three investigated cell under zero external bias (b) Electric field dependent sub-band-gap EQE normalized to 50 kV/cm.

2.4.2 Low temperature TRPL measurements

The room temperature sub-GaAs-bandgap EQE experimentally verifies the electric field enhanced carrier escape rate in InAs/GaAs QDSC. The electric field enhanced carrier escape limits the TSPA and associated IBSC applications. However, the radiative

recombination process may also affect the TSPA from Equation 2.4. To experimentally detect the effect of electric field on the radiative lifetime of the ground state, TRPL measurements were conducted. The TRPL spectra represent the decay rates of PL from QD ground state. The decay time depends on the total lifetime. Carrier dynamics of the ground state electron can be given as Equation 2.5.[84]

$$\frac{d(N(t))}{dt} = -\frac{N\,(t)}{\tau_{total}} \qquad 2.5$$

Here, *N(t)* is the total number of carriers in the QD ground state. In order to isolate the radiative recombination lifetime, the other components should be evaluated. The earlier simulations shows the electron thermal escape is the fastest (10^{11} s^{-1}) at 300K for all samples, so the thermal escape components should be suppressed by lowering temperature. The very slow ground state electron tunneling rate (less than 10^{-12} s^{-1}) with 5 kV/cm and 15 kV/cm electric field strengths cannot change the TRPL signal. The 50 kV/cm electric field increases the ground state electron tunneling rate towards 10^{7} s^{-1}, but radiative recombination (10^{8} s^{-1} to 10^{9} s^{-1}) is the dominant process, so the time component extracted at low temperature (15K) refers to the radiative recombination lifetime.

Figure 2.7 shows the electric field dependent ground state TRPL at 15K. The QDSCs with 5 kV/cm field show a mono-exponential decay with extracted lifetime of 2.5 ns. With increasing electric field to 15 kV/cm and higher, the decay curve shows a bi-exponential decay with a fast lifetime component of 1.3 ns for 15 kV/cm and 1.1 ns for 50 kV/cm. Kada *et al.* have correlated the mono-exponential-decay and the fast component in the bi-exponential decay to the radiative recombination rate in a single QD[85]. The fast component is expected to increases with increasing electric field

because the QCSE should reduce wavefunction overlap.[69] However, because an excitation wavelength of 800 nm was chosen (above GaAs band-gap at 15K), the relaxation of carriers in the GaAs barrier to the ground state is first through wetting layer and excited states. Due to field introduced broadening[82], part of the detected ground state PL emission is from the exciton recombination of the tail of the wetting layer and the excited states. Because electrons in excited states or wetting layer states are less bounded, the radiative recombination lifetime is reduced due to increased wavefunction overlap. As a result, the value of fast components in the QD with 50 kV/cm and 15 kV/cm are smaller than the lifetime in the 5 kV/cm QDSC. This reduced fast component with increasing electric field has also been shown by Kasamatsu *et al.* in the temperature dependent TRPL measurements using excitation wavelength at 900 nm.[52]

The slow lifetime component is from exciton recombination between different layers along the growth direction. Kojima *et al.* suggested that there is an interconnection between the InAs QDs caused by the elongation of the electron envelope function along the growth direction even with a spacer layer of 40 nm.[72] When the electric field increases from 15 kV/cm to 50 kV/cm, the slow component increases from 2.1 ns to 7.1 ns. This demonstrates that an increasing electric field increases the radiative recombination lifetime by partially separating the electron and hole wavefunctions in the ground state along the growth direction.[45], [52]

A half-filled carrier population in the IB is required for TSPA to allow optical transitions of carriers both into and out of the confined states. The IB with partially filled electrons requires reduced radiative recombination and suppressed carrier escape. The higher electric field in the InAs/GaAs QDSC extends the lifetime of radiative

recombination but it also enhances the carrier escape. However, TSPA could perhaps still be optimized under an electric field [51] if barrier modifications[86] are made to reduce carrier thermal escape.

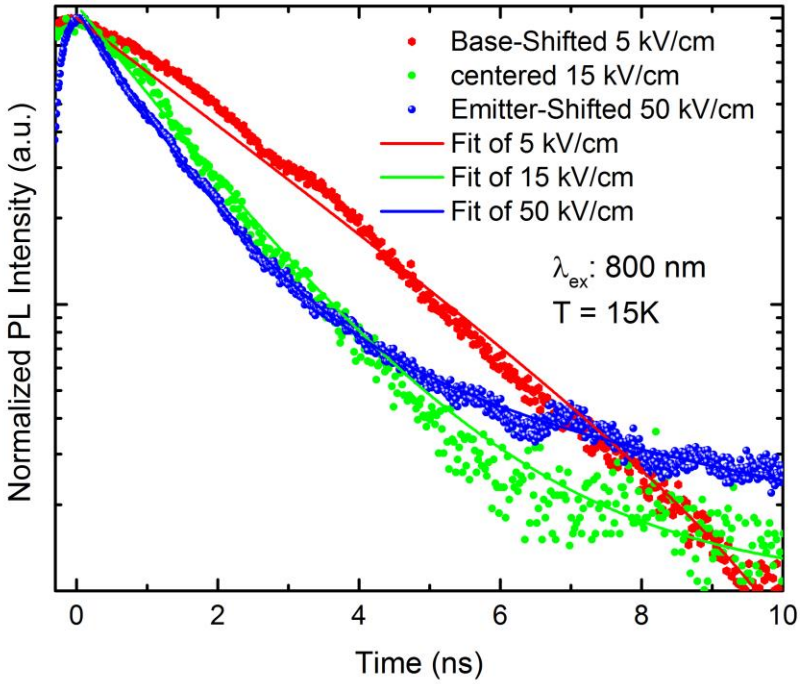

Figure 2.7 Electric field dependent ground states PL decay measured at 15K. The excitation wavelength was 800 nm.

2.4.3 Temperature dependent EQE

To The simulations predict that carrier escape is dominated by the thermal escape. To experimentally examine effect of electric field on carrier escape from the ground state, temperature dependent EQE (TDEQE) measurements were also conducted on the investigated QDSCs. Figure 2.8(a) shows TDEQE normalized to 300K from the ground state excitation for each design. When the temperature is above 100K, thermal escape dominates the ground state carrier escape, so the ground state carrier collection in all three samples decreases with lower temperature. When the temperature is decreased

below 100K, the thermal escape rate is reduced below 1×10^{7} s^{-1}. The TSPA process is also too slow to be considered given the low-intensity of the monochromatic light. Tunneling in the low electric field QDSCs (5 kV/cm and 15 kV/cm) should be limited since the rate is orders of magnitude less than the radiative recombination rate. One should expect that the EQE of these two QDSCs is near zero below 100K. However, this was only the case of the 5 kV/cm sample, while the 15 kV/cm showed a residual EQE near 15% of its 300K value. For the QDSC with highest electric field of 50 kV/cm, the simulation in Figure 2.5(b) shows the tunneling of ground state electron is near 10^{7} s^{-1}, which is an order of magnitude lower than to the radiative recombination rate (5×10^{8} s^{-1}) from TRPL measurements. This would also not account for the high residual EQE (~30% of the 300K value) observed in the 50 kV/cm sample. There may be two possible reasons for the stable residual EQE observed at temperature below 100K:

(1) carrier collection from the absorption of the tail of the wetting layer and GaAs[82], [87];

(2) A size-selective tunneling effect[88] caused by faster carrier tunneling rate in the smaller dots. Keep in mind that the QD size used in the simulation is only an average value from AFM measurements, while the QDs size is actually a Gaussian distributed around the average value.

To verify the electric field reduced barrier height in the simulation, the temperature dependent EQE can be fit using Equation (5), which is derived from the rate equations for the QDs under steady state conditions.[88] The EQE depends on the fraction of carriers that escape prior to recombining. The numerator of Equation 2.5 is the total escape rate, including thermal escape rate in Equation 2.2 and tunneling in Equation 2.3. The

denominator refers the carrier lifetime shown in Equation 2.4. A radiative recombination lifetime on the order of 1 ns was used for the fitting and non-radiative recombination was ignored.

$$EQE_{normalized} = \frac{\frac{1}{\tau_t}+\frac{1}{\tau_{th}}}{\frac{1}{\tau_{total}}} \qquad 2.6$$

Figure 2.8(b) shows the extracted electric field dependent activation energy using Equation 2.6 and the barrier height calculated from the band structure simulation. The fit activation energy decreases with increasing electric field, which confirms the theoretical prediction that the effective barrier height decreases with increasing local electric field. The values of the fit activation energy were 140±5 meV, 131±4 meV and 123±3 meV for the QDSCs with QD local field of 5 kV/cm, 15 kV/cm and 50 kV/cm, respectively. The values are slightly lower than the effective electron barrier from the band structure simulation, which may be affected by difference in the size of the QDs in the investigated QDSCs and the QD in the simulation. As well, the difference between the simulation and extracted activation energy increases with increased electric field, which may be because carriers in the 50 kV/cm QDSC experience thermally assisted tunneling [17], [43] that was not accounted for the simulation.

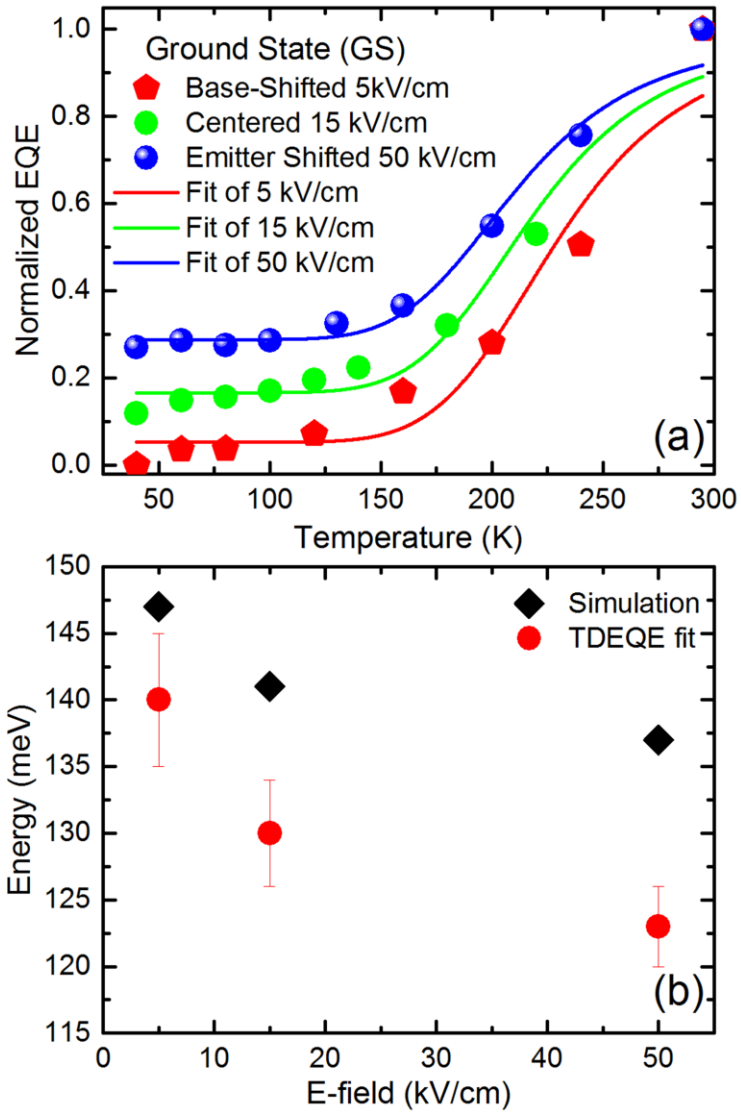

Figure 2.8 (a) GS EQE of all three investigated cells; (b) fitted activation energy and calculated effective barrier height of the electrons.

Additionally, Figure 2.9 shows the temperature-dependent EQE normalized to 300K from the first excited state. In the 50 kV/cm sample the tunneling escape and thermal escape are almost equivalent at room temperature. Due to the temperature independent fast tunneling in the excited states, only a small reduction (20%) in EQE from 300K to 60K is observed in the 50 kV/cm sample. The 15 kV/cm samples shows a similar effect,

albeit with a larger drop in EQE with temperature since the tunneling rate in this sample has decreased and is on the same order as the radiative recombination rate. The 5 kV/cm sample shows behavior similar to the ground state, due to limited tunneling from the QD, although some degree of size-dependent tunneling may still result in the observed residual EQE below 75K. The extracted radiative lifetime from fitting via Equation 2.5 is on the order of 0.1 ns, which is correlated with the literature value[89]. The extracted activation energy shows the same decreasing trend with increasing electric field. The value of the fit activation energy is 70±2 meV, 66±3 meV, and 62±7 meV for the QDSC with increasing electric field from 5 kV/cm to 50 kV/cm, which is close to the value of the ES barrier height from the band structure simulation.

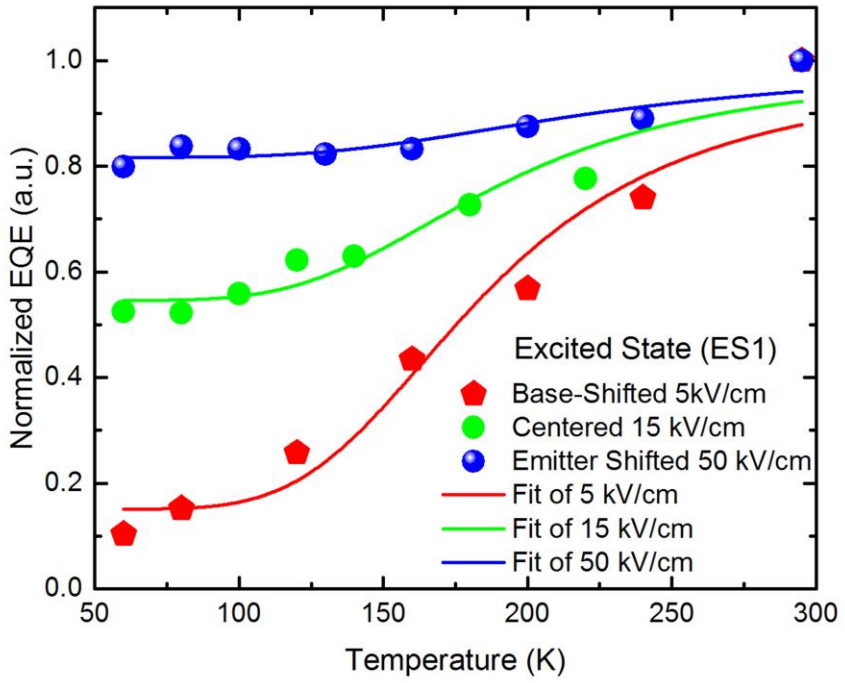

Figure 2.9 Temperature dependent normalized first excited state EQE and the fit of the three investigated design with varied electric field around QD.

2.4.4 Electric field dependent TSPA

To directly measure the effect of electric field on TSPA, Figure 2.10 shows a schematic of TSPA-introduced photocurrent measurement setup. A Cryoindustries 10K M-22 cryo-system, with a CaF_2 window to reduce the loss of infrared (IR) input light, was used to cool the sample to 10K. A continuous monochromatic light generated by a Tungsten lamp attached in OL750 Spectroradiometric Measurement system is used to pump carriers into an IB, while a second IR photon source (Omega 800^0C blackbody radiation sources with 1500 nm filter) is coincident upon the sample to enable the second photon excitation from the IB. A chopper is positioned in front of the IR light source in order to generate an alternating current (AC) signal of the carrier collection from optical transition out of the IB.

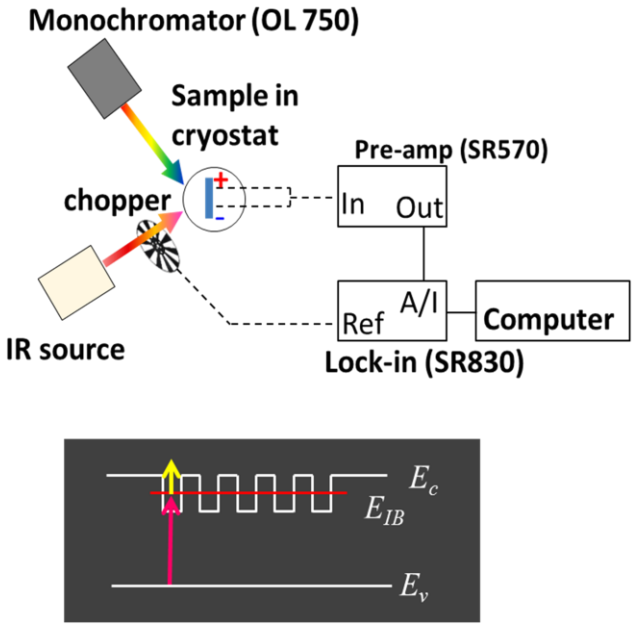

Figure 2.10 Schematic measurement setup to characterize photocurrent production as a direct result of optical transitions of electrons from IB to CB. Monochromatic light is used to pump electron from into an IB and an IR source is used to pump electron out of the IB.

The centered InAs/GaAs QDSC was used as the sample to directly detect the electric field effect on TSPA. Because of the effect of unintentional background doping., as shown in the inset of Figure 2.11, the simulated electric field via Sentaurus TCAD [90] generally linearly decreases with increasing forward bias at the center of the intrinsic region. To update the design of QD-IBSC for real application with a load, it is important to investigate whether TSPA reaches maximum at the point of P_{max}. Figure 2.11 shows an example of an one sun AM0 (the spectrum and intensity of the sun outside Earth) IV curve of the centered QDSC, where P_{max} is at 0.82 V, correlating an electric field intensity around 1 kV/cm.

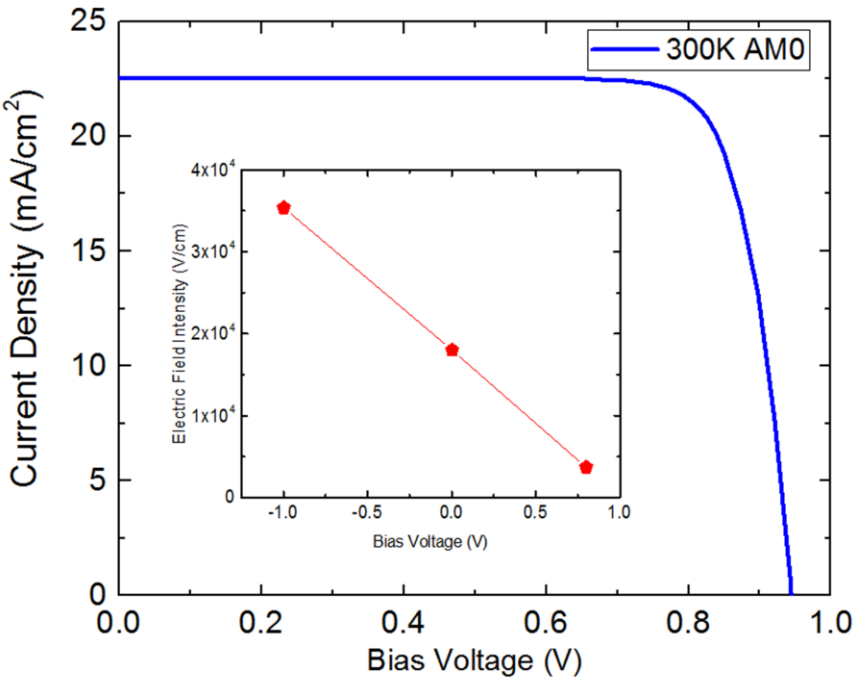

Figure 2.11 300K AM0 IV measurement of the centered QDSC; inset is simulated electric field versus bias voltage at the center of the 600 nm intrinsic region.

To experimentally investigate the effect of electric field on TSPA, Figure 2.12(a) shows 10K voltage biased TSPA. With increasing forward bias from 0 V to 0.7 V, TSPA first

increases and then reaches the maximum at 0.5 V (7 kV/cm), and then it starts to decrease. This voltage dependent TSPA is consistent with Sagabe *et al.* room temperature InAs/GaAs QD-IBSC delta EQE measurements (difference between EQE with a second light source on and off) [91]. Because tunneling decreases with reducing electric field (forward bias), carrier escape introduced EQE reduces (shown in Figure 2.12(b), blackbody sources is off, only chopping monothematic light) and TSPA initially increases; while number of carrier recapture (and recombination) in the QDs also increases with forward bias, so there is a TSPA optimized voltage point at 0.5 V due to the balance of escape and recombination process.

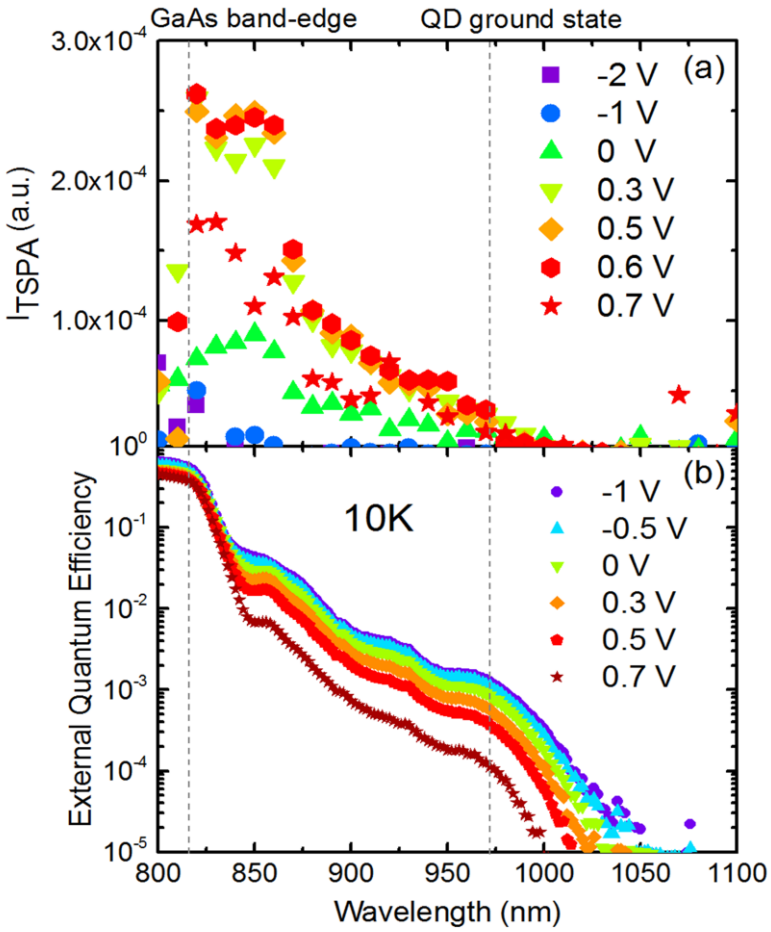

Figure 2.12 10K voltage bias dependent (a) TSPA (b) EQE of the centered QDSC

2.5 Conclusion

To achieve a QD-IBSC, TSPA should be the dominant escape process of carriers in the IB. To improve the efficiency of TSPA at room temperature, both carrier escape and recombination in the IB should be suppressed. In the studied InAs/GaAs QDSCs with a varying electric field across the QD embedded region of the device, thermal escape and carrier tunneling are shown as the primary mechanisms of carrier collection at room temperature. Increasing local electric field reduces the effective barrier height by raising the average energy of the electron wave function in the QDs.

As a result, both carrier tunneling and thermal escape from InAs/GaAs QDs increase with an increasing electric field. At 300K, fast thermal escape limits the TSPA in these InAs/GaAs QDSCs. Tunneling escape from excited states becomes dominant only when the electric field exceeds 50 kV/cm. Room temperature EQE shows increased carrier collection from the excited states because of electric field enhanced carriers escape and charge separation. The increased carrier collection from the QD ground state (VB-IB transition) at higher fields may be due to the field introduced broadening of absorption from the wetting layer as well as reduced carrier recapture. On the other hand, the rising slow components with increasing electric field in the low temperature TRPL experiments demonstrate that an electric field extends radiative lifetime by spatially separating electrons and holes. TDEQE measurements show the ground state carrier collection is reduced with decreasing temperature because thermal escape is suppressed, which correlates with the simulations. The simulated effective barrier height was verified by the extracted activation energy from TDEQE. The electric field across InAs/GaAs QDs not only enhances carrier escape from the IB, but also improves charge separation across the

intrinsic region that extends carrier radiative lifetime in the IB. Furthermore, voltage bias dependent TSPA shows that TSPA reaches a maximum with the presence of a electric field around 7 kV/cm in the investigated InAs/GaAs QDSC. To balance the effect of electric field on electron escape and recombination, a proper solar cell design such as wide-band-gap material should be considered to optimize the probability of TSPA.

Chapter 3

Barrier modification of QD-IBSCs

3.1 Introduction

As stated in Chapter 2, so far, InAs/GaAs QD-IBSCs have been widely studied as a prototype of IBSC. However, at room temperature, a small difference between the IB and CB in InAs/GaAs QDSCs thermally couples the IB and CB and reduces the TSPA rates. In order to enable voltage preservation and increase current output, thermal escape rate should be reduced below TSPA rate, while TSPA rate should exceed recombination (radiative and non-radiative) rate. Generally, there are two approaches to reduce carrier escape from an IB in QD-IBSCs, either by decreasing temperature or increasing the height of the barrier. Because the QD-IBSCs are expected to work at room temperature or above, several methods have been investigated to increasing barrier height, like direct doping in QD [92], increasing the thickness of spacer layer between layers of QDs [17], adding the field damping layer [50], [93], and barrier modification [76], [77], [94], [95]. To achieve a conversation efficiency of 63% under maximum solar concentration, a detailed-balance model predicts that the optimum values of 1.96 eV for the band gap of the VB and CB, 1.24 eV and 0.72 eV for the band gap between the VB-IB and IB-CB, respectively. Therefore, this chapter focuses on barrier modification.

To improve the performance of QD-IBSCs by barrier modification, numerous combinations of the QDs and barriers have been published, like GaSb QDs in GaAs [76], GaSb QDs in InGaAs [96], InAs/GaAs QDs with AlAs capping layer [94], InGaN QD with GaN QD barrier [97], InAs QDs with InGaP barrier [95], and InAs QDs in $Al_{0.3}GaAs$ [13] and so on. Experimental results with wide band gap QDSC did show increased two photon absorption than InAs/GaAs QDSCs [44], [95], but efficiency of the

wide band gap barrier QDSC is below 5% [13], [33], [98]under one sun illumination, which still needs to be improved by adjusting the solar cells design and QD growth conditions. To increase band gap of host material to the optimized value and suppress carrier escape rate from an IB, InAs QDs with the barrier of $In_{0.5}GaP$ (1.9 eV at 300K) or $Al_{0.3}Ga_{0.7}As$ (1.84 eV at 300K) are addressed in this chapter. The performance of these QD-IBSCs was evaluated via standard IV and EQE measurements. Carrier dynamics were investigated via voltage bias EQE and temperature dependent EQE measurements, while TSPA performance was also directly characterized by chopping an additional IR light source. In addition, simulations of band-structures of other advanced III-V QD systems including GaSb/GaAs and type II InP/InGaP are also demonstrated and discussed.

3.2 Development of InAs/$In_{0.5}$GaP QD-IBSCs

3.2.1 1st Generation InAs/$In_{0.5}$GaP QD-IBSCs

Theory

Figure 3.1 shows room temperature band structure simulation results of a InAs QD with different barrier using eight band ***k·p*** calculation [99] that discussed in chapter 2. At 300K, the band gap of GaAs is 1.42 eV, while The InGaP band gap is 1.93 eV that is close to the ideal host material bandgap of 1.95 eV, as shown in Figure 1.3(a). Based on the AFM results in previous study [55], [77], the InAs QD height for the simulation is fixed of 2 nm, while the QD diameter is 20 nm. Similar to the results showed in Chapter 2, two electron confined levels and many hole confined levels can be observed in each QD. The calculated electron ground state in InAs QD with GaAs barrier is 0.14 eV, associated with ground state transition at 1.16 eV (wavelength of 1068 nm). The ground

state transition energy decreases with increasing QD height, which can be varied between each growth. Those are consistent with chapter 2 results.

When InAs QD is embedded in an InGaP barrier, the barrier height of electron is increased to 0.29 eV. By using Equation 2.2 and 2.3, the calculated total ground state electron escape rates of InAs/GaAs QD and InAs/InGaP QD, including thermal escape and tunneling, are on the order of 10^{11} s^{-1} and 10^{9} s^{-1}, respectively, so the InAs QD with InGaP barrier effectively suppresses electron escape. InAs/InGaP QD ground state transition energy is 1.02 eV (wavelength of 1215 nm). However, as a fact, the hole ground state also increases with InGaP barrier. The calculated ground state hole barrier height of InAs/GaAs QD and InAs/InGaP QD is 0.12 eV and 0.62 eV, respectively. The deeper hole confinement may decreases carrier collection by hole capture [100] introduced fast recombination with electric field less than 50 kV/cm [101].

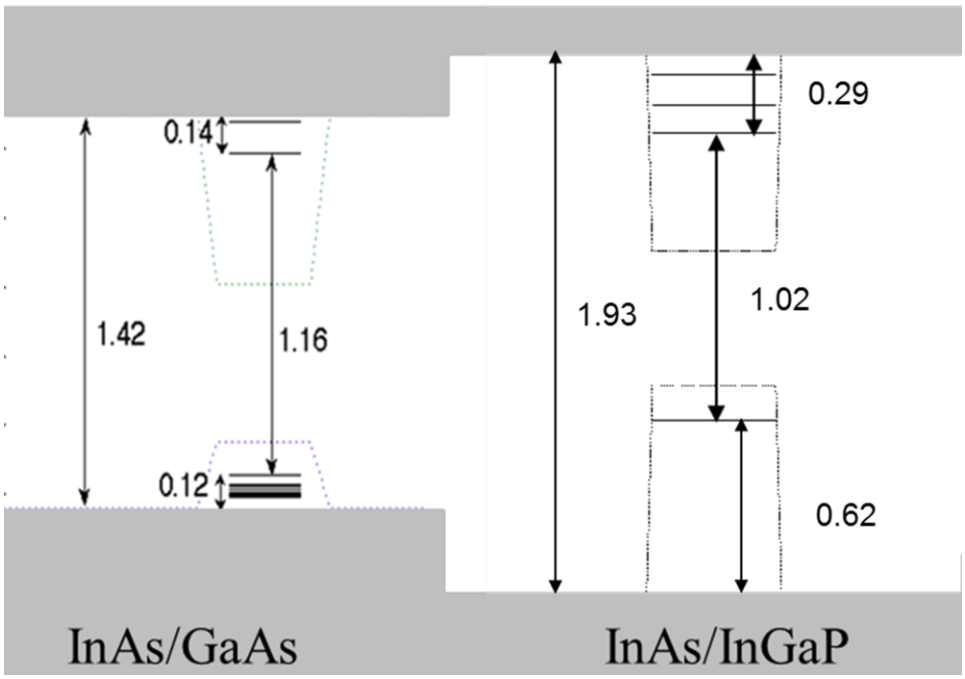

Figure 3.1 300K Band structure of InAs QD with GaAs barrier and InGaP Barrier

Sample and experiments

Three PV devices are studied, including two ten-layer InAs QD embedded *p-i-n* GaAs PV devices with different cladding layer of InGaP or GaAs, and a GaAs baseline cell as reference. The investigated structures were grown on 350 μm thick Si-doped GaAs (100) substrate misoriented toward to the [110] direction with an angle of 2°, using a low-pressure rotating disk MOVPE reactor (Veeco P125LDM) [102] at NASA. Figure 3.2 shows the layer schematic for these investigated devices. After growth of 2000 nm (1×10^{18} cm^{-3}) n-type GaAs base, the InAs QD are formed by the strain-driven Stranski-Krastanow growth mode. The InAs coverage was 1.8 ML for all samples. After QD formation, the QD is capped followed low temperature GaAs layer. Then the InGaP barrier layer or high temperature GaAs layer of 4.6 nm are placed, followed by a GaP strain-balancing layer and a final GaAs barrier layer. This unit is repeated within a 200 nm intrinsic region for ten periods before completing the 500 nm (1×10^{18} cm^{-3}) p-emitter and contact layers. At short circuit, the build in voltage calculated based on doping level is 1.35 V, so the electric field is 54kV/cm in the *p-i-n* devices, which is used to improve hole escape rate from InAs/InGaP QD embedded PV devices. Solar cells were then fabricated using standard III–V processing and microlithography techniques as discussed in chapter 1. Individual cells were isolated using wet chemical etching techniques. Anti-reflective coatings were not used. Measurements were performed on 1×1 cm^2 mesa with grid fingers (area coverage less than 4%) on the QDSC.

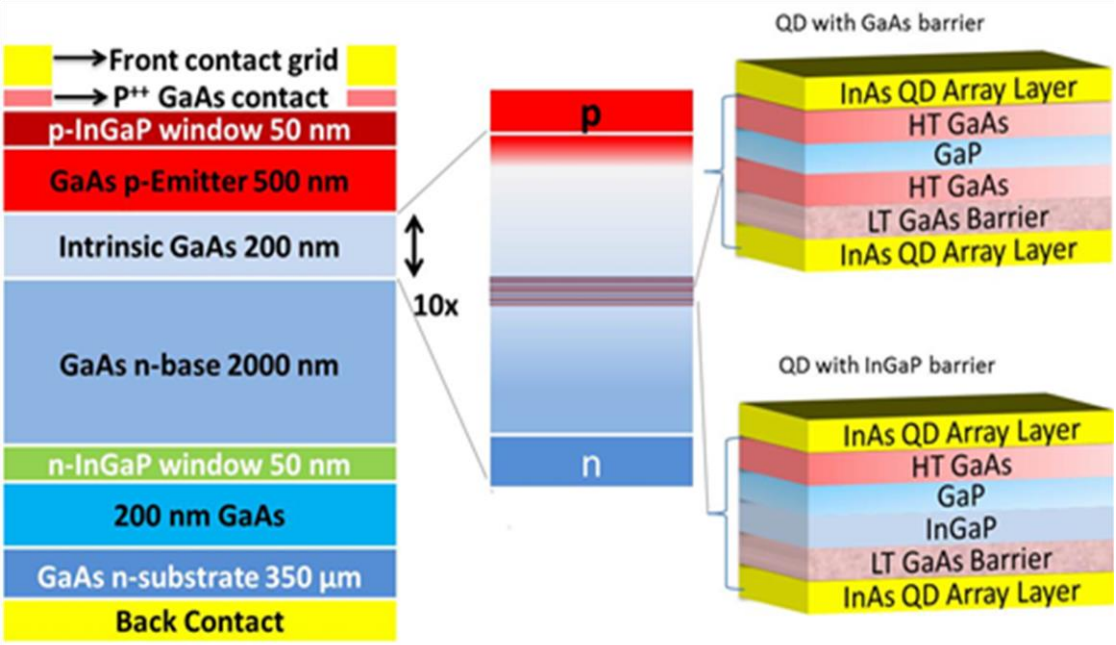

Figure 3.2 Structural layer layout for 10-layer InAs QD embedded GaAs *p-i-n* solar cell device with barrier modification

Similar to Chapter 2, the EQE measurements were completed with OL750 Spectroradiometric Measurement system. The temperatures of the measured solar cells were cooled by a Cryoindustries 10K M-22 cryo-system and monitor via thermal couple connected to the Lakeshore Model-330 temperature controller. Voltage bias was applied with Stanford 570 low-noise current preamplifier.

Results and discussion

As discussed by Forbes *et al.*[86], the increased recombination in the coalescence InAs QD on an indium rich InGaP surface introduces a degraded Voc from one-sun AM0 IV measurements in InAs/InGaP QDSCs. To examine the carrier collection with different solar cell structures at room temperature at short circuit condition, Figure 3.3 (a) shows the EQE measurements of the investigated cells. A degradation of the bulk response (400-850 nm) is found in InAs/InGaP QDSCs.

Figure 3.3(b) shows the sub-GaAs-bandgap log-scaled EQE. The EQE from the transition between wetting layer states (around 920 nm) are higher in QDSC with GaAs barrier than that in QDSC with InGaP barrier. This is mainly due to shallower confinement in wetting layer states of QD with GaAs barrier, so the escape rate is faster. Compared to the InAs/GaAs QDSC, the EQE from the QD state absorption around 1050 nm is improved in QDSC with InGaP barrier. The integrated J_{sc} above 950 nm also shows an increment of 118 μA/cm^2 in the QDSC with InGaP barrier. This indicates an enhanced optical absorption between the VB-IB. Additionally, in the InAs/InGaP QD PV devices, the experimental ground state transition (~1050 nm) is blue shifted than the calculated value (1215 nm) in Figure 3.2, indicating a smaller average QD size during the MOCVD growth.

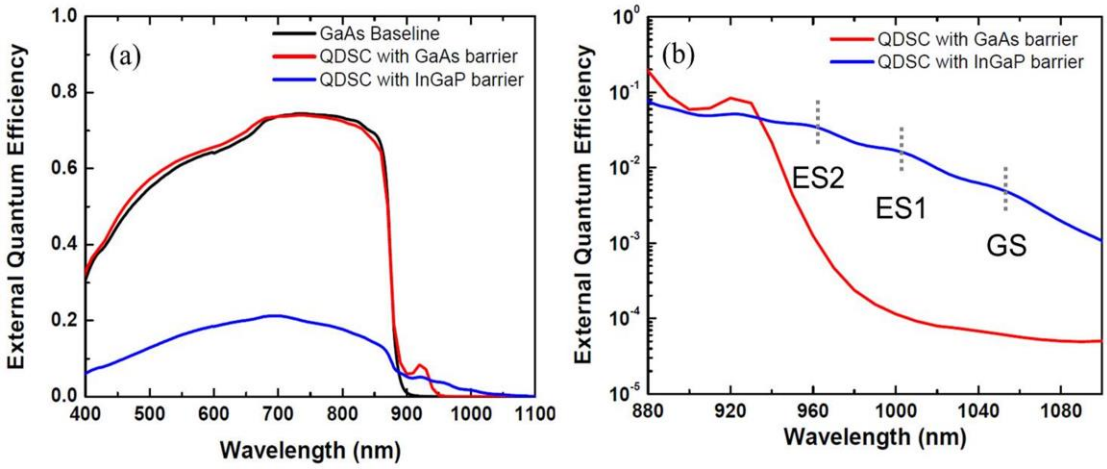

Figure 3.3 (a) External quantum efficiency of the investigated solar cells at room temperature, (b) semi-log scale EQE (> 880 nm) of the QDSCs

To explain the degradation in carrier collection from short wavelength (400-850 nm) photon excitation in the InAs/InGaP QDSC, Figure 3.4(a) shows calculated light fraction as a function of depth in GaAs using Beer–Lambert law as shown in Equation 3.1

$$I(\lambda) = 100e^{-\alpha(\lambda)x} \qquad 3.1$$

Where I is the light intensity, depending on the position along the device growth direction and wavelength of the incident photons; α is the absorption coefficient of GaAs at each wavelength; λ is the incident photon wavelength; x is the depth of GaAs. As can be seen, 95% photons with wavelength less than 550 nm are absorbed in the 500 nm p-type GaAs emitter, where electron is the minority carrier need to transport across the intrinsic region before being collected. Over 50% photons with wavelength above 750 nm are absorbed in the n-type base, where hole is the minority carrier. Similar to the electron, the holes needs to transport across the intrinsic region. Thus carrier collection in the range between 400-850 nm indicates a carrier transport related recombination in the intrinsic region, where ten-layer InAs/InGaP QDs are embedded.

Figure 3.4(b) shows a band structure simulation via nextrnano [29]. For carriers generated in the GaAs emitter and base, the InGaP layer acts as a barrier, which reduces the bulk carriers tunneling rate and increases capture rate during carriers transport across the intrinsic region. Such degradation was also found in the GaAsP/GaAs quantum well solar cell [103]. Furthermore, the high barrier inhibits the fast carrier remission after being captured by QDs [104]. The average holes barrier is larger than the electrons barrier. Due to a heavier mass of a hole than an electron, the holes thermal escape rate is slower than the electron, so the hole escape is rate limiting process. Gioannini *et al.* suggested that if holes' escape are slower than electros in a QDSC, electrons tend to radiatively recombine inside QDs instead of remission after being captured into QD [12]. Because of the large degradation of bulk carrier collection from emitter and base, the performance, including short circuit current and open circuit voltage, of InAs/InGaP QD embedded in the *p-i-n* GaAs solar cell is lower than the reference GaAs cell.

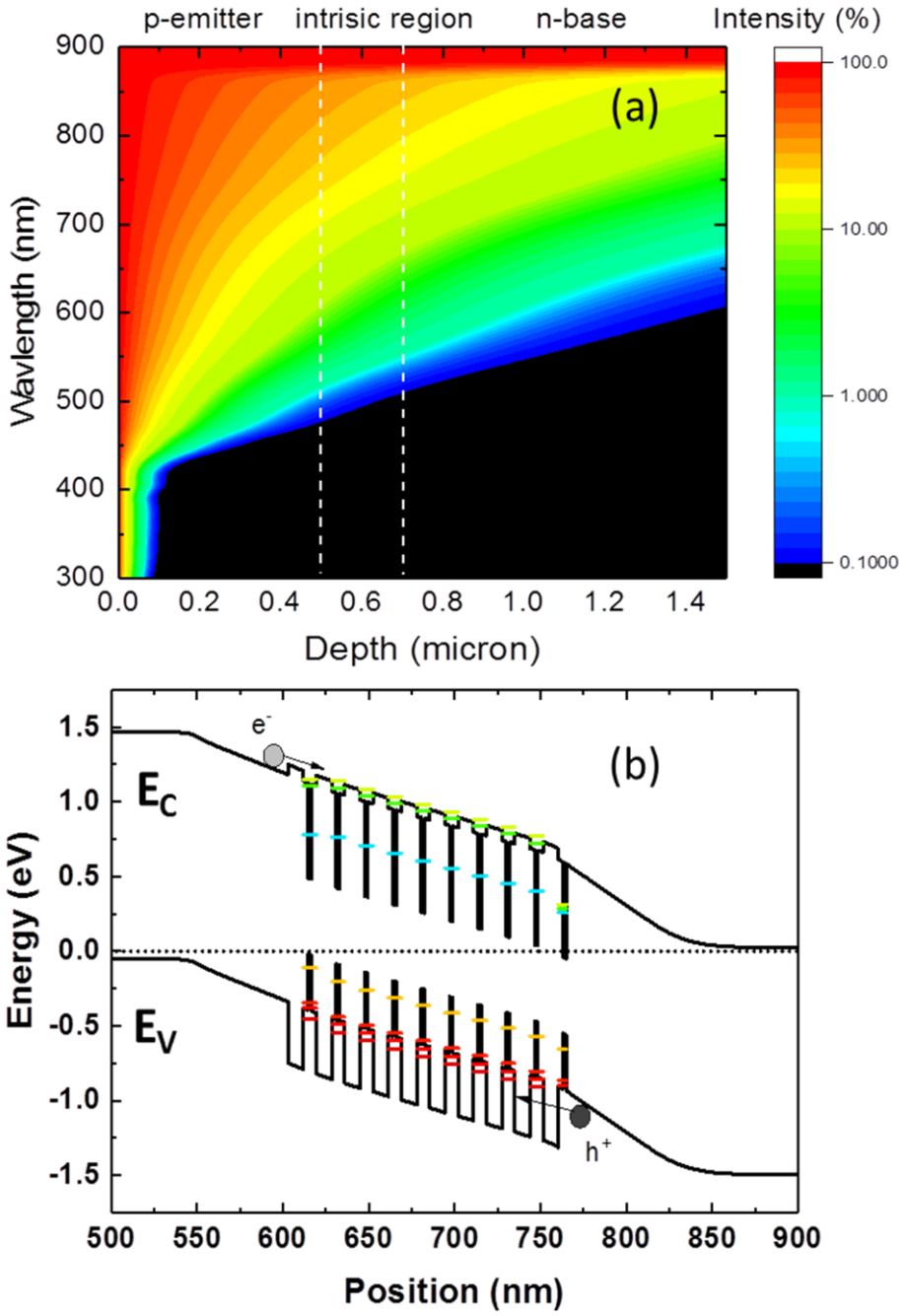

Figure 3.4 (a) Light fraction as a function of depth in GaAs (b) 300K band structure simulation of the *p-i-n* InAs/$In_{0.5}$GaP QDs embedded GaAs device via nextnano software under dark at short circuit condition are used to show photo-excited bulk carrier need to tunneling through the InGaP barrier before being collected.

In order to experimentally verify the degradation of carrier collection at short circuit condition is due to the recombination in the InAs/InGaP QD embedded intrinsic region, Figure 3.5 (a) shows 300K voltage bias dependent EQE. The bias voltage ranged from -3 V reverse bias to 0.4 V forward bias. As discussed in chapter 2, the electric field across the intrinsic region increases with reverse bias voltage. An increasing electric field enhances bulk carrier tunneling rate and transport rate across the intrinsic region, so the bulk EQE increases with reverse bias voltage. With forward bias voltage, significant degradation can be observed. Such degradation in current output was also observed in multiple quantum well solar cell by Sugiyama *et al* [105], which suffers from similar issues of carriers loss (from short wavelength absorption) during the transport. Figure 3.5(b) shows the EQE normalized to -3V at each wavelength to detect the carrier collection at different wavelength. The longer wavelength (920 nm and 1000 nm) photon excited carriers are from the QDs absorption, so the carriers have to first escape from the QD confinement before transport across the intrinsic region. The increasing electric field also affects the carrier thermal escape/tunneling from the QDs as discussed in chapter 2. As a result, at short circuit condition, normalized EQE of the carriers generated inside the QDs (920 nm and 1000 nm) is lower than that of the carriers from bulk material absorption (520 nm and 700 nm). To improve the carrier collection from the emitter and base absorption, wide-band-gap material should be considered to replace the GaAs emitter and base.

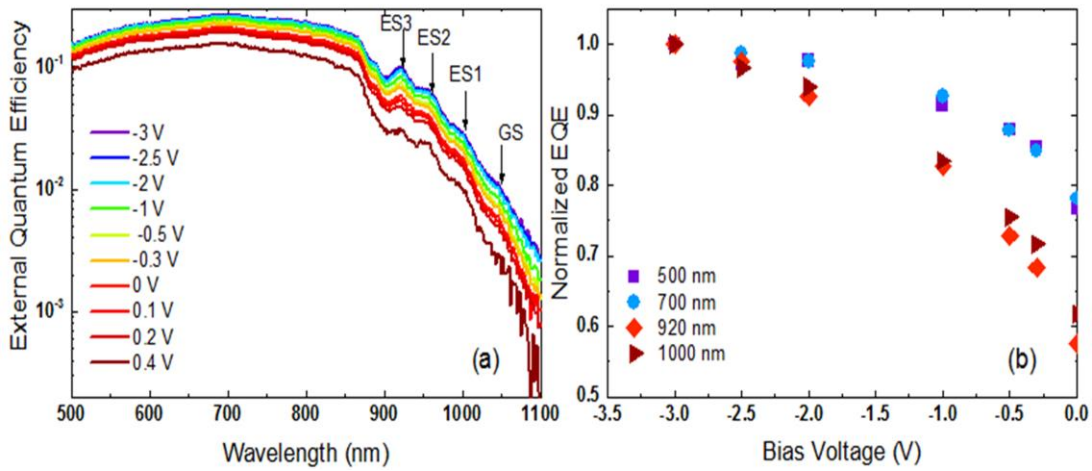

Figure 3.5 Room temperature bias dependent (a) EQE of QDSCs with modified p-i-n NASA grown $In_{0.5}GaP$ barrier, (b) Normalized external quantum efficiency.

However, due to the superior carrier collection from QD absorption associated bulk degradation in the QDSC with InGaP barrier, temperature dependent EQE was conducted to investigated the thermal coupling effect on the PV device performance. Here, thermal coupling includes thermal escape [106] for carriers from QD to the conduction band and valence band, and carrier capture [107] via phonon scattering from conduction band or valence band into QD. The thermal escape enhance carrier collection but affects the output voltage preservation [106], while carrier recombination inside QDs after being captured degrades carrier collection from bulk absorption.

Figure 3.6 (a) shows the temperature dependent EQE of the GaAs reference cell, the band edge blue shifts with decreasing temperature due to bandgap variation (described by the Varshini equation) [108]. Temperature varies from 295K to 15K. The EQE slightly increases with decreasing temperature. After EQE constant increases at temperature of 155K, the EQE drops again. Similar trends of temperature dependent EQE of GaAs pin solar cells also can be found elsewhere [109], [110]. At 15K, the EQE from wavelengths below 700 nm is still higher than the EQE measured at room temperature. Such

temperature dependent EQE in the GaAs solar cell are due to the reduced nonradiative recombination and temperature dependent mobility [111] in GaAs at low temperature.

Figure 3.6 (b) shows the temperature dependent EQE of the QDSC with InGaP barrier. The bulk response first slightly decreases to temperature of 175K. After this the EQE starts to increases with temperature below 155K. At 15K, the EQE from wavelength below 800 nm is much higher than the EQE measured at room temperature, especially the EQE around the wavelength of 700 nm, which shows a 50% increment as compared to the room temperature EQE. With decreasing temperature, such enhancement in EQE of the entire bulk material absorption indicates reduced carrier loss from improved transport of electrons across the i-region, which may be from the combined effects of improved transport rate across the reduced capture rate [100] and reduced recombination rate [112]. The sub-GaAs bandgap collection also suffers carrier loss during the transport across the intrinsic region after carrier escape from the confined levels. Furthermore, tunneling dominates carriers' escape from shallow confinement [113], so the EQE from transitions between shallow confined level (880~920 nm) follows the same trend as the bulk EQE. The EQE above 950 nm slightly decreases with lowering temperature, which is due to the reduced thermal escape rate with decreasing temperature.

Using Equation 2.6 [114], the fitted activation energy of QDSC with InGaP barrier from figure 3.6 (c) is 132 meV, 65 meV and 67 meV for the transition at room temperature around 950 nm, 1002 nm and 1050 nm respectively. These small extracted activation energies are attributed to the hole states. Because heavier mass and larger valence band offset are in QD with InGaP barrier as showed in Figure 3.1, the ground state hole escape rate ($10^8 s^{-1}$) is slower than the ground state electron escape rate ($10^9 s^{-1}$), which again

verifies hole is the rate limiting carrier in the escape process [115] in InAs/InGaP QDs. The reduced fitted activation energy towards the deep confined level with transition above 1000 nm indicates, instead of direct thermal escape from deep confined levels to continuous density of states, the carrier escape may first involve thermal escape to some intermediate confined level then tunneling [116].

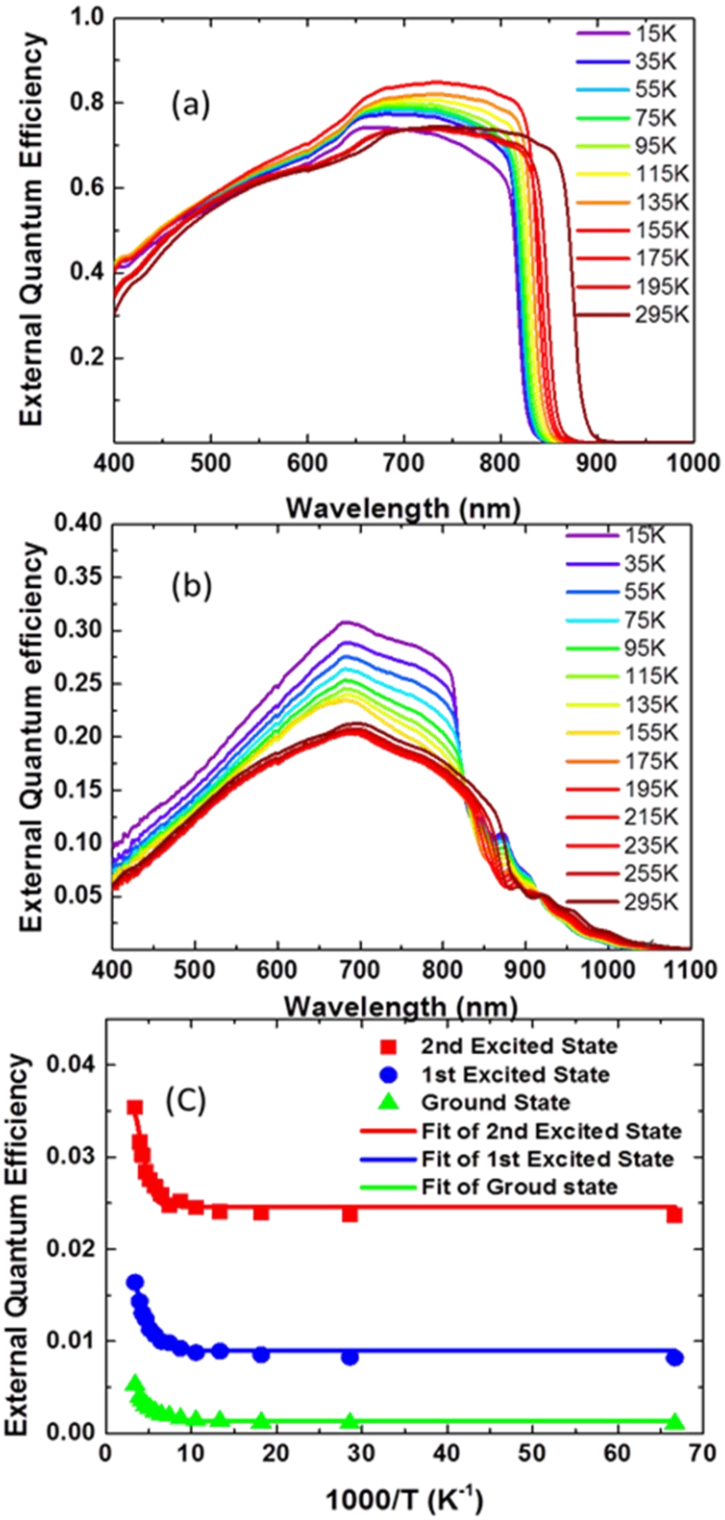

Figure 3.6 Temperature dependent EQE on (a) GaAs reference cell, (b) QDSC with InGaP barrier; (c) Arrhenius plot of EQE intensity from different confined transition for activation energy extraction of the QDSC with InGaP barrier.

To verify the hypothesis on the tunneling related carrier escape from the confined states and further detect the effects of electric field on carrier collection, Figure 3.7 shows 10K voltage bias dependent EQE used to eliminate the thermal coupling effect. The range of bias voltage is between -3.5 V reverse bias and 0.7 V forward bias; forward bias voltage above 0.7 V were unreliable as the increases forwards bias current. As mentioned, the strength of electric field increases with reverse bias, which leads to a faster transport rate across the intrinsic region. Compared to the room temperature EQE, the 10K EQE shows 50% improvements in all wavelength, due to reduced capture and and recombination rate. Similar to the room temperature measurements, the entire EQE (bulk absorption and sub-GaAs band gap absorption) increases with reverse bias voltage.

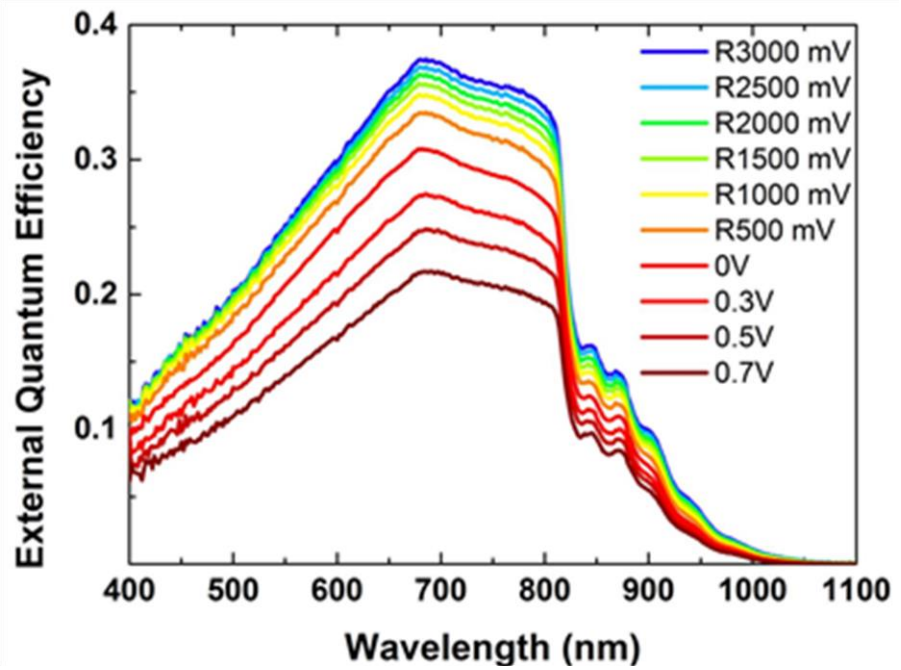

Figure 3.7 10K Voltage bias to the QDSC with InGaP barrier.

Additionally, Figure 3.8 shows extracted bias dependent EQE at different wavelength. As can be seen, with reverse bias from 0 V to -3.5 V, the slope of EQE verses bias voltage are increases from short wavelength of 400 nm to long wavelength of 800 nm. At

10K, the EQE of 400 nm is stable with reverse bias, while EQE 800 nm show 25% increment in -3.5V compared EQE at 0V. The phenomenon indicates that the increasing electric field mainly enhances hole tunneling rate and collection. As shown in Figure 3.4 (a), the absorption of photons at 400 nm is mainly in the p-emitter, so only electron has to transport across the intrinsic region. The absorption at 800 nm is along the entire device length. The n-type GaAs base length is 2000 nm, which almost three times longer than the total length (700 nm) of the emitter and intrinsic region so the hole also transport across the intrinsic region in order to be collected.

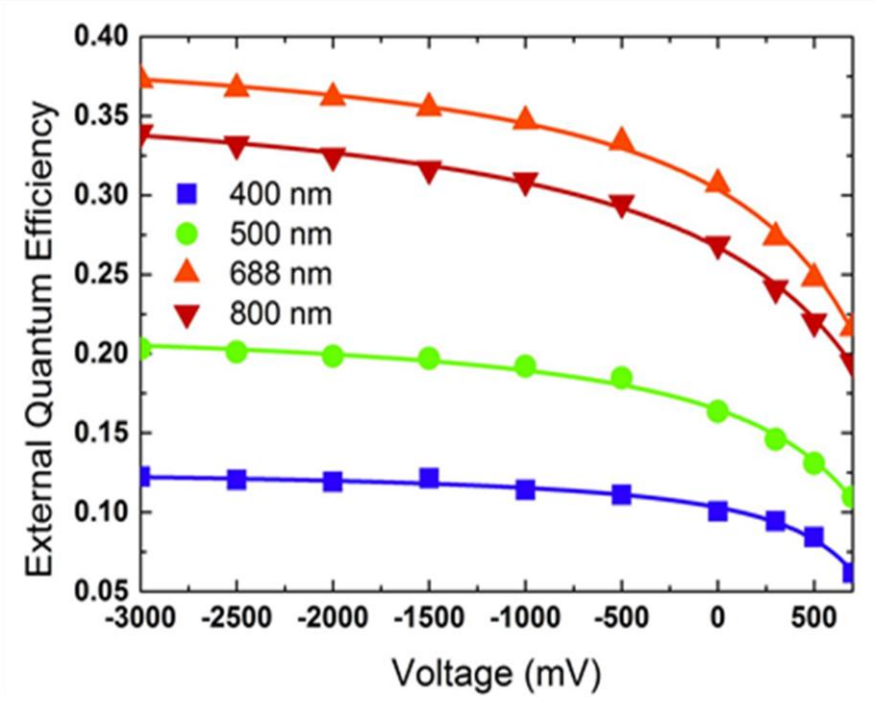

Figure 3.8 10K Voltage bias EQE on the QDSC with InGaP barrier at different wavelength

3.2.2 2nd Generation InAs/In$_{0.5}$GaP QD-IBSC

Sample and experiments

The 1st Generation InAs/InGaP QDs embeddend *p-i-n* GaAs device shows degraded carrier collection from the emitter and base, so InGaP was used in emitter and base to

reduce carrier blocking and recombination loss across the intrinsic region in the 2nd generation InAs/InGaP QD-IBSC. Due to the change of personnel, the 2nd generation InAs/InGaP devices were grown in a 3×2" Aixtron close-couple showerhead metal organic vapor phase epitaxy (CCS-MOVPE) reactor located at RIT. The polarity was switch from *p-i-n* to *n-i-p* due to the growth limitation on a p-typed doped wide-band-gap window layer on top of a p-type InGaP emitter.

Figure 3.9 shows the updated layer schematic for InAs/InGaP QD embedded *n-i-p* InGaP solar cells. After 50 nm p-type InGaP back surface field layer, a 1500 nm (5×10^{16} cm^{-3}) InGaP base was grown before the 600 nm intrinsic layers. Similar to the generation 1st InAs/InGaP QD super-lattice, an insertion of GaAs layer before and after InAs QD growth prevents the presence of InGaAsP alloys associated extra-large QD [77], [95], which degrades the quality of epi-layer growth and introduces defects that increase recombination around QD. This unit was repeated within the i-region for ten periods before completing the 100 nm n-emitter (2×10^{18} cm^{-3}) and 20 nm Si-doped (8×10^{17} cm^{-3}) AlInP window layers. Solar cells were then fabricated using standard III–V processing and microlithography techniques. Individual cells were isolated using wet chemical etching techniques. Anti-reflective coating was not applied. Measurements were still performed on 1×1 cm^2 mesa without grid fingers on investigated cells.

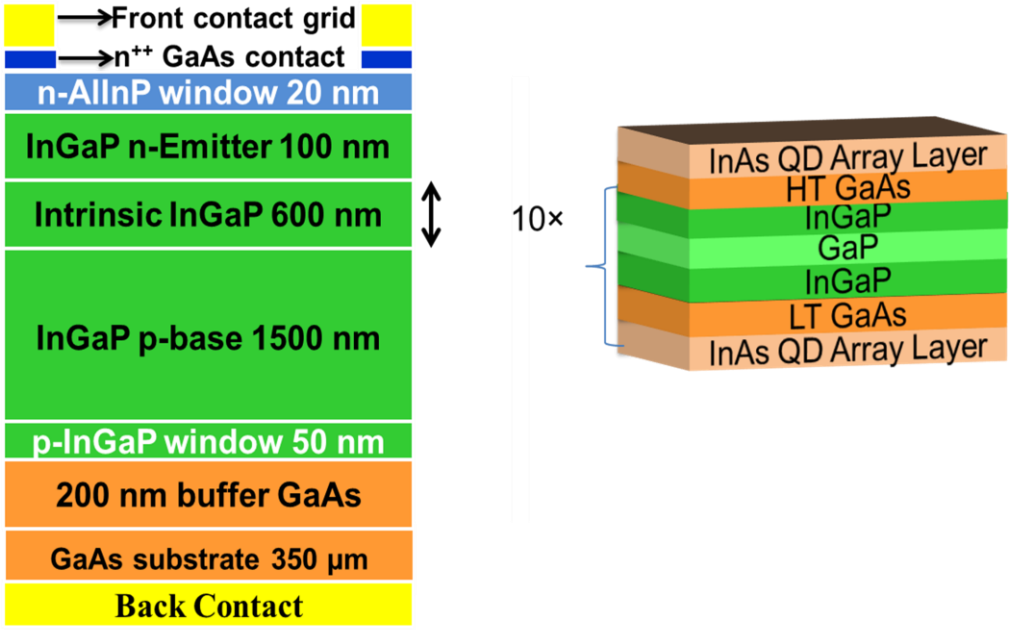

Figure 3.9 Structural layer layout for InAs/InGaP QD embedded InGaP *n-i-p* solar cell device.

One-sun AM1.5 illuminated IV measurements were performed with a two-zone TS Space Systems solar simulator with a Keithley 2400 SMU. EQE was completed with an IQE200 Spectroradiometric Measurement system. Voltage bias was applied with a Stanford 570 low-noise current preamplifier. Temperature dependent EQE measurements were analyzed using OL750 Spectroradiometric Measurement system in a Cryoindustries 10K M-22 cryo-system. The temperature was monitored via a thermal couples connected to a Lakeshore Model-330 temperature controller.

Results and discussion

Because QD-IBSCs can be used for both space and terrestrial applications, light IV measurements under 1 sun AM1.5 illumination were used to evaluate the solar cells performance on the 2nd generation InGaP solar cells. Figure 3.10 shows the room temperature IV curve of the *n-i-p* InGaP baseline and the InAs/InGaP QDSC. The

baseline InGaP without antireflection coating shows an excellent output efficiency of 12.3% with an open circuit voltage of 1.3 V. However, a significant degradation in the InAs/$In_{0.5}$GaP *n-i-p* QDSC in terms of short circuit current, fill factor and open circuit voltage. Table 3-1 summarizes the collected data. The degradation may be due to the increasing defects related recombination center during epitaxy layer growth. The strain introduced surface roughness is showed in the inset Nomarski image. The growth condition including temperature, III/V ratio and so on should be further optimized to achieve high quality InAs/$In_{0.5}$GaP QDSC structure.

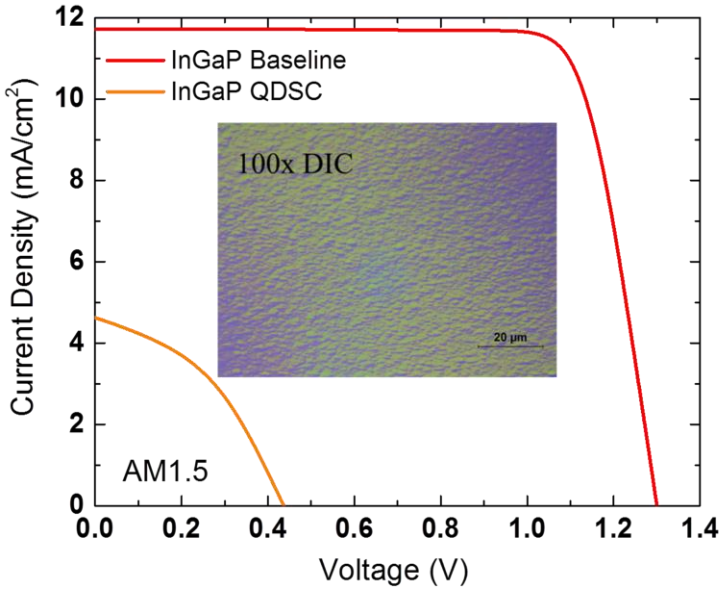

Figure 3.10 (a) IV curves of InGaP baseline and InAs/InGaP QDSC. The inset is Nomarski image of the InAs/InGaP QDSC surface that shows strain introduced surface roughness.

Table 3-1 Measured RIT grown *n-i-p* InGaP solar cells AM1.5 IV Characteristics

Sample	Jsc (mA/cm^2)	Voc (V)	FF (%)	Efficiency (%)
InGaP baseline	11.7	1.30	80.7	12.3
InAs/InGaP QDSC	4.6	0.44	41.1	0.8

The room temperature EQE measurements help to further analyze reasons for the short circuit current degradation. Figure 3.11(a) shows the EQE of the RIT grown *n-i-p* InGaP baseline and InAs/InGaP QDSCs. Compared to the $In_{0.5}GaP$ baseline, the InAs/InGaP QDSC shows large degradation in the short wavelength (300-700 nm), which correlates the reduced short circuit current J_{sc}. The large degradation of EQE in the bulk absorption of the InGaP QDSC may be due to the degraded material quality from coalesced QD and dislocations during QD growth [86].

Figure 3.11(b) shows the room temperature log scaled EQE spectra beyond the band edge of InGaP. InGaP QDSC shows an increased sub-band-gap carrier collection from QD absorption compared the baseline cell. The absorption edge of InAs/InGaP QDSC extends to 1200 nm, which is below the simulated sub-band-gap transition energy (1215 nm), as shown in Figure 3.1. The integrated InAs/InGaP sub-band-gap (> 680 nm) J_{sc} is 1.53 mA/cm^2 and the J_{sc} (>950 nm) is 112 μA/cm^2. The InAs/InGaP QD systems show the lower transition energy from IB to CB close to the ideal IBSC applications and enhanced >1000 nm carrier collection compared InAs/GaAs QDSCs in literature [56].

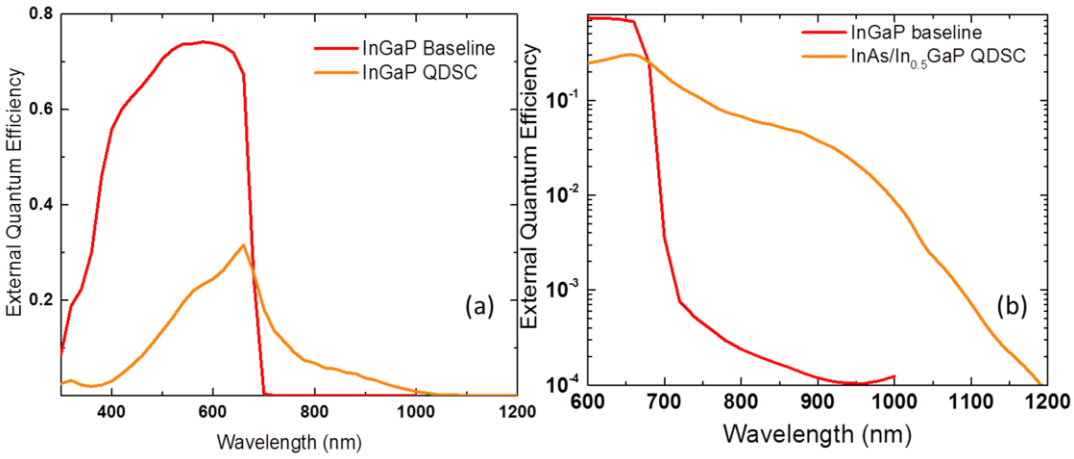

Figure 3.11 Room temperature EQE of the RIT grown *n-i-p* (a) $InGa_{0.5}P$ baseline and QDSCs (b) sub-InGaP bandgap EQE in log-scale.

In order to detect carrier collection in the *n-i-p* $In_{0.5}GaP$ QDSC, voltage biased carrier collection efficiency (CCE) measurements were conducted. The CCE concept was proposed by Fujii *et al.* [117], which is originally defined as a ratio of the number of carriers extracted as a photocurrent to the total number of the carriers photo-excited within the p-n junction area. However, because there are several loss channels including dark current subtraction, radiative recombination, carrier capture in the QDs or QWs, etc, it is difficult to measure carrier loss during the transport with embedded QDs or quantum wells (QWs). It is more reasonable to consider that, at any given temperature, voltage bias dependent CCE is ratio of the number of carriers being collected at arbitrary voltage to the number of carriers being collected under maximum reverse bias during the test. This is due to reverse bias will increase the width of depletion region. There less diffusion introduced dark current flows across *pn* junction, so more photo-excited minority carriers can be collected and vice versa. On the other hand, for QDs embedded region, more carriers escape from these confined levels, and then generated photocurrent due to increasing tunneling and thermal escape. Since EQE is the number of carrier being collected divided by the number of photon into a PV device, based on the assumption that absorption won't change with bias, CCE can also be interpret as Equation 3.2

$$CCE(\lambda, V) = \frac{EQE(\lambda,V)}{EQE(\lambda,V_{reverse\ maximum})} \qquad 3.2$$

Figure 3.12 shows the voltage bias dependent CCE [118] at 500 nm and 1000 nm. The reverse bias was varied from -3 V to 0 V, corresponding to a change in the electric field around QD from 14 kV/cm to 65 kV/cm. Both 500 nm and 1000 nm CCE largely increases with increasing electric field. All minority holes absorbed by the emitter and front layer of intrinsic region have to transport through the QD matrix prior to being

collected in the *n-i-p* InAs/InGaP QDSC. For the degradation of 500 nm under zero bias, the minority holes could be captured into QDs [119], because of slower mobility introduced low carrier velocity under low electric field. Furthermore, the captured minority hole cannot be easily swept out from InAs/InGaP QD, which is due to deeper hole confinement (the difference between the hole ground state to the InGaP valence bandedge is 0.62 eV) than electrons confinement (the difference between ground state electron and InGaP conduction band is 0.29 eV), as shown in Figure 3.1. With increasing electric field intensity, the velocity of the holes across the intrinsic region increases, which reduces the capture probability. The CCE from sub-band-gap absorption (1000 nm) increased with reverse bias due electric field enhanced carrier escape [113] and extended radiative lifetime. As discussed in chapter 2, the extended radiative lifetime results from the reduced wave function overlap between electron and holes [120][51].

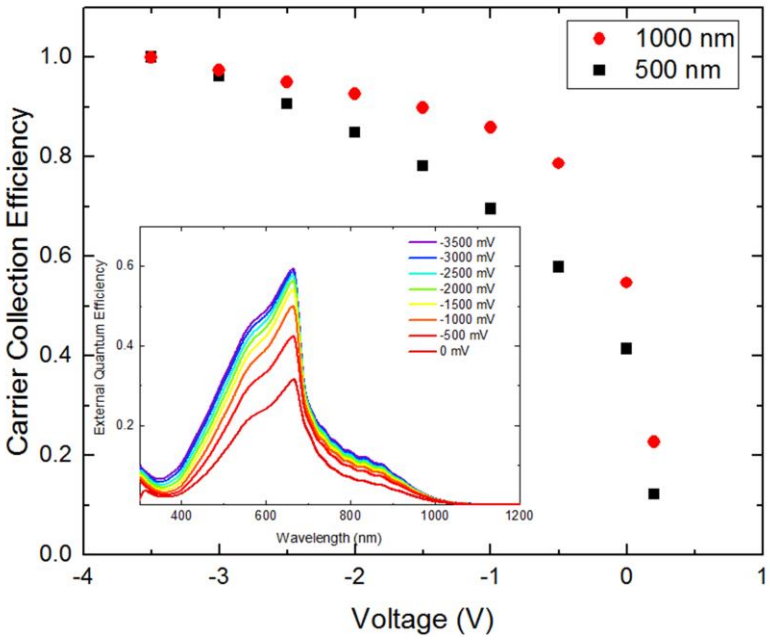

Figure 3.12 Room temperature voltage bias CCE at 500 nm and 1000 nm on the *n-i-p* InAs/$In_{0.5}$GaP QDSC. The inset is the voltage bias EQE.

3.3 Development of InAs/$Al_{0.3}$GaAs QD-IBSC

3.3.1 Introduction

To reduce thermal escape from QDs and achieve the highest IBSC conversion efficiency of 63% under maximum solar concentration, the optimized band gap values are 1.96 eV [44] for the host material, and 1.24 eV and 0.72 eV between the VB-IB and IB-CB, respectively. It has been proposed to use wide-band-gap materials including $In_{0.5}$GaP (1.9 eV at 300K) [95], [121] or $Al_{0.3}$GaAs (1.84 eV at 300K) [13], [14] as the host material. As discussed in Section 3.2, because InAs/$In_{0.5}$GaP QDs have deeper confinement than the InAs/$Al_{0.3}$GaAs QD system [122], a large loss in carrier collection was observed due to hole capture and recombination in the QDs [121], [122].

The ideal use of $Al_{0.3}$GaAs barriers would be without the integration of any GaAs wells within the superlattice (SL), however that is challenging since $Al_{0.3}$GaAs often getters oxygen, which creates trap states at the QD interface if QDs are grown directly on $Al_{0.3}$GaAs [78]. Furthermore, the $Al_{0.3}$GaAs growth temperature necessary for direct growth of InAs QDs is lower than the optimal temperature for $Al_{0.3}$GaAs, so the optical and electrical properties are degraded [123]. To achieve high quality crystalline films, InAs/GaAs/$Al_{0.3}$GaAs Dwell SL was used, which shows suppressed thermal escape in previous studies [122], [123]. This section evaluates the performance of an MOCVD grown InAs/$Al_{0.3}$GaAs Dwell IBSC. Band structure was simulated to evaluate the insertion of a GaAs layer on the electron confinement depth. Besides room temperature IV and EQE measurements, room temperature voltage bias experiment was used to detect carrier collection efficiency under different bias condition. Temperature dependent EQE measurements were used to experimentally detect carrier thermal escape and extract activation. This section also demonstrates temperature and voltage-bias dependent TSPA

in the Dwell structure by directly measuring TSPA-introduced photocurrent. To further improve device design, this section discusses the roles of absorption, recombination and charge separation on TSPA.

3.3.2 Simulations on InAs/$Al_{0.3}$GaAs QD systems

Using eight band ***k•p*** calculation [99] that discussed in chapter 2, a Poisson-Schrodinger solver was written in C^{++} program with material parameters from the most cited literature [59]. Figure 3.13 shows the simulated band structure at 300K of InAs QD directly grown on $Al_{0.3}$GaAs with a diameter and height of 20 nm and 2 nm, respectively. The band gap of $Al_{0.3}$GaAs is 1.84 eV at room temperature, which is close to the optimized host material (1.96 eV) shown in Figure 1.3(a). The calculated ground state electron barrier height relative to the $Al_{0.3}$GaAs (E_L) is close to 400 meV.

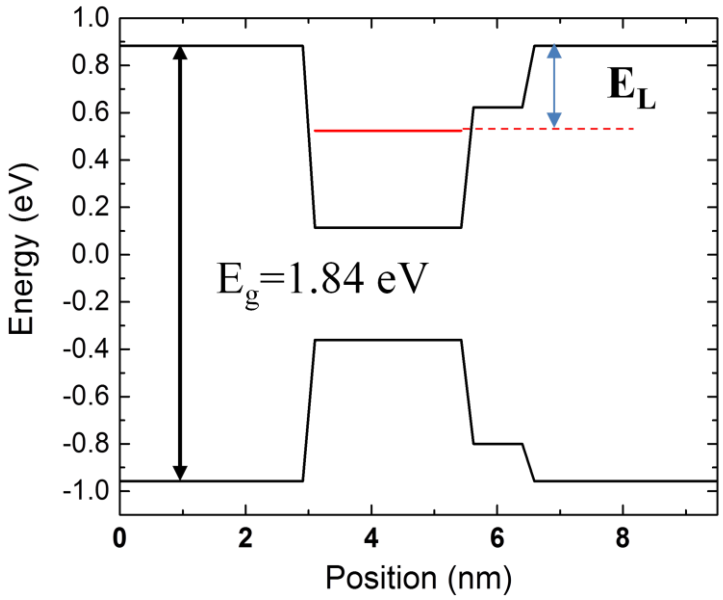

Figure 3.13 room temperature band-structure simulation of InAs/$Al_{0.3}$GaAs QD via eight-band ***k·p*** method

With the extracted electron ground state barrier height from the band structure simulation, the electron thermal escape rate is estimated via Equation 2.2, which is $10^7 s^{-1}$ at 300K. The optical generation rate is shown in Equation 3.3

$$R_{optical} = \sigma_{optical} \times \Phi \qquad 3.3$$

Where $\sigma_{optical}$ is the optical capture cross section[75], [76]; Φ is the photon flux given by the irradiance from the solar spectrum that would excite transitions between InAs QD states and $Al_{0.3}GaAs$ conduction band. The optical cross section for InAs/$Al_{0.3}$GaAs QDs is not well characterized, but it can be approximated by average measurement results from InAs/GaAs QDs, where $\sigma_{optical}$ is 1×10^{-14} cm^2 [124]–[126]. Figure 3.14 shows a comparison of the optical and thermal escape rate under varied solar concentration. The thermal escape dominates at AM1.5 illumination, while TSPA can be dominant under 1000 suns concentration of AM1.5 illumination with the slower thermal escape rate at room temperature in the InAs/$Al_{0.3}$GaAs matrix. This result shows that InAs/AlGaAs QD-IBSC is promising to function at room temperature.

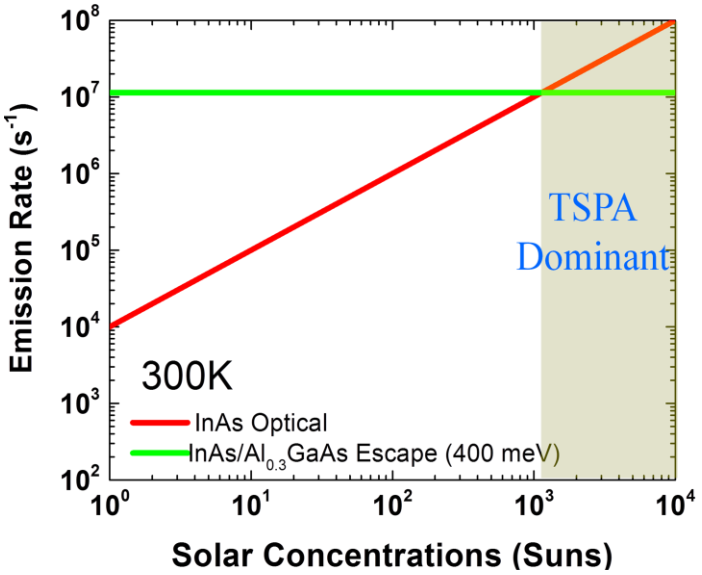

Figure 3.14 Optical (red) and thermal emission (green) rate of electrons in InAs/$Al_{0.3}$GaAs QD under different solar concentration.

An insertion of a GaAs inter-layer between $Al_{0.3}GaAs$ and InAs QD can improve the QD surface density and optical performance [127], while a room temperature IBSC requires a deep confined states to reduce thermal escape. As shown in Figure 3.15, band structure simulations are used to estimate the effect of the insertion GaAs layer thickness on the ground state confined electron depth. The inset shows the repeat layer structure of $InAs/Al_{0.3}GaAs$ QDs. After the QDs formation directly on $Al_{0.3}GaAs$ or the GaAs inter-layer, the QD is capped followed a low temperature GaAs layer. Then a 4.6 nm $Al_{0.3}GaAs$ barrier layer is placed, followed by a GaP strain-balancing layer. Because of an increment of quantum confined well width (3 nm to 6 nm), the ground state electron barrier height E_L increases (from 355 meV to 390 meV) with increasing GaAs interlayer thickness. As a result, the insertion of the GaAs layer could be adopted as a method to improve QD quality and maintain the confinement depth of electron.

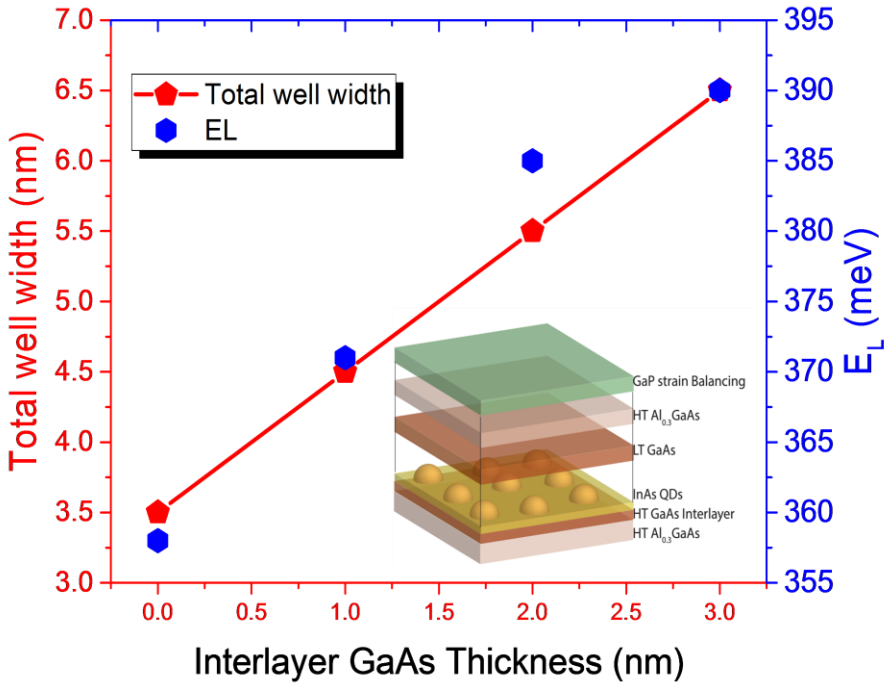

Figure 3.15 Electron confinement depth in $InAs/Al_{0.3}GaAs$ with varied GaAs interlaver thickness. The inset is a sketch of OD laver structure.

3.3.3 Experimental

Figure 3.16 shows the investigated cell structure of 10-layers of InAs QDs embedded in an *n-i-p* $Al_{0.3}GaAs$ solar cell. This cell was grown in a 3×2" Aixtron close-couple showerhead metal organic vapor phase epitaxy (CCS-MOVPE) reactor on a Zinc-doped GaAs substrate with a 2^0 offcut towards the (110) orientation. The metalorganic precursors used were trimethylindium, trimethygallium, trimethyaluminum, and arsine, with disilane as the n-type dopant for the 50 nm (1×10^{18} cm^{-3}) $Al_{0.3}GaAs$ emitter and diethylzinc as the p-type dopant for the 1500 nm (5×10^{16} cm^{-3}) $Al_{0.3}GaAs$ base. The average built-in electric field across the 10-layer QD superlattice in the 600 nm intrinsic region is 14 kV/cm based on Sentaurus Device^{TM} simulations. In the QD superlattice, prior to the formation of InAs QDs, 3 nm of GaAs was grown after 3 nm of $Al_{0.3}GaAs$ to prevent the intermixing of aluminum near the InAs QDs [127]. InAs QDs are formed by the strain-driven Stranski-Krastanow growth mode with InAs coverage between 1.8 ML-2.0 ML. After QD formation, the QD layer is capped with a low temperature 3 nm GaAs layer to maintain the InAs QD height during the following high temperature $Al_{0.3}GaAs$ layer. The 4.6 nm $Al_{0.3}GaAs$ barrier layer is grown at 620^{o}C, and is followed by a GaP strain-balancing layer. The investigated $Al_{0.3}GaAs$ PV devices were fabricated using standard III–V processing techniques as demonstrated in Chapter 1. Individual cells were isolated using wet chemical etching techniques. No anti-reflective coating was applied. Measurements were performed on 1×1 cm^2 mesa-isolated device without grid fingers.

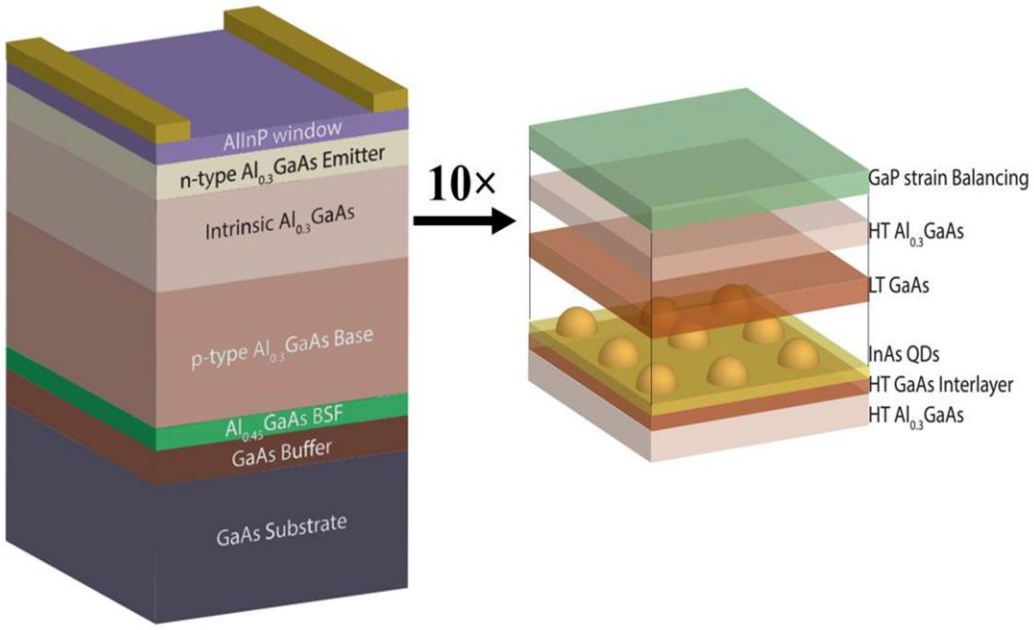

Figure 3.16 Structural layer layout for QD embedded GaAs p-i-n solar cell device

One-sun AM1.5 illuminated IV measurements were performed with a two-zone TS Space Systems solar simulator with a Keithley 2400 SMU. EQE was completed with an IQE200 Spectroradiometric Measurement system. Voltage bias was applied with a Stanford 570 low-noise current preamplifier. The low temperature external quantum efficiency (EQE) data was collected via an OL750 spectroradiometric measurement system. Additional temperature-dependent photoluminescence (TDPL) experiments were completed by pumping the sample with a 100 mW 532 nm laser, and the PL signal was detected with an InGaAs detector and a Princeton Instrument monochromator. Atomic force microscopy (AFM) measurements were completed with a Bruker Dimension 3100 scanning probe micrometer. The statistical analysis of the surface QDs was achieved with the image recognition software SPIP^{TM} by Image Metrology. The experimental set up for the TSPA-introduced photocurrent measurement setup is shown in Figure 2.10. A Cryoindustries 10K M-22 cryo-system, with a CaF_2 window to reduce the loss of infrared

(IR) input light, was used to cool the sample to 30K. A continuous monochromatic light generated by a Tungsten lamp was used to pump carriers from the VB to IB, while a second IR photon source (Omega 800^0C blackbody radiation sources with 1500 nm filter and 14mW 1300 nm laser) is coincident upon the sample to enable the second photon excitation from the IB to CB. A chopper is positioned in front of the IR light source in order to generate an alternating current (AC) signal of the carrier collection from the IB-CB optical transition.

3.3.4 Results and discussions

Figure 3.16 (a) shows the IV curves of the $Al_{0.3}GaAs$ baseline and InAs/$Al_{0.3}GaAs$ Dwell-IBSC and table 3-2 summarize the measured results. $Al_{0.3}GaAs$ baseline and QDSCs shows 6.6% efficiency with an open circuit voltage of 1.26 V, while the efficiency of the InAs/$Al_{0.3}GaAs$ Dwell-IBSC is 4.0% with a degraded open circuit voltage of 0.96 V. Both baseline and Dwell-IBSC shows a degraded short circuit current around 7 mA/cm^2, which indicates similar layer degradation in both cells. To investigate carrier collection at short circuit condition, Figure 3.16 (b) shows the short wavelength EQE (300-600 nm) reduction in both the $Al_{0.3}GaAs$ baseline and the InAs/$Al_{0.3}GaAs$ QDSCs. It indicates that the n-doped $Al_{0.3}GaAs$ emitter growth should be optimized to reduce the oxidized non-radiative trap centers. The integrated sub-$Al_{0.3}GaAs$ band-gap J_{sc} is 1.17 mA/cm^2 in the InAs/AlGaAs Dwell-IBSC, which correlates the larger J_{sc} in the Dwell-IBSC than the baseline in Figure 3.17(a).

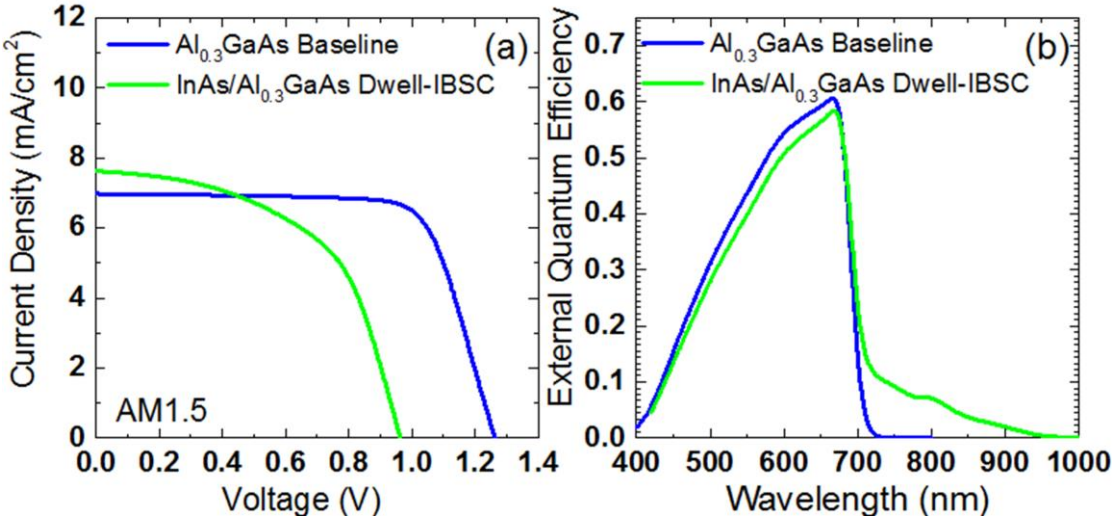

Figure 3.17 300K (a) AM1.5 IV curves of $Al_{0.3}GaAs$ baseline and InAs/$Al_{0.3}GaAs$ Dwell QDSC (b) EQE of the investigated $Al_{0.3}GaAs$ PV devices.

Table 3-2 Measured RIT grown *n-i-p* InGaP solar cells AM1.5 IV Characteristics

Sample	Jsc (mA/cm^2)	Voc (V)	FF (%)	Efficiency (%)
$Al_{0.3}GaAs$ Baseline	7.0	1.26	74.9	6.6
InAs/$Al_{0.3}GaAs$	7.6	0.96	54.3	4.0

Dwell DDwellIBSC

To theoretical verify the hypothesis on the degraded $Al_{0.3}GaAs$ emitter introduced short-wave length photon excited carrier collection, Sentaurus TCAD was used to fit the experimental EQE measurements. As mentioned, Sentaurus TCAD is an iterative solver for the Boltzmann and Poisson equations capable of simulating electrical characteristics of semiconductor devices, so carrier lifetime of emitter and base can be extracted from the fitting. Figure 3.18 shows the fitted curve of the $Al_{0.3}GaAs$ baseline. The extracted hole in the emitter is less than 1 ns. Two methods can be used to improve carrier collection in $Al_{0.3}GaAs$ device: (1) increase the emitter growth temperature to reduce Al-

O bonding introduced non-radiative recombination center during MOCVD growth; (2) reduce the thickness of the emitter.

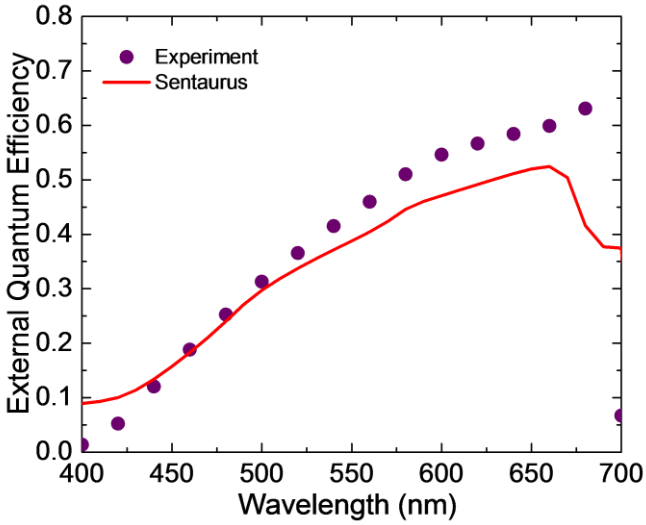

Figure 3.18 Fitted $Al_{0.3}GaAs$ baseline EQE curve from Sentaurus TCAD to extract carrier lifetime.

Furthermore, to experimentally verify the hypothesis on the degraded emitter reduction of the short wavelength carrier collection, Figure 3.19 shows the room temperature voltage bias EQE of the InAs/$Al_{0.3}GaAs$ Dwell-IBSC. The CCE at 1000 nm is stable to a reverse bias of up to -3V, which indicates that almost all carriers generated from sub-band-gap absorption are collected under short circuit conditions from InAs/$Al_{0.3}GaAs$ matrix. The CCE of 500 nm slightly increases with reverse bias voltage, which is also associated with the electric field mitigated loss of the minority holes during transport across the intrinsic region. With increasing forward bias from 0 V to 0.5 V, both 500 nm and 1000 nm CCE decrease with forward bias. The forward bias flattens the band in the intrinsic region by reducing the electric field, which increases the carrier loss in recombination because inhibited separation of electron and holes.

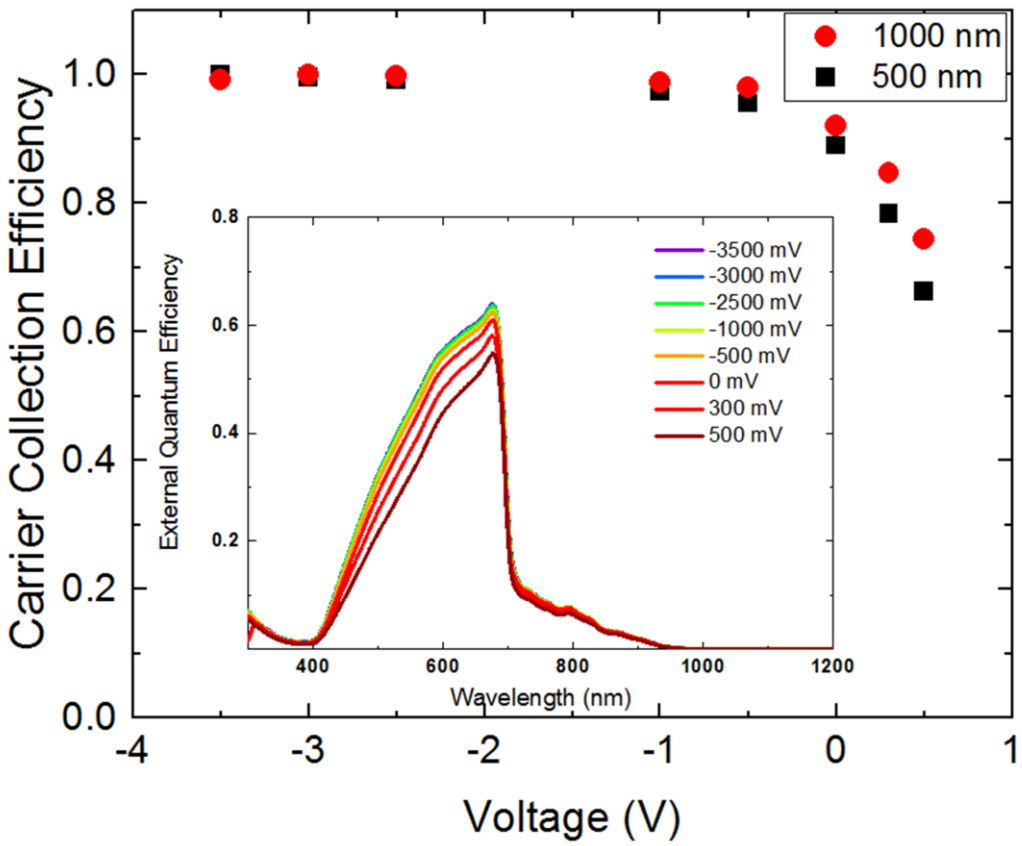

Figure 3.19 Room temperature voltage bias CCE at 500 nm and 1000 nm on the nip InAs/$Al_{0.3}$GaAs QDSC. The inset is the voltage bias dependent EQE.

To characterize carrier collection from Dwell confined region, Figure 3.20 shows the log-scaled sub-$Al_{0.3}$GaAs band gap EQE and PL measurements. The InAs QD ground state is around 1000 nm as shown in the measured PL curve. InAs/$Al_{0.3}$GaAs Dwell absorption edge is around 1100 nm. According to the simulation shows in the plot the ground state transition energy of 2 nm InAs/$Al_{0.3}$GaAs is 1.07 eV (~1158 nm), so the blue shifted absorption edge indicates that the height of QD in the InAs/$Al_{0.3}$GaAs Dwell-IBSC may be smaller than 2 nm. However, compared to the conventional InAs/GaAs QDSCs in literature [128], the InAs/$Al_{0.3}$GaAs systems show the lower transition energy from IB to CB close to the ideal IBSC applications and enhanced carrier collection above 1000 nm.

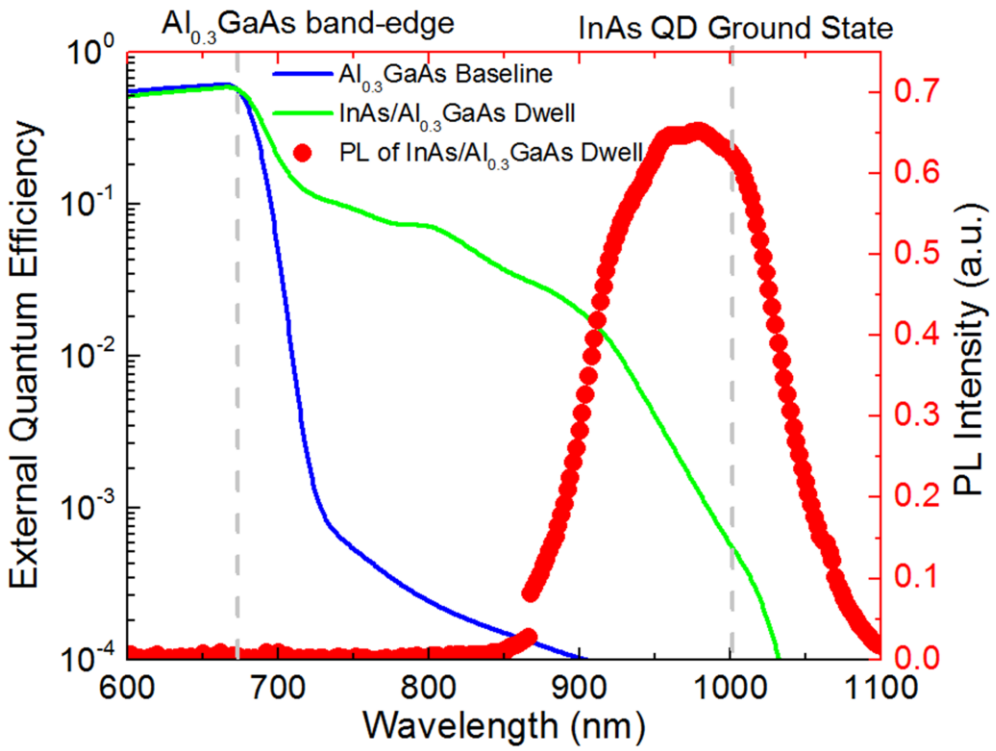

Figure 3.20 Room temperature log-scaled EQE of the *n-i-p* InAs/$Al_{0.3}$GaAs devices and PL curves of the Dwell-IBSC

Figure 3.21 shows the normalized EQE measured at 1000 nm with respect to temperature of the InAs/$Al_{0.3}$GaAs QDSC sample, which was used to extract the activation energy. The thermal escape is the dominant process in the deep sub-band-gap carrier collection [43], because the second photon process is too slow (10^3 s^{-1}) to be considered at low intensity input mono wavelength light, and the tunneling rate(10 s^{-1}) from deep confined level is negligible at the electric field below 15 kV/cm [129]. The thermal activated spectral response at 1000 nm is suppressed to 0.01 when temperature is below 200K. Using the Equation 2.6, the extracted activation energy E_a is 324 meV. Such deep activation energy in the InAs/$Al_{0.3}$GaAs QDSC is promising for the IBSC application by suppressed tunneling and thermal escape. The extracted activation is lower than the predicted barrier height of 380 meV in the simulation, which may be due to the

insertion of GaAs interlayers or the varied composition of the QDs during the growth. The inset of temperature dependent EQE shows all sub-bandgap spectral response including the shallow confinement around 700 nm decreasing with lowering temperature from 300K to 20K, which indicates that carrier collection from shallow confinement is also dominated via thermal escape. The tunneling from the excited states and wetting layer is also mitigated by using $Al_{0.3}GaAs$ as barrier.

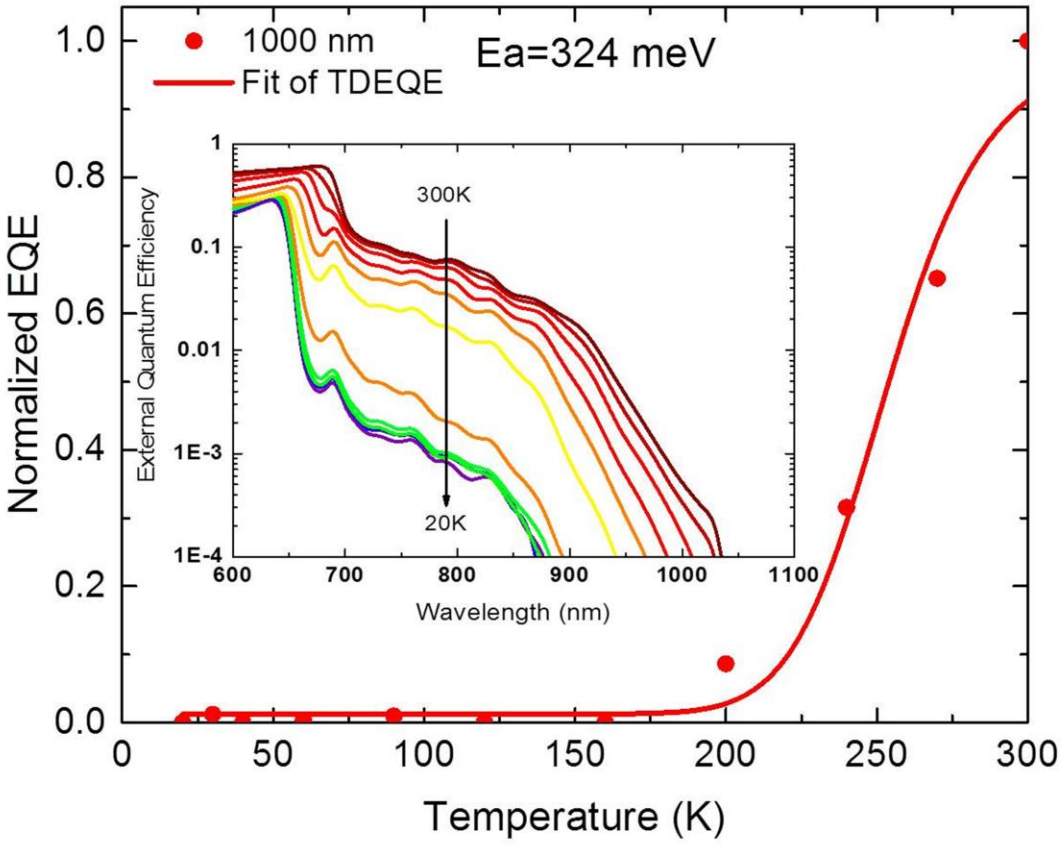

Figure 3.21 Normalized EQE from InAs/$Al_{0.3}GaAs$ QDSC with varied temperature from 300K to 20K at 1000 nm. The inset is the temperature dependent EQE.

In order to the investigated InAs/$Al_{0.3}GaAs$ QDSC for IBSC applications, Figure 3.22(a) shows the measured temperature-dependent TSPA-introduced photocurrent using a 1500 nm band pass filter filtered 800°C blackbody source as the second light source.

With increasing temperature, the TSPA signal decreases due to increasing carrier thermal escape from the confined level. The increased electron barrier height [122] relative to $Al_{0.3}GaAs$ allows TSPA-introduced photocurrent to be observed even at 80K. TSPA via filtered 800^0C black body excitation is mainly from the GaAs/$Al_{0.3}GaAs$ quantum well (650-850 nm). This was also observed by Asahi *et al.* [123] in their Dwell structure. Figure 3.22(b) shows the temperature dependent TSPA using the 1300 nm laser as the second photon sources, which also shows a decrement with increasing temperature. Because of the increment of the incident photon density, the threshold temperature for TSPA is up to 110K. Compared to Figure 3.22(a), the TSPA intensity increases an order at the same wavelength, while the shape of the curve is also different: TSPA decreases slowly towards a longer wavelength. Furthermore, Figure 3.22(a) shows almost zero TSPA photocurrent from QD optical transitions (>850 nm), while Figure 3.22 (b) shows observable TSPA above 900 nm. Figure 3.22 (c) shows the 40K EQE and PL measurements, indicating the band-edges of $Al_{0.3}GaAs$ and GaAs are around 640 nm (1.93 eV) and 840 nm (1.48 eV) respectively, while the QD ground state PL emission is around 920 nm (1.35 eV).

The elimination of TSPA at the ground state may be due to limited optical generation rates from the VB to IB, where the optical generation rate depends on the product of the incident photon flux and the optical cross-section of the investigated QDs [75], [76]. The incident photon flux is limited by the filtered black body light sources: integrated band radiance (1500 nm-10 μm) of 2.17×10^4 W/m^2/Sr is two orders of magnitude lower than the integrated band radiance of 2.56×10^6 W/m^2/Sr from the Sun (a 6000K black body). Meanwhile the optical cross-section is affected by the QD absorption coefficient that

strongly depends on the QD surface density. A 1×1 μm^2 AFM image of InAs QDs is shown in the inset of Figure 3.22(a). A QD density of 8.4×10^9 cm^{-2} explains the small QD absorption.

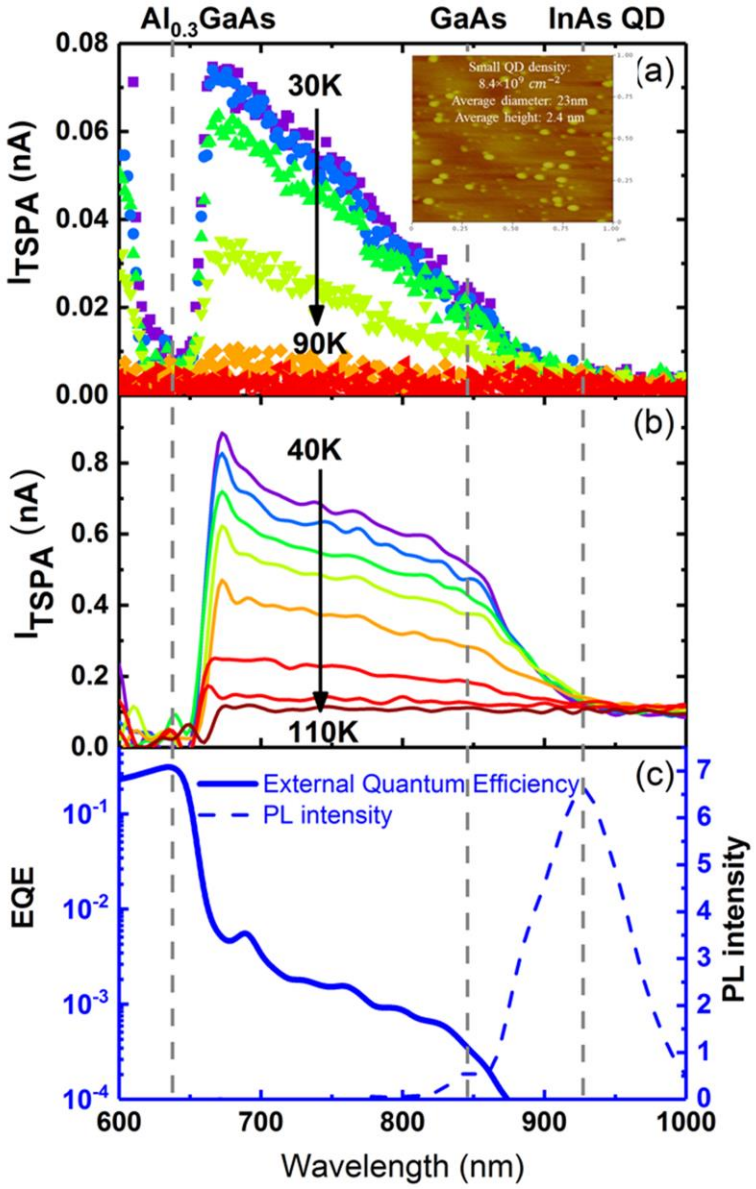

Figure 3.22 (a) Temperature dependent TSPA using 800°C black body sources with 1500 nm filter, with inset of 1×1 μm^2 AFM. (b) Temperature dependent TSPA using 14 mW 1300 nm laser (c) 40K EQE and PL measurements

The experimental TSPA performance in terms of working temperature and optical generation rate can be improved by increasing incident light concentration, photon recycling, improved QD surface morphology, and number of layers of QDs. On the other hand, Figure 3.22(a) and Figure 3.22(b) both show that TSPA decreases at longer wavelengths. This interesting phenomenon was also observed in other types of QD systems [130], [131], which contradicts the argument that fast escape via thermal means or tunneling eliminates the TSPA from shallow confined levels (650-850 nm). To quantitatively analyze temperature-dependent TSPA, Normalized TSPA is used to exclude the factor of carrier density in the confined levels that depends on the absorption from the VB to a certain confined level. The normalized TSPA intensity is a ratio between the optical generation rate (R_{TSPA}) over the other competing processes including thermal escape, recombination, and tunneling, which can be summarized in the rate Equation 3.4

$$I_{TSPA_{normalized}} = \frac{R_{TSPA}}{R_{TSPA}+R_{r\&t}+Aexp(\frac{-E_a}{kT})} \quad 3.4$$

where $Aexp(-E_a/kT)$ is the term for thermal escape rate that exponentially increases with temperature, A is the constant of thermal escape depending on the mass of the escaped carriers and average height of the QDs, k is the Boltzmann constant, T is the temperature and E_a is activation energy. $R_{r\&t}$ is the total rate of recombination and tunneling, which is considered stable with temperature. Figure 3.23 (a) shows the normalized TSPA intensity at 700 nm and 800 nm with temperature varied from 30K to 90K. The extracted activation energies are 80±3 meV and 94 ±3 meV for 700 nm (1.77 eV, 160 meV band-offset from $Al_{0.3}GaAs$) and 800 nm (1.55eV, 380 meV band-offset from $Al_{0.3}GaAs$),

respectively. Figure 3.23(b) shows the shows the normalized TSPA intensity from the laser excitation at 700 nm (QW region) and 870 nm (InAs QD region) with temperature varied from 40K to 110K. The extracted activation energies are 38±3 meV and 41 ±3 meV for 700 nm and 870 nm, respectively. Unlike the activation energies extracted from temperature-dependent EQE or PL measurements that associate rate-limiting carriers and different electron-hole models [132], the activation energy extracted from TSPA only belongs to electrons in a certain confined level.

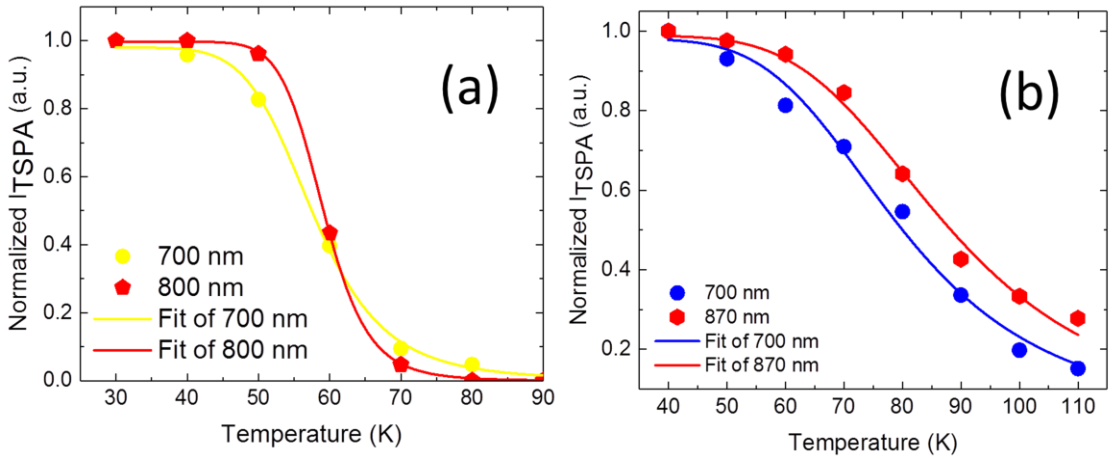

Figure 3.23 (a) Normalized TSPA intensity from 800°C black body source with varied temperature from 30K to 90K at 700 nm and 800 nm.(b) Normalized TSPA intensity from 800^0C black body source with varied temperature from 40K to 110K at 700 nm and 870 nm.

To discuss the physics behind the extracted activation energy from TSPA measurements with difference IR sources, Figure 3.24 shows the band structure simulation of a single Dwell at 40K under short circuit conditions (electric field is 14 kV/cm). The energy difference between the electron ground state and excited state is 93 meV, which is close to these extracted activation energies from 800^0C black body sources excitation, while the activation energies extracted from laser excitation are consistent with the difference between GaAs band-edge and electron excited states (41 meV). These activation energies

extracted from TSPA using difference light sources may be due to the IB-CB transition peaks at certain wavelength [133], [134]. As mentioned in Equation 3.3, TSPA rate depends on the product of optical cross-section and incident photo flux. Compared to the filtered 800°C black body source with a board spectrum tail above 1500 nm, the 1300 nm laser is mono-wavelength with higher photon flux. Thus, the efficient IB-CB transition under 800C black body sources may be from the electron ground state, while the efficient IB-CB transition under laser excitation may be from electron excited states.

Additionally, the energy difference between each of the localized energy levels and the edge of the conduction band is referred to as the barrier height of the electron. The barrier height of the InAs QD ground state electron (E_L) is 392 meV, which eliminates electron tunneling and thermal escape towards 40K. However, the E_L is larger than the experimentally extracted activation energy (E_a=324±8 meV) from the TDEQE measurements. The difference between the simulation and experiments could be two possible reasons: first, the extracted activation energy is an average value of the barrier height at different temperatures instead of at 40K. Second, the buried QD height was slightly smaller than the surface QD from the AFM image due to the capping processes in MOCVD [123].

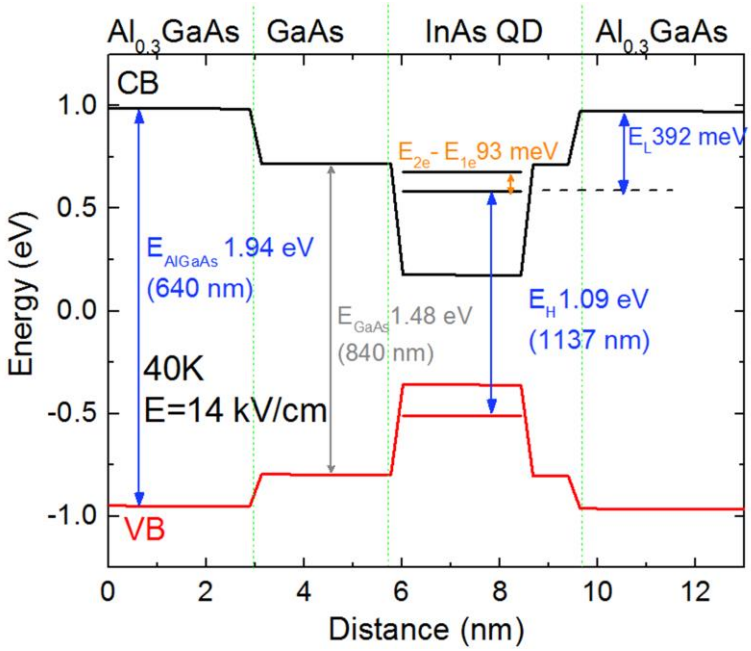

Figure 3.24 Calculated band structure of a single Dwell with local electric field under short circuit conditions at 40K

Also the extract ratio of R_{r+t}/R_{TSPA} is below 0.02, which indicates slow recombination and tunneling at the TSPA-active QD layer. To explain the dynamic carrier processes occurring in the temperature-dependent TSPA measurements towards an understanding that leads to design optimization, Figure 3.25 shows a simplified band structure of the *n-i-p* Dwell IBSC that depicts absorption, recombination, and charge separation. Absorption of photons with energy lower than the $Al_{0.3}GaAs$ bandgap generates electron-hole pairs in the confined levels formed by $Al_{0.3}GaAs$/GaAs quantum wells and the InAs wetting layer on GaAs. The photo-excited carriers in the shallow confined levels can then escape, either by thermal escape or tunneling. After a carrier escapes, it is possible that it could be recaptured to the confined states and repeat the above process. The photo-excited carriers left in the confined states can either be excited by TSPA, relax to a lower confined energy level, or recombine.

Due to a built-in electric field across the intrinsic region, the number of electrons may be not equal to the number of holes in a given layer [101]. This charge separation along the growth direction reduces the carrier recombination rate inside the QDs [45] and increases the electron lifetime [135]. This is significant at low temperature, where the TSPA rate mainly competes with the radiative recombination rate because of the reduced thermal escape resulting from deeper QD confinement [136]. Despite the lower TSPA rate at the shallow confined states, TSPA can still pump carriers out after relaxation into the deep confined level and be detected. Furthermore, because of the lower density of states in deeper confinement, the number of photo-excited carriers decreases with longer wavelength below the bandgap. The total number of carriers that relax into deeper confined levels may also decrease, which decreases state filling and the TSPA absorption coefficient. Therefore, TSPA signal decreases towards longer wavelengths (deeper confinement) as shown in Figure 3.24(a)/(b).

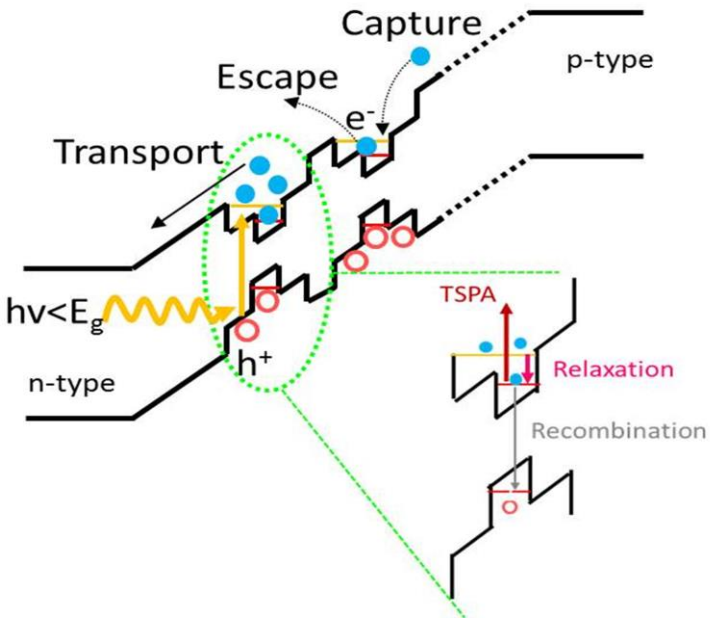

Figure 3.25 Simplified band diagram of the *n-i-p* InAs/GaAs/$Al_{0.3}$GaAs Dwell solar cell at 30K.

To verify the hypothesis discussed above, Figure 3.26 shows the voltage-biased TSPA-introduced photocurrent measurements at 40K, which is consistent with the voltage bias results of the InGaAs/GaAs QDSC [130]. It was observed that the TSPA signal is stable with reverse bias from 0 V to -2 V. The increasing electric field with reverse bias improves the charge separation that increases the recombination lifetime but also increases the tunneling rate. Stable TSPA is a balance between the rates of recombination and tunneling. Increased tunneling enables faster carrier escape from shallow confined states, which reduces the number of carriers relaxing into the QDs and ultimately decreases TSPA photocurrent, so TSPA is quenched with further reverse bias at -3 V. On the other hand, forward bias reduces both the electric field around the QD region as well as charge separation, so fast recombination in the shallow confined states limits TSPA photocurrent.

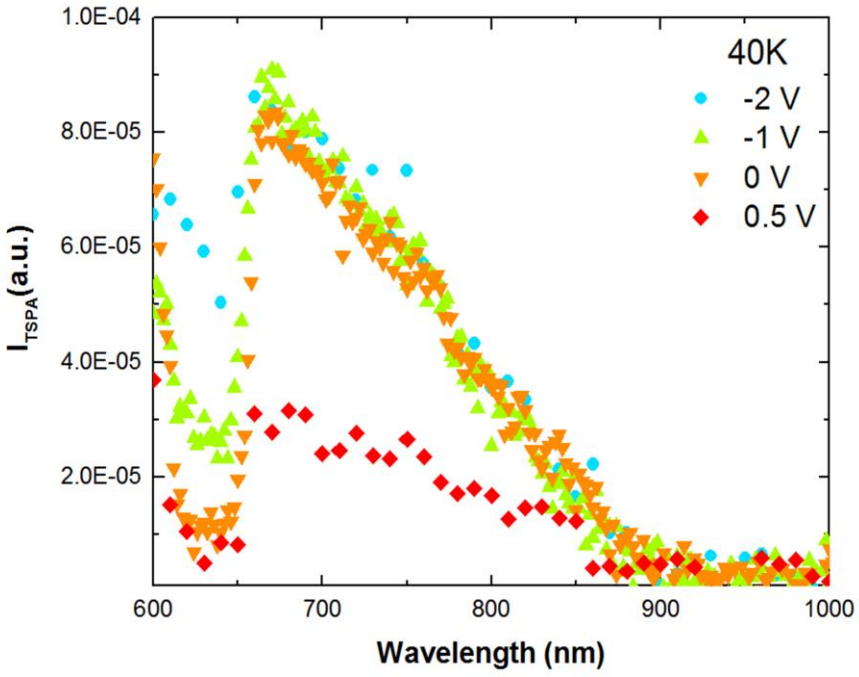

Figure 3.26 Voltage biased TSPA photocurrent at 40K.

3.4 Simulations on alternative III-V QD systems

3.4.1 Simulations result of GaSb/GaAs QD

Other QD systems are also investigated via MOCVD growth for future room temperature IBSC applications. Figure 3.27 shows the 300K eitght-band ***k·p*** band structure simulation of GaSb/GaAs QD via nextnano^{++} software [29]. The nextnano^{++} is a Schrödinger-Poisson-Current solver written in C^{++}. The shape of QDs is set as a truncated pyramid. The Schrodinger equation is solved with the eight-band ***k·p*** method for the conduction ban and the heavy, light, and split-off hole valences band, which shows a type II band alignment that enables extended radiative lifetime of IB-CB transition [137]. The IB in the GaSb/GaAs QD is located at the confined hole level. The simulated ground state hole confinement related to the GaAs valence bandedge (E_L) is 0.69 eV of the GaSb/GaAs QD with a 2 nm in height and 20 nm in diameter. Such deep hole confinement enables potentially high working temperature of TSPA [131].

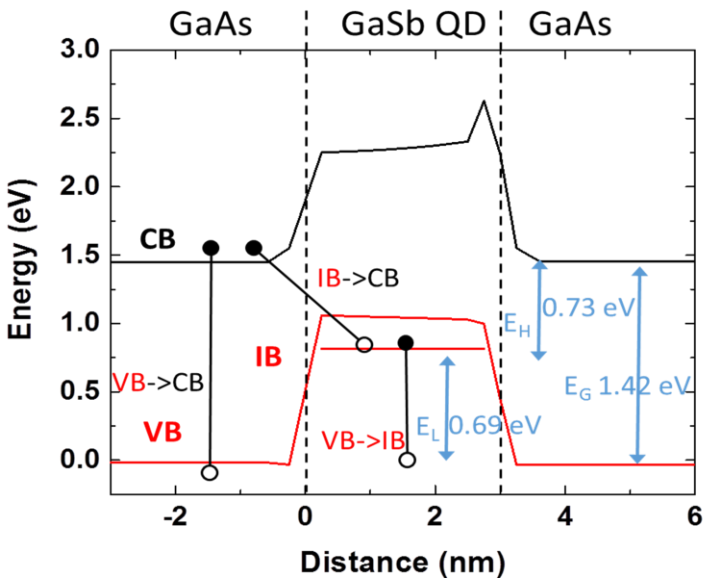

Figure 3.27 Simplified band diagram of the *n-i-p* InAs/GaAs/$Al_{0.3}$GaAs Dwell solar cell at 300K.

Due to Sb/As atom diffusion process during the MOCVD GaSb QD growth, the hole barrier height E_L and then energy difference (E_H) between IB and CB are varied on the size of the QD as well as the Sb content of the Ga(As)Sb QD [138]. As expected, Figure 3.28 (a) shows with increasing Sb content the transition energy E_H decreases, while the localized energy/confined hole barrier increases (shown in Figure 3.28 (b)). The larger size of QDs shows the deeper hole confinement. When Sb is fully diffused in the QD (100% Sb), the confined hole barrier is between 690 meV to 810 meV, so it is important to control V/III ratio, growth temperature, growth interruption and etc. in order to optimize the hole barrier height for efficient IBSC application.

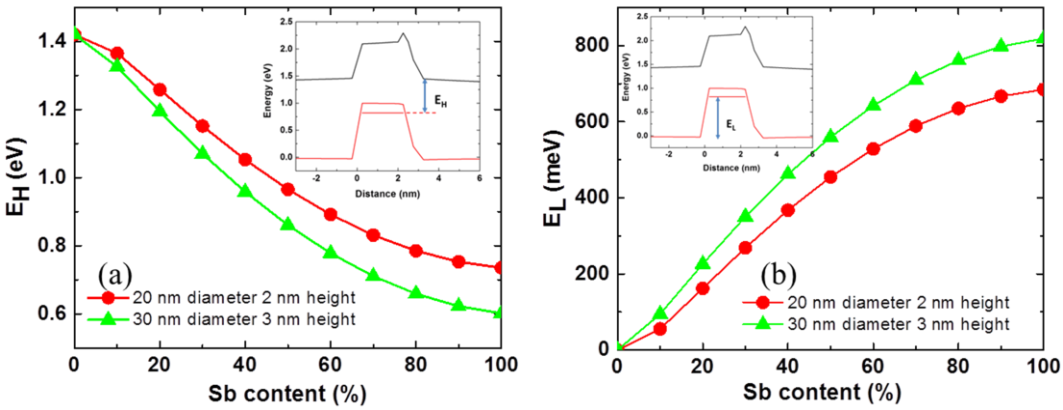

Figure 3.28 Results of nextnano simulation on Sb content and QD size dependent (a) energy transition between confined hole and conduction band (E_H) and (b) localized energy (E_L).

3.4.2 Simulation results of type II InP/InGaP QD

In additional, type II InP/InGaP QD has been proposed for IBSC application [33], [139], [140], so Figure 3.29 shows the room temperature band structure an InP/InGaP QD with an height and diameter of 20 nm and 50 nm, respectively. The simulation shows InGaP as an ideal host material with a band gap of 1.9 eV. The confined depth of electron

is 300 meV. In additional, an almost flat valence band alignment reduces the probability of an hole capture [119] and recombination inside the InP QD. Since the growth of such extra-large type II InP/InGaP were only demonstrate via molecular beam epitaxy, to realization MOCVD grown type II InP/InGaP QD for IBSC applications, various parameters are required to be carefully evaluated.

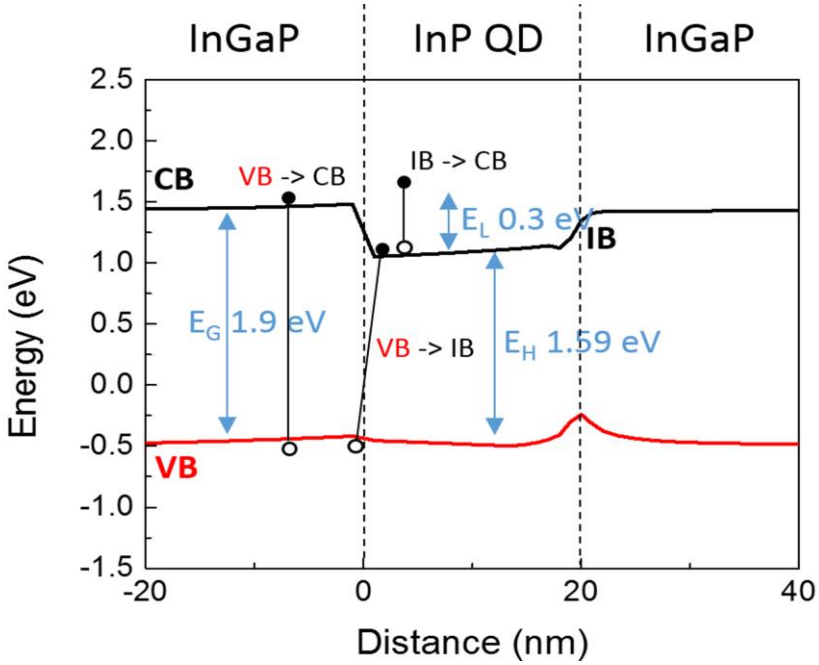

Figure 3.29 Simplified band diagram of the *n-i-p* InAs/GaAs/$Al_{0.3}$GaAs Dwell solar cell at 300K.

3.5 Conclusions

3.5.1 Conclusion on InAs/InGaP QDSCs

In summary of 1st generation devices, two QDSCs and a reference GaAs *p-i-n* cell were fabricated and measured. The GaAs solar cell with InAs/GaAs/InGaP QD shows an improved sub-band-gap carrier collection, but it degrades EQE from GaAs absorption. The improved sub-band-gap carrier collection is from increased absorption by additional confined levels formed by the InGaP barrier. The reduced collection from above GaAs band gap absorption may due to the carrier loss during transport across the intrinsic

region. Temperature and voltage bias dependent EQE measurements were performed on the investigated solar cells to observe carrier collection under difference operation condition. In the InAs/GaAs QDSC with InGaP barrier, temperature dependent EQE decreases with reduced temperature to 175K, but then EQE start to increase with decreasing temperature. With enhanced electric field achieved by reverse bias, both bulk and QD EQE increases at 10K.

To reduce emitter and base carrier transport loss, in the 2nd generation InAs/InGaP QDSC, InGaP emitter and base are used. Compared to the InGaP baseline, although the InGaP QDSC shows an increased sub-InGaP band-gap carrier collection and a lower transition between CB and IB that towards the ideal IBSC, the epi-grown material quality should be enhanced during QD growth in order to finally achieve high efficient IBSC, Also through the band structure simulation and voltage biased EQE measurements, due to the large hole confined depth introduced carrier capture and recombination, an alternative QD system in an InGaP device should be investigated to improve the band alignment to improve the carrier collection efficiency and conversion efficiency.

3.5.2 Conclusion on InAs/$Al_{0.3}$GaAs QD-IBSC

The InAs/$Al_{0.3}$GaAs QD system is promising for high temperature IBSC under concentrated suns illuminations. To improve the growth morphology and reduce Al-oxygen introduced traps of InAs/$Al_{0.3}$GaAs QD for IBSC application, Dwell structure are designed, fabricated and investigated. The high activation energy of 324 meV extracted from the InAs/$Al_{0.3}$GaAs Dwell confirms the prediction from the band structure simulation. The temperature-dependent and voltage bias-dependent two-step photon absorption processes were investigated in the MOCVD-grown InAs/GaAs/$Al_{0.3}$GaAs

Dwell-IBSC. It was found that the working temperature of TSPA is up to 80K under IR (1500 nm) filtered 800^0C black body illumination. Due to the limited QD ground state absorption resulting from low QD surface density, QD ground state TSPA was not observed, though could be improved by increasing incident photon density (sun concentration). Instead, TSPA was observed from shallow confined levels formed by the $Al_{0.3}GaAs/GaAs$ wells, which is mainly due to the combination of enhanced absorption and charge separation. The enhanced absorption of the wells introduces higher carrier concentrations in the shallow confined levels, and the charge separation results in longer radiative lifetimes.

Based on the observed experimental results, three areas for improvement can be addressed. First, the first step of two-step photon absorption (between the deep confined levels) should be enhanced to improve direct TSPA, which could be achieved by improving QD surface density, the number of QD layers, and photon recycling [32]. Second, the QD capture process affects carrier collection and distribution in a given QD layer. Novel QD systems like $InP/In_{0.5}GaP$ [33] or $GaSb/Al_xGaAs$ could be used to reduce the hole or electron capture/recombination in the QD, respectively, by careful QD growth optimization and device design. Third, efficient TSPA requires a reduced recombination rate and escape rate. The electric field decreases the recombination rate via charge separation, while it also increases the escape rate. To balance the effect of electric field and finally achieve a high efficiency room temperature IBSC, it is important to investigate the magnitude of the electric field required at P_{max} condition for a specific design in order to achieve a photon ratchet for a given IBSC design [34], [35] [141].

3.5.3 Conclusion on the simulations of alternative QD Systems for IBSC applications

Alternative QD systems including GaSb/GaAs QD and type II InP /InGaP QD were investigated via band structure simulations. Both systems show advanced properties including extending recombination lifetime, deep IB carrier confinement depth and etc, which are favorable for future room temperature IBSC applications. However, growth optimization is required to finally achieve a decent device via MOCVD.

Chapter 4

Development of InGaP PV devices for low intensity light applications

4.1 Introduction

The development of photovoltaic (PV) device under low intensity illuminations began with radioisotope batteries [20]. There are two types of radioisotope batteries [142], which are distinguished by different nuclear to electrical conversation mechanisms. One type of the radioisotope batteries directly generates electron-hole pairs by the ionizing nuclear radiation [143], [144], which only requires a material with wide bandgap to minimize dark current [62] and improves the device efficiency temperature coefficient because of additional heat generation [145]. The other type of radioisotope batteries first convert high energy alpha/beta particles into photons by phosphorescence processes [146], and then the phosphor radioluminescence is converted to electrical energy for an operation lifetime of several decades [20]. Thus, phosphor radioluminescence enabled radioisotope batteries, in order to achieve a high efficiency, not only dark current should be minimized, but also carrier collection under a certain phosphor spectrum illumination should be optimized.

Moreover, there is a new market (value towards $267B by 2020 [147]) emerging from internet of things (IoT). The IoT refers to a large-scale network of smart nodes and sensors (embedded in home appliances, buildings, vehicles, etc.), which are connected wirelessly and communicate functionally to complete tasks. The number of connected devices is predicted up to 30-50 billion by 2020 [18]. Most nodes/sensors are off grid devices (power consumption ranging from 0.1-1000 μW [18], [20]), which require long-

term energy sources to function. PV devices, as one of the methods to harvest ambient energy, have been considered as replacement for less sustainable battery technology with limited charge cycles [148]–[150]. Some of the sensors are for indoor applications, so they require the PV devices output high power under low intensity light illuminations.

Traditional terrestrial solar cells are optimized under standard test conditions (STC) to simulate outdoor illumination during the day. The power intensity (100 mW/cm^2 [151]) of STC with AM 1.5 sun spectrum is much higher than the power intensity ($1\mu W/cm^2$-$1mW/cm^2$ [152]) of an indoor fluorescent lamp, or light emitting diode, or phosphor radioluminescence. Low intensity light sources affect PV devices conversion efficiency due to an increasing importance of the dark current [152] and shunt resistance [153]. To optimize PV devices' performance and cost under indoor illumination, the PV devices should be designed and evaluated under these specific light sources [31].

To date, several photovoltaic material have been investigated for the indoor light applications, including silicon [153], [154], GaAs [155], AlGaAs [150], dye-sensitized PV [156], pervoskite [148], [157], organic PV [158] [159] and so on. Compared to the sun light has a long infrared tail towards a few microns, as shown in Figure 1.7, indoor light sources usually associate with a narrow spectrum within the visible region (400-700 nm). Based on the detailed balance model, all photons with wavelength less than 700 nm should be absorbed with minimum thermalization loss, Freunek *et al.* theoretically predicated an optimal band gap of 1.9-2.0 eV with a power conversion efficiency up to 60% under varied artificial indoor light sources [19]. As a result, wide-band-gap III-V materials are promising for higher conversion efficiency for indoor applications [149]. However, as one of the III-V material with a band gap of 1.9 eV at 300 K, design of a

single junction InGaP device has not been fully investigated under low light illumination. In this chapter, a detailed design and performance of single junction InGaP photovoltaic devices under low intensity light sources illumination are reported. The effect of parameters PV devices have been statistically evaluated, including doping and thickness in the emitter and base on the efficiency of *n-i-p* InGaP. Additional dark current-voltage characteristics and external quantum efficiency were also performed and discussed for future device optimization.

4.2 Device design and experiments

Because the selections of material, doping concentration, layer thickness and material quality (minority carrier lifetime) depend on epi-growth methods, any III-V PV devices start with a review of devices growth capability. All investigated devices are grown by a 3×2" Aixtron close-couple showerhead metal organic vapor phase epitaxy (CCS-MOVPE) on a two-inch p-type GaAs substrate. Figure 4.1 shows the layer structure and associated energy band layout for the *n-i-p* InGaP photovoltaic device design. A thin (~20 nm) n-type AlInP was used to reflect minority holes in the emitter and passivate the device leading to a low dark current [12]. A thin intrinsic layer (10 nm) is used to improve the charge separation at the junction, which is expected to introduce a lower dark current under low intensity light illumination. Although p-doped AlInP as back surface filed (BSF) has been reported to improve charge collection by reducing interface recombination [160], heavily doped p-type (50 nm) InGaP was used a BSF. This is because Zinc, the MOVPE p-type dopant, becomes less electronically active with increasing Al of the epi-growth [161], which creates an upper doping limit.

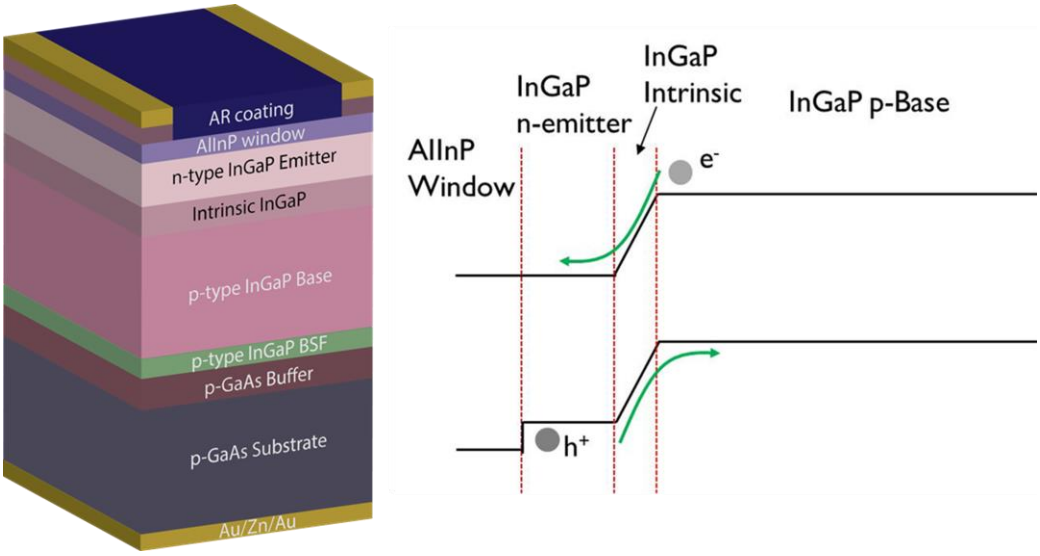

Figure 4.1 Layer structure schematic and related band diagram (under no bias) of the *n-i-p* InGaP structure

Because optimization of the PV devices design is a compromise between light absorption and carrier combination, based on the MOVPE growth capability and related material quality, several parameters should be tuned to maximize the efficiency performance under a specific artificial spectrum (or several specific spectrums). Figure 4.2(a) shows a set of input betavoltaic phosphor spectra used in the simulations to estimate doping and layer thickness effects on the conversion efficiency. Both spectrums have a relatively narrow band with a full width half maximum (FWHM) less than 100 nm. The ice blue phosphor peak intensity is at 455 nm, while the green phosphor has a red shifted peak around 523 nm and extended tail towards 650 nm. The integrated intensity of both spectrums was normalized to 1μW/cm^2, which corresponds to isotope power source level. In addition, the investigated two phosphor spectra cover a wide range (90%) of the most indoor light sources spectra that shown in Figure 1.7, so the PV devices optimization under these phosphor two phosphor spectra is also effective under indoor light sources for the IoT applications.

In order to demonstrate the different spectrum effect on device design, Figure 4.2(b) shows light fraction as a function of depth in InGaP calculated via Equation 3.1. As can be observed, over 90% photons with wavelength less than 450 nm (photon energy >2.76 eV) are absorbed in 100 nm thick InGaP, which is within the n-type emitter thickness, so the emitter carrier lifetime is important to harness those high energy photons. Within 1000 nm InGaP, almost 99% photons with wavelength below 550 nm (photon energy >2.25 eV) can be absorbed, while over 10% photons with wavelength above 550 nm cannot be absorbed to excite electron-hole pairs. Therefore, for InGaP PV device design, the total InGaP thickness can be within 1000 nm to fully use the blue phosphor spectrum, but the total thickness should increases to harness the green phosphor spectrum or other indoor light sources contains lower energy photons (>550 nm).

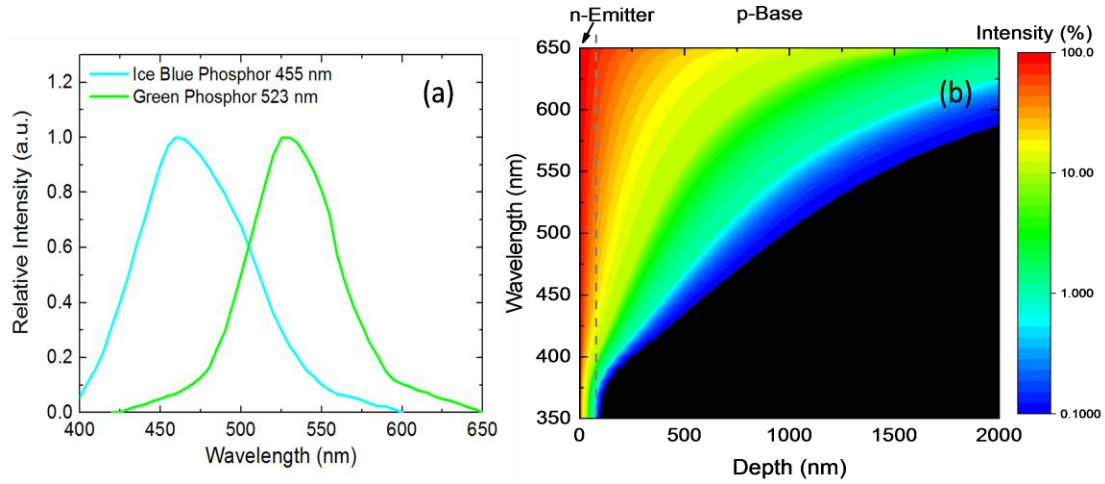

Figure 4.2 Relative intensity of two phosphors sources centered at 455 nm and 523 nm (b) Light fraction as a function of depth in InGaP

Doping-dependent recombination and diffusion lengths of minority carriers affect the dark current, while the total depth of the devices determines the total number of photons absorbed. Therefore, the four investigated parameters included the n-emitter doping, n-emitter thickness, p-base doping, and p-base thickness. These parameters were evaluated

based on the efficiencies simulated using Sentaurus TCAD [90] under each of the narrow phosphor illumination spectrums shown in Figure 4.2. The Sentaurus software is physics-based, by solving the self-consistent Poisson equation and continuity equations (electron and hole) across the device depth. The lifetimes are fixed at the average values extracted from previous MOVPE-grown InGaP devices, by fitting the IV and EQE curve via Sentaurus TCAD. Figure 4.3 shows an example of fitted 300K EQE of the already grown and fabricated *n-i-p* InGaP device (a 10 nm InGaP etch stop on the top of the 20 nm AlInP window layer, followed by 100 nm emitter and 1500 nm base) to extract carrier lifetime. JMP software was used for the design of experiment and data analysis. Full factorial designs were employed to reduce the number of Sentaurus simulations.

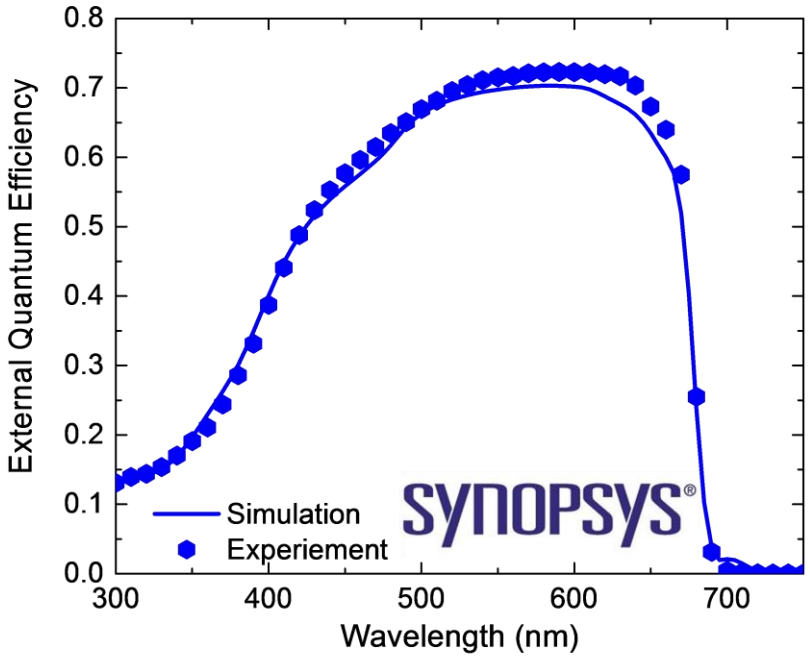

Figure 4.3 A example of a previous grown *n-i-p* InGaP PV device EQE and fitted curve using Sentaurus TCAD to extract carrier lifetime.

Figure 4.4 (a)-(f) shows the relationships of the input parameters and efficiency under the two phosphor spectra. The electron and hole lifetime is set at 50 ns and 90 ns,

respectively. Because InGaP hole doping dependent mobility is in a range of 15-150 $cm^2/V \cdot s$ [162], which is much lower than doping dependent electron mobility 400-4300 cm2/V•s [162], the emitter doping was varied between 1×10^{17} cm^{-3}~1×10^{18} cm^{-3}, and the emitter thickness was varied between 50 nm to 100 nm. The p-base doping is in the range of 5×10^{16} cm^{-3} to 5×10^{17} cm^{-3}. Because at a fixed doping level, the electron mobility is at least an order higher than the hole mobility, which contributes a longer diffusion length if the lifetime values of electron and hole are on the same order, the p-base thickness was simulated from 500 nm to 2000 nm.

As shown in Figure 4.4 (c)/(g), a lower doping in the base results a higher efficiency, due to reduced doping dependent recombination. Because the hole lifetime is 90 ns and a narrow emitter design range (50-100 nm), the effect of doping (Figure 4.4 (a)/(e)) and thickness (Figure 4.4 (b)/(f)) at the selected range only changes the efficiency less than 1%, while the efficiencies under both phosphor spectra are more sensitive to the base length/doping. The absorption tail (above 500 nm) in both spectra increases with increasing devices thickness. Because the 455 nm phosphor has a larger fraction of high energy photons, this introduces higher thermalization loss [6]. Therefore, the average ice blue phosphor conversion efficiency (25.2%) is lower than the average green phosphor conversion efficiency (29.8%). This efficiency difference indicates that PV designs for narrow spectrum light sources are sensitive to the bandgap of the PV material. Additionally, as shown in Figure 4.4 (d)/(h), due to a larger tail above 550 nm in the 523 nm phosphor, the efficiency is more sensitive to layer thickness variation, which is consistent with Figure 4.2(b).

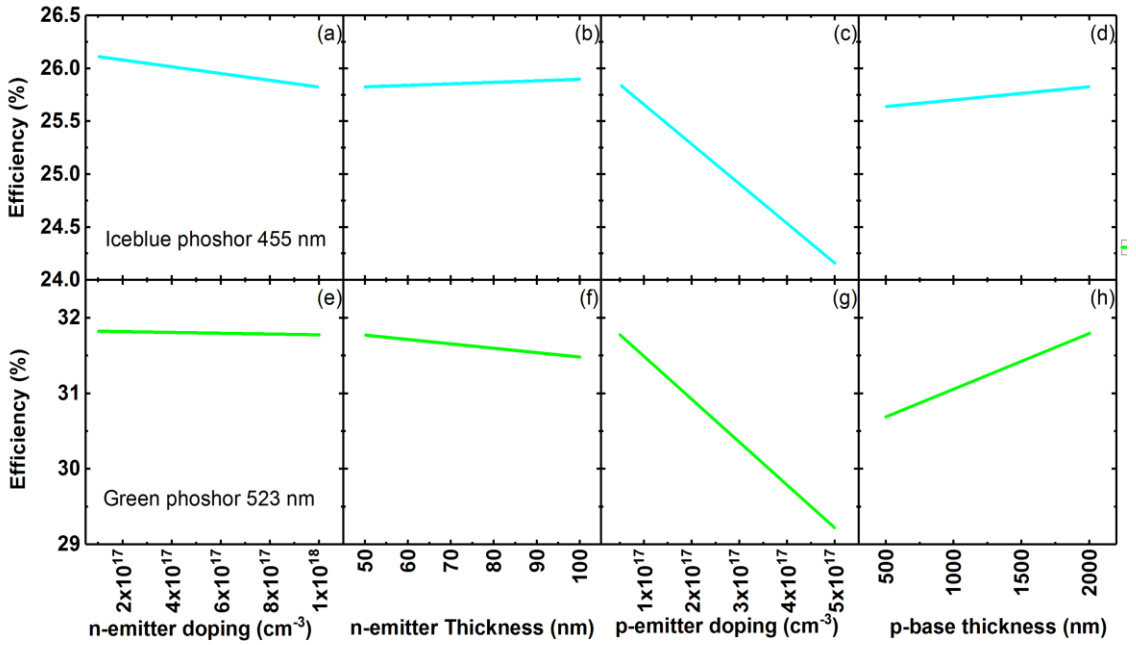

Figure 4.4 Relationship of the variable input parameters and efficiency under ice blue and green phosphor illumination (input power density at 1 μW/cm^2)

According to the simulations, two designs (A and B) with slightly different layer structure are generated. Design A has a 1500 nm zinc-doped (5×10^{16} cm^{-3}) base and a 100 nm Si-doped (1.6×10^{18} cm^{-3}) emitter, while design B has a longer base of 2000 nm and a thinner emitter of 50 nm. Overall, design B is thicker in order to increase absorption of light above 550 nm according to the Beer-Lambert law. A heavily doped GaAs contact layer was incorporated for ohmic contact formation in both designs. Individual cells (1×1 cm^2) with less than 4% grid fingers shadowing were fabricated by a metal lift-off process to maximum absorption. Devices were isolated using wet chemical etching techniques. Additionally, a dual layer ZnS (56 nm)/MgF_2 (110 nm) anti-reflective coating (ARC) was designed via TFcalc software by using the transfer matrix method to minimize the reflection between 400-700 nm.

Experimental results from InGaP design A under intensity-dependent phosphor illumination have been reported elsewhere [20]. Although the measured efficiency of 29% under 1 μW/cm^2 523 nm centered green phosphor illumination is slightly lower than with simulation results (31% with 1500 nm base length), comparing to other commercial PVs, InGaP is the most efficient under low light conditions. The slightly (2%) efficiency difference between experimental and simulation may be from the difference between cells or lifetime variation between different MOCVD growth round.

In this chapter, IV measurements were performed with commercial warm and cold LEDs (input power range: 1-1000 μW/cm^2) with a Keithley 2400 source meter unit, in order to evaluate the designed devices power conversion efficiency for the IoT applications. The warm and cold LED spectrum were measured and calibrated via ASD FieldSpec spectroradiometers. To understand device physics for future design optimization, additional experiments were conducted. Reflection measurements were completed with a Filmetrics F20 spectrometer. Room temperature EQE measurements were taken with a Newport IQE-200 Spectroradiometric Measurement system. Dark J-V measurements were also completed with the Keithley 2400 source meter unit.

4.3 Results and discussion

4.3.1 LED intensity dependent power conversion efficiency

To experimentally detect different spectrum effect on device performance for low light applications, Figure 4.5 shows intensity-dependent InGaP device (design B) power conversion efficiencies under different LED light illuminations. The efficiencies increase (from 31.1% to 42.5%) with increasing incident light intensity (from the order 1μW/cm^2 to 1mW/cm^2), due to enhanced short circuit current (J_{sc}), open circuit voltage (V_{oc}) and fill factor. The improved fill factor results from the reduced impact of the shunt resistance

[163], [164]. The trend of intensity-dependent efficiencies has being observed by many other groups [20], [150], [163] with other indoor light sources and PV devices. The range of InGaP device efficiencies in Figure 4.5 is consistent with literature that shows 35% efficiency under 100 $\mu W/cm^2$ cold LED illumination[20]. Such high conversion efficiencies represent a significant improvement over previous reports, which indicate the device design is effective for both betavoltaic and IoT applications.

The Figure 4.5 inset shows the relative intensity of the two LEDs used in the measurements. Compared to the cold LED with a peak at 447 nm, the spectrum of the warm LED red shifts with a 605 nm peak. Again, due to reduced thermalization losses in the warm LED—even with a boarder spectrum than the phosphor light sources—the efficiencies measured under warm LED are slightly larger than the efficiencies measured under phosphor illumination. Therefore, in order to minimize thermalization and transmission loss as discussed in the design section 4.2, the selection of material band gap is important for PV device conversion efficiency under different spectra.

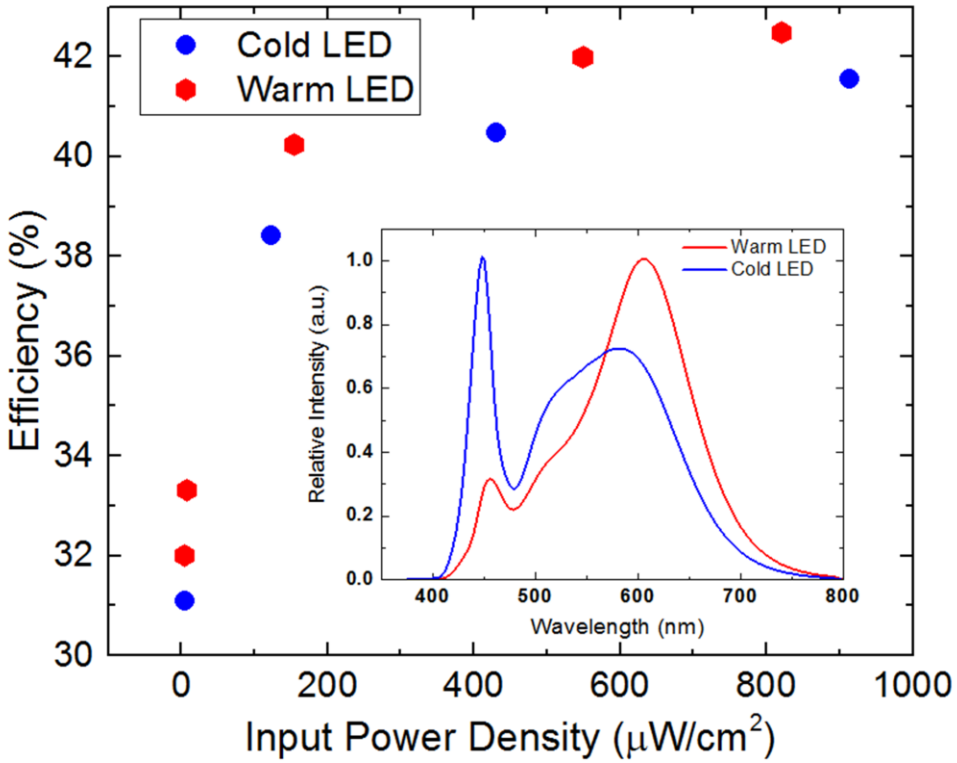

Figure 4.5 (a) Incident-power-dependent InGaP device (design B) efficiency under different LED light illuminations. Inset shows the relative intensity of the two LEDs used in the measurements.

4.3.2 Light IV measurement under 600 nm 1.27 μW/cm^2 illumination

In order to compare designs A and B, low-power illuminated J-V characteristics were completed with an OL750 spectroradiometric measurement system with the wavelength fixed at 600 nm and a power density limited to 1.27 μW/cm^2. The wavelength fixed at 600 nm correlates to the peak of the indoor spectrum (fluorescent light and warm white LED) [31]. Furthermore, a 600 nm peak also matches the phosphor emission from Tritium vials. The power on the order of 1μW/cm^2 matches scintillation light from phosphors for tritium-powered sensor networks [152]. Such low power light allows the effect of the shunt resistance on efficiency to be observed. Figure 4.6(a) shows the 600 nm centered spectrum for the light IV measurements. Figure 4.6(b) shows the light IV

curves of design A and design B under 600 nm 1.27 μW/cm^2 illumination. Both cells show a high efficiency over 30%, which is consistent with simulations. Both cells have a fill factor around 80% which indicates the shunt resistance does not dominate device performance. The short circuit current density of design A (491 nA/cm^2) is lower than that of design B (511 nA/cm^2). The open circuit voltage (V_{oc}) in design B is 0.04 V less than design A. The reduction in V_{oc} in design B indicates larger dark current.

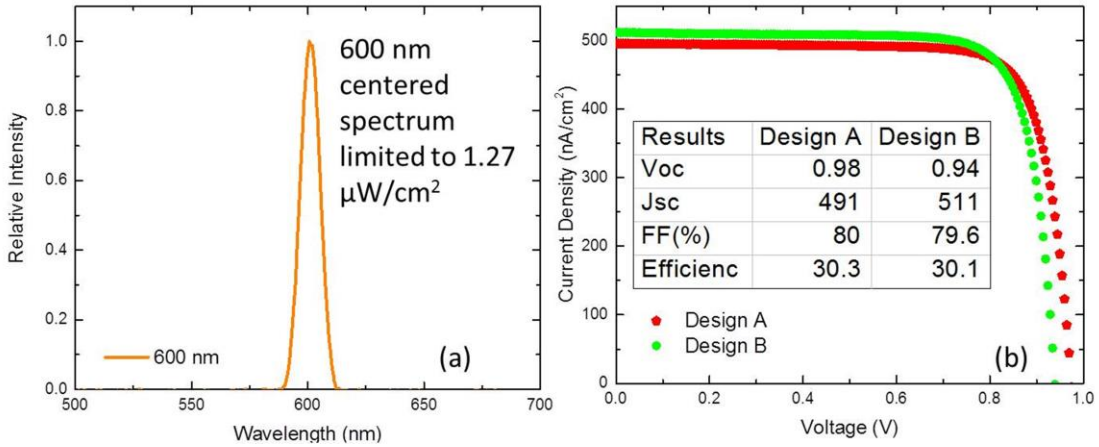

Figure 4.6 (a) Spectrum of the 600 nm centered for the light IV measurements (b) Measured current density vs. voltage curves under 1.27 μW/cm^2 illuminations.

4.3.3 EQE measurements and front surface reflection measurements

To detect wavelength-dependent carrier collection of the two designed InGaP, Figure 4.7 (a) shows room temperature EQE measurements before anti-reflection coating, which illustrates the improved EQE above 600 nm in design B. As discussed in Figure 4.2(b), this experimental observation is mainly due enhanced absorption in a thicker base. The electron and hole lifetime extracted from Sentaurus TCAD EQE fitting is 35 ns and 50 ns, respectively. These values are slightly lower than the lifetime used in the device design, which may introduce a deviation between simulated and measured efficiency.

Figure 4.7(b) shows InGaP PV devices EQE after anti-reflection coating, both designs show a 20% EQE improvement compared to the Figure 4.7 (a). Furthermore, both designs show similar EQE between 400 and 550 nm. Because the reflectance, shown in Figure 4.7 (c), is lower between 400-450 nm for design B, the EQE is higher in design B than in design A. The reflectance between 450-700 nm is reduced due to the effective ZnS/MgF_2 anti-reflective coating, so the EQE is close to 1 in this region. The improved EQE of design B is also consistent with the *Jsc* improvements shown in Figure 4.6.

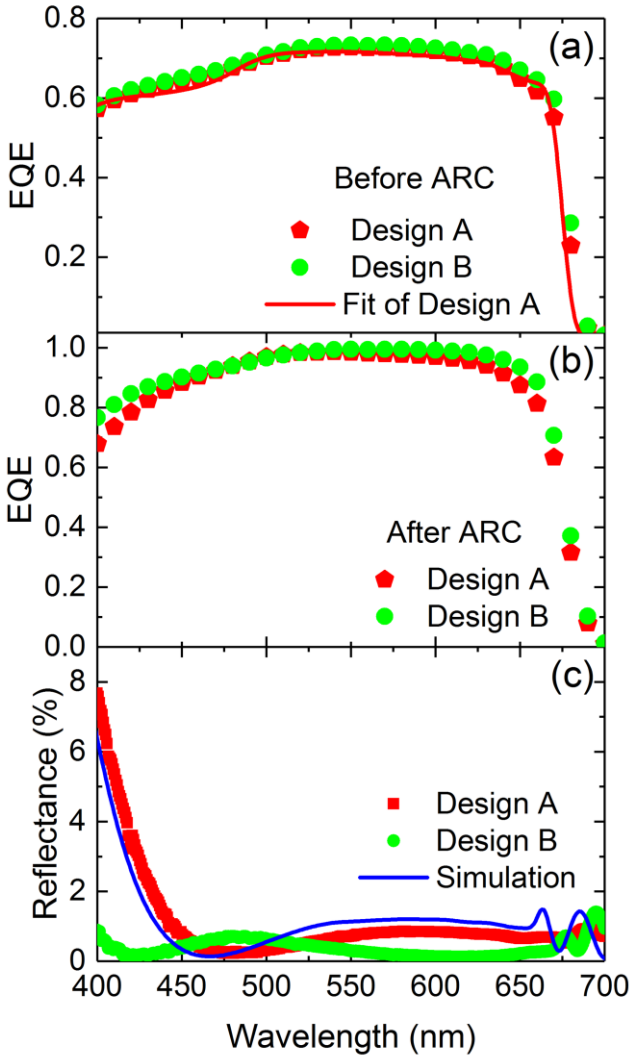

Figure 4.7 Room temperature EQE of the designed InGaP PV devices: (a) without ARC.(b) with ARC (c) Reflectance data from both simulation and measurements**.**

4.3.4 Dark IV measurements

To investigate the recombination process in design A and B, Figure 4.8 shows the dark IV measurements on the investigated solar cells. Design A shows a generally lower dark current than design B at each forward bias voltage. The higher dark high current correlates with the lower open circuit voltage (V_{oc}) as showed in Equation 4.1.

$$V_{oc} = \frac{nkT}{q} ln(\frac{J_L}{J_0} + 1) \quad 4.1$$

Here, n is the ideality factor. k is the Boltzmann constant. T is the temperature, q is the charge, J_L is the light generating current, J_0 is the dark saturation current. The dark current also affects the fill factor (FF) that showed in Equation 4.2, where P_{max} is the maximum of the product of $J(V)V$, which cannot be obtained explicitly, so it is difficult to derived directly from Equation 4.2 that increasing dark current decreases the fill factor. However, the shunt resistance and series resistance embedded dark current that can be fit via a double diode equation. In Equation 4.3, increasing values of the shunt resistance and series resistance make the IV curve less square, so the FF factor decreases.

$$FF = \frac{P_{max}}{J_{sc} \times V_{oc}} \quad 4.2$$

$$J = J_{01}\left\{exp\left[\frac{q(V-JR_s)}{n_1 kT}\right] - 1\right\} + J_{02}\left\{exp\left[\frac{q(V-JR_s)}{n_2 kT}\right] - 1\right\} + \frac{V-JR_s}{R_{shunt}} \quad 4.3$$

Here, J is the measured current density and V is the bias voltage. J_{01} and J_{02} are the reverse saturation current densities of diode 1 (recombination in the quasi-neutral region [155]) and diode 2 (recombination loss in the depletion region [165]), respectively. The ideality factor of a diode associates different recombination processes [166]. n_1 and n_2 refer to the ideality factors of this diode. n_1 is usually equal to 1, indicating Shockley-Read-Hall recombination in different type of recombination-generation centers from crystal lattice dislocations, impurity atoms or surface defects; n_2 is usually equal to 2,

indicating two-carrier recombination in the depleted region. The depleted region mainly refers to the *pn* junction. Additionally, surface recombination happens in a depleted region, but some experimental results demonstrated that the surface recombination ideality factor is closer to 1 [167] due to the limited availability of carriers [168]. R_s is the series resistance and R_{shunt} represents the shunt resistance. The extracted parameters are shown in the inset table. At lower bias voltages (<0.6 V), the J_{01} dominates the dark current in these devices.

Under illumination on the order of 1μW/cm^2, the Figure 4.8(b) shows the integrated J_{sc} from the measured EQE in Figure 4.7(a), under different light sources. Similar to the measured IV from the 600 nm illumination, the J_{sc} is on the order of 1×10^{-7}A/cm^2, so the V_{oc} (around 1V) is affected by both the J_{01} and J_{02}. Because design A has a thinner base than design B, design A shows a lower J_{01} than design B due to reduced bulk recombination. The slightly larger J_{02} (6×10^{-12} mA/cm^2) in design B may be from the surface recombination. Compared to design B, A slighter larger shunt resistance in design A also reduces the overall dark current. However, as shown in Figure 4.7(b), the integrated J_{sc} of design B is higher than design A because of a higher EQE. Especially under LED illumination for IoT applications, the V_{oc} difference between design A and B is negligible when an incident light power density above 10 μW/cm^2.

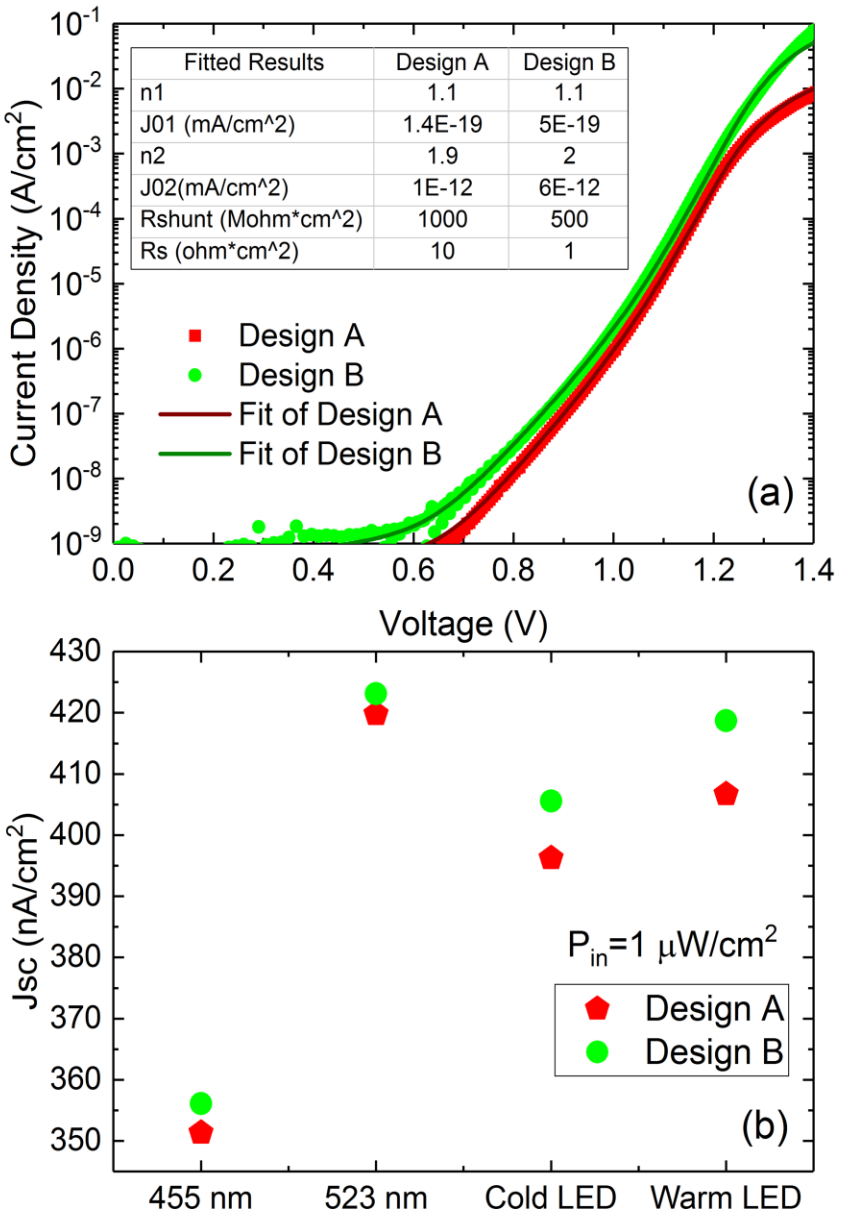

Figure 4.8 (a) Measured and simulated dark current –voltage characteristic for the *n-i-p* solar cells with design A and B. (b) integrated J_{sc} from EQE under different light sources with input power limited to 1 μW/cm^2.

To increase the diffusion length of electrons in the n-type base, higher quality InGaP via MOVPE growth is required for a longer carrier lifetime. The thickness of the intrinsic region should also be considered to further separate charges along the device growth direction [169]. Additionally, the shunt resistance is lower in design A, reflected in the

slightly reduced FF in device B as shown Figure 4.6 (b). Therefore, the shunt paths introduced during growth (such as point defects) and fabrication (such as sidewall recombination [170]) should be eliminated in the future. The difference in series resistance may be due to the anti-reflection coating not being fully removed from the top of the grid finger during the dark IV measurements, which only affects photovoltaic device performance under high intensity light illumination.

4.4 Conclusion

This chapter demonstrates a detailed procedure of the design and performance of InGaP PV devices. The selections of material, doping concentration, layer thickness and material quality (minority carrier lifetime) depend on epi-growth capability. The optimization of PV devices design is a compromise between light absorption and carrier recombination, so several parameters should be tuned to maximize the efficiency performance under a specific artificial spectrum (or several specific spectrums).

It shows reduced front surface reflection (below 1% between 450-700 nm) using MgF_2/ZnS as anti-reflection coating. Both devices show over 30% efficiencies with an open circuit voltage toward 1 V. Meanwhile, due to recombination in the surface, bulk, and sidewalls, the devices with a total thickness over 2 μm shows a slight V_{oc} (0.04V) drop compared to the thinner devices. To further increase InGaP device efficiency under extreme low intensity light (on the order of $\mu W/cm^2$) for radioisotope batteries applications, efforts should address side wall passivation during fabrication, increasing device surface area, improving the back surface field, flipping the polarity from *n-i-p* to *p-i-n*, and improving material quality by optimizing epitaxial growth conditions.

Chapter 5

Nanowire growth for applications in photovoltaic device

5.1 Introduction

Semiconductor nanowire (NW) heterostructures have attracted considerable attention in recent years because of their great potential in microelectronic and optoelectronic nano-devices [171]. The nanowires are interface strain free, so they provide broad material selection, and have quantum confinement when their diameters are on order of the De Broglie wavelength. Indium arsenide (InAs) nanowire devices are motivated by the InAs physical properties. First of all, it is a narrow-band gap semiconductor (0.354 eV) and problems with ohmic contacting of wires should be minimal. Secondly, it has high electron mobility (up to 20000 $cm^2V^{-1}s^{-1}$) [171]. This is due to its small electron effective mass (m*=0.023 m0), which is three times lower than that of GaAs. Low effective mass also provides strong quantum confinement effects with a large energy level separation in the wires. Additionally InAs is less effective against surface depletion that usually results from surface states, because InAs surface Fermi level is within the conduction band, so conductive InAs nanowires can be obtained easily without any surface passivation. The development of the InAs nanowires growth is critical to nanowire devices, such as field effect transistors [172][173], tubular conductors [174], PV devices [175], photo-detectors [176].

For PV devices applications, nanowires are active in the application for antireflective coating [177], light trapping absorbers [178][179], back reflectors [180], improved charge transport [181]. Recently, there have been many experimental demonstrations of

InAs NWs grown on InAs [182][171] or Si substrate [183], [184]. In comparison, InAs grown on GaAs substrates have been less reported, especially for the potential space application to reduce the solar cell degradation after hard radiation.

The simplest method of nanowires epitaxy is via the vapor–liquid–solid (VLS) mechanism, which is to apply a nanoparticle (NP) catalyst to the substrate surface to form a nucleation site prior to InAs epitaxy. These NPs are typically colloidal Au particles in suspension with small diameters (30-50 nm). The InAs nanowires grow in directions that with lowest total free energy. This free energy is usually dominated by the surface free energy of the interface between the metal catalyst and the semiconductor [185]. In order to optimize InAs nanowire VLS growth processes via MOCVD technique including aspect ratio, diameter and surface density, several growth parameters have been investigated, including GaAs substrate orientation, ratio of group V to III precursor flow rates (V/III ratio), and growth temperature [186]. This chapter further investigates the selective area InAs VLS growth ability with patterned anodic aluminum oxide (AAO) [29].

Furthermore, although the InAs nanowire diameter can be controlled to some extent by the catalyst diameter and the InAs nanowire length can be tuned by growth rate and time, there are still important issues to control and reproduce NW in position, size and shape. As a results, it has been reported to control the position of the metal catalysts as well as their size by using lithographic techniques [187][188]. Electron beam lithography was applied as an alternative method to control the size and growth area of the InAs nanowires. The morphological characterization was studied by scanning electron microscopy (SEM). Additionally, the crystal structure of catalyst free InAs nanowires on

GaAs substrate using PS/PMMA DBC nano-patterning was carefully studied [28] via transmission electron microscopy.

5.2 Theory of the growth mechanism III/V nanowire

Figure 5.1 shows a schematic process for the InAs nanowires grown via the VLS mechanism, which was first demonstrated by Wagner and Ellis in 1964, when they epi-grew the one dimensional silicon whiskers structure via chemical vapor deposition [189]. Figure 5.1 (a) shows Au nanoparticles are deposited onto the surface the (111) GaAs substrate that enables vertical growth. The Au can be deposited either by a spin coating process with its colloidal form or physical vapor evaporation (PVD). These Au NPs are used as a catalyst to form a liquid eutectic with the desired NW material. Figure 5.1(b) shows droplets of the metal alloyed by the constituents of the growing material. When the metal particle is supersaturated, it begins to form one dimensional growth. Because reactants are supplied in the vapor phase, the base diameters of the nanowires correlate to the seed particles diameter. Figure 5.1(c) shows nanowire is vertically grown by precipitation from a droplet. Because of catalytic absorption of the gaseous reactants from the surroundings, this progress is driven by the crystallization from super-saturation within the droplet. Figure 5.1(d) demonstrates that the additional flux of dissolved species leads to further precipitation and NW growth, so both diameter and length of the nanowires increases.

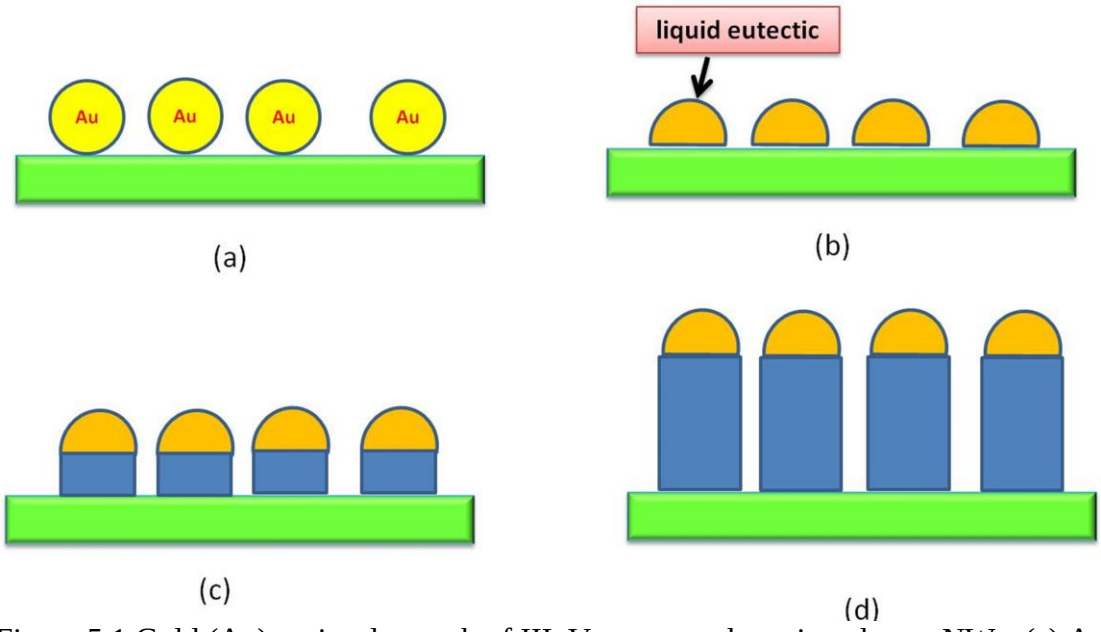

Figure 5.1 Gold (Au)-assisted growth of III–V compound-semiconductor NWs. (a) Au NPs are deposited onto the substrate. (b) They are ideal sinks for the group III species supplied from vapor and form an Au-group III alloys. (c) III–V material is deposited preferentially at the nanoparticle-substrate interface. (d) Adsorption and diffusion of reaction species contributing to further NW growth.

The growth temperature of the InAs nanowire is between 350°C to 600°C [190][191][192]. In fact, solid solubility of As in Au is very low, less than 1% [193][190], but melting of an Au-In alloy may increase the As solubility because As is highly soluble in both liquid Au and liquid In [190]. The eutectic temperature for some phases is at a relatively low-temperature (below 500°C). This allows growth from liquid Au–In in a wide concentration region as long as the growth process can be performed with small arsenide content in a liquid droplet. The small scale of the alloyed Au nanoparticles also suffers from the size-dependent melting effects, according to the Gibbs–Thomson relation [194]. Therefore, the melting point of the alloy nanoparticles may be depressed relative to the bulk melting point, and eutectic melting may occur at a

lower temperature than that predicted by the bulk phase diagrams. For the catalyst free InAs nanowires growth, the mechanism of the growth is also VLS-like, where indium remains in the liquid phase. The InAs nanowire grows at the interface of the supersaturated Indium liquid and solid InAs nanowires [110.], [121].

5.3 Experiment

InAs NWs with Au seeds were grown in a Veeco D125 LDM rotating disk MOVPE reactor at NASA Glenn Research Center (Cleveland, OH). Prior to the InAs nanowire epi-growth, the (111)B GaAs substrates were cleaned via Acetone and IPA rinse. Native oxide on the (111)B GaAs substrate was etched in an HCl/H_2O (2:1) solution for one minute. Poly-l-lysine (PLL) from Ted Pella was also used as an adhesion promoter for the 50 nm Au colloidal NP. The negatively charged Au NP stick to the positively charged PLL, so the affinity of the Au NP for PLL prevents the NPs from aggregating while the suspension dries on the substrate [196][197]. Additionally, Au thermal evaporation with PVD75C was used get patterned Au seeds with the AAO membrane. The porous AAO membranes were self-organized in the interface of solution and oxide under an applied field [37]. The distance between the pore can be tuned by varying electric field intensity. Oxalic acid was used to oxidize the aluminum, and then phosphoric acid was used to widen the pore and remove the barrier layer.

Compared to AAO membrane, there are more steps in fabrication to realization of selective area epitaxy (SAE) using E-beam lithography with SiO_2. Two masks are designed with L-edit CAD software. Figure 5.2 shows the graphic data system (GDS) file of two-inch the nanowire masks. First mask with global alignment marks and local alignment marks are required for the metal alignment in order to complete E-beam

pattern printing. There are four global alignment marks (3×2000 μm crosses) and twelve 1.1 mm ×1.1 mm areas for be E-beam patterning. Eight local alignment marks of 3×80 μm crosses for the E-beam Joel 9300 registration were placed inside each 1 cm × 1 cm green square. Additional alignment marks were placed outside the green square for wafer dicing in order to optimize the growth parameters on the each E-beam pattern. The second mask was used for the etching of SiO_2 outside the E-beam patterned area to control the InAs nanowires growth. Mask printing was completed with a Heidelberg DWL 2000 high resolution pattern generator at the CNF.

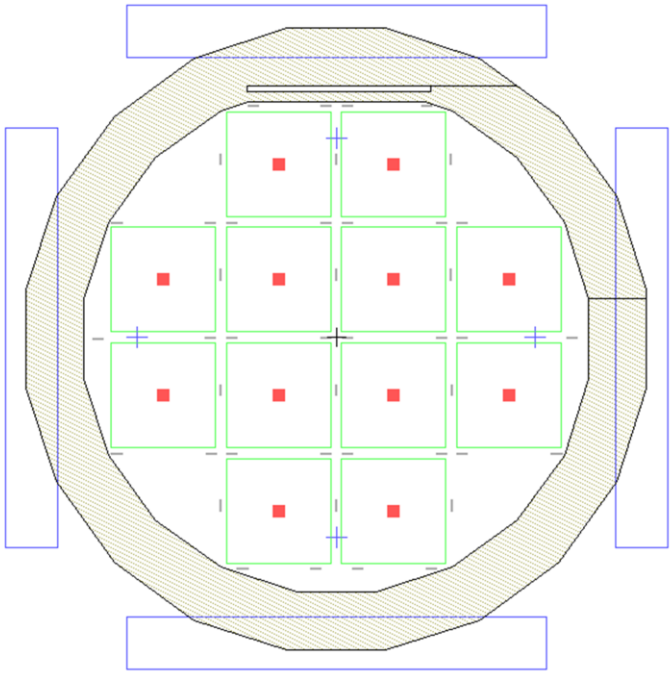

Figure 5.2 Nanowire E-beam mask design

Figure 5.3 shows the flow chart of the E-beam mask fabrication. A layer of SiO_2 with varied thickness of 20 nm to 50 nm was deposited on the surface of (111)B GaAs substrate via plasma-enhanced chemical vapor deposition (PECVD). The varied thickness of SiO_2 layer was used to complete the E-beam dose tests. Then the GaAs substrate is cleaned with Acetone and IPA, following with the HMDS application. After the substrate

cleaning, a set of photoresists of LOR and N-LOF 2020 were spin coated with an SCS spin coater as shown in step 2. After baking the wafer with photoresist, alignment and exposure with the first mask were completed with a Karl Suss MA56 contact aligner, following photoresist development was applied with CD26. After a soft bake at 115°C of the developed wafer, 20 nm Ni and 1μm Ag were deposited to form the metal alignment marks as shown in the third step. Here, Ni was used to improve the adhesion of the Ag to the GaAs substrate. The metal lift-off process was completed with PG remover overnight. Optical inspection after removing photoresist was used to check all alignment marks via Nikon LV 150 microscope.

The fourth step associates with E-beam mask design and making, which were complete with L-edit. Additional pattern file, job file and schedule file for E-beam exposure were completed at CNF, which can be compiled to estimate the E-beam exposure time to the cost on the real E-beam writing. E-beam electron-resists were ZEP520A. After E-beam exposure, the development was finished with ZED N520 before applying MIBK solvent. The fifth step started with E-beam photoresist descum, which was required prior to the oxide etching, in case there was any un-developed ZEP residual left on the SiO_2. Reactive-ion etching (RIE) with Oxford 81 tool for ZEP 520 descum was with 30 sccm O_2, 30 mTorr total pressure, 90 W (0.25 W/cm^2) in 5 seconds, following SiO_2 etching were completed with 50 sccm CHF_3 and 2 sccm O_2, 50 mTorr total pressure in 80 seconds. SEM was used to check the dry etch results of the e-beam patterning. The sixth step is etching the rest of SiO_2 outside the e-beam patterned region, because the nucleation rate of InAs on SiO_2 is much faster than that on GaAs. The spin coating and developing photoresist is similar as the second step. Then in the seventh step, the residual

SiO_2 was removed by the 3 seconds BOE etching. Wafer dicing was completed by American dicing as the final fabrication step before sending out the substrates to NASA for the InAs nanowires growth.

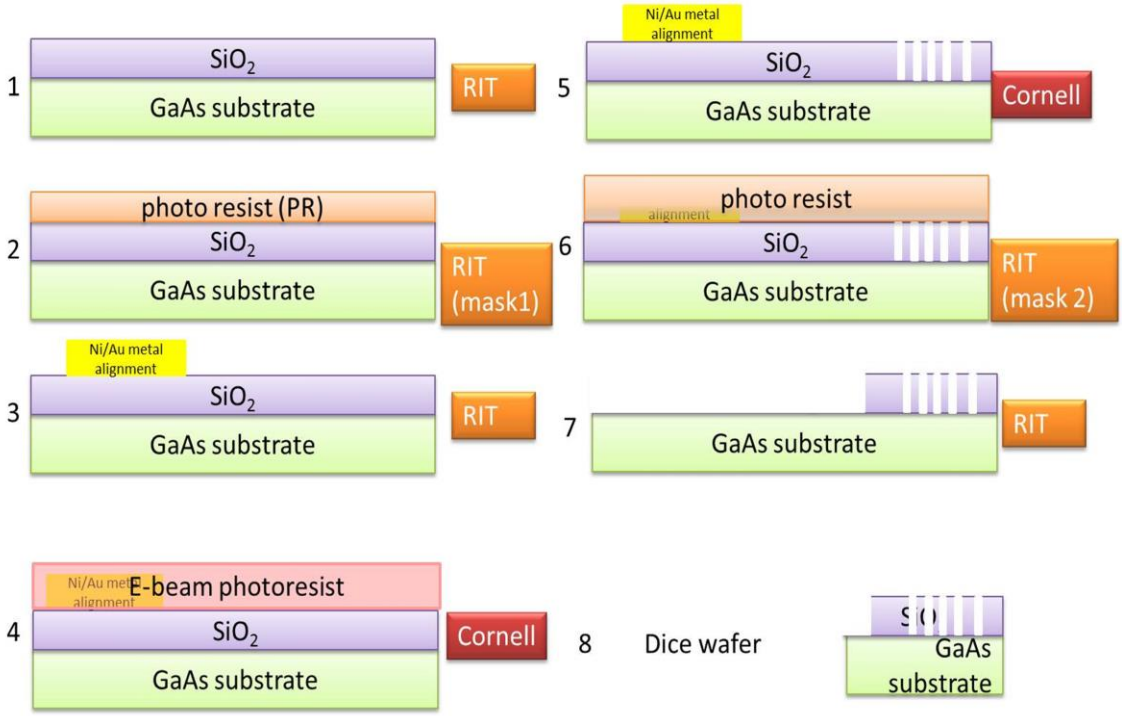

Figure 5.3 Flow chart of E-beam mask fabrication for nanowire growth

During the InAs nanowires epi-growth, the GaAs substrates were placed into the MOVPE reactor chamber in a flow of hydrogen as carrier gas. Table 5.1 shows the typical InAs NW growth parameter. With relatively low reactor pressure (60 Torr), a constant flow of the group-V precursor gas arsine (AsH_3) was maintained during heating to prevent substrate decomposition. Following a high temperature (~575°C) deoxidation step under the arsine atmosphere, the wafer was cooled to the nucleation temperature. Trimethylindium (TMIn) was injected into the chamber with the arsine to generate the metallic droplets on the substrate surface at temperature ranging from ~350ºC. The growth temperature was varied between 375ºC and 725ºC, which was measured in-situ

using a thermocouple. Due to the placement of the thermocouple, the measured temperature may be slightly different with the real growth temperature in the GaAs substrate. Assuming that thermal conduction is sufficient, the temperature difference between the thermocouple and the sample surface does not affect the conclusion of the study. The V/III ratios can be controlled by adjusting the flow rate of Arsine. The V/III ratio is 95 and 12 for the InAs NWs grown with AAO and the rest InAs NWs, respectively. After the growth was complete, the precursors and heaters were turned off to lower the sample temperature to 30°C before removal from the reactor.

Table 5-1 Typical InAs NW growth parameter

Parameter	Value
Reactor pressure	60 Torr
Catalyst	50 nm Au Particle
Rotation	1000 rpm
Adhesion Promoter	Poly-l-lysine
Carrier gas	Hydrogen
Organometallic precursors	Trimethylindium and Arsine
Partial pressure of Trimethyindium	2.0×10^{-3} torr
Partial pressure of Arsine	0.02 torr ~0.12 torr

The SEMs, including LEO EVO50 LaB_6 system and LEO ZEISS 1550 field emission scanning electron microscope (FESEM), were used to complete the InAs nanowires morphological characterizations: assessing overall length, shape, density and the orientation of these InAs nanowires. The accelerated electrons in an SEM carry

significant amounts of kinetic energy, and this energy is dissipated as variety of signals produced by interactions between electron and sample, when the incident electrons are decelerated in the solid sample. By changing how the electrons are bent and how the beam of electrons strikes the sample, the magnification and focus can be adjusted. Images of three different views were taken: a top-down view, 45º tilt, and cross-section view. Notice that due to the fact SEM utilizes electrons to form an image, samples must be specially prepared. All water must be removed from the samples, because the water would vaporize in the vacuum. Some samples need to be made conductive by covering the sample with a thin layer of conductive material (Au, etc). Clean cleaved InAs nanowire samples in this chapter were attached to the sample stage via clippers or a round carbon tape.

5.4 Results and discussion

5.4.1 InAs nanowire growth with Au seeds

Figure 5.4 shows the cross-section view of the InAs nanowire grown on the GaAs (111)B substrate with spin-coated Au Seeds. The InAs Nanowire is normal to the substrate align in <111> direction. The average diameter of the nanowire is 0.55 μm (measured by image processing program of ImageJ [198]) and the length of nanowire is 3.74 μm. This indicates that (111)B substrate is favorable for Indium deposition and diffusion. The nanowire on (111)B with Au seed showing a strong tapering effect with a larger base and narrow tip (0.05 μm, correlating to the Au seed diameter). The aspect ratio (length/base diameter) and the tapering ratio (tip diameter/base) can be tuned by varying growth temperature and III/V ratio during the MOCVD growth [186].

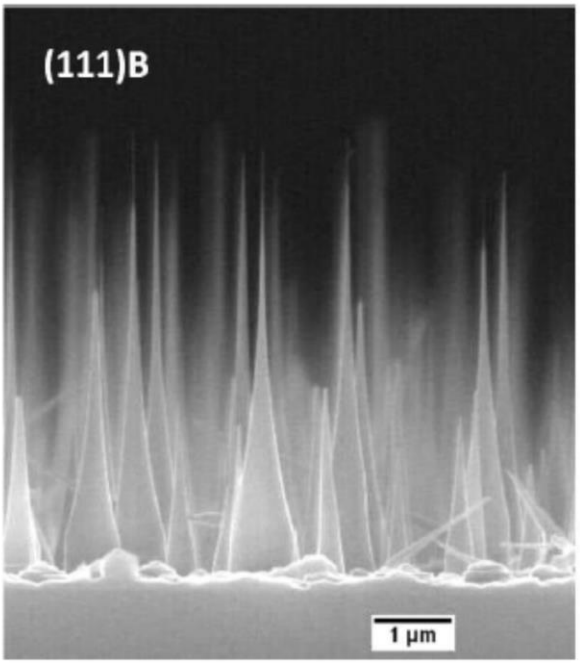

Figure 5.4 Cross-section SEM image of InAs nanowires grown on (111)B using Au seed

5.4.2 InAs nanowire growth with AAO Mask

To achieve selective area nanowires VLS growth, Au was first patterned with the AAO membrane. Figure 5.5 (a) shows a photo of the AAO membrane before Au evaporation on the (111) GaAs substrate, which shows an irregular shape from electro-deposition. Figure 5.5 (b) shows the SEM image with a magnification of 80 kX. The observed broken membrane is from over etching with phosphoric acid during through-hole etching process. To measure the diameter of each pore formed by the self-assembled membrane, Figure 5.5(c) shows the zoomed-in SEM image with a magnification of 130 kX. The shape of each pore in is hexagonal with a relatively thin wall between each other. Using the ImageJ software [198], the measured mean value of the diameter of the pore is 70 nm with a standard deviation of 3 nm.

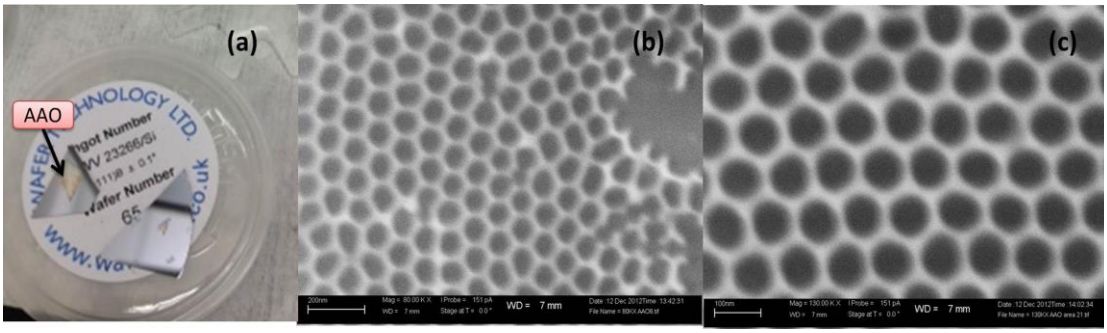

Figure 5.5(a) photo of AAO, and Top down SEM image (b) Magnification of 80 KX (c) Magnification of 130 KX.

Figure 5.6 (a) shows SEM images after Au thermal evaporation to the GaAs wafer, and AAO membrane was tried to be removed with ultrasonic bath. There are there layers from left to right with different contrast. The darkest layer is the GaAs surface with Au seeds, and the rest two layers are the residual AAO membrane. Figure 5.6 (b) shows the SEM image of the second layer of AAO in the Figure 5.6 (a), and the barrier between each pore is thicker compared to figure 5.6 (c), which could be the non-uniformity of the AAO deposition across wafer or the Au coating. Figure 5.6 (c) shows the pattered Au seeds with reduced average size of 55 nm. Compared to the AAO opening diameter, the reduced Au diameter be due the opening of AAO has larger surface opening than the bottom. Some of the patterned gold has been unintentionally removed by ultrasonic bath.

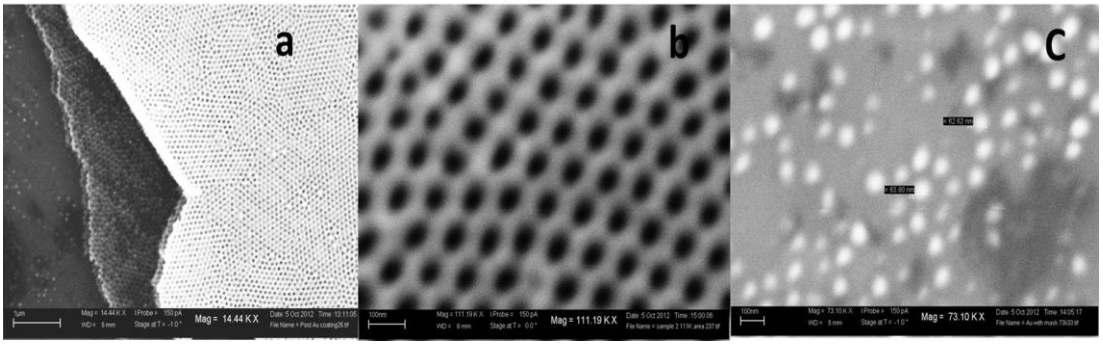

Figure 5.6 SEM image of AAO membrane (a) at low magnification, (b) at high magnification, and (c) patterned Au catalyst via thermal evaporation

Figure 5.7 (a) shows the SEM image from the growth results of growth of InAs NW on GaAs with pattern Au seeds. The V/III ratio during growth was set with 95, and the growth temperature is 375°C. The nanowires are off-patterning and some extra-large lumps can be observed. This may be to the initial migration of Au along the (111) GaAs surfaces prior to the InAs growth [194], which is observed by Zhang *et al.* [199], so the originally patterning was interrupted. Figure 5.7 (b) shows SEM image of the InAs NWs growth on the Au evaporated GaAs surface, which shows improved surface density (over 10 nanowires per square micrometers) of NWs compared to Figure 5.7 (a). This phenomenon may be due to the uniform in the Au covering.

Figure 5.7 45° degree titled SEM image of InAs NW with Au thermal evaporation (a) patterned (b) un-patterned.

Figure 5.8 (a) shows 45° titled SEM image of the InAs growth on AAO membrane. Instead of nanowire one dimensional nanowire growth, there are all lumps formed on the top of the AAO surface. Figure 5.8 (b) shows a top-down SEM image. The measured diameter of the lumps is over 200 nm. These lumps indicate a comparable growth in all directions. Some InAs was grown through the opening of AAO membrane. In order to

take a close observation, Figure 5.8 (c) shows the zoom-in SEM image with a magnification of 80 kX. The size of InAs seems first to depend on the opening of AAO membrane and is enlarged along the surface of AAO membrane.

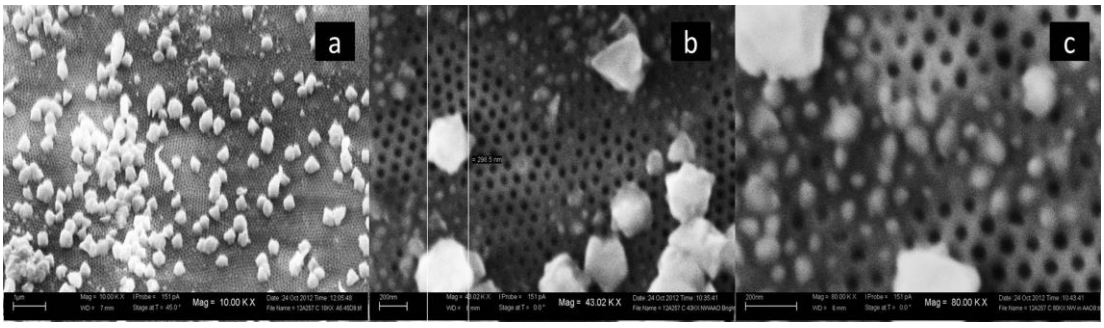

Figure 5.8 SEM image of Nanowire grown with patterned AAO (a) 10KX magnification in 45° tilted degree, (b) 40 KX magnification, (c) 80 KX magnification.

5.4.3 InAs nanowire selective area growth via electron beam patterning

An alternative method to realize InAs nanowire selective area epi-grwoth can be achieved by using masks formed by electron beam lithography [200]. SiO2 are widely used as the layer to transfer the pattern because it can be removed easily by HF based solution, which doesn't affect the III-V nanowire. From the dose test, the optimized dose of the electron beam exposure on a 20 nm SiO_2 layer is between 350 $\mu C/cm^2$-450 $\mu C/cm^2$.

Figure 5.9 (a) shows the SEM image of the developed SiO_2 mask after e-beam exposure under dose of 350 $\mu C/cm^2$. The real exposure time over 4 hours for three 1.1 mm× 1.1 mm, which were much longer than the schedule file predicted, because the JEOL6300 E-beam writer cannot read large data and print at the same time. Additionally, strict alignment also extended the JEOL 6300 writing time. The average diameter of the hole is 290 nm. Figure 5.9 (b) shows the mask after reactive ion etching. The SiO_2 inside the exposed hole has been removed. The diameter of the etched hole was slight reduced to

260 nm, because the exposure of the photoresist in the edge is not enough. Figure 5.9 (c) shows the SEM image before dicing, which removed SiO_2 outside the e-beam exposed area with BOE etch. Due to isotropic etch, although there are photoresist covered on the pattern, the diameter of the opening was increased to 310 nm.

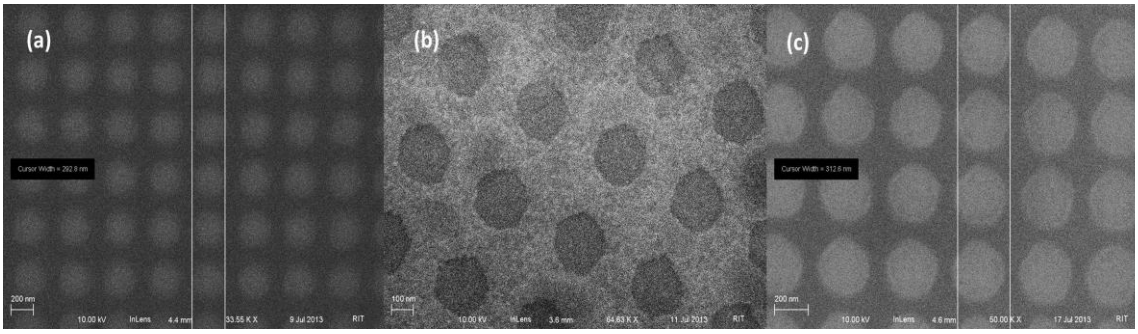

Figure 5.9 SEM image of 20 nm thick SiO2 patterned mask for nanowire growth (a) before dry etch (b) after dry etch, (c) before dicing

Figure 5.10 (a) shows the best results of the catalyst free InAs nanowires growth with three E-beam masks. The growth temperature was 625°C, which is consistent with literature. In order to form a *p-n* junction, InAs nanowires with different doping in the core and shell structure were planned to grown within these patterned opening. However, although the growth time and temperature had been adjusted, most Si doped InAs and Zn doped InAs were covered on the masks surface, instead of forming nanowire in the mask opening. Figure 5.10 (b) shows the top down SEM image with a higher magnification of 35kX. Instead nucleating into the opening of the pattern and growing perpendicular to the substrate to form nanowire, a thin layer of InAs is grown on the surface of GaAs and finally covers the pattern. There some layer growth steps also can be observed.

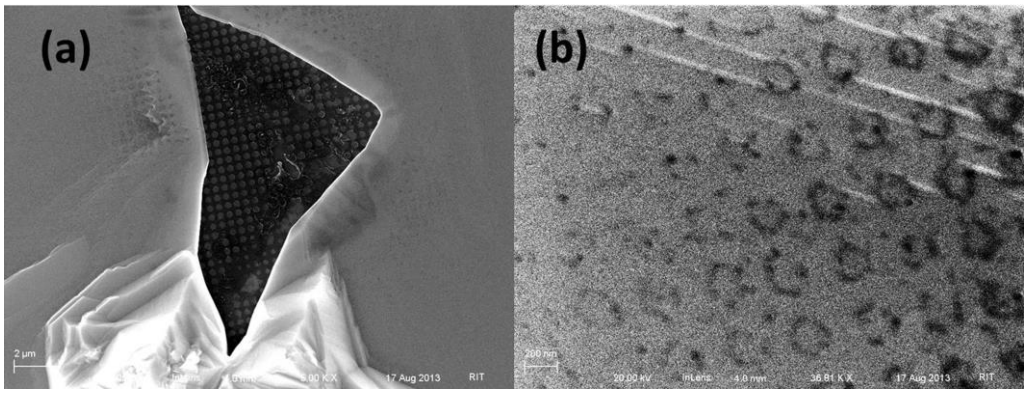

Figure 5.10 Top-down SEM image of nanowire growth with E-beam patterned SiO_2 masks (a) magnification of 5 kX (b) magnification of 36 kX.

In order to make more masks for nanowire growth with a limited funding, it is important to reduce the e-beam writing time. The second beam exposure was change to JEOL 9500 E-beam writer, less requirement in the alignment was placed in the programming file. Figure 5.11 (a) shows the second patterned SiO_2 mask before dicing. The observed oval-shaped stigmation was from the less confined alignment. Furthermore, instead of pattern a circle, the open shape were change into oval with applied larger E-beam dose over 500 $\mu C/cm^2$. The second E-beam expose time for 12 pads was decreased to within one hour. The length and width of the opening is around 100 nm and 200 nm, respectively. Figure 5.11(b) shows top-down SEM image of the optimized core-shell InAs nanowire growth with fixed V/III ratio of 8. Despite most area are covered with InAs, some patterned nano-rods still can be observed with diameter around 220 nm. Figure 5.11 (c) shows the zoom-in SEM image of these patterned nano-rods. It is found that the growth first appears vertically to the surface as expected, but then growth rate along the lateral direction is faster than vertical direction, so the nanowires start to connect to each other laterally. This InAs nanowire lateral overgrowth in the <110>

direction was also observed by K. Tomioka *et al* [188]. The failure of the nanowire vertical growth may be from a combination effect of the small period (barrier thickness between the opening) and the growth temperature.

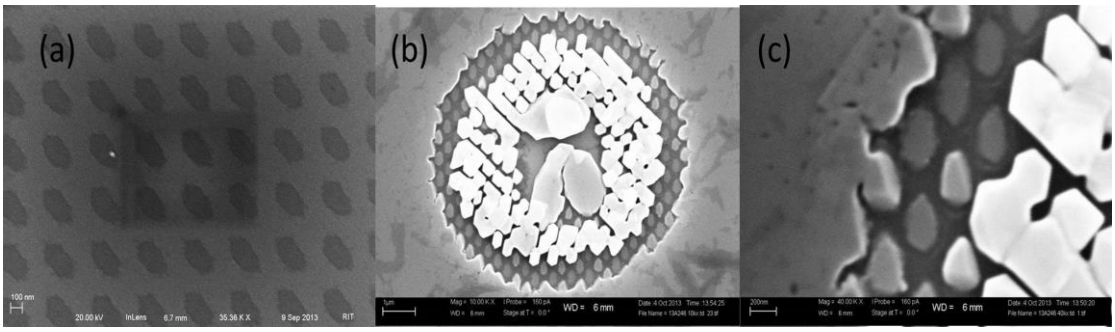

Figure 5.11 Top-down SEM images of (a) second SiO_2 mask with reduced writing time, nanowire growth with the second mask (b) 10 KX magnification (c) 40 KX magnification.

5.4.4 Crystal structure analysis of catalyst free patterned nanowire grown by diblock copolymer

Additionally, a polystyrene/ploymethyl methacrylate (PS-b-PMMA) diblock copolymer (DBC) patterning technique was used in the selective area InAs Nanowire growth in MOCVD. The growth were completed by the collaborator Wisconsin University and the growth detail was record elsewhere [36]. The defect and structural properties of the InAs nanowires were analyzed by transmission electron microscopy (TEM) using an FEI Tecnai F20 high resolution transmission electron microscope (HRTEM) operated at 200 kV. Cross-section samples for TEM were prepared using two face-to-face bonded cleaved pieces of the wafer. A coarse cross-section lamella was cut from the center of the NW bundle and transferred to a tripod grinder before ion-milling. The lamella was sliced into thin sections using a Gatan 691 Precision Ion Polishing System (PIPS) Ar-ion-

milling technique. All measurements and fast Fourier transform (FFT) were performed by Image J software [198].

Low-resolution TEM images indicate that the nanowires have a tight diameter distribution with nanowires that range in length from 1 to 3 μm. To further investigate the interface of InAs/GaAs heterostructures, Figure 5.12 shows high resolution TEM images of the nanowire sample taken with the beam aligned along the ⟨110⟩ zone axis of the GaAs substrate. InAs nanowires grew normal to the (111)B GaAs as shown in Figure 5a. Although SiN_x cannot be observed in Figure 5.12(a), it is clear the nanowires were nucleated and grown only in selected regions of SiNx from the periodic spacing observed in both the TEM and SEM images. Notice that NWs are narrower at the base surrounded by the SiNx mask but then become wider for the portion which protrudes above the mask. At the base, the nanowire is confined inside the SiNx patterning pores with the diameter confined to approximately 25 nm. Once the nanowire length exceeds the thickness of the SiNx mask, lateral growth can occur in addition to vertical growth. From the TEM image in Figure 5.12, we estimate that the diameter increases from ∼25 nm at the base to ∼27 nm above the SiNx mask. The dark and bright stripes seen in Figure 5.12 (a) indicate that twin planes or stacking faults [25], [201] exist along the length of the nanowire. This can be seen clearly in Figure 5.12(b) as a change in the direction of the columns of atoms along the length of the nanowire. The resulting zigzag pattern of the side facets seen along the length of the nanowire is also evidence of a primarily zinc blende (ZB) structure with extensive twinning. The ZB structures follow an ABCABC stacking sequence with each letter representing a bilayer of InAs pairs. A twin plane defects occur when a single bilayer is incorrectly stacked in a ZB crystal, which reverses the stacking

sequence from ABC to CBA. For example, in a section ABCABACBA, growing from left to right, A is the faulted stacked layer that creates the twin plane. Sequential twin planes or equivalently sequential twinned bilayers result in a platelet of the wurtzite (WZ) ABAB structure[202], [203]. Elevated growth temperatures are known to promote twin defect formation in GaP and GaAs nanowires [201]. In fact, Joyce *et al.* have shown that nanowires grown at higher temperatures (Tg > 500 °C) and with V/III ratios greater than 50 tend to have a higher density of twin planes within a primarily ZB lattice than nanowires grown below 425 °C with V/III ratios less than 50 [202]. Additional studies could lead to alternative growth conditions that be further optimized to reduce the density of twin planes.

Measurements of the InAs diameter yield a uniform diameter of 25 ± 3 nm along the growth direction, correlating well to the SEM measurements. Also based on the top-view SEM images, little to no tapering is observed along the nanowire length in SA-MOCVD, in contrast to previously published results where InAs nanowires were grown using the VLS process utilizing Au seeds [190], [204].

The interface between the InAs nanowire and the GaAs substrate is also visible in Figure 5.12(b). The dotted line was drawn as a guide to the eye and connects a number of interfacial misfit dislocations observed at the InAs−GaAs interface. The curved GaAs substrate to InAs nanowire interface was likely formed during the dry etching process since GaAs is slowly etched by CF4. A few interfacial misfit dislocations were observed at the GaAs−InAs interface under these diffraction conditions. Misfit dislocations relieve the lattice mismatch strain at the interface between the nanowires with larger diameter

(>20 nm) and the substrate, as reported previously [205]. Beyond the interface, in the bulk of the InAs nanowire, a series of twins with 1−4 ML periods are observed.

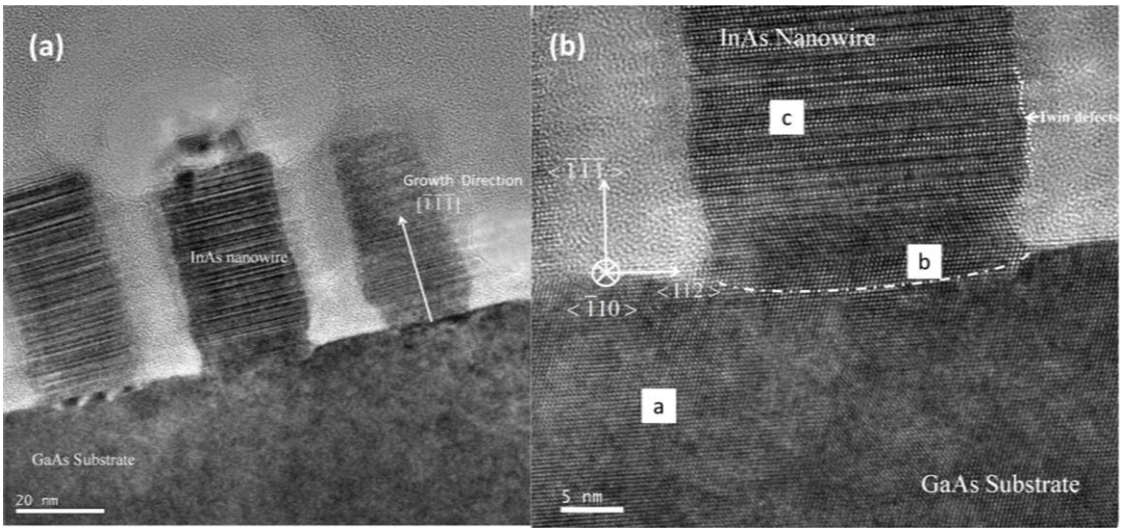

Figure 5.12 (a) Low-and (b) high-magnification TEM micrographs of an InAs nanowire grown on a GaAs (111)B substrate with notations

Figure 5.13 (a−c) present the associated fast Fourier transform (FFT) power spectrum patterns taken from the GaAs substrate (region a), InAs−GaAs interface (region b), and InAs nanowire (region c) as indicated in Figure 5.13 (b). Three diffraction planes for ZB materials are labeled in Figure 5.13 (a) and (b) as a guide to the eye. As can be seen in Figure 5.13 (a), the GaAs substrate is characteristic of a ZB structure (lattice constant was fixed at 0.565 nm). However, in Figure 5.13 (b), InAs nanowires initially grow with a ZB structure on GaAs substrate. Two interwoven but distinguishable diffraction patterns are observed with lattice constants 0.57 ± 0.01 and 0.59 ± 0.03 nm (relaxed InAs has a lattice constant of 0.605 nm). This shows that the InAs/GaAs interface is relatively sharp and strain is partially relieved at the interface misfits [206]. There may also be some degree of In−Ga intermixing, although the experimental uncertainty in the lattice constant measurement precludes making this determination with certainty (region b) [207].

Finally, the FFT in Figure 5.13 (c) shows an overlapping pattern of a ZB pattern possessing many twin defects [208]. The elongated streaks are due to the rotational twins of the nanowire ZB lattice [209].

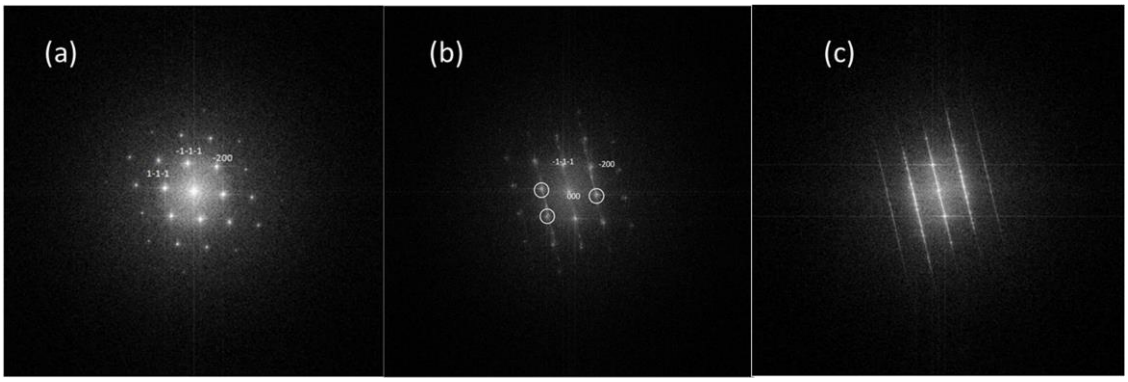

Figure 5.13 Fast Fourier transform patterns obtained from the TEM micrograph of Figure 5.12(b) from the regions indicated: (a) the GaAs substrate, (b) InAs−GaAs interface region, and (c) the bulk of the InAs nanowire

5.5 Conclusion

The development of InAs nanowire growth on (111)B GaAs substrate MOCVD was demonstrated with Au-assisted and catalyst-free selective area growth. Several patterning mask are successfully made, including the AAO membrane and E-beam lithography patterned SiO_2 layer. It shows that Au seeds can be patterned with the AAO, but the following growth InAs nanowire were non-patterning due to the growth was initiated with a horizon growth (lowest Gibbs energy direction). The InAs growth condition with E-beam exposed masks should be further optimized to enable a vertical growth rates faster than a lateral growth rate. Finally, crystal structure of catalyst-free InAs nanowires patterned via PS-b-PMMA was characterized via TEM. The TEM characterizations indicate that InAs nanowires are fully strain-relaxed with interfacial misfit dislocations near the growth interface of InAs and GaAs without additional threading dislocations, while the InAs nanowire shows a ZB crystal structure associating twin defects. For the

opto-electric devices, especially solar cell applications, the growth temperature, ratio, patterning opening affected the InAs nanowires growth in a MOCVD are crucial and required to be carefully evaluated and established to finally improve growth uniformity and eliminate existing defects.

Chapter 6

Summary and future work

This dissertation first describes developments of the QDSCs for IBSC applications in chapter 2 and 3. There are generally three challenges in the MOCVD epi-grown III-V QD-IBSCs: First, TSPA should dominates at room temperature among the competing processes; second, optimization of QD systems growth for the ideal band alignment for 63% efficiency under concentrated light sources; third, improve QD absorption within limited layer and surface densities. Chapter 2 addresses the first challenge, so carrier dynamics in InAs/GaAs QDSCs were carefully studied. To optimize TSPA at room temperature, other competing process including escape, recombination should be suppressed. It shows that an electric field decreases barrier height, so thermal escape and tunneling increase, while the electric field improves charge separation and radiative recombination lifetime. To optimize TSPA rate, the electric around QD region should be tuned to be able to balance the effect from both carrier escape and recombination inside a specific design of QD-IBSC. Barrier modification in InAs/GaAs QD-IBSC and investigations of alternative QD systems can be adopted to increase TSPA working temperature.

Chapter 3 discusses barrier modification in the MOCVD: experimental results on InAs QD in wide-band-gap materials, including InGaP and $Al_{0.3}GaAs$, are studied. Furthermore, the band structures of alternative QD systems including GaSb/GaAs QD and type II InP/InGaP were also demonstrated. To generally address the issues and solutions on the barrier modification study, Figure 6.1 (a) shows an ideal band alignment of QD-IBSC, only carrier in an IB is confined. However, in fact, as shown Figure 6.2 (b),

both electron and hole are confined in the QD systems, so the recombination rate increases at a flat band condition (external bias from the load towards V_{oc}). In this case, future work be on using certain electric field and devices layer design that enable a photon ratchet [34], [35], [210] IBSC. It also should be noted that MOCVD growth on all other QD systems other than InAs/GaAs QDs should be optimized in order to reduce defects center and improve QD morphology, which is critical to improve QD-IBSC efficiency.

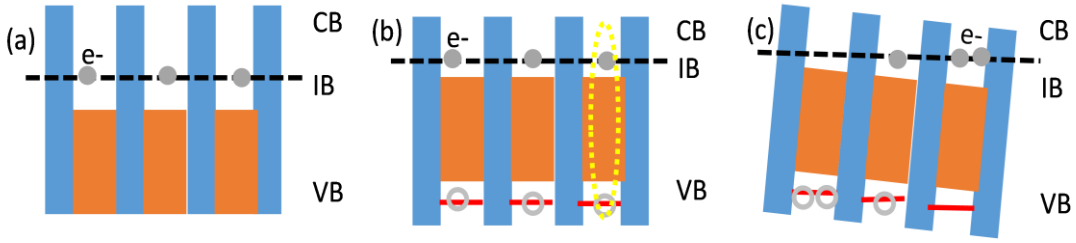

Figure 6.1 (a) Ideal barrier of QD-IBSC, carriers stay in IB for TSPA. (b) Reality in QD systems, carrier recombination in IB (c) Engineering direction: photon ratchet

For the third challenge on the enhancements of QD absorption and carrier concentration in an IB, light trapping with back surface patterning high has showed improved sub-bulk material band gap carrier collection in both quantum well solar cell [211] and InAs/GaAs QDSC[32]. Recently, Asahi *et al.* observed a strong TSPA in GaAs/$Al_{0.3}$GaAs heterstrocture solar cell with an insertion of InAs QD at room temperature [212], which indicates structures with higher optical absorption coefficient could be incorporated in a QD-IBSC. Figure 6.2 shows a preliminary design of GaAs/$Al_{0.3}$GaAs quantum well aided InAs/$Al_{0.3}$GaAs QD-IBSC. The idea to use this structure is to increases IB carrier concentration by using tunneling carrier from QW absorption, while fast hole escape from quantum well improve charge separation [213]. In fact, with properly back surface

patterning, TSPA rates in quantum well IBs [15] also can be improved to finally achieve voltage preservation [214].

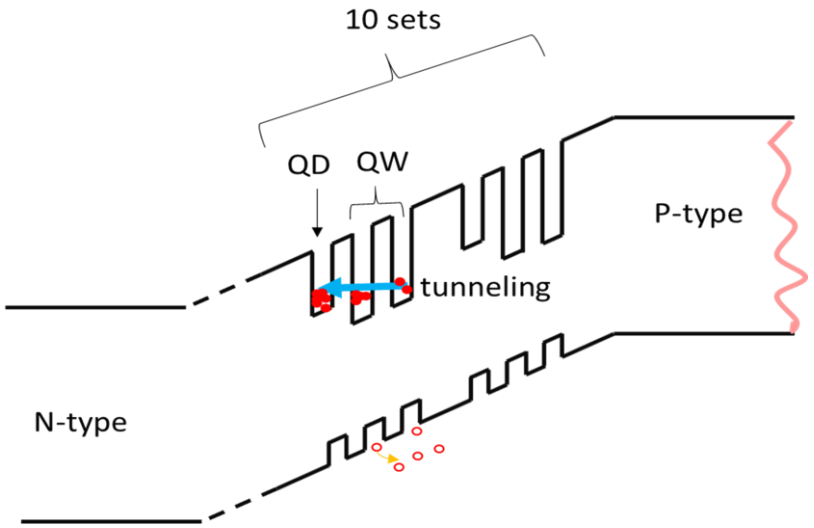

Figure 6.2 Design of *n-i-p* InAs/$Al_{0.3}$GaAs QD-IBSC with additional QW and back surface patterning that used to enhance photon absorption to boost carrier concentration in IBs and increase TSPA

The second part of the dissertation (Chapter 4) shows the developments of low light single junction InGaP devices. The designed and fabricated devices show a high conversion efficiency between 25%~40% under different indoor light sources with varied intensity [20]. Future work should be mainly focus on maintain the high efficiency and reduce the cost of material (especially the substrate [215]) and fabrication process. For MOCVD grown InGaP low light PV devices, improving material quality during the growth and enable *p-i-n* InGaP device can further improve open circuit voltage and efficiency. Additional mask design with fewer grid fingers on a larger (> 1 cm^2) device could also reduce the impact of side wall recombination on efficiency.

Last but not the least, because 84% cost of III-V PV devices is on substrate [22], III-V nanowire growth is crucial to reduce the cost of PV devices by increasing flexibility of

substrate selection. Furthermore, the optimization of III-V nanowire MOCVD growth has a much boarder application than PV devices, such as light emitting diode [216], transistor [217] [218] and etc. As discussed in Chapter 5, several masks have been successfully developed for nanowire selective area growth. Both Au-assited and catalyst free InAs nanowires growth results have been evaluated on (111)B GaAs substrate, which indicate a fundamental understanding of the diffusion and nucleation process in a specific MOCVD and patterning mask is very important to achieve uniform, defect free nanowire. Design of experimental on different growth parameters (temperature, growth temperature, partial pressure and etc.) will be beneficial to improve the fundamental understand and reduce experimental runs in a certain projects within a certain time. Future work should focus on III-V nanowire on Si substrate to improve the commercial application of these techniques.

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2. **Yushuai Dai,** Hyun Kum, Micheal A Slocum, George Nelson and Seth M Hubbard, "High efficiency single-junction InGaP photovoltaic devices under low intensity light illumination", in Photovoltaic Specialist Conference (PVSC), 2017 IEEE 44th, Washington DC, 2017.
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9. **Yushuai Dai,** Stephen Polly, Staffan Hellstroem, David V. Forbes and Seth M Hubbard., "Electric Field Effect on Carrier Escape from InAs/GaAs Quantum Dots Solar cells", *Photovoltaic Specialists Conference (PVSC),* 2014 40th IEEE
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