

CHARACTERIZATION OF WELLS FOR THE CMOS PROCESS

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ABSTRACT

SUPREM simulations were run to determine a junction depth of 3um and a sheet resistance of approximately 5kohms/square to be used in wells for CMOS fabrication. From these results an experiment involving an implant energy of 80 KeV, doses of $4E12/cm^2$, and $8E12/cm^2$, drive-in temperatures of 1100C and 1150C, and drive-in times between 2 and 8 hours was performed. Sheet resistances, measured using a four point probe, and junction depth, measured using a groove and stain tool, correlated well to SUPREM simulations.

INTRODUCTION

The first step in a CMOS process is the well level. There are two major methods with which to create a well: diffusion and ion implantation. Both diffusion and ion implantation are used to introduce impurity atoms in silicon. While diffusion is a thermal process, ion implantation is a kinetic process. High temperatures are necessary to diffuse impurities in silicon, while implantation dopes by providing the ionized atoms with enough energy to penetrate the surface of the material. Ion implantation allows us to obtain more accurate doping concentration profiles at the expense of crystal damage.

During an implant, ions are created in a source such as an RF gas discharge or a Penning source. Ions are extracted from this source, accelerated (10 - 5000 KeV), and focused to a beam. Undesired ions are removed by means of a mass separation magnet so that a beam of very pure dopants is made available. When the accelerated ions strike the silicon they penetrate it to a depth determined by their energy (KeV) [1].

Bombardment of a silicon crystal by a beam of ions, whose energies are about ten times greater than the energy holding the silicon atoms in their lattice, results in displacement of the silicon atoms by both direct and secondary impact. The damage and disorder due to any implant has to be removed by annealing so that the only electrical properties of the silicon altered by the implant are those dependant on carrier concentration. Mobilities and lifetimes are both greatly reduced by disorder in the lattice and must be preserved for devices to reach their design specifications. Annealing is also required to allow the implanted dopant atoms to reach proper substitutional

lattice positions and to ionize (activate). At annealing temperatures above 950C full activation occurs; 100% bulk mobility, and lifetime completely recovered. It should also be mentioned that the silicon consumed during oxidation accompanying drive-in of an implant is the damaged layer of the surface [2].

There are four important practical features of ion implantation. Dose can be accurately controlled for 10^{16} ions/cm² equal to the heaviest diffused predeposition down to less than 10^{11} ions/cm² (several orders of magnitude down on what can be achieved by diffusion) and ion implantation is always more accurate. Implantation can take place through a thin oxide. The implant may also be buried without disturbing surface concentration. Masking material dose not need to survive high temperatures, so metals or even photoresist can be used. Large impurity doses do not require long times: more impurity can be put in at room temperature than could be done with long diffusions at 1100C [3].

The p-well process had been the commonly used technology for earlier CMOS circuits before the technique of ion implantation was widely used for threshold control. Since the gates of the n- and p-channel transistors are tied together and the applied gate voltage keeps one device on and the other one off, the threshold voltages of the two devices should be closely matched. In most recent designs, the control of the threshold is accomplished by ion implantation. Traditional p- and n-well structures make use of a deep impurity diffusion to form the well. Since impurity atoms diffuse vertically and laterally, a lot of the lateral area is used up, resulting in a lower packing density. With ion implantation, since the annealing temperature doesn't need to be as high as a diffusion temperature, the implanted profiles show minimal lateral spread. The resulting profile yields many improvements such as high conductivity and a low ohmic drop, improved punch-through voltage, reduced junction capacitance and body effect, and better latch-up immunity [4].

EXPERIMENT

Different processes were researched [5-8] and numerous SUPREM simulations were run from which it was determined that a junction depth of 3 microns and a sheet resistance of around 5Kohms/square was desired. From this, an experiment involving doses of 4×10^{12} /cm² and 8×10^{12} /cm², energies of 150 KeV for the phosphorous implant and 100 KeV for the boron implant, drive-in temperatures of 1100C and 1150C, and drive-in times between 2 and 8 hours was planned. Upon processing, however, it was found that the implanter can only maintain focus of ion beams up to 80 KeV, so that is what was used. A summary of experimental conditions is given in Table 1.

A mask set was designed using the wells shaped as resistors. The resistors were of different lengths and widths three of which are 16 squares and three of which are 11 squares in size. four P-type and four N-type <100> wafers were cleaned and

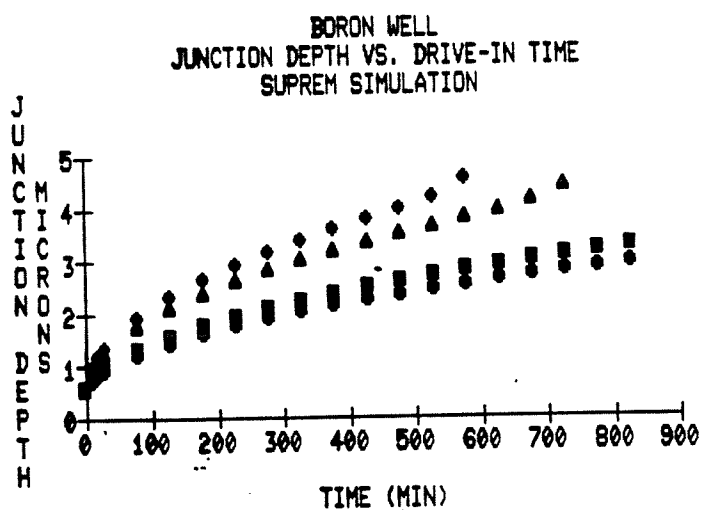
TABLE 1 EXPERIMENTAL CONDITIONS	
PHOSPHOROUS	ENERGY =80 KEV
WELL:	
	DOSE=4E12 and 8E12 atoms/cm2
	DRIVE-IN TIME=2,4,6 and 8 hours
	DRIVE-IN TEMPS=1100C and 1150C
BORON WELL:	ENERGY=80 KeV
	DOSE=4E12 and 8E12 atoms/cm2
	DRIVE-IN TIME=2,4,6 and 8 hours
	DRIVE-IN TEMPS=1100C and 1150C

approximately 7000A of oxide was grown in wet O2. This oxide was the mask during implantation. KT1820 resist was applied and the wafers were photolithographically patterned. This left bare silicon where the implant was desired. The wafers were cleaned, implanted, and driven in. The wafers were broken into four pieces to accommodate all the drive-in times and temperatures. The drive-in was done in wet O2 for 10 min. Then the remaining time in N2. The thin oxide deposited during this step was to keep damaging nitrogen atoms away from the bare silicon surface. It was originally planned to process the contact cut and metal layers and probe for the sheet resistance at the probe stations, but due to time restrictions this was not done. Instead, after drive-in the sheet resistance of the implant was measured using a four point probe in large implanted regions outside of the resistor patterning and junction depth was measured using a groove and stain tool.

RESULTS/DISCUSSION

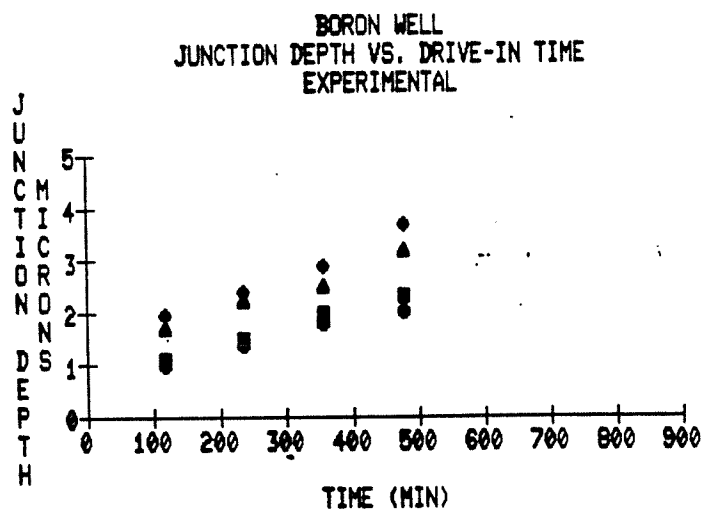
Figure 1 shows the junction depth vs. drive-in time for both boron and phosphorous implanted wells. One can see that the SUPREM simulations gave smooth curves for the junction depth vs. drive-in time graphs for both the boron and the phosphorous wells. These curves increase with increasing drive-in time as was expected. The experimental results showed actual junction depths that were a little shallower for the same energy, dose, and drive-in time and temperatures. However, they were not far off from the simulated results.

Figure 2 shows the sheet resistance vs. drive-in time for both boron and phosphorous implanted wells. For the boron well the sheet resistance quickly increased then very slowly decreased with increasing drive-in time where the phosphorous implant sheet resistances quickly decreased then very slowly decreased with



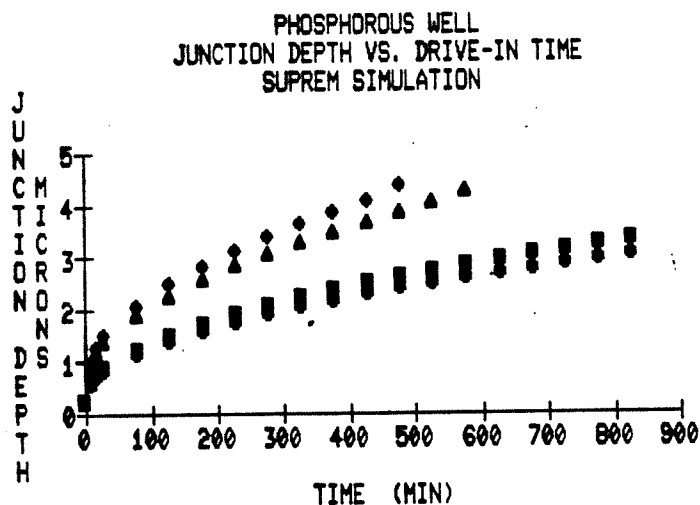
ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1180° C
- 80 KeV - 8E12 - 1180° C
- ▲ 80 KeV - 4E12 - 1150° C
- ◆ 80 KeV - 8E12 - 1150° C



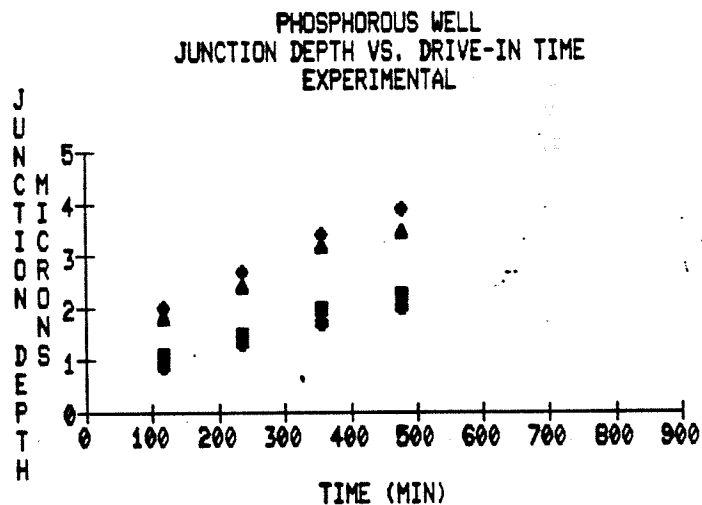
ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1180 DEG. C
- 80 KeV - 8E12 - 1180 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C



ENERGY - DOSE - DRIVE-IN TEMP

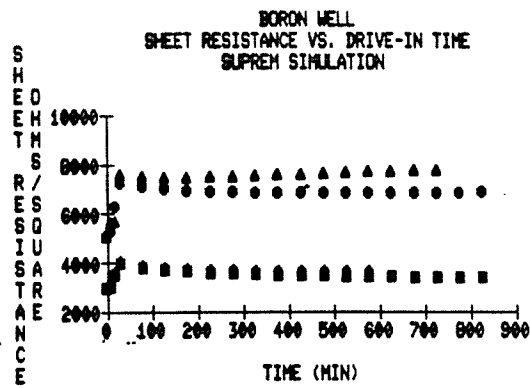
- 80 KeV - 4E12 - 1180 DEG. C
- 80 KeV - 8E12 - 1180 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C



ENERGY - DOSE - DRIVE-IN TEMP

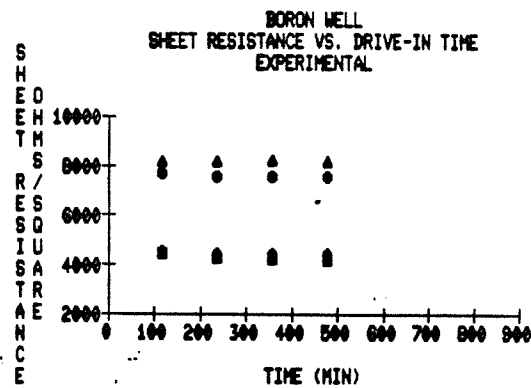
- 80 KeV - 4E12 - 1180 DEG. C
- 80 KeV - 8E12 - 1180 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C

Figure 1: junction depth vs. drive-in time



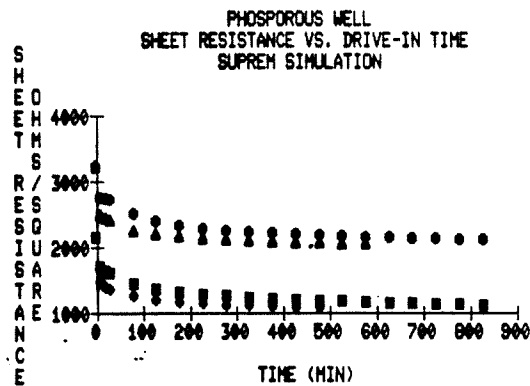
ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1100 DEG. C
- 80 KeV - 8E12 - 1100 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C



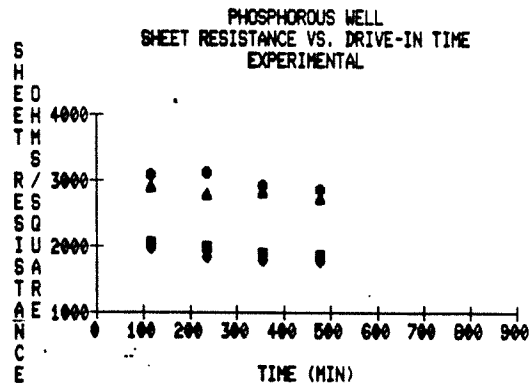
ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1100 DEG. C
- 80 KeV - 8E12 - 1100 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C



ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1100 DEG. C
- 80 KeV - 8E12 - 1100 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C



ENERGY - DOSE - DRIVE-IN TEMP

- 80 KeV - 4E12 - 1100 DEG. C
- 80 KeV - 8E12 - 1100 DEG. C
- ▲ 80 KeV - 4E12 - 1150 DEG. C
- ◆ 80 KeV - 8E12 - 1150 DEG. C

Figure 2: sheet resistance vs. drive-in time

increasing drive-in time. The time period of this quick increase or decrease corresponds to the time of oxidation at the beginning of drive-in. The reason for this sharp increase in sheet resistance for the boron implant is the loss of dopant to the oxide making it more resistive. The reason for this sharp decrease in sheet resistance for the phosphorous implant is what is called the 'snow plow effect' where dopant is piled up at the surface giving a decrease in resistance. It is my judgement that SUPREM dose not model resistivity due to damage anneal. If it did, the graphs would have shown a steeper decrease in resistance over time, unless it occurred during oxidation. The experimental results were higher than the simulated and showed almost straight curves after two hours in each case. Thus, the dopant atoms are fully activated at this time; they have reached proper substitutional lattice positions and the damage is annealed.

SUMMARY

The well level of a CMOS process characterized by SUPREM simulations as well as experimental data. Junction depth and sheet resistance was analyzed as a function of implant energy and dose as well as drive-in time and temperature. Experimental data for the junction depth agreed well with simulated data. The experimental data for the sheet resistance also agreed fairly well, but it is my opinion that the SUPREM data dose not correctly simulate the annealing process in the case of resistivity. This information will hopefully prove to be useful in the upcoming CMOS processing here at RIT.

ACKNOWLEDGMENTS

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