ADVANCES IN PROCESS MODELING AT RIT
SUPREM III and MINIMOS

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ABSTRACT

Process technology for integrated circuit fabrication continues to change and an efficent simulation of process capability must be assured, to avoid time-consuming and costly empirical approaches. Suprem III and MINIMOS are process/device modeling programs that will permit the process/device engineer to accurately simulate complete silicon fabrication technologies. An initial report on these two software packages is given here.

INTRODUCTION

Suprem III is the third generation of the process simulator Suprem. Written at Stanford University, version III attempts to substantially update previous simulator capabilities. Enhancements include five material layers that can be incorporated into the simulated structure and one hopes more accurate models for oxidation,diffusion and ion implantation.

Suprem III has recently been installed at RIT on the UNIX system. It is a computer aided program that allows the user to simulate the various processing steps used in the manufacture of silicon integrated circuits or discrete devices. The processing steps being dopant deposition and drive-in, oxidation of silicon and silicon nitride, ion implantation, chemical vapor deposition, epi growth and also etching of subsequent materials. The results of interest formulated by the model are the thickness of the layers that make up a device structure and the distribution of dopant within these layers. Suprem III can also calculate other material properties such as polysilicon grain size and sheet resistivity

MINIMOS, a software package from the Technical Institute of Vienna, is set up for two-dimensional MOSFET simulations. MINIMOS has the ability to generate two-dimensional doping profiles or to utilize two ,more accurate, one-dimensional simulations for gate and source/drain regions from Suprem and incorporate them into two-dimesional profiles of a paticular device.

This report will describe some capabilites of Suprem III, and justify a change-over from previous versions;also included will be a description of MINIMOS 4.0 and it's capabilities.

These two software packages will be both educational as well as extremely helpful in creating new process and device technologies here, at RIT.

SUPREM III

As stated earlier, the specific goal of characterizing Suprem III was to justify an update from the older version of Suprem II. One advantage is that five layers can be incorporated into the simluated structure as seen in Figure 1.

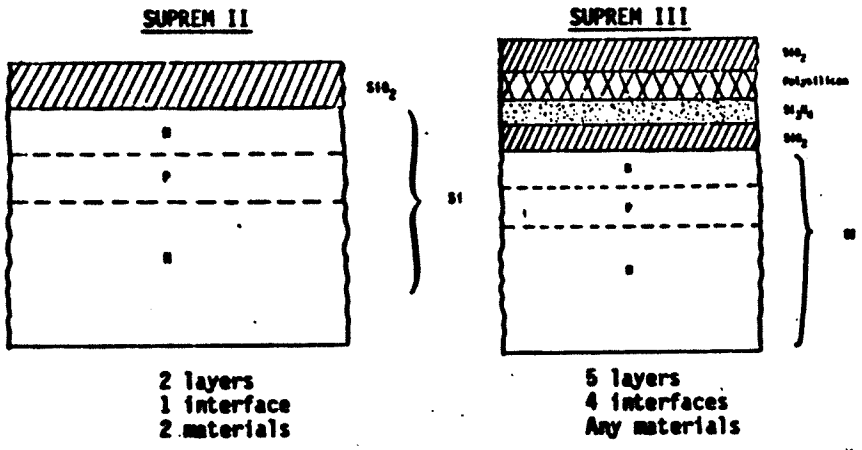

Figure 1: Material Layer Comparison

With polysilicon incorporated into the program the user may simulate such poly structures as high-value resistors, polysilicon gates or highly dopped emitters. With the use of a silicon nitride oxidation layer the user will be able to look into LOCOS applications. Each of these were not possible with the older version. Suprem III also had the capability of the user modifying the various parameters and coefficients associated with the prediction for each material layer. This will help the user taylor Suprem III to a desired process. Presently it is not possible to characterize the ability of Suprem III in modeling polysilicon and nitride layers due to the small database of nitride runs available and the UNIX program presently has a glitch when predicting polysilicon resistivities (predicts poly resistivities at about 10e24 ohms/cm, unacceptable).

When making a direct comparison between Suprem III and Suprem II in modeling oxidation, ambient drive-in, and ion-implantation, for current processes used at RIT, the two have been found to give similar results. A comparison was made using the RIT Factory NMOS process as a model. This NMOS process consists of starting out with the standard 8-20 ohm/cm P <100> wafers, performing several oxidations, various implants for threshold adjust, a polysilicon gate deposition and solid source diffusion for source and drain regions. The initial oxidation for 1000 angstroms of oxide is performed in a dry oxygen ambient at 1100 degrees for 50 minutes. The field oxides and gate oxides

grown in the same environment as the initial 1000 angstroms of oxide except growth time of the field oxide is 130 minutes and 30 for the gate oxide. The enhancement device receives a threshold adjust implant of boron at a dosage of 7.0e11 at an energy of 30 Kev. The depletion device receives the same implant as the enhancement plus an added implant of phorphorous at a dosage of 3.0e12 at an energy of 65 Kev. After threshold adjust, 9000 angstroms of polysilicon is deposited and is then concurrently doped with the source and drain regions by a solid phosphrous at 900 degress C for five minutes followed by a wet oxidation/drive-in for ten minutes at the same 900 degrees. Table 1 is a comparison of these results.

	Suprem II	Suprem III
Initial (1000 A) oxide	968 A	967 A
Field oxide	9959 A	9687 A
Gate oxide	712 A	706 A
Source/drain resistivity	50.7 ohm/sq	60.4 ohm/sq
Source/drain junction depth	0.507 um	0.553 um
Enancement Device Vt	1.35 volts	1.344 volts
Depletion Device Vt	-3.73 vol's	-4.44 volts

Table 1: SUPREM Comparison

From the results listed it can be noted that there is no difference between the two models when predicting oxide thickness. In the case of the phosphrous source/drain solid source diffusion, it is seen that Suprem III has slightly higher resistivties and greater junction depths. In the case of threshold voltages, both simulators give good results, but Suprem III has a greater negative voltage for the depletion device. This is due to the fact that Suprem III is taking into account a doped poly gate simulation, which has a higher work function than the default values set for the polysilicon region when used in calcualting threshold voltages in Suprem II. At present there is not data base at all for the NMOS process to determine which of the simulators is giving better actual results but it should be noted that Suprem III does make an attempt at having better predictive models than older versions and it should be accepted as better until there is a better data base of the on going proceeses at RIT.

MINIMOS

In additon to Suprem III, MINIMOS 4.0 will be added to the list of process simlators. Written at the Technical University of Vienna, MINIMOS 4.0 is a two-dimensional MOS transistor simulator. The software has the ability of calculating various 2-D profiles from parameters set by the user. By taking into account gate size, channel implants, source/drain doping and device biasing, MINIMOS creates a 2-dimensional models of the internal behavior of the device. Plots such as electron concentration, hole concentration, current density and doping can be generated.

MINIMOS offers several possibilities for the definition of the doping profile. First MINIMOS can calculated its own profiles or SUPREM can be used to calculate doping profiles much more accurately. From these profiles MINIMOS solve Poisson's equation for two dimensions and predicts the desired profiles.

The best way to further explain MINIMOS would be to give an example of a particular input file and show some examples of the results. Figure 3 is an input file where MINIMOS would determine the doping files internally.

The TITLE line is used to identify the file. In the DEVICE line the device is characterized as being an N-channel with a gate length of 2.0um, channel width of 10.0 um and having a gate oxide of 400 angstroms. The BIAS statement specifies an operating point may wish to look at; here the drain to source voltage is 5.0 volts, gate voltage is 2.5 volts, and the voltge of the substrate is 0.0 volts. The PROFILE statement is used to define background concentration (2.0e15 atm/cm2) and source/drain doping (40 Kev implant of phosphorous at a dosage of 1.5e15 atms/cm2 through 500 A of oxide, then drivien in for 15 minutes at 900 degrees). The IMPLANT statement is for modeling various implants in the channel region; here will be a channel implant of boron at 20 kev for a dosage of 7.1e11 atms/cm2 and driven in for 15 minutes at 900 degrees centigrade.

```
TITLE     RIT TRANSISTOR
DEVICE    CHANNEL=N TOX=0.400E-05  L=2.0E-04 W=10.0E-04
BIAS      UD=5.0  UG=2.5   UB=0.0
PROFILE   NB=2.0e15 ELEM=PH DOSE=1.5e15 AKEV=40 Tox=500.E-8
+         TEMP=900 TIME=15
IMPLANT   ELEM=B DOSE=7.E11 AKEV=20 TEMP=900 TIME=15
END
```

Figure 2: MINIMOS INPUT FILE

If the user wishes to use Suprem III to calculate the doping profiles, Suprem simulations must be performed for the source/drain and gate regions. A PRINT LAYER CONCNETR NET FILENAME=file.out statement must be used at the end of each

SUPREM III input file to generate files that contain impurity distributions that can be run by MINIMOS.

The following is a description of the plots shown in figure 3, generated from MINIMOS. These were created by John Faricelli of Digital Equipment Corporation, Hudson Massachussetts with the help of Surprem III and MINIMOS software. They represent a 2X10 um NMOS enhancement device using the RIT NMOS factory process.

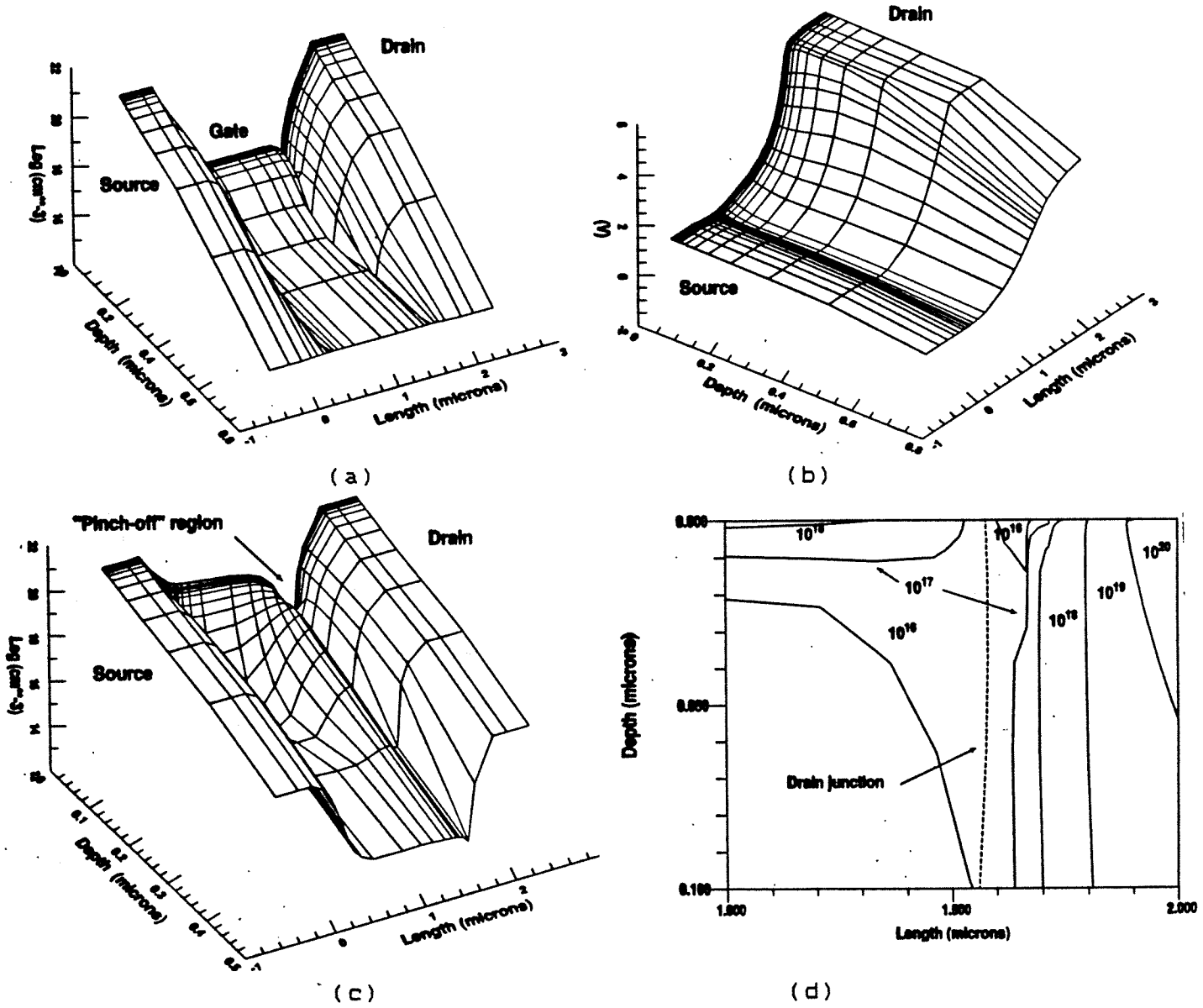

Figure 3: MINIMOS Examples

Figure 3(a) is a "3D" plot of doping concentraton. The channel implant can be seen as the small "hump" in the doping between the source and drain regions. This type of plot would be helpful in prediciting the effects of lateral diffusion on channel lenghths and find where the current density will be the greatest under the oxide ; MINIMOS can calculate current density

also. Figure 3(b) is a "3D" plot of potential in the device for a bias of Vds=5V and Vgs=2.5 volts. From the very step gradient in potential from drain to source region, voltage drops to nearly 0 volts at about 1 um into the channel, is an indication that this device may have a high field within it. This may lead to oxide breakdown near the drain junction and other problems. Figure 3(c) is a "3D" plot of the electron concentration. The "pinch-off" point can be seen as the drop in concentration near the drain junction. Figure 3(d) is a "2D" contour plot of the electron concentration near the drain region in pinch-off. The "pinch-off" region, on the 2-D plot is the electron concentration at 10e16 electrons/cm2 that goes from 0.0 to 0.015 microns deep. From this we can see that the device is not truly pinched off.

CONCLUSIONS

SUPREM III and MINIMOS are process/device modeling tools which are intended to be design aids in developing new devices and accompanying processes. With the update to SUPREM III and obtaining the VMS version, the process engineer will have a more usuer friendly package than previous version and have graphics capabilities not available now with SUPREM II. MINIMOS will not only allow a device engineer to quickly see the effects of doping, channel length and bias effects on a device but will also serve as an educational tool in showing the student the various internal characteristics of MOS transistors.

Also RIT will (hopefully) be obtaining a VMS version of SUPREM III from Digital Equipment Corporation. Not only will the VMS version be more user-friendly than the UNIX version, and possibly be "bug-free" upon installation, it will have the ability of producing graphics plots of the diffusion profiles on the HP7550 and DECLVP16 plotters, and on the VT340, VT240 and Workstation terminals. This is not possible now with the current VMS version of Suprem II.

ACKNOWLEDGMENTS

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REFERENCES

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