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Interpretation and Regulation of Electronic Defects in IGZO TFTs Through Materials & Processes

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A Dissertation Submitted in Partial Fulfillment of the Requirements for the Degree of Doctorate of Philosophy in Microsystems Engineering Program

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Kate Gleason College of Engineering

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ABSTRACT

Kate Gleason College of Engineering

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Degree: Doctor of Philosophy **Program**: Microsystems Engineering

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Dissertation Title: Interpretation and Regulation of Electronic Defects in IGZO TFTs Through Materials & Processes

The recent rise in the market for consumer electronics has fueled extensive research in the field of display. Thin-Film Transistors (TFTs) are used as active matrix switching devices for flat panel displays such as LCD and OLED. The following investigation involves an amorphous metal-oxide semiconductor that has the potential for improved performance over current technology, while maintaining high manufacturability. Indium-Gallium-Zinc-Oxide (IGZO) is a semiconductor material which is at the onset of commercialization. The low-temperature large-area deposition compatibility of IGZO makes it an attractive technology from a manufacturing standpoint, with an electron mobility that is 10 times higher than current amorphous silicon technology. The stability of IGZO TFTs continues to be a challenge due to the presence of defect states and problems associated with interface passivation.

The goal of this dissertation is to further the understanding of the role of defect states in IGZO, and investigate materials and processes needed to regulate defects to the level at which the associated influence on device operation is controlled. The relationships between processes associated with IGZO TFT operation including IGZO sputter deposition, annealing conditions and back-channel passivation are established through process experimentation, materials analysis, electrical characterization, and modeling of electronic properties and transistor behavior. Each of these components has been essential in formulating and testing several hypotheses on the mechanisms involved, and directing efforts towards achieving the goal. Key accomplishments and quantified results are summarized as follows:

- XPS analysis identified differences in oxygen vacancies in samples before and after oxidizing ambient annealing at 400 °C, showing a drop in relative integrated area of the O-1s peak from 32% to 19%, which experimentally translates to over a thousand fold decrease in the channel free electron concentration.
- Transport behavior at cryogenic temperatures identified variable range hopping as the electron transport mechanism at temperature below 130 K, whereas at temperature

greater than 130 K, the current *vs* temperature response followed an Arrhenius relationship consistent with extended state transport.

- Refinement of an IGZO material model for TCAD simulation, which consists of oxygen vacancy donors providing an integrated space charge concentration $N_{Vo} = +5\times10^{15}$ cm^{-3}, and acceptor-like band-tail states with a total integrated ionized concentration of $N_{TA} = -2\times10^{18}$ cm^{-3}. An intrinsic electron mobility was established to be $\mu_n = 12.7$ cm^2/V·s.
- A SPICE-compatible 2D on-state operation model for IGZO TFTs has been developed which includes the integration of drain-impressed deionization of band-tail states and results in a 2D modification of free channel charge. The model provides an exceptional match to measured data and TCAD simulation, with model parameters for channel mobility ($\mu_{ch} = 12$ cm^2/V·s) and threshold voltage ($V_T = 0.14$ V) having a close match to TCAD analogs.
- TCAD material and device models for bottom-gate and double-gate TFT configurations have been developed which depict the role of defect states on device operation, as well as provide insight and support of a presented hypothesis on DIBL-like device behavior associated with back-channel interface trap inhomogeneity. This phenomenon has been named Trap Associated Barrier Lowering (TABL).
- A process integration scheme has been developed that includes IGZO back-channel passivation with PECVD SiO_2, furnace annealing in O_2 at 400 °C, and a thin capping layer of alumina deposited *via* atomic layer deposition. This process supports device stability when subjected to negative and positive bias stress conditions, and thermal stability up to 140 °C. It also enables TFT operation at short channel lengths ($L_{eff} \sim 3$ µm) with steep subthreshold characteristics ($SS \sim 120$ mV/dec).

The details of these contributions in the interpretation and regulation of electronic defect states in IGZO TFTs is presented, along with the support of device characteristics that are among the best reported in the literature. Additional material on a complementary technology which utilizes flash-lamp annealing of amorphous silicon will also be described. Flash-Lamp Annealed Polycrystalline Silicon (FLAPS) has realized n-channel and p-channel TFTs with promising results, and may provide an option for future applications with the highest performance demands. IGZO is rapidly emerging as the candidate to replace a-Si:H and address the performance needs of display products produced by large panel manufacturing.

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Chapter 1. INTRODUCTION

1.1 THIN-FILM TRANSISTORS (TFTS)

The display industry has witnessed a dramatic displacement of Cathode Ray Tube (CRT) by Flat Panel Display (FPD) during the last two decades. The growth of Active Matrix Liquid Crystal Display (AMLCD) for FPD has undergone a tremendous upsurge. In LCD technology, pixels are connected to addressing line via Thin-Film Transistors (TFTs). When the TFTs are in the on-state, the pixel capacitor is charged and the established voltage (E-field) sets the liquid crystal position. In the off-state the stored charge holds the alignment state until a new signal arrives on the pixel bit-line. The on/off current ratio is important for TFTs because the on current determines the rate at which the pixels are charged while the off current is associated with the need to refresh a pixel. TFTs are also used in Active Matrix Organic Light Emitting Device (AMOLED) display technology, which is current-driven rather than voltage-driven.

The concept of thin-film transistor was first proposed and awarded a patent in 1933 [1], yet it was not realized until 1962, when P.K. Weimer at RCA laboratory fabricated the first TFT using cadmium sulfide [2].The first AMLCD matrix was demonstrated in 1973 using CdSe as active material for TFTs [3]. However, the demonstration of amorphous silicon TFT spurred the worldwide interest in TFT for AMLCD applications [4], [5].

1.2 OVERVIEW

Hydrogenated amorphous silicon (a-Si:H) has been the preferred choice of material for TFTs used as the switching devices for AMLCD. It has been the backbone of the FPD industry worth more than $100 B/year. The scientific community has been directed towards alternative materials and processing techniques for TFTs due to several factors. These include an evolving market for flexible and transparent display applications; increased demand of large-area displays with higher resolution and refresh rate; and thinner, lighter, low-power display technologies for hand-held portable devices. Due to low carrier (electron) mobility, a-Si:H cannot keep up with these demands. The two most viable candidate materials to fulfill these requirements are polycrystalline silicon (poly-Si) and Amorphous Oxide Semiconductors (AOS).

Low-Temperature Polycrystalline Silicon (LTPS) using Excimer Laser Annealing (ELA) has been in use for small format display devices for quite some time, offering higher levels of integration and device performance. Unlike a-Si:H, LTPS is CMOS capable and therefore more circuitry can be put on glass which can help realizing System-on-Glass (SoG) concept and can also lead to thinner and lighter display screens. Metal-oxide semiconductors have been extensively studied over the past decade due to their potential application in the FPD industry as a replacement for a-Si:H, and an alternative for LTPS. Indium-Gallium-Zinc-Oxide (IGZO) has become a viable technology as demonstrated by the recent commencement of commercial FPD backplane production [6]–[9]. In view of the recent advancements, it is expected that both polycrystalline Si-based and metal-oxide based technologies will be applied for high-performance displays in coming years.

1.3 MOTIVATION

Technology and customer expectations are evolving rapidly and fueling the research for innovative solutions to the shortcomings of existing technologies. Current high-performance display technology is not compatible with large-area manufacturing which directly adds to the cost of products. The FPD industry is looking for semiconductor materials/processing techniques with performance advantages over a-Si:H while still maintaining high manufacturability.

IGZO has been proven to be the most viable replacement for a-Si:H due to its easy inception in current fab plants for a-Si:H without any major investment in process tooling. Amorphous channel material has the inherent advantage of uniformity due to lack of grain boundaries, therefore the requirement for compensation circuits is minimum. The process technology is also compatible with extra-large glass panels such as Gen 10.5 (2.9 m × 3.4 m). The applicability of IGZO TFT panel has been demonstrated on Gen 8.5 glass for AMOLED display by BOE Technology [7] and LG [8].

IGZO has low processing temperature and is optically transparent; these properties can be exploited for transparent and flexible electronics. Optical transparency also provides a high aperture ratio and thus a lower power backlight is sufficient which increases battery life for hand-held devices. The low-off state leakage is important for wearable electronics as it improves battery life by enabling driving scheme of lower refresh rate without causing any flickering [10], [11]. Higher mobility of IGZO also renders high resolution and narrow bezels due to the improved charging characteristics for both pixels and integrated gate drivers [11].

Figure 1.1 reflects the motivation in a pictorial manner which is to explore the semiconducting materials for thin-film electronics that are compatible and manufacturable with large-area substrate. ELA-LTPS offers very high quality LTPS but production cost is high. An optimized solution manages the tradeoff between performance and cost. IGZO offers high manufacturability with a significant device performance improvement over a-Si:H. The display industry is diverse enough to utilize both of these technologies for suitable applications. Table 1-I summarizes the advantages and challenges for each; depending on the specific application either IGZO or LTPS may be preferred.

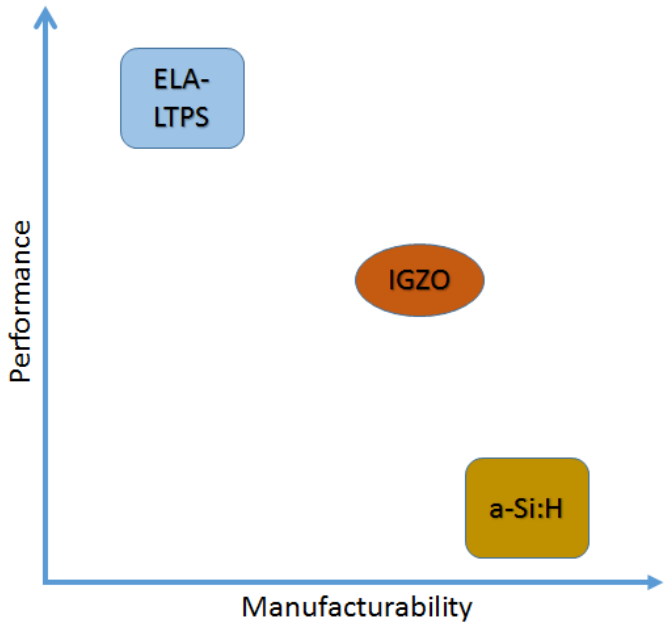

Figure 1.1: Performance vs manufacturability chart for different TFT technologies.

Table 1-I: TFT technology comparison.

Property	a-Si:H	ELA-LTPS	IGZO
Microstructure	Amorphous	Polycrystalline	Amorphous
Mobility ($cm^2/V \cdot s$)	~1	~100	~10
Device Type	NMOS	CMOS	NMOS
Process Complexity	Low	High	Low
V_T Uniformity	Good	Poor	Good
V_T Stability	Poor	Good	To be improved
Challenges	Performance	Yield, Scalability	Reliability

1.4 GOALS OF THIS STUDY

Despite the demonstrated performance of Indium-Gallium-Zinc Oxide (IGZO) thin-film transistors (TFTs), the influence of process variables on the material properties, and the correlation of the material properties with the device operation is not explicit. This is especially the case considering ongoing challenges with material passivation and device stability. IGZO exhibits n-type conductivity due to the presence of defect states. Defect states play multiple roles which establish both conductive properties of the material as well as anomalies in device behavior. Thus, the interpretation of defect states is of considerable importance.

The goal of this study is to characterize and interpret the electronic defect states in IGZO material and regulate the defects through processing and materials. The following listing summarizes the key accomplishments achieved in each component/element of investigation.

- The influence of annealing conditions on sputter deposited IGZO is investigated. Complementary measurements such as XPS/SIMS are performed to interpret the influence of annealing on IGZO material.
- An electrical interpretation of dielectric/IGZO interface defects after passivation material processing for improved stability.
- A TCAD material model refined for passivated devices by incorporating interface defect states and validated by predicting the behavior of different gate electrode configurations which is verified experimentally. A hypothesis based on TCAD simulation is proposed for the electrical modeling of DIBL-like behavior and suppressed through process integration.
- A physically-based empirical TFT model is presented to extract the device parameters and understand the device operation. This model accounts for the effect of both gate and drain biases on the occupation state of the tail-states which results in a 2D modification for the free channel charge.
- Process integration schemes such as choice of device structures, passivation materials and annealing conditions are investigated for improved performance and stability of TFTs. Application of encapsulation layer resulted in improved device stability against thermal and bias stress.

1.5 DOCUMENT OUTLINE

The remainder of the document is organized as follows:

Chapter 2 reviews the developments in IGZO TFT technology. Metal-oxide semiconductors have been introduced and literature survey for binary, ternary and quaternary oxide semiconductors is provided. The emphasis is given to IGZO material. Origin of semiconducting properties of IGZO are discussed along with the influence of film deposition and thermal annealing conditions. A review on back-channel investigations and bias-induced instability is presented. The aim of this chapter is to provide necessary information regarding the recent development in IGZO technology for a clear understanding and appreciation of current work.

Chapter 3 is devoted to the characterization of IGZO films for application in TFT technology. The as-deposited films are analyzed for composition, uniformity, crystallinity and resistivity. The influence of thermal annealing in oxidizing ambient is discussed. The influence of defects states is revealed during I-V measurements. Material characterization techniques are employed to investigate the change in film composition after annealing and is correlated with electronic properties of IGZO films.

Chapter 4 is dedicated to the development of the bottom-gate IGZO TFTs. This comprises process optimization including contact metallurgy, annealing temperature/ambient, gate dielectrics and passivation materials. Contact metallurgy and placement of annealing step in the fabrication process are discussed for unpassivated IGZO TFTs to develop a baseline process. Electrical results are provided for several passivation material candidates. Bulk defect states and interface defect states are numerically

calculated for different gate dielectrics through varying IGZO channel thickness. Experiments on annealing and the use of passivation materials are conducted to determine the resulting influence on IGZO film properties and device operation. This chapter concludes with the establishment of a controlled process for reproducible IGZO TFT performance which served as a platform for additional investigations.

Chapter 5 is dedicated to the TCAD simulation of the TFT operation using Silvaco® Atlas™. An IGZO material model is used for predicting the current-voltage characteristics. The influence of different defect states on the TFT behavior is discussed which helps in understanding the underlying physics behind the device operation. The material model is adjusted to match with the experimental data from Chapter 4. Interface defect states are added to the IGZO material model to develop an understanding of the passivation process for IGZO TFTs. The influence of defects states is revealed during I-V measurements. Charge transport behavior in IGZO is studied using low-temperature measurements down to 10 K.

Chapter 6 is dedicated to the TFT device modeling. Due to the presence of defect states in IGZO material, the conventional extraction methods are not adequate. The shortcomings of these methodologies are presented. Silvaco ATLAS is employed to understand the non-idealities observed in the conventional models due to the presence of ban tail-states. From this understanding, a TFT on-state model is developed to extract the device parameters. This model is compatible with SPICE level 2 model used for Si-technology.

Chapter 7 discusses some complex behaviors observed in IGZO TFTs. Hypothesis based on the extensive experimental data is presented and backed up by Atlas TCAD

simulation established in Chapter 5. These behaviors are suppressed by employing appropriate gate electrode configuration. Encapsulation of finished TFT is investigated for stability against thermal and bias stress. Topics for further examinations are discussed along with the hypotheses that need verifications through further experimentations.

Chapter 8 is devoted to Si-based TFT technology, which competes with oxide semiconductor technology. PMOS and NOMS TFTs using Flash lamp annealed polycrystalline silicon (FLAPS) have been demonstrated which make a strong case for future adoption.

Chapter 9 concludes the thesis by providing a summary of key contributions. Suggestions on further work based on the results obtained over the course of this study are provided to pursue in future.

Chapter 2. DEVELOPMENTS IN IGZO TECHNOLOGY

Amorphous silicon has been the primary choice in TFTs for decades because it can be deposited on large substrates at low cost, on-state current is acceptable, and off-state current is good. To improve upon its electrical properties, hydrogenated amorphous silicon (a-Si:H) was used in which hydrogen atoms passivate dangling bond defects [4], [5]. The demand of high pixel density and high refresh rate for better performance requires high switching speeds, which in turn depends on mobility which for a-Si:H has an upper limit of ~1 $cm^2/V{\cdot}s$ [12]. The flat-panel industry is currently at the point where high-performance TFTs are required to meet product demands.

Excimer laser annealed (ELA) low temperature polycrystalline silicon (LTPS) is already in production for switching matrix in flat panel displays. It enables both n-channel and p-channel FETs with high carrier mobility. Therefore, better resolution and high definition displays can be realized. However, the ELA process is expensive. Its applicability to the larger size glass panels (such as Gen 10) is still questionable. Alternative technologies for crystallizing silicon deposited on glass substrate have been extensively researched, however no other technique has been proven viable for manufacturing.

Amorphous oxide semiconductors (AOS) offer an order of magnitude increment in mobility over a-Si:H while maintaining low cost. AOS have undergone tremendous advancement in recent years and offer an alternative technology to directly replace a-Si:H

TFTs. These wide band gap materials offer higher aspect ratio due to transparency in the visible wavelength region. This combined with low temperature processing paves the way for realizing flexible and transparent display products.

The focus of this work is exploring indium-gallium-zinc-oxide (IGZO) semiconductor as TFT channel material for high-performance display applications. The remainder of this chapter provides a background on the oxide semiconductor, specifically IGZO technology.

2.1 METAL-OXIDE SEMICONDUCTORS

There has been an increasing interest in metal-oxide thin-film transistors (TFTs) for display and imaging array applications which require higher performance over a-Si:H TFTs. AOS materials offer higher electron channel mobility. In addition, the deposition techniques for metal-oxide materials are compatible with large glass panel (Gen 8 – Gen 10) manufacturing, unlike low temperature poly-silicon (LTPS). The improvement in metal-oxide semiconductor materials has resulted in transistor performance that is significantly higher than a Si:H, without the added process complexity required by LTPS manufacturing.

The early reports on metal oxide semiconductors involved TFTs fabricated using binary systems such as ZnO, SnO_2, In_2O_3 and Ga_2O_3. Recently, multicomponent oxide semiconductors have been explored. Metal oxide semiconductors exhibit n-type behavior with electron concentration 10^{16}-10^{21} cm^{-3}. The origin of conductivity is attributed to the native defects such as oxygen vacancies (V_O) and/or metal interstitials [13], [14]. These materials show high mobility (10 $cm^2/V{\cdot}s$) even in the amorphous state. This is due to their different electronic structure than Si-based material systems. Unlike covalent Si, oxide

semiconductors are ionic in nature and charge transfer occurs from metal s-orbitals to oxygen p-orbitals [15], [16], as discussed in detail in Section 2.2.3.

2.1.1 Binary Oxides

The search for oxide semiconductor started with investigations on binary metal-oxide such as In_2O_3 Ga_2O_3, SnO_2 and ZnO [17]–[23]. In_2O_3 TFTs have been reported with very high mobility (~100 $cm^2/V{\cdot}s$) but with large off-state leakage due to high electron concentration ~10^{18} cm^{-3} [17], [24]. Ga_2O_3 TFTs show low off-state leakage but the on-state current drive is poor with a reported mobility value of 0.05 $cm^2/V{\cdot}s$ [19]. SnO_2 TFTs show device operation in depletion mode where reducing the SnO_2 thickness (~10-20 nm) shifted the characteristics to enhancement mode, suggesting the presence of depleted top-surface [20].

The best performing binary oxide semiconductor is ZnO and has interested researchers due to its excellent semiconducting properties. Device using ZnO as the active channel has been reported to have high mobility and on/off ratio [11]. It is easy to deposit films of ZnO at low temperature using spray pyrolysis [27], sputtering [28], solution-based deposition [29], MOCVD [30] and ALD [26]. A comprehensive list of publications on ZnO transistors is provided in ref [31]. The transfer characteristics of a plasma enhanced atomic layer deposited (PEALD) ZnO TFT are shown in Figure 2.1 [32]. The saturation mobility, threshold voltage and subthreshold swing of the TFT reported were 20 $cm^2/V{\cdot}s$, 4.5 V and 200 mV/dec. respectively. Though the transistor performance is acceptable for the application as liquid crystal switch array, the grain boundaries in polycrystalline ZnO films present a challenge in terms of device performance uniformity [24], [33], [34]. Adding other metal cations ensures the amorphous structure of deposited film by

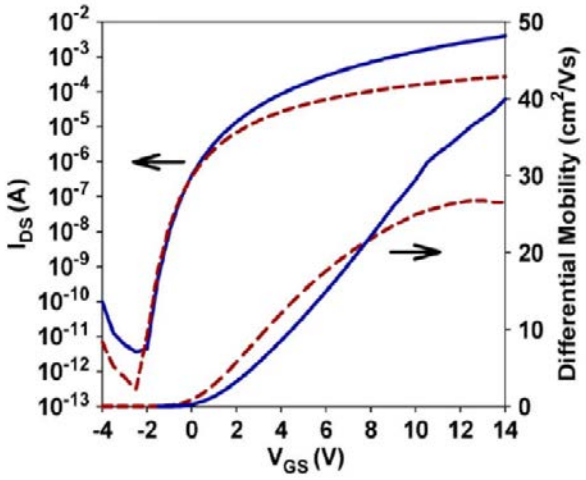

Figure 2.1: Transfer characteristics of PEALD ZnO TFT [32].

frustrating crystallization and it also helps in regulating/controlling the amount of defect states for desired electronic properties. Material simplicity of binary systems is the main advantage whereas difficulty in achieving an amorphous structure with acceptable electronic properties has been a challenge.

2.1.2 Ternary & Quaternary Oxides

The investigations on transparent conductors at Tokyo Institute of Technology in 1996, led to the work on amorphous double oxides composed of heavy metal cations [16]. The working hypothesis of these materials predicted that the double oxide of cations with $(n-1)d^{10}s^0$ configuration would be potential candidate for transparent conductors. These materials exhibited n-type behavior, where oxygen vacancies (V_O) and/or extra cations behaved as electron donors and the conduction band was formed by the s-orbital of the cations [35]. Due to the spherical symmetry of the s-orbitals, the mobility value in these materials does not reduce significantly when structure changes from crystalline to amorphous.

Table 2-I: Summary of different metal-oxide semiconductor investigated for thin-film transistor application with the deposition method.

AOS	Method	Select Reference
ZnO	Sputtering	[21]
	PLD	[22]
	Solution based	[23]
SnO_2	Sputtering	[20]
In_2O_3	Sputtering	[18]
	Evaporation	[17]
Zn-Sn-O	Sputtering	[49]
	PLD	[36]
	Solution based	[37]
In-Zn-O	Sputtering	[38]
	Solution based	[39]
In-Ga-O	Sputtering	[40]
In-Zn-Sn-O	Sputtering	[41]
Hf-In-Zn-O	Sputtering	[57]
Ga-Sn-Zn-O	Sputtering	[42]
In-Ga-Zn-O	PLD	[51]
	Sputtering	[53], [58], [59]
	Solution based	[43], [92]

Since then, many ternary and quaternary oxides have been explored for thin-film transistor applications [36]–[43]. Indium zinc oxide thin-film transistors have been investigated [44]–[46]. The fabricated TFTs showed high mobility but suppressing the electron concentrations was difficult. The reported devices operated in depletion mode [46]. Other multicomponent oxide semiconductors have also been investigated such as HfInZnO [47], ZnSnO [26], [27], however InGaZnO (IGZO) showed the most promising

results with good mobility and on/off ratio [50]–[53]. Most of the research in amorphous oxide semiconductors have been dedicated to IGZO.

Table 2-I shows some oxide semiconductor materials used as the TFT active channel material and the deposition technique used for fabrication.

2.2 CHARACTERISTICS OF IGZO

For better uniformity across the large glass substrate, it is advantageous to use an amorphous material since the electrical properties do not suffer due to the presence of different number of grains in each TFT channel. IGZO can have a uniform amorphous state owing to the multiple metal oxides having different lattice structures which frustrates the crystallization [54]. IGZO offers several advantages in terms of low processing temperature, high mobility, choice of gate dielectric, low off-current state, excellent uniformity and ease of fabrication.

The research in IGZO started by the demonstration of single-crystalline $InGaO_3(ZnO)_5$ TFT [55]. The film had a layered superlattice structure with alternate InO_2^- and $GaO(ZnO)_5^+$ layers stacked along <0001> axis. A 2 nm ZnO epitaxial layer was grown using pulsed laser evaporation on single crystal yttria-stabilized zirconia (YSZ) substrate. This was then used as a template to deposit 120 nm $InGa_2(ZnO)_5$ layer at room temperature. An annealing was performed at 1400 °C for 30 min which resulted in the growth of single crystal. TFTs were fabricated in top-gate configuration with HfO_2 as gate dielectric and ITO as source, drain and gate electrodes. The device characteristics are shown in Figure 2.2. The field effect mobility of ~ 80 $cm^2/V{\cdot}s$ and on-off current ratio of 10^6 was reported.

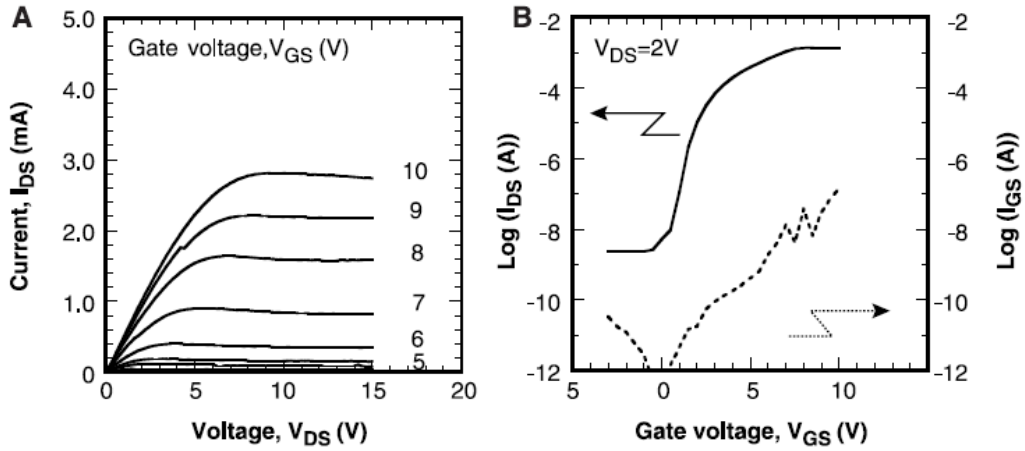

Figure 2.2: First demonstration of single crystal IGZO TFT [55].

Though the process is not suitable for practical purposes it fueled research in the area of IGZO semiconductor.

Over the last decade, a significant amount of research has been carried out in exploring amorphous oxide semiconductors (AOS) as a potential replacement of a-Si:H for the active material in TFTs [33], [34], [58], [59]. In 2004, Nomura *et al* presented results on amorphous IGZO (a-IGZO) TFT on a flexible substrate which launched research in the field of a-IGZO [51]. The transfer characteristics of a-IGZO TFT are shown in Figure 2.3. This demonstration was more practical and did not require high temperature anneal or crystalline semiconductor. IGZO has gained wide popularity and is considered to be the most appropriate candidate for next generation display products [60]–[63]. The rest of this section discusses the properties of IGZO and influence of process effects on its electronic properties.

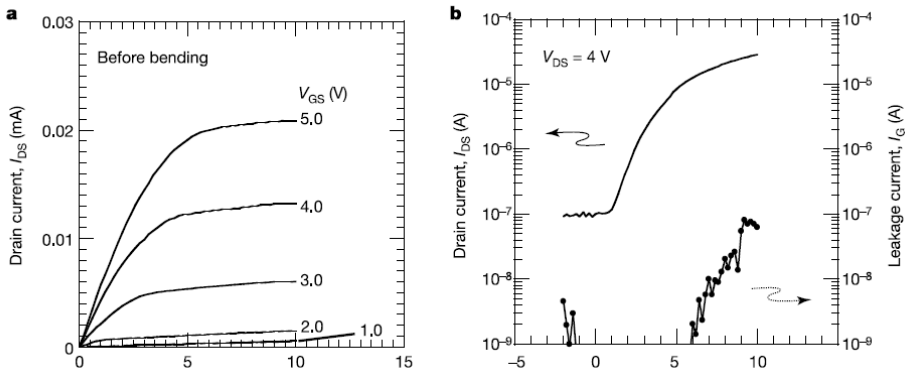

Figure 2.3: First demostration of amorphous IGZO TFT [51].

2.2.1 IGZO Composition

In-Ga-Zn-O is composite of In_2O_3, Ga_2O_3 and ZnO. In_2O_3 shows the highest mobility out of all three compounds but it also has high carrier concentration due to the inherent inclination towards forming V_O. Chang *et al* reported that the V_O formation energy increased with increasing neighboring Ga atoms and helped in suppressing V_O and carrier concentration [64]. The mobility of IGZO increases with increasing the concentration of indium and decreases with gallium. However increasing indium content and decreasing gallium concentration also cause the problem of stability due to presence of oxygen vacancies [65]. Ga_2O_3 is more stable due to stronger bond between Ga and O, therefore the addition of Ga suppresses the formation of V_O and reduces electron concentration to ~10^{16} cm^{-3} [64]–[66]. Adding ZnO with Zn^{2+} compared to In^{3+} and Ga^{3+} frustrates crystallization and ensures an amorphous film. Several compositions of In-Ga-Zn-O have been investigated over the years. The 1:1:1:4 ratio ($InGaZnO_4$) is most widely used because of the improved stability, excellent electronic properties and reproducibility over other compositions [65].

2.2.2 Native Defects

Like other AOS, IGZO is intrinsically an n-type semiconductor where the conductivity is attributed to oxygen vacancies (V_O) [5], [28], [40]–[43]. V_O can act as electron donors as [69], [70]:

$$V_O = V_O^{2+} + 2e^- \quad (2.1)$$

Most of the theoretical studies have been conducted on ZnO and have been extended to IGZO. Some theoretical results do not agree with V_O^{2+} mechanism and suggest that Zn interstitials might be responsible for the n-type behavior [71]. Van de Walle *et al*, based on the first principle calculations, described that the V_O are not shallow donors in ZnO and therefore cannot explain the intrinsic n-type behavior [72]. On contrary, Albe *et al* suggested that V_O are shallow donors in In_2O_3 and SnO_2 but the behavior is more complex in ZnO [68]. Du *et al* studied the oxygen self-diffusion by using oxygen isotope ZnO heterostructures and confirmed that V_O in ZnO are 2+ charged instead of neutral and are responsible for n-type conductivity [73]. The theoretical studies often contradict each other in terms of V_O formation energy and location of V_O in band gap are therefore not found conclusive. Hydrogen has also been considered as the electron donor in oxide semicondutors. In 1956, Lander *et al* proposed hydrogen acts as a donor based on annealing of single crystal ZnO in hydrogen ambient which resulted in the increase in ZnO conductivity [74]. Since then there have been various reports on hydrogen acting as a shallow donor in ZnO based on theoretical and experimental studies [51], [52]. First principle calculations in IGZO suggest that hydrogen forms –OH bond and liberates one electron [77] which was verified by experimental data as well [78]. SiN_x with high

hydrogen content has been used for self-aligned S/D doping with hydrogen which increases the IGZO conductivity in S/D region [79].

Experimentally, the carrier density of many AOS materials have been measured as a function of oxygen partial pressure during the material deposition such as IGZO [80], ZnO [81], In_2O_3 [82], IZO [83]. The electron density was found to decrease with increase in oxygen partial pressure confirming that the V_O were the primary source of free electrons.

2.2.3 Electron Transport in IGZO

The outermost electronic configuration of the metal cation in IGZO is $(n-1)d^{10}ns^0$ [51], [65]. The outermost s-orbitals have large radii as well as spherical symmetry which render significant overlap with adjacent orbitals possible irrespective of any disorder. The amorphous state exhibits high mobility owing to the efficient transport path [54]. This type of overlap is absent in conventional semiconductors *viz*. silicon, which has highly directional sp^3 covalent bonding (Figure 2.4) [51]. In addition to spherically symmetric orbitals, other structural requirements should be met for efficient charge transport such as short metal- metal distance and metal-oxygen-metal bonds [84]. Orita *et al* conducted a semi-empirical study for different metal oxides and concluded that Ge and As may not be able to offer efficient conduction paths to electrons in amorphous state [84].

In general, amorphous semiconductors exhibit opposite Seebeck coefficient sign compared to Hall coefficient. Amorphous silicon is an extreme case where the sign changes from negative to positive when the doping changes from p-type to n-type [85]. The anomaly in Hall coefficient sign is attributed to the short carrier mean free length which invalidates the Maxwell Boltzmann transport assumption [86]. In contrast, the

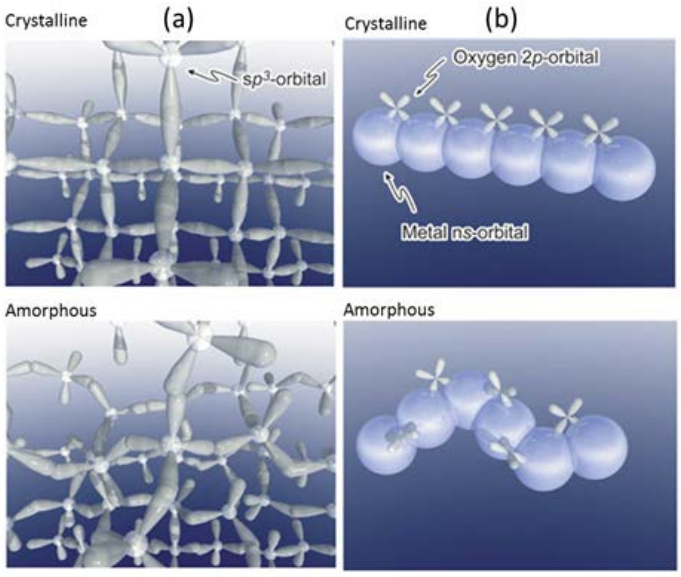

Figure 2.4: Schematic orbital drawing of electron conduction path (a) covalently bonded semiconductor like Si, (b) ionic oxide semiconductor like IGZO [51].

Seebeck coefficient of AOS materials matches with the sign of Hall coefficient [87]. The normal sign of Hall coefficient in AOS suggests that the electron mean free path is longer compared to a-Si:H. This indicates that the conduction is not through the quantum mechanical hopping *via* band tail states or variable range hopping (VRH), as in the case of a-Si:H.

The electron transport in amorphous semiconductors is limited by the presence of tail-states. The number of defect states in IGZO is much lower than a-Si:H. Due to the spherical symmetry of s-orbital conduction band in IGZO, there is always some overlap between adjacent atoms which provides the path for conduction. The current conduction at room temperature follows the thermal conduction where electrons have enough energy to go the conduction band and follow the normal Arrhenius behavior [88].

2.3 IGZO THIN-FILM PROCESSES

In this section, a brief literature review on the details of IGZO deposition methods, annealing and passivation, along with associated interaction effects is presented.

2.3.1 IGZO Deposition

IGZO can be easily deposited on large-area glass substrates which makes it economical and easily transferrable to the current flat-panel display production facilities. IGZO has been deposited using PLD [51], sputtering [80], sol-gel [67], [68] and solution-based technique [91]. Though solution based techniques are advantageous for cost effectiveness, the performance of devices is not as good compared to sputtering [92], [93]. Therefore, most of the efforts are dedicated to developing sputtered IGZO TFTs.

As discussed in previous section, V_O act as dopants in IGZO. The amount of doping can be therefore controlled by changing the amount of oxygen during the deposition process. A higher oxygen partial pressure during deposition decreases the number of V_O and therefore the electron concentration and causes a positive threshold voltage shift in TFT transfer characteristics [80], [94], [95]. Similarly increasing the sputtering power decreases the threshold voltage as the metal ions in the films are higher [95], [96]. The variations in the performance of IGZO devices deposited using different sputter parameters can be compensated by post fabrication anneal [95].

2.3.2 IGZO Annealing

For high performance IGZO TFTs, annealing has been accepted as an indispensable tool to reduce the subgap states that are abundantly present in the as-deposited films [97]–[100].

Depending on the condition of as-deposited IGZO films, different anneal conditions are reported in literature. For instance, Jang *et al* annealed fabricated devices in the vacuum [101] while Fuh *et al* reported that annealing in vacuum leads to high conductivity of the IGZO films [97]. The anneal conditions depend on the electronic state of as-deposited films and therefore a wide spectrum of anneal conditions is published in the literature.

Annealing has been established to reduce the band tail states [77] and regulate the V_O concentration [102]. Annealing results in more ordered network which has lower level of native defects. During bias stress testing, it is observed that the devices which were annealed longer (200 h compared to 2 h), exhibit improved stability owing to the ordered network which is less prone to the defect generation [98]. Annealing at 10 atm pressure of O_2 ambient is reported to improve the bias induced instability under illumination by suppressing the formation of V_O defects [99]. Steam ambient annealing has also been explored and showed improvement in the TFT characteristics due to the stronger oxidation power of water related species and stabilization of chemical bonds [103]. The anneal temperature was decreased by annealing in ozone ambient instead of oxygen ambient [100]. Microwave annealing for 300 s was reported to be equivalent to 1 h anneal at 300 °C in reducing trap states [104].

Despite the wide spectrum of anneal conditions reported in literature, the influence of annealing in regulating the defect states and hence the electronic properties of IGZO has been accepted. The favorable conditions for annealing depend on the as-deposited film properties as well as TFT fabrication process, therefore proper consideration should be given in investigating the effect of anneal steps such as ambient, temperature and time when establishing the anneal conditions.

2.3.3 Back-Channel Passivation

Oxide semiconductor surface is very sensitive to the ambient and therefore has been used for gas sensing applications. A review of oxide semiconductor application in gas sensing is provided in references [105] and [106]. IGZO has also been investigated for gas sensing applications [70]. The exposed IGZO has been reported to interact with ambient oxygen which behaves as acceptor ions and creates a depletion region and supports enhancement-mode operation (Figure 2.5a) [56], [70], [107]:

$$O_{2(g)} + e^- \rightarrow O^-_{2(s)} \qquad (2.2)$$

The equilibrium constant, *K*, of above reaction is given by [107]:

$$K = \frac{[O_2^-]_s}{P_{O_2}[n]} \qquad (2.3)$$

where $[O_2^-]_s$, P_{O_2} and $[n]$ are the concentration of adsorbed oxygen, partial pressure of oxygen and electron density, respectively. Equation (2.3) suggests that the increase in electron concentration and/or increase in oxygen partial pressure would result in an increase in adsorbed oxygen. These effects have been observed experimentally [56], [107].

In case of TFT application, the ambient interaction of IGZO channel leads to instability in device performance, which is undesirable [88], [89]. IGZO surface also interacts with H_2O forming an accumulation region right below the surface through the following reaction resulting in depletion-mode behavior (Figure 2.5b) [97], [108] :

$$H_2O_{(g)} \rightarrow H_2O^+_{(s)} + e^- \qquad (2.4)$$

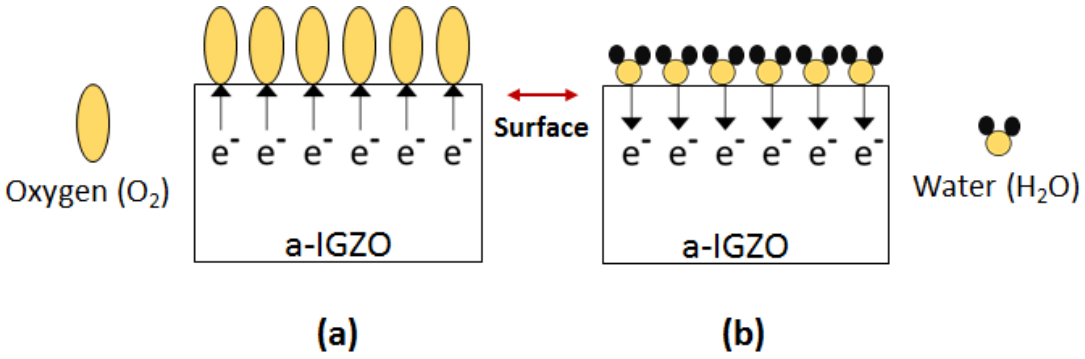

Figure 2.5: Schematic showing the role of (a) adsorbed oxygen as electron acceptor, (b) adsorbed water as electron donor.

Application of a passivation material reduces the interaction of back-channel with the ambient and results in improved stability of TFT over time and/or under bias-stress [62], [109]–[113]. However, the deposition of passivation material on IGZO results in modifications in surface/bulk properties and a proper understanding of the influence of passivation material application is critical.

2.4 BIAS INDUCED INSTABILITY

After realizing the high mobility TFTs another important concern is to investigate the instability of transistors under the bias stress because the display devices are turned on/off for long duration. A lot of work has been done in understanding the instability mechanism in IGZO TFTs and investigating ways to suppress it. Positive bias stress (PBS) and negative bias stress (NBS) at the gate terminal with source and drain grounded are commonly used for this study. During NBS, if the transistor is exposed to visible light (imitating the light source in LCD display), the stress test is referred as negative bias under illumination stress (NBIS).

2.4.1 Positive Bias Stress (PBS)

An increase in device threshold voltage is reported under positive gate bias stress (PBS) for unpassivated IGZO TFTs [107]. The IGZO back-channel is sensitive to the presence of oxygen and water vapors (Figure 2.6). The adsorbed oxygen at the IGZO back-channel behaves as an acceptor type defects and captures an electron creating depletion region near the interface. During PBS, the channel is in accumulation and has a high electron concentration. From Equation (2.3), an increase in [n] results in increase in the amount of adsorbed oxygen (O_2^-). This causes the formation of a depletion layer at IGZO back-channel which resulted in a positive shift in transfer characteristics. An improvement in bias induced instability was found for passivated devices [109], [111], [113]. The presence of passivation material at the back-side suppresses the interaction of IGZO channel with the ambient and therefore offers more stability against bias stress. Hosono *et al* attributed the stability after passivation to the reduction in tail-states for passivated devices [52].

The positive shift in device characteristics under PBS has also been attributed to the electron trapping near the IGZO/gate dielectric interface or in the gate dielectric [69], [114]. The trapped electrons repel the electrons in the channel region making it harder for the gate to create an accumulation region. This manifests itself as an increase in the threshold voltage. This mechanism explains the parallel shift under bias stress.

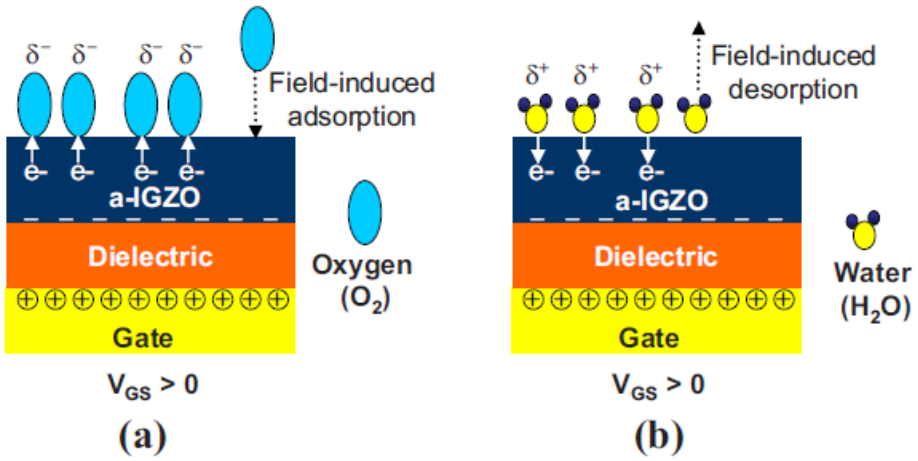

Figure 2.6: Cartoon representation of field induced (a) adsorption of oxygen molecules under PBS, (b) desorption of water molecules under PBS [107].

2.4.2 Negative Bias Stress (NBS)

NBS results in a negative characteristics shift due to induction of positive charge centers at the associated dielectric/IGZO interfaces. Most of the recent results claim TFTs to be stable under NBS [115]–[117]. The reason for this improvement is most likely due to improved back-channel passivation. There are still reports published in 2017 on negative shift under NBS [118]. However most of the recent publications are focused on NBIS; device characteristics are reported to shift left (lower V_T) under the illumination where the shift is dependent of wavelength of the light source. Higher shift is observed under lower wavelength (higher energy) [115], [116]. The mechanism proposed for NBIS is the ionization of oxygen vacancies [99], [119], [120]. Another explanation involves the capturing of photogenerated holes at IGZO/gate dielectric interface [121], [122]. There are essentially no free holes in IGZO but it is generally claimed that high energy photons provide sufficient energy to create electron-hole pairs. These “hot” holes then move

towards the gate dielectric interface under NBS and get trapped which then causes a decrease in threshold voltage.

Bias stress instability under illumination remains a challenge, however for display products light shield are used which avoids illumination of the channel to the back light [6], [8]. Internal or external compensation schemes can be used to suppress the effect of bias induced instability [7], [123], [124].

2.5 CONCLUSION

This chapter reviews the progress made in metal oxide semiconductor technology over the past decade. Due to the polycrystalline nature of binary films, multi-component oxide semiconductor films have been investigated for application in TFT technology. Mixing different metal oxide frustrates the crystallization and the resulting films are amorphous in nature. IGZO, owing to its superior on-state and off-state performance over other multicomponent semiconductor candidates, has been extensively studied and is the focus of the current study.

IGZO behaves as an n-type semiconductor owing to the presence of defects states. Oxygen vacancies, metal interstitials, and hydrogen have been reported to be responsible for the conductivity. Results from first principle calculations have not been conclusive about the role of oxygen vacancies and its energy states. However, experimental studies support that oxygen vacancies behave as donor; IGZO conductivity changes with the oxygen partial pressure during deposition and/or anneal. Different compositions of IGZO have been studied however, $InGaZnO_4$ is the most widely used due to the high carrier mobility while maintaining low off-state leakage. IGZO deposited using sputtering results

in superior TFT performance over other methods as well as a process which is economical and scalable to large glass panels.

Annealing conditions are critical in determining the IGZO electronic properties. In literature, various anneal ambient/duration has been reported. The optimum anneal conditions depend on the electronic state of as-deposited films and the subsequent processing.

IGZO material is very sensitive to the ambient and interacts with water/oxygen which modifies the electronic properties. This interaction causes instability in IGZO device behavior during room temperature storage as well as during bias-stress tests. The interaction with ambient of the IGZO surface can be minimized by the application of passivation material. However, the deposition process introduces interface defect states which are important to identify.

Chapter 3. ELECTRONIC PROPERTIES AND MATERIALS SCIENCE OF IGZO

The spectrum of IGZO sputter parameters and annealing conditions used by the IGZO community is broad, which suggests that a unique "optimized" combination does not exist. Excellent I-V transfer characteristics achieved by several research groups are all quite similar, suggesting that the same "ideal" semiconducting properties can be achieved by various combinations of sputter deposition parameters and annealing conditions. However, considering the challenges with process development, it is also expected that not every sputter deposition recipe would be able to ultimately result in an IGZO film with appropriate semiconducting properties and yield good TFT characteristics.

The electronic properties of IGZO films invariably change by deposition process conditions in conjunction with the subsequent processes. The properties of sputtered films depend on several process-related factors such as chamber pressure [34], [96], [125], [126], sputter power [34], [131] and ambient conditions [58], [128]–[130], as well as tool-related factors such as distance between substrate and target [96], base pressure [125], and other machine variables. It is extremely challenging to reproduce the work of others due to differences in configuration of process tools. The anneal conditions have a critical impact on the properties of the IGZO film, therefore it is important to perform material analysis which quantifies differences between process treatments.

This study involves an electrical interpretation of IGZO defects, along with materials characterization using X-ray reflection and spectroscopic analysis. The as-

deposited films were analyzed for crystallinity, resistivity, thickness and composition. Annealing has been widely accepted as an indispensable tool for producing higher quality TFTs [103], [131], [132], thus the effect of thermal processing on IGZO material properties has been thoroughly studied. Bottom-gate thin-film transistors were fabricated for studying the influence of these process variables on transistor behavior. Van der Pauw structures were fabricated adjacent to the TFTs for sheet resistance measurements. These structures were designed to undergo the same processing as the TFT and therefore represent the "true" channel behavior. Secondary Ion Mass Spectroscopy (SIMS) and X-Ray Photoelectron Spectroscopy (XPS) were employed to measure any post-anneal compositional change in the IGZO films.

The details of TFT fabrication and experiments for optimization of the anneal recipe are discussed in Chapter 4 along with the investigations on IGZO TFTs passivation.

3.1 IGZO SPUTTER DEPOSITION

The IGZO material investigated in this study was deposited in an Applied Materials Centura production RF sputter system in a single wafer, load-locked chamber using a 12.8 inch $InGaZnO_4$ target and Ar-O_2 ambient with a substrate chuck temperature of 200 °C. The flow of Ar was set to 30 sccm and the flow of O_2 was set to 4 sccm which established a pressure of ~2.3 mT. The sputtering power was ramped to 600 W with a 50 W/s rate to avoid any initial shock to the target; subsequently the power was increased to 750 W for film deposition. The wafers were prebaked at 200 °C in a separate chamber before deposition for desorption of any water molecules on the surface. The short sputter time supported high film quality; a typical 50 nm film took ~72 s for deposition. Several

material analysis techniques were performed to characterize the properties of as-deposited film.

3.2 CHARACTERIZATION OF AS-DEPOSITED FILMS

The as-deposited films were analyzed for composition, uniformity, crystallinity and resistivity using characterization techniques as discussed in this section.

3.2.1 X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a non-destructive technique to analyze the atomic structure of the specimen. An X-ray beam is shined on the material under investigation and the scattered X-rays are measured as a function of exit direction. If the X-ray wavelength is on the order of the atomic distance, it results in a constructive and destructive diffraction pattern, giving peaks of higher and lower intensities respectively. The constructive diffraction occurs when the Bragg's condition is satisfied, which can be mathematically expressed as:

$$2d \cdot \sin(\theta) = n\lambda \qquad (3.1)$$

where d is the interplanar spacing, θ is the angle of incidence, n is the order of reflection and λ is the wavelength of incident X-rays. The absence of any peak in an XRD suggests that the specimen has no long-range order or is amorphous in nature.

IGZO films can be deposited in crystalline [19], [20] and amorphous [5], [21], [22] form. Due to different crystalline structures of ZnO, In_2O_3 and Ga_3O_3 lattices, the films deposited under normal conditions are amorphous in nature [15]. Nevertheless, it is crucial

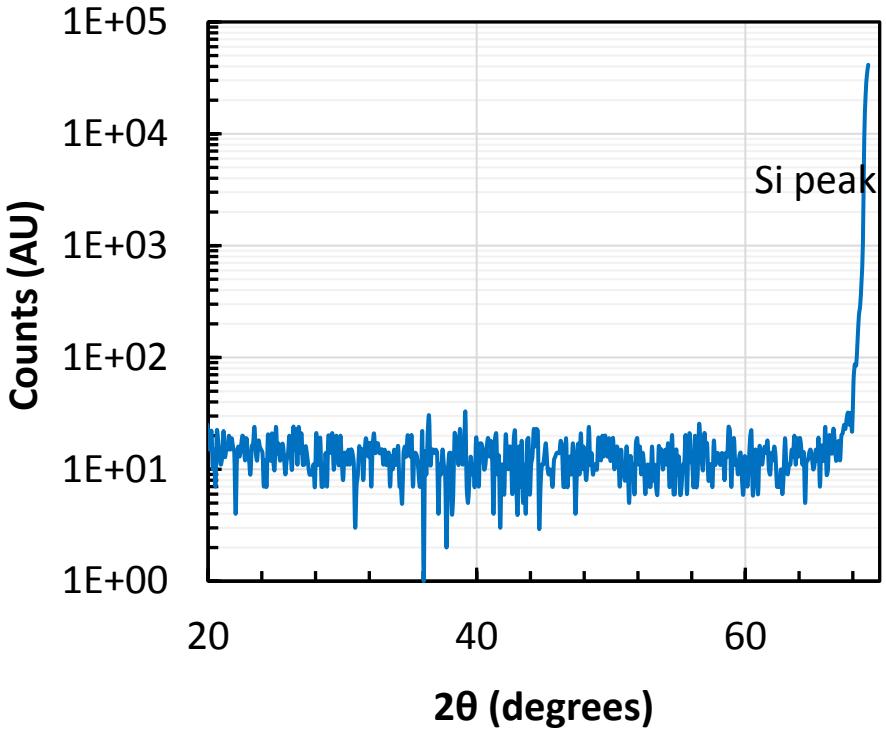

Figure 3.1: XRD spectrum of as-deposited IGZO films on a silicon wafer. The absence of any peak confirms the amorphous nature of the deposited films. The peak at ~70° is from the Si wafer used as substrate.

to analyze the deposited IGZO film for crystallinity. X-ray analysis was performed using a home-made sealed tube X-ray source with a Huber four full circle diffractometer with copper source/target. A Si (111) monochromator was used for higher resolution. The Cu $K\alpha_1$ radiation was maximized to make it as monochromatic as possible.

The XRD measurements of the as-deposited film is shown in Figure 3.2. The diffraction pattern does not show any peaks related to component metal-oxide or single crystal IGZO confirming the amorphous nature of the as-deposited films

3.2.2 X-ray Reflectivity (XRR)

X-ray Reflectivity (XRR) measurements utilize the fact that the reflectivity of a material increases when the incident angle is very small. This technique can be used to study multilayer films and analyze the surface smoothness, thickness and density. The X-rays reflected from each surface/interface result in constructive and destructive diffraction and show fringes in the output diffraction pattern which can be used to calculate these parameters. The film thickness can be calculated using:

$$2d\sqrt{\sin^2\theta_{in} - \sin^2\theta_c} = m\lambda \qquad (3.2)$$

where d is the thickness of the film, θ_{in} is the angle at which intensity is maximum, θ_c is the critical angle for total external reflection, m is the fringe order (an integer) and λ is the incident wavelength. Equation (3.2) can be simplified by neglecting the refraction to:

$$d = \frac{\lambda}{2 \cdot sin\Delta\theta} \qquad (3.3)$$

where $\Delta\theta$ is the difference in the angle at which two maxima occurs.

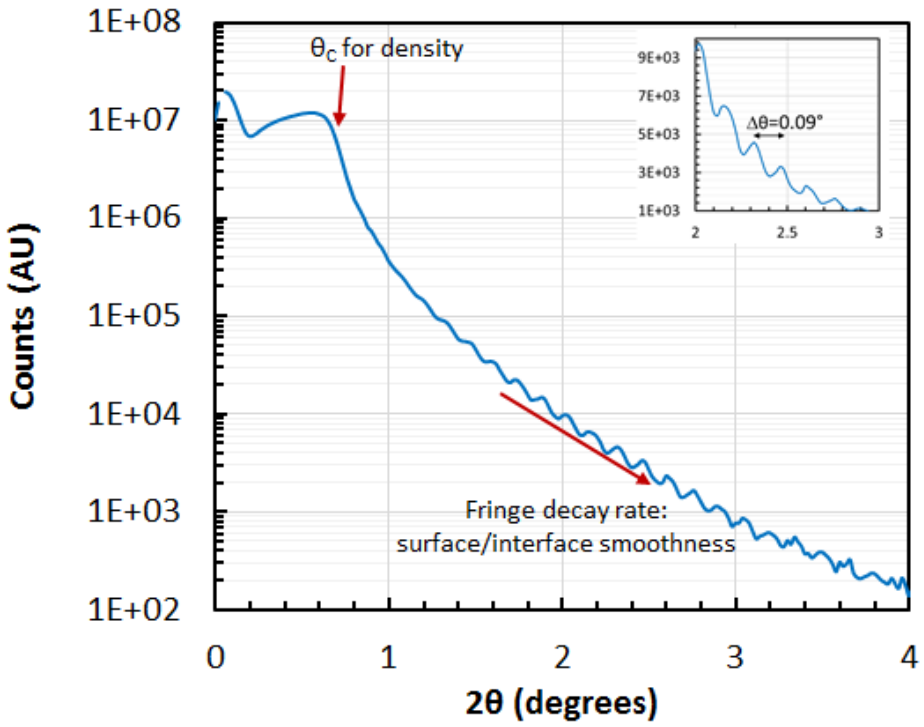

Figure 3.2: XRR spectrum of as-deposited IGZO on a silicon wafer. The thickness calculated from fringes was 49.3 nm which is very close to the target thickness of 50 nm.

In this work, XRR analysis was used to measure the thickness of the deposited films and compare the surface roughness after thermal treatment. The quantitative analysis of film density and surface roughness was not conducted. The XRR spectra of as-deposited film is shown in Figure 3.3. The $\Delta\theta$ measured between two adjacent peaks is 0.09°. The thickness calculated using Equation (3.3) is 49.3 nm which is very close to the targeted thickness of 50 nm.

3.2.3 X-ray Photoelectron Spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) can be used for analyzing the chemical composition of the sample. The core photoelectron intensities can be used for quantitative

analysis and the shift in the peaks binding energy can be correlated with change in chemical environment [135].

During photoelectron spectroscopy, the sample is subjected to a monochromatic radiation and the resulting photoelectrons are observed. The kinetic energy of the photoelectron is given by:

$$hv = E_b(k) + E_{kin} \qquad (3.4)$$

where $E_b(k)$ is the binding energy of the k-th level and E_{kin} is the kinetic energy of the electron. Using an electron energy analyzer, a spectrum of number of detected electrons per energy window versus the kinetic energy can be obtained. This energy window is called the pass energy. The binding energy can be deduced from the kinetic energy of the detected electrons. Each element has a unique spectrum; by comparing the peak intensities, a quantitative analysis on the composition of the specimen can be performed. The accuracy of this analysis depends on the atomic sensitivity. The shift in peak positions can be used to identify the chemical state. Since the mean free path of electrons is very small, the ejected electrons corresponds to only the top few atomic layers and therefore the top 2-5 nm thickness of sample is analyzed. For depth analysis, the sample surface can be etched using an Ar-ion gun.

A model representation of XPS emission process is shown in Figure 3.4. An incoming photon knocks off the electron from the core level which is detected using electron analyzer. The kinetic energy and intensity of these photoelectrons give the XPS spectra. During relaxation, an electron from an outer orbital may fall to the inner orbital vacancy along with the ejection of an Auger electron carrying the excessive energy.

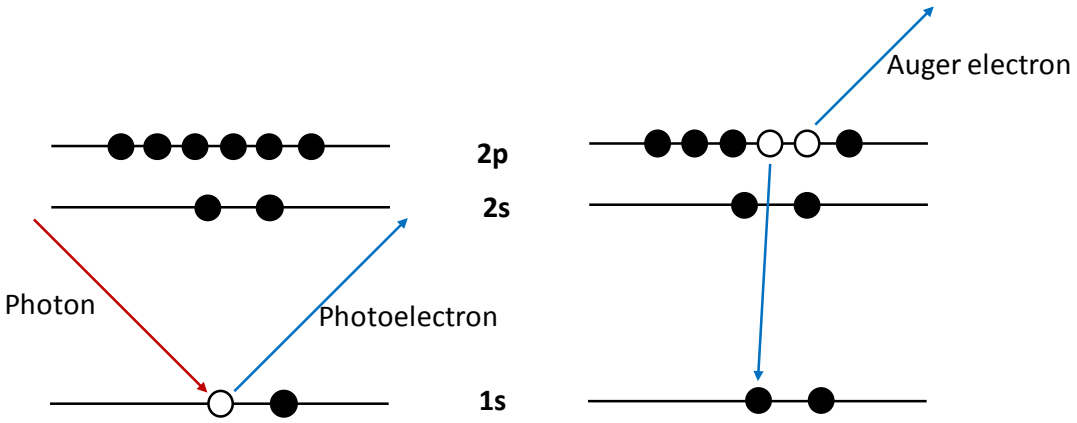

Figure 3.3: Model representation of XPS emission. The incident photon ejects an electron from the core level (photoelectron). During relaxation, an electron from the higher orbital fills the electron vacancy and the excess energy is carried by Auger electron.

Surface analysis was performed on a Physical Electronics multiprobe system with XPS and Auger Electron Spectroscopy (AES) capabilities. The system has a double pass cylindrical analyzer. Mg Kα (1253.6 eV) was used as X-ray source. The argon ion beam at ~ 4.5 kW was used to raster scan an area of ~ 5 mm × 5 mm to etch the sample for depth profiling. The base pressure of 1×10^{-10} T was achieved and etching was done at 5×10^{-8} T. The X-ray source does not use a monochromator. This provides lower resolution but offers higher beam intensity. The system has electronics upgraded from RBD Instruments along with software upgrade for data acquisition and analysis.

The XPS of a 50 nm as-deposited IGZO film is shown in Figure 3.5. The pass energy of 100 eV was used for this measurement. The data show clean spectra with clear peaks for indium, gallium, zinc and oxygen with a small quantity of carbon on the surface along with other Auger peaks.

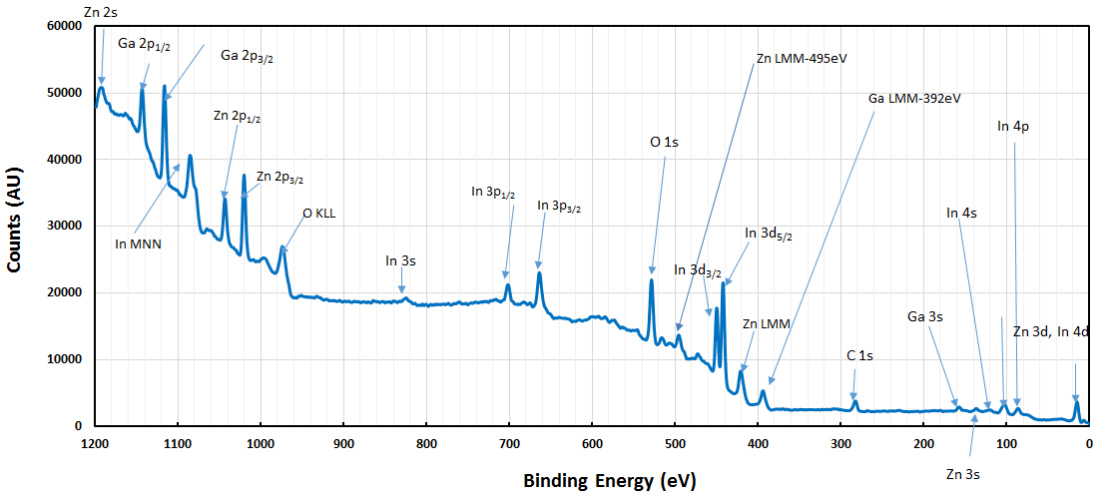

Figure 3.4: XPS measurements of as-deposited IGZO films. The spectrum is clean with each peak clearly identified with no trace of any impurity except the surface carbon.

3.2.4 Auger Electron Spectroscopy (AES)

For Auger Electron Spectroscopy (AES), electrons are used for the excitation. Unlike XPS, the Auger spectrum does not depend on the input energy. The peaks in AES spectra are not as intuitive as the XPS peaks; however a plot of differential intensity is easier to interpret. For this study, the output power of electron beam was set at 3 kW with a beam energy of 4 eV peak to peak modulation.

The atomic percentage of film is calculated using the default sensitivity factors given by the RBD Instruments data acquisition software. The atomic ratio calculated using the default sensitivity factor is not accurate but is valid for comparative study. The AES spectrum of as-deposited IGZO sample is shown in Figure 3.6. The atomic percentage calculated from the area under the peak is given in Table 3-I.

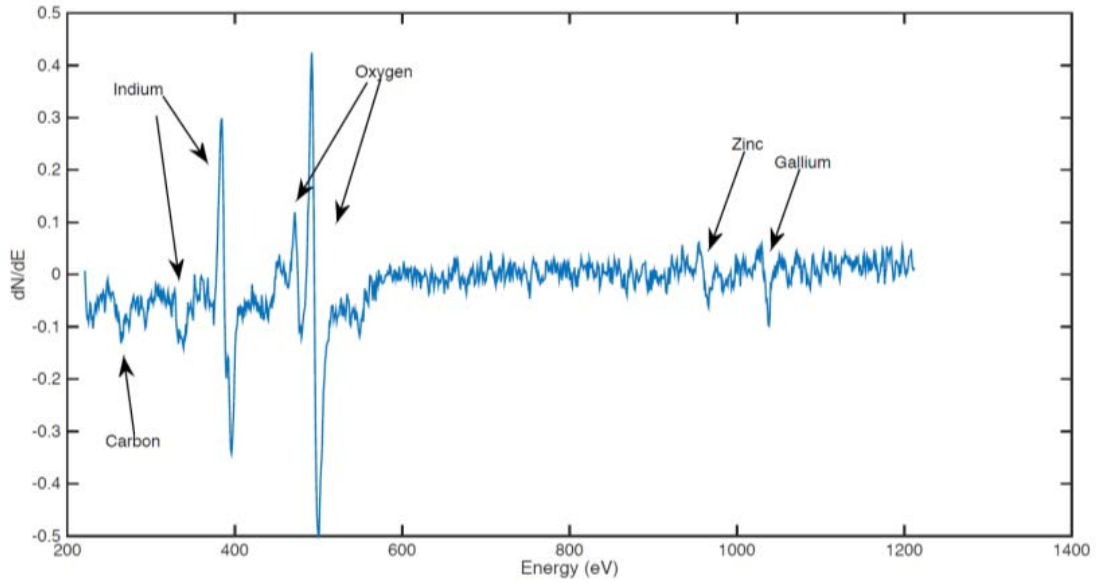

Figure 3.5: Auger spectrum of as-deposited IGZO films showing peaks for In, Ga, Zn and O with little surface C peak.

Auger spectroscopy was used to analyze the compositional uniformity along the thickness of the sample. The AES offered an advantage over XPS depth profiling. The IGZO samples fluoresce under Ar^+ ion and electron beam bombardment making it easy to align both at the same spot. This was not the case during XPS analysis as X-rays hitting the IGZO sample did not give any visibly detectable signals and it was hard to determine if the sample etching and XPS analysis were done at the same spot. The depth profile of as-deposited films is shown in Figure 3.7 . The elemental distribution is uniform along the entire thickness of the film.

Table 3-I: Atomic percentage of In, Ga, Zn and O estimated from the area under the Auger peaks using default sensitivity factors. Note that the atomic percentage is not accurate and is only good for comparative studies.

Element	Atomic ratio
In	19
Ga	19
Zn	14
O	48

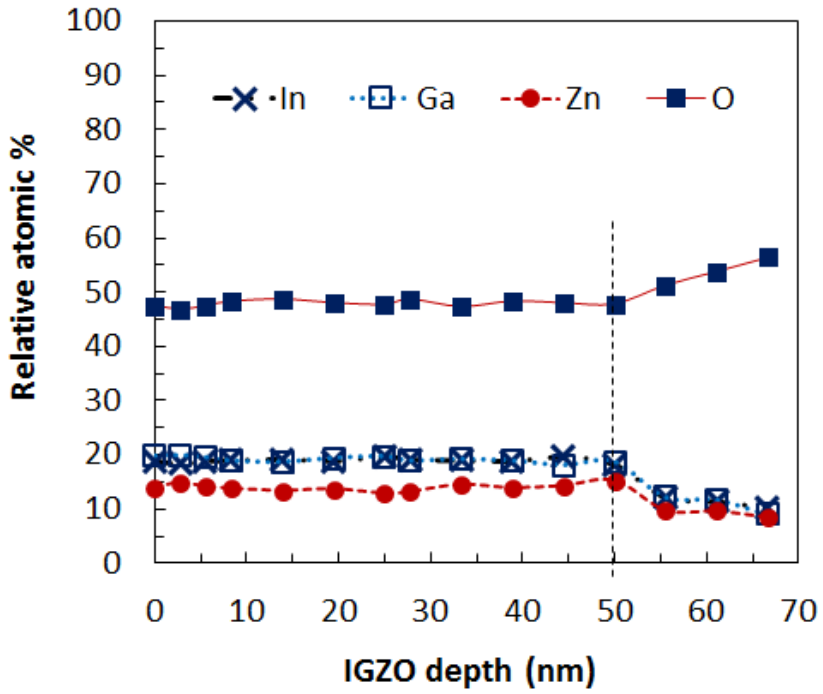

Figure 3.6: Depth profile of as-deposited IGZO films using AES. The area under the peak is used to calculate the atomic percentage. The default sensitivity factors are used for atomic percentage calculation which may not reflect actual stoichiometry of the specimen but is good for comparative study. Note that atomic percentage after 50 nm is misleading because of the signal from Si substrate.

3.2.5 Resistivity Measurement

The 4-point probe measurement and Hall effect measurement techniques did not yield a measurable response, suggesting a very high resistivity as-deposited film. An electrometer with the ability to measure extremely small current levels was used to measure the resistivity of a 50 nm IGZO film deposited on a glass substrate. The current versus time graph is shown in Figure 3.8. The current decreased in a non-linear fashion and then saturated at 0.6 pA after 100 min of measurement. The change in resistivity over time is attributed to the adsorption of oxygen at the exposed IGZO surface which created a depletion region, as discussed in Section 2.3.3 [8], [24], [25]. The resistivity of as-deposited film was ~100 kΩ·cm which is consistent with a semiconductor material for TFT applications. However, as will be shown, the electrical properties of IGZO TFTs are highly dependent on process conditions.

3.3 OXIDIZING AMBIENT ANNEALING

Early in this study it was established that a thermal anneal was needed to result in acceptable thin-film transistor operation. As shown in Figure 3.9, with 50 nm thick as-deposited IGZO material, the transfer characteristics are very poor in the absence of a thermal anneal. The devices exhibit no gate controlled charge modulation and could not be turned off even at a gate voltage (V_{GS}) of -10 V. The density of subgap states in unannealed IGZO films is high due to defects created during sputtering or fabrication process. The thermal anneal process has been almost universally accepted as beneficial for suppressing the density of subgap states in IGZO and dialing in channel conductivity by controlling the amount of oxygen vacancies (V_O) and thus improving the semiconducting

properties of IGZO films [15], [131]. The anneal ambient regulates the amount of V_O in the film which essentially act as donors and provide charge carriers. However, the details of anneal process differ across the scientific community and vary as much as a 200 h anneal in vacuum [98] to 1 h anneal in ozone ambient [100]. The response of annealing depends primarily on the initial electronic state of the IGZO film.

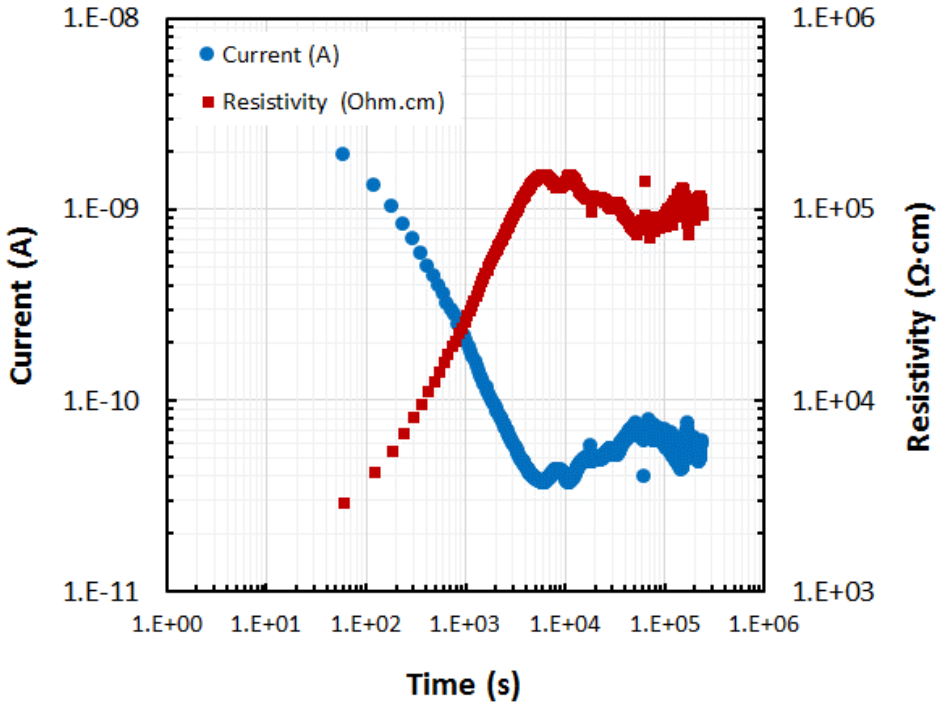

Figure 3.7: Resistivity of as-deposited IGZO film over time. The applied voltage was 0.25 V. The resistivity of films increased for the first ~100 min and then saturated at ~ 100 kΩ·cm.

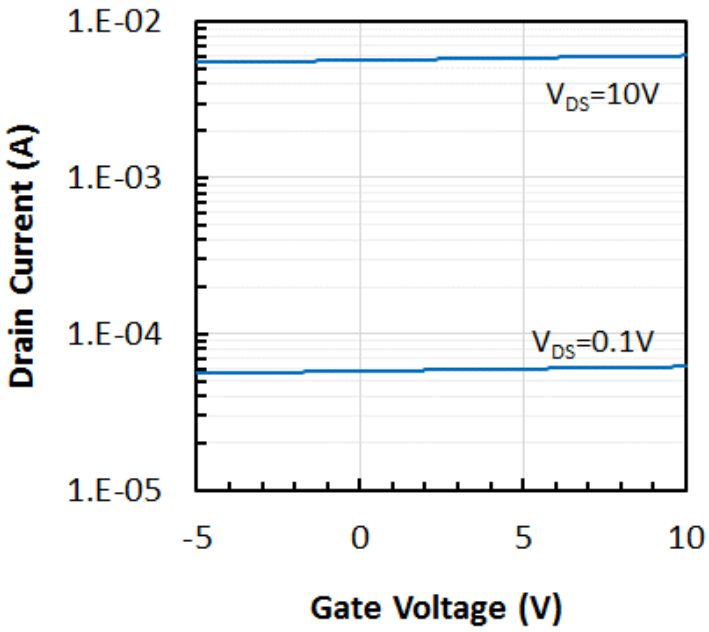

Figure 3.8: Transfer characteristics of IGZO TFT without any thermal anneal. The device showed no gate control and could not be turned off even at high negative V_{GS}. The TFT channel dimensions were L=21 µm & W=100 µm.

In this section, investigations on the change in IGZO material properties after thermal anneal process are discussed. The anneal process under investigation is performed after the fabrication of TFT at 400 °C for 30 min in N_2 ambient with a ramp-down in air ambient. The details on establishing the favorable anneal recipe are discussed in Section 4.3.

3.3.1 XRD & XRR Measurements

The first step in this analysis was to verify the crystallinity of IGZO films after the thermal processing. Figure 3.10 shows XRD results of annealed samples. The absence of the peak corresponding to crystalline IGZO at $2\theta \sim 32°$ confirms the amorphous nature of films after the 400 °C thermal treatment [136].

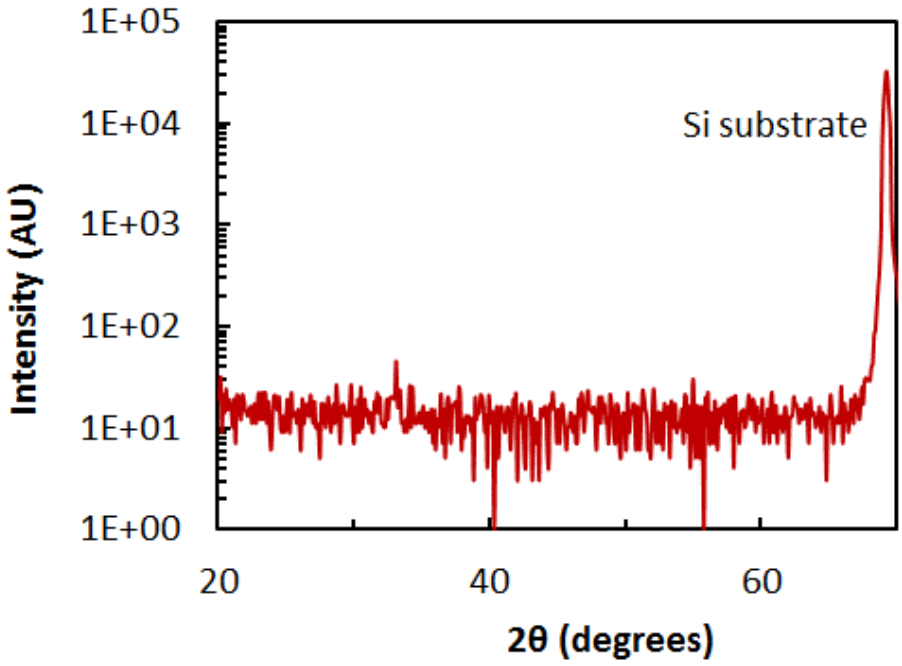

Figure 3.9: XRD spectrum of 400 °C annealed IGZO sample. The film remained amorphous after the thermal process.

3.3.2 SIMS Measurements

Secondary ion mass spectroscopy (SIMS) is a destructive technique to analyze the composition of a material. This technique relies on the removal of material by sputtering and then analyzing the ejected material using a mass analyzer [137].

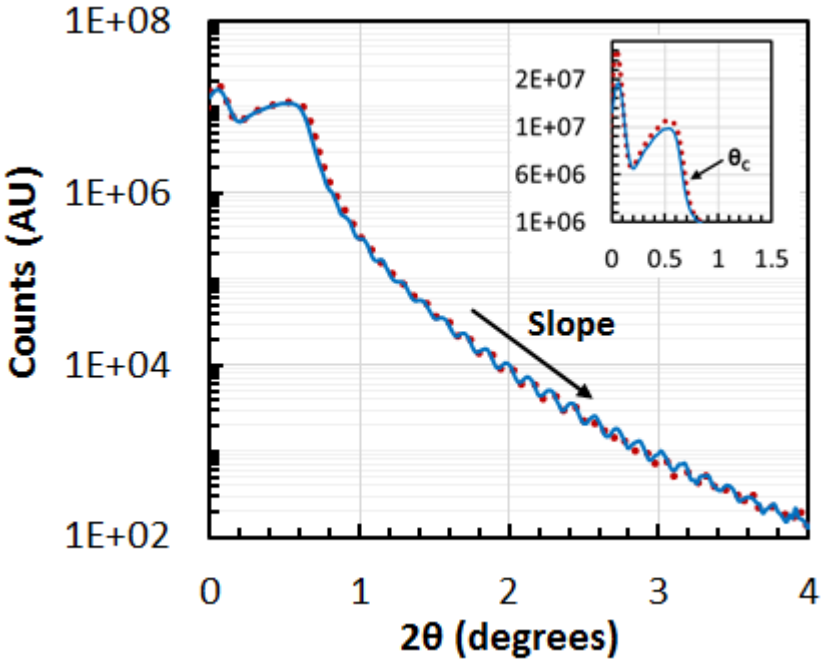

Figure 3.10: XRR spectrum of annealed IGZO sample (solid line) overlaid with the spectra of unannealed sample (dashed line). The fringe gap and the slope of spectra remained unchanged, verifying no appreciable change in film thickness or surface roughness after annealing. The inset shows the magnified spectra near the critical angle, confirming no change in IGZO density after anneal.

The SIMS measurements for unannealed and annealed samples are shown in Figure 3.12. The measurements were taken in Cs attachment mode *i.e.* the secondary species were acquired as CsM^+, where M stands for In, Ga, Zn or O. The composition of the annealed IGZO layer is very close to the composition of the unannealed sample with no apparent elemental redistribution resulting from annealing. The anneal did not change diffusion depth of metal ions and did not affect profile shape across the interface.

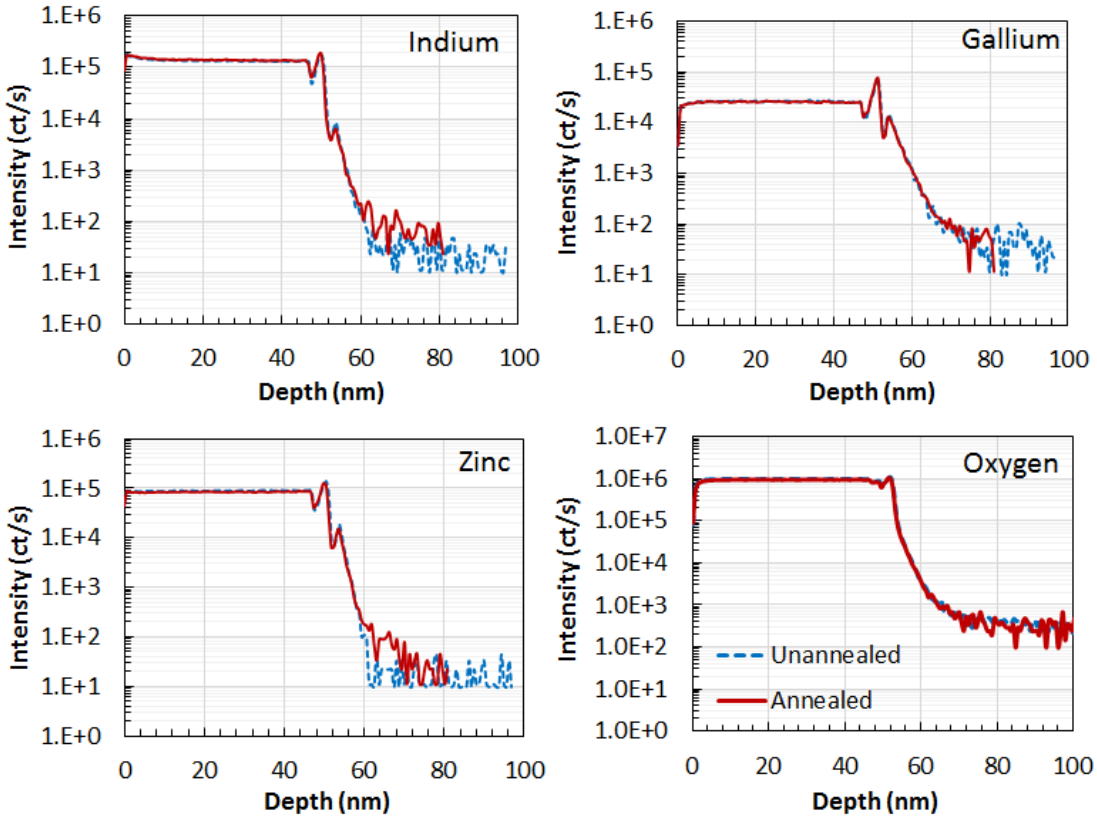

Figure 3.11: SIMS depth profile for In, Ga, Zn and O before and after annealing. The measurements do not show any noticeable difference in intensities across IGZO thickness and profile shape across the interface after annealing.

3.3.3 XPS Analysis

In addition to the knowledge of chemical composition, XPS can provide information regarding the chemical environment of the species in the sample. Though there is no direct measurement technique for measuring the V_O in a film, the O-1s peak analysis can provide a relative measure of oxygen near vacancy defects. The sample was etched for 5 min using Ar-ions before measuring the spectra to remove any surface contamination or weakly bonded O-species such as $–CO_3$, -OH, adsorbed H_2O or chemisorbed O_2. A pass energy of 25 eV was used for the oxygen peak analysis to improve accuracy. The asymmetric

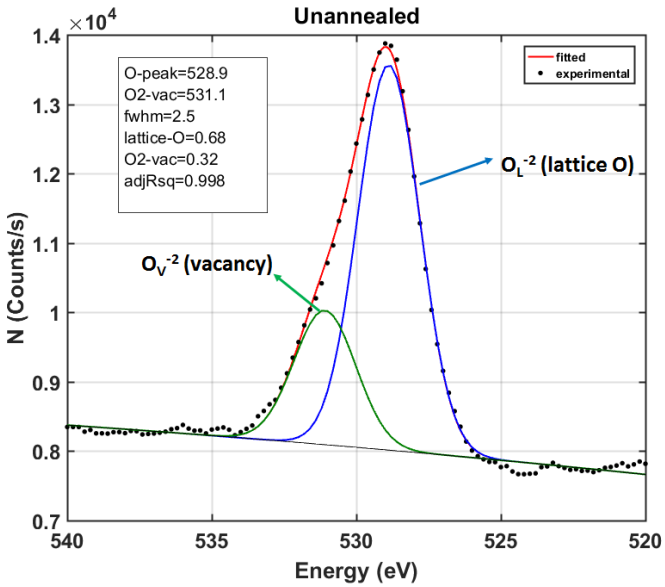

Figure 3.12: XPS analysis of the O-1s peak for unannealed sample. The amount of V_O can be relatively assessed by deconvoluting this peak. The peak shifted towards higher binding energy is due to the presence of V_O.

O-1s peak can be resolved in two Gaussian peaks centered at 528.9 eV and 531.1 eV. The quality of the fit is shown in Figure 3.13 after correcting for the background. The peak at lower binding energy (528.9 eV) corresponds to the metal-oxygen bonds in IGZO and is referred to O_L^{2-}, for lattice oxygen. This is a measure of oxygen in fully oxidized and stoichiometric surrounding [138]. V_O correlate to the shoulder corresponding to the higher binding energy of O^{2-} in the vicinity of an oxygen vacancy [139], [140]. The peak at higher binding energy (531.1 eV, O_V^{2-}) is attributed to the O-atoms in the vicinity of O-vacancy *i.e.* O-deficient areas in the matrix. This component can be related to the density of V_O in the film.

The O-1s peak for annealed sample is shown in Figure 3.14. The peak is deconvoluted into two Gaussian peaks. During the peak fitting, the separation between the two peaks (2.2 eV) and the full width half maxima (FWHM) of the resolved peak (2.5 eV)

are kept constant across the samples. The ratio of the area of O_V^{2-} peak to the area of full O-1s peak is used for a relative measure of V_O change. This ratio is given in Table 3-II for unannealed and annealed samples. The higher ratio for unannealed samples signifies the higher amount of V_O which was reduced during annealing [32], [33]. The 5 min etch of the surface before taking the measurements ensured the surface did not retain any loosely bound O-species. Therefore, a peak at higher binding energy (~533 eV) corresponding to those species was not observed [102].

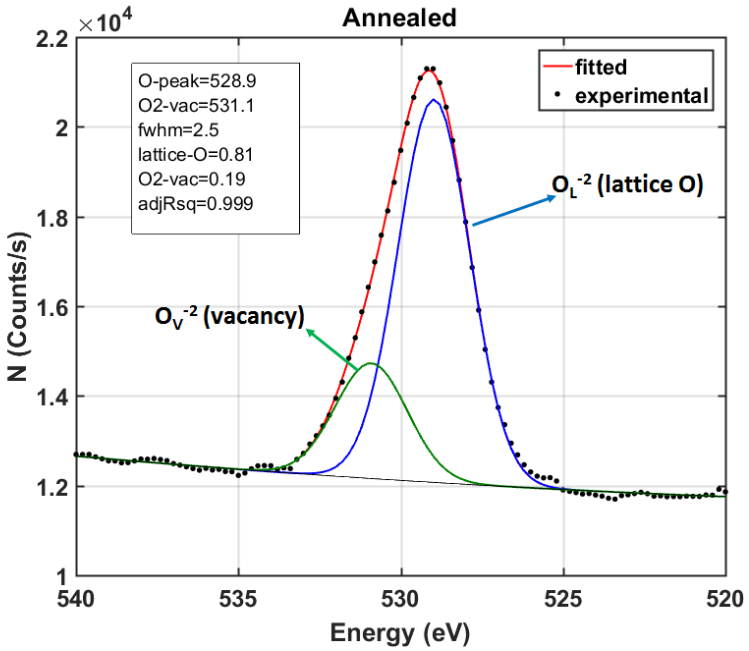

Figure 3.13: XPS analysis of the O-1s peak for the annealed sample showing a decrease in the relative intensity of O_V^{2-} peak which corresponds to a decrease in amount of V_O after annealing.

Table 3-II: Ratio of area under the deconvoluted V_O peak to the area of O-1s peak. The ratio is lower after annealing in oxidizing ambient indicating the density of V_O decreased after anneal.

Sample	O_V^{2-} / (total O-1s)
Unannealed	0.32
Annealed	0.19

The XPS analysis showed that the amount of lattice oxygen increased after anneal. The core levels of In-3d5/3 and Ga-2p3/2 did not show any shift after annealing while Zn-2p3/2 peak showed a systematic shift towards higher binding energy, as shown in Figure 3.15. This suggests that reduction in V_O was associated with increased oxygen bonding with Zn atoms.

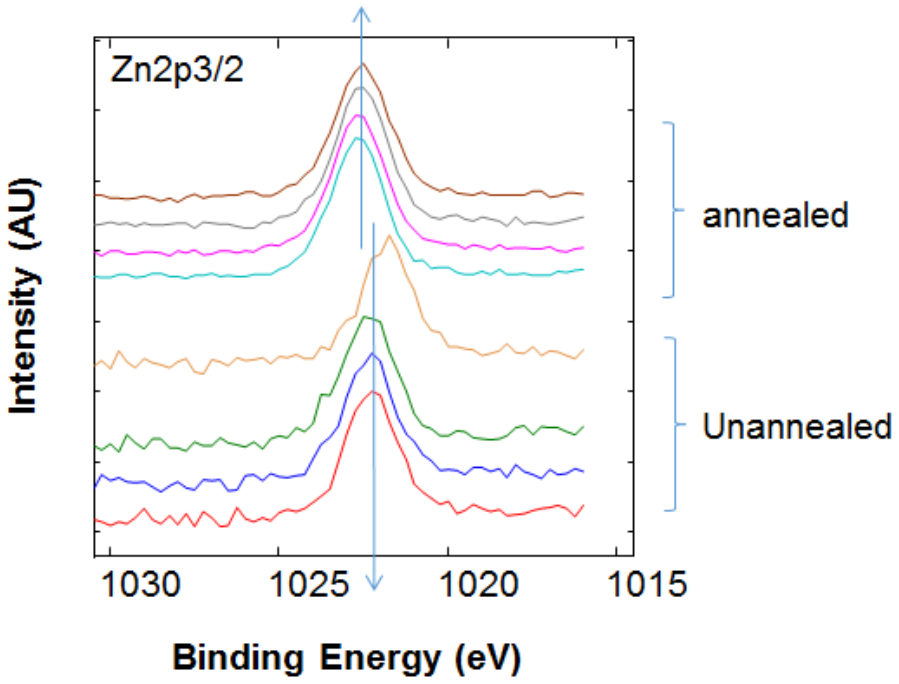

Figure 3.14: XPS analysis of Zn-2p3/2 core levels showing a shift after annealing. This is attributed to the reaction of zinc metal with oxygen after oxidizing ambient anneal.

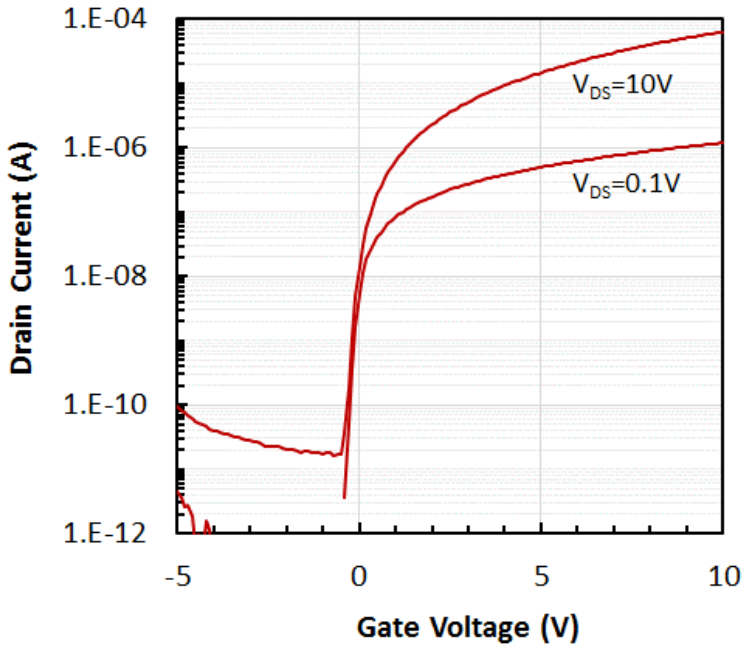

Figure 3.15: Transfer characteristics of IGZO TFT annealed at 400 °C in oxidizing ambient. The device shows excellent transistor properties with a clear on/off state and steep SS. The TFT channel dimensions were L=21 µm & W=100 µm.

The transfer characteristics of the fabricated TFT after annealing are shown in Figure 3.16. The device exhibits excellent gate control over the channel charge with a steep subthreshold swing. The improvement in TFT operation is attributed to the anneal process with an associated reduction in defect states which includes V_O. The role of defects on the electrical properties of IGZO TFTs is discussed in Section 5.2.

The device performance is excellent after an oxidizing ambient anneal. This device did not have any back-channel passivation, which resulted in voltage shifts in the transfer characteristic observed during weeks of aging and is attributed to the adsorption/diffusion of water at the IGZO back-surface [111], [142]. To improve the stability of devices, various dielectrics were applied for surface passivation of exposed IGZO. This topic remains a challenge in process integration, as most thin-film deposition processes render

IGZO more conductive, as shown in Table 3-III. However with an appropriate annealing and integration scheme, excellent results can be achieved with certain passivation materials. Figure 3.17 shows transfer characteristics of an alumina passivated device exhibiting performance equivalent to an unpassivated device.

Table 3-III: Resistivity value of IGZO films after the application of various passivation materials using 4-point probe measurement on the Van der Pauw structures. The TFT on these wafers showed working transistor characteristics before the passivation material deposition. The IGZO thickness is 50 nm.

Passivation material	**Rs (Ω/□)**	**ρ (Ω·cm)**
PECVD SiO_2 (TEOS)	600	0.003
Sputtered quartz	430	0.0021
E-beam alumina	3000	0.015

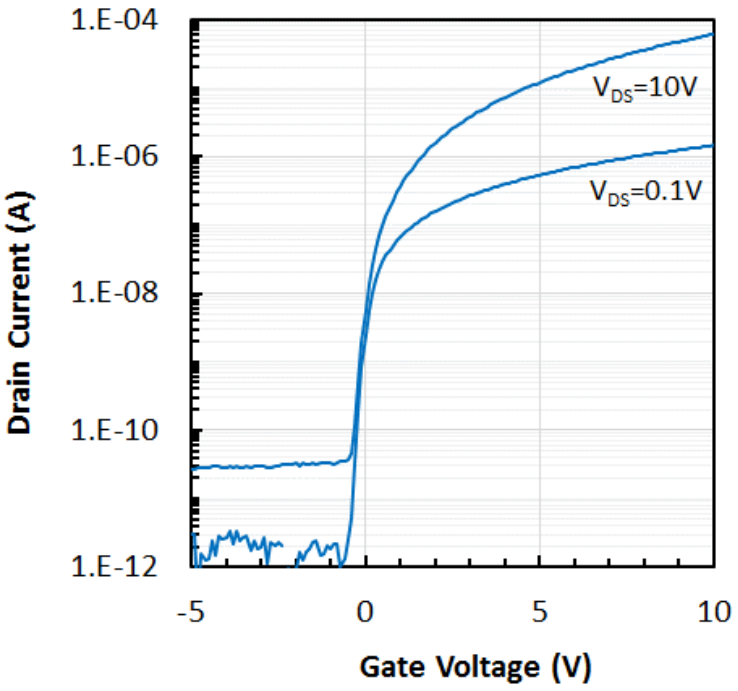

Figure 3.16: Transfer characteristics of evaporated alumina passivated IGZO TFT. The TFT channel dimensions were L=21 µm & W=100 µm.

3.4 CONCLUSION

The RF-sputtered IGZO films are characterized for application in thin-film electronics. XRD measurements have verified the amorphous nature of as-deposited films. The AES measurements have shown a uniform composition throughout the film thickness. Bottom-gate IGZO TFTs without any anneal, showed no gate modulation due to high carrier concentration.

An annealing in oxidizing ambient at 400 °C yielded good TFT characteristics. The crystallinity, thickness and surface roughness of films did not change after the thermal processing, as verified by XRD and XRR measurements. Analysis techniques including SIMS and XPS were used to study the composition of the material after anneal, and quantify differences in composition (*e.g.* oxygen content). SIMS analysis did not show any change in film composition or elemental profile post anneal. The XPS analysis confirmed the decrease in V_O in IGZO films after anneal. This reduced the free carrier concentration in the film, providing appropriate resistivity for TFTs.

The passivation of exposed back-channel of IGZO TFT is imperative for device stability and process integration standpoint. The application of passivation material at the IGZO back-channel results in a higher-conductivity channel, due to creation of additional defect states (V_O) in the bulk or at the interface. An appropriate anneal and process integration scheme mitigates this effect.

Chapter 4. DEVELOPMENT OF THE BOTTOM-GATE IGZO TFT

Despite the demonstrated performance of indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs), the influence of process variables on the material properties and the correlation of the material properties with the device operation are not explicitly known. Defect states play multiple roles which establish both conductive properties of the material as well as anomalies in device behavior. Therefore the interpretation of these states is of considerable importance.

The focus of this work is to characterize the electronic defect states in IGZO film for its application in thin film electronics and to regulate these defects through an understanding of process influences. The importance of thermal annealing of sputtered IGZO films for improved device operation, has been widely established [52], [143], [144]; however the temperature, gas ambient, and process integration details vary [97], [98], [100], [103], [104], [145], [146]. This chapter details the fabrication processes of bottom-gate IGZO TFT and electrical characterization. The initial discussion establishes a baseline process without passivation material added to the back-channel interface. During this phase of the investigation, the selection of contact metallurgy, gate dielectric and annealing conditions were determined.

The results of the experiments are used to extract the density of defect states in bulk IGZO and at IGZO/dielectric interface. These values are used for adjusting the TCAD material modeling discussed in Chapter 5.

In bottom-gate configuration, the back-channel of fabricated TFTs is exposed to the ambient, so the application of a passivation material on the back-channel is imperative for stability and process integration. However, as discussed in Section 3.3, passivation material deposition renders the deposited film conductive. Therefore, a clear understanding of the effect of passivation material deposition is important. A study on the influence of the back-channel passivation material on the operation of IGZO TFTs is presented. Process modifications resulting in improvement of device performance are discussed.

4.1 UNPASSIVATED IGZO TFT

In this section, details on TFT fabrication are provided. The TFTs are fabricated in bottom-gate and top-contact configuration, which is commonly referred to as staggered bottom gate structure as the gate and source/drain (S/D) contacts are on the opposite side of the channel. The S/D and gate metals are designed to overlap to facilitate the S/D contact to IGZO. Therefore, the channel length is defined by the S/D metal.

4.1.1 Baseline TFT Fabrication

A 50 nm molybdenum layer was deposited on oxidized silicon or glass substrate using CVC-601 sputter tool. The sputtering was performed in Ar ambient at 2.7 mT pressure. A DC power of 1000 W was applied to the 8” target. These settings yield a sputter rate of ~15 nm/s. A base pressure of $1.6\times^{-6}$ Torr was achieved after an overnight pumpdown to ensure high quality films. The Mo film was patterned using photolithography to define the bottom gate electrode and wet etched using phosphoric acid etchant at room temperature.

The gate dielectric is a 100 nm SiO_2 layer deposited by AME P5000 PECVD tool at 390 °C using TEOS precursor. A 50 nm IGZO film was then sputter deposited with parameters identical to those in Section 3.1.2. The IGZO mesa was patterned using photolithography and etched in a dilute HCl solution (6:1 DI water). The etch-rate of IGZO measured on monitor wafers was ~2.5 nm/s. An etch time of 25 s (25% over etch) was used to ensure the IGZO was completely etched.

Annealing was either performed at this point (pre-metal anneal) or after the source/drain metal definition (post-metal anneal). Contacts were opened to the gate electrode using 10:1 BOE solution. The source/drain (S/D) contact metal, either evaporated Al or sputtered Mo, was then defined using a lift-off resist process. Aluminum was evaporated in CHA flash evaporator. Mo was sputtered in CVC 601 in Ar ambient at 2.2 mT using DC power of 200 W. The sputter power was reduced to protect the LOR 5A lift-off resist. Note that Al was evaporated on top of the Mo contact metal prior to lift-off in order to avoid oxidation of Mo during the subsequent annealing process. The cross-section schematic and top-view optical image of fabricated device is shown in Figure 4.1.

The large TFT test structures are designed for ease in electrical testing while avoiding additional processing for interconnects. Electrical testing was done using an HP-4145B parameter analyzer on 4-probe Van der Pauw structures, and TFTs of constant channel width (W = 100 µm) and various channel lengths ranging from L = 3 to 45 µm. All I_D-V_{GS} transfer characteristics presented were taken with a gate voltage up-sweep and medium measurement integration time unless otherwise noted, with low-drain and high-drain bias conditions at 0.1 V and 10 V, respectively.

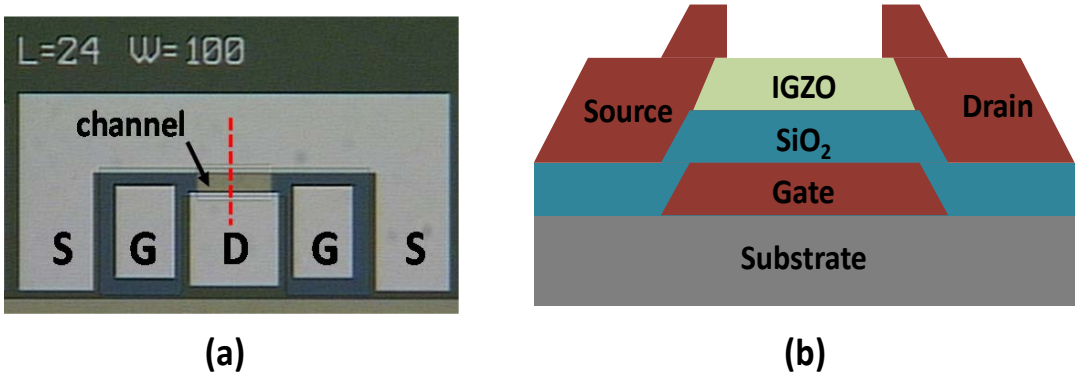

Figure 4.1: (a) Micrograph of a bottom-gate IGZO TFT with labeled source (S), gate (G) and drain (D) electrodes, with a cross section view taken through the channel at the red dotted line shown in (b). Either Al or Mo is used as the source/drain contacts to the IGZO. The L = 24 µm channel length is defined by the gap between the source and drain metal. The W = 100 µm channel width is defined by the IGZO mesa etch.

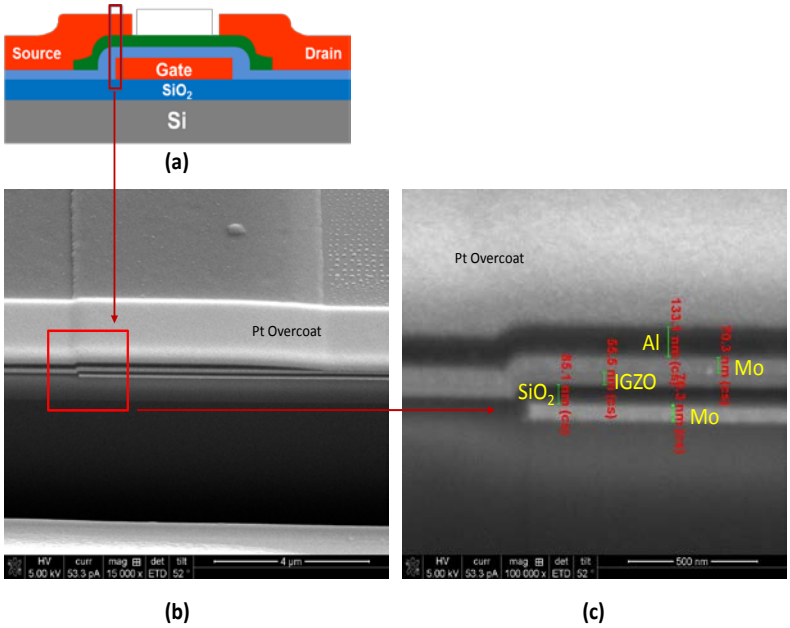

Figure 4.2: (a) Schematic view of the cross-section of TFT (b) Low magnification SEM image of the boxed region in (a). The Pt overcoat is used to protect the top surface/edge of the region of interest. (c) View of layer structure and profile from boxed region in (b). Mo/Al bilayer is used for S/D contact metal.

4.1.2 Mask-Defined Channel Length (L_{mask})

After fabrication, focused ion beam - secondary electron microscopy (FIB-SEM) was used to examine the device structure (Mo S/D, post-metal anneal). The edges of final device were FIB cross-sectioned and imaged for edge profile and thickness. A platinum overcoat was put down on the sample before milling in order to protect the surface. Figure 4.2 shows the FIB-SEM images of the final TFT after annealing along the gate edge. All layers of films can be distinctly seen indicating that there is no cross-diffusion of deposited films after the annealing.

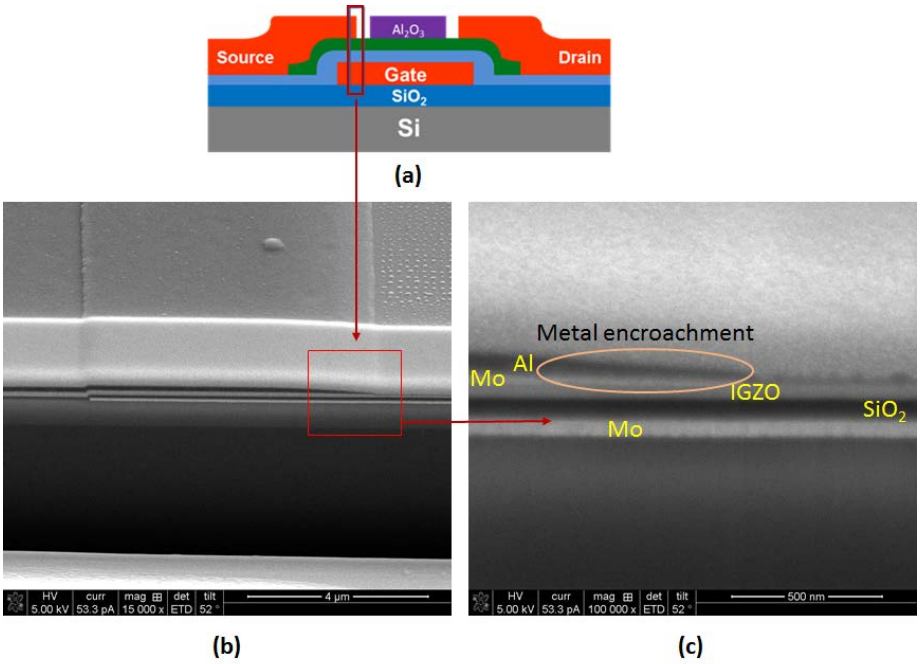

Figure 4.3: (a) Cartoon representation of the cross-section of TFT. The red box represents the area which was imaged. (b) Low magnified image of the boxed region of (a). (c) High magnification image of the boxed region shown in (b) showing the encroachment of S/D metal (Mo/Al) in the undercut region after developing lift-off resist. This leads to a decrease in metal defined channel length.

As stated in fabrication details S/D metals are defined through lift-off resist process. The lift-off resist dissolves faster in CD-26 developer used during lithography. This leaves an overhung profile of lift-off resist. Subsequent metal (Mo/Al) deposition encroaches below this profile from both sides of the channel. This can be seen in the FIB cross-section along the edge of source metal (Figure 4.3). This encroachment of S/D metal makes the metal defined channel length (L_{eff}) shorter than the mask defined length (L_{mask}). Figure 4.4 shows an optical image of the device channel region after the lift-off resist coating. The lift-off resist protects the channel region, but it is undercut at the edges, as shown in magnified image and metal deposition fills this undercut. Due to this, the mask defined channel length is decreased by ~3 µm.

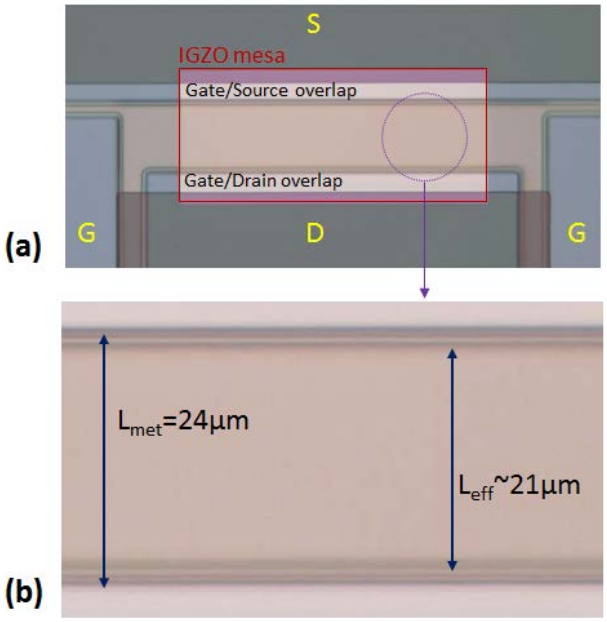

Figure 4.4: Micrograph of 24 µm device after lift-off resist coating. The IGZO mesa and G/S/D overlapped region are marked in (a). (b) The magnified image of the circled area in (a). The lift-off resist is undercut reducing the effective channel length by ~1.5 µm on each side. The L_{mask}= 24 µm device is effectively L_{metal} = 21 µm device. This was also confirmed by Terada-Muta analysis, see Section 4.2.3.

4.2 CONTACT METALLURGY

Contact metallurgy can have a dominant influence on device performance. There are several examples of metals used as source-drain contact electrodes for IGZO TFTs including Au/Ti [147], [148], indium-tin-oxide (ITO) [128], Mo [149], Pt/Ti [108], aluminum-zinc-oxide (AZO) [150], and Cu [151]. Although cited references discuss the influence of contact metallurgy on device characteristics, surprisingly most of them do not discuss the dependence of the contact behavior on the annealing process which is especially important for Al-contact devices [152]–[156]. Researchers have reported but not adequately addressed observations made on the behavior of Al-contact devices following a post-metal anneal [154]. Aluminum is either not included in studies pertaining to the comparison of various metal electrodes for IGZO [155] or annealing is not done after Al deposition [152], [153], [157] or the issue is avoided by inserting an additional metal layer between IGZO and Al contact [158], [159]. Reports on Mo-contact and Al-contact devices often do not discuss the effect of annealing on the contact behavior [152], [160].

4.2.1 M-S Contact Potential

To understand the behavior of contacts, device simulation using Silvaco® Atlas™ was performed. Figure 4.5 shows an ATLAS simulation of the energy barrier established between various contact metals and IGZO using the material model presented in Chapter 5. The simulation solved for a zero-bias initial condition, with a vertical cut taken through the source contact (at X = 0 μm). Titanium has a relatively small M-S barrier, and results in ohmic-like behavior as source/drain electrodes with minimal impact on transistor behavior [148]. Aluminum has a lower workfunction, and should ideally result

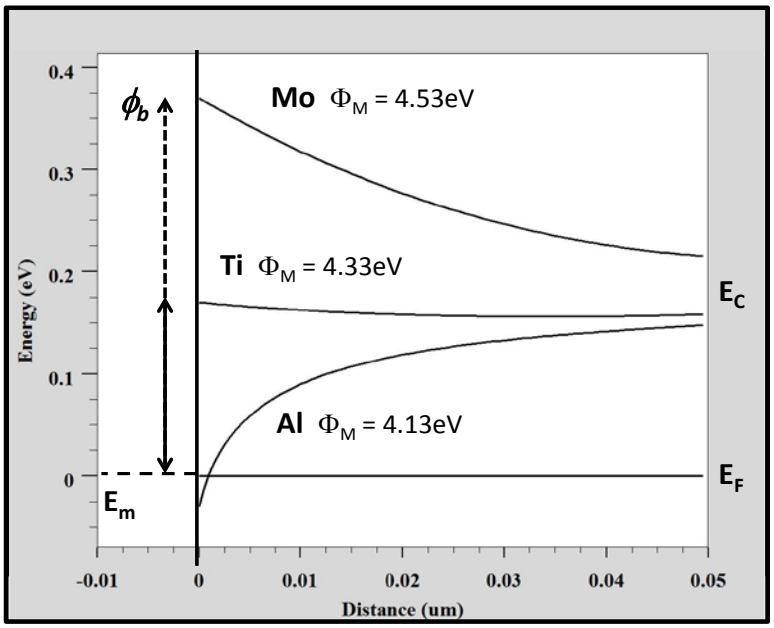

Figure 4.5. Energy band diagram generated by Silvaco® Atlas™ showing the energy barriers associated with contact metals and IGZO. The workfunction of Al should ideally provide an ohmic contact, whereas the Mo contact appears to present a significant source barrier (ϕ_b). Non-idealities such as M-S interface states are not considered. Note that the conduction band energy (E_C) does not line up for each case due to additional influence (band-bending) from the Mo gate metal workfunction.

in ohmic contact behavior, whereas molybdenum has a higher workfunction and should present a higher Schottky barrier contact. However, Mo has been widely used as source/drain metal in IGZO TFTs [98], [122], [149], [161], [162]. In this study, Al and Mo metals are investigated for contact metallurgy.

4.2.2 TFT Contact Behavior

In this section, investigations on Mo and Al as the source/drain contact metal for IGZO TFTs are discussed. First, the results of pre-metal (after IGZO deposition but before source/drain metal deposition) and post-metal (after source/drain metal deposition)

annealing in air ambient are established. The influence of different gas ambient conditions on the resulting contact and channel behavior is then presented in Section 4.3.

Devices fabricated without any thermal treatment exhibited very poor electrical behavior as shown in Section 3.3, and such results are not discussed here. The first set of results obtained were from the pre-metal anneal treatment in air ambient (45% humidity, class 1000 clean room) at 350 °C for 1 h, done immediately after the IGZO mesa definition. Figure 4.6 shows the I-V transfer characteristics of Al-contact and Mo-contact devices, showing almost perfect overlay. While the TFT performance for this treatment does not demonstrate impressive channel mobility, the characteristic overlay of the two different source/drain contact metals indicates that the channel regions of the devices are essentially the same, and that the difference between the influence of the evaporated Al or sputtered Mo processes on the channel behavior is insignificant. In addition, the TFT characteristics are clearly dominated by the channel conductance, with no suggestion of non-ohmic behavior by either the Al-contact or and Mo-contact devices.

Because of the influence of device operation, the literature is full of inconsistencies in parameter extraction methods for IGZO TFTs. This topic is thoroughly addressed in Chapter 6. At this stage of the investigation, a minimal set of parameters with simplified extractions routines is used for relative comparisons between experimental treatments. Channel mobility and threhold voltage are extracted using gradual channel approximation transistor equation in saturation mode [163]. Threshold voltage is taken as the V_{GS} value at drain current, I_{DS} = 1 nA. Effective mobility in saturation mode, μ_{sat}, is extracted at V_{DS} =V_{GS} =10 V. Subthreshold swing (SS) is extracted from the high drain bias I_D-V_{GS} curves at the maximum slope.

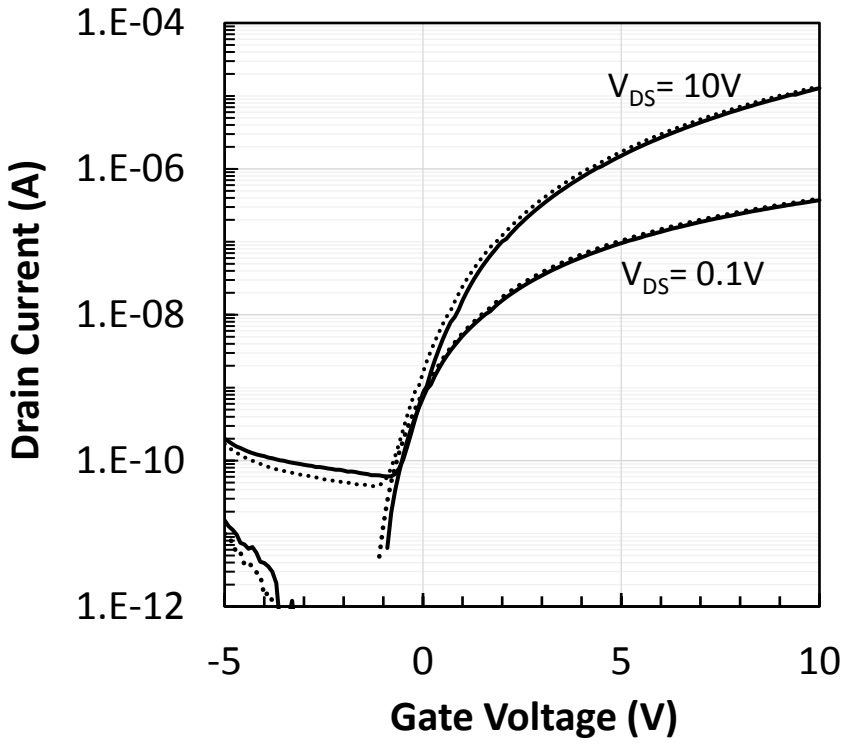

Figure 4.6: Overlay of transfer characteristics for Al-contact (dotted line) and Mo-contact (solid line) devices that had a pre-metal air anneal 350 °C for 1 h. The TFT channel dimensions were L = 9 µm & W = 100 µm. The extracted subthreshold swing and saturation-mode channel mobility are SS ~ 550 mV/dec & μ_{sat} < 1 cm^2/V·s.

The influence of a post-metal 350 °C air anneal treatment on device performance is shown next. Figure 4.7 shows the results of a Mo-contact device, with demonstrated improvement over the pre-metal treatment, both in the on-state (μ_{sat} ~ 3.2 cm^2/V·s) and the off-state (*SS* ~ 250 mV/dec) performance. In addition, the characteristic is right-shifted, or more enhancement-mode.

The Al-contact devices show very different results, which demonstrate significant degradation over the pre-metal treatment (Figure 4.8). Essentially no on-state current was observed in the low V_{DS} characteristic, whereas the saturation characteristic is right-shifted with a much higher *SS*. The transfer characteristics from the post-metal anneal treatment

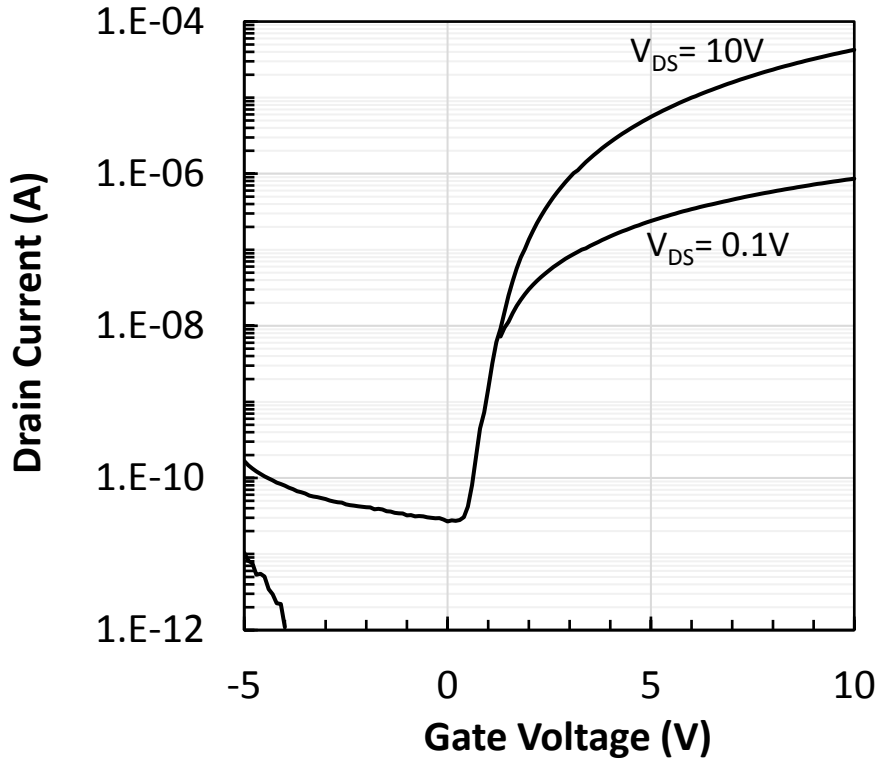

Figure 4.7: Transfer characteristics for a Mo-contact IGZO TFT after a post-metal anneal in air at 350 °C for 1 h. The TFT channel dimensions were L = 9 µm & W = 100 µm. The extracted subthreshold swing and saturation-mode channel mobility are SS ~ 250 mV/dec & μ_{sat} ~ 2.7 $cm^2/V{\cdot}s$.

are dominated by the contact behavior, which has established a significant barrier to current flow. This result is expected to be due to the formation of an interfacial AlO_x layer during the annealing process. Additional experiments on Al-contact devices with post-metal annealing in oxidizing ambient conditions demonstrated similar results, with no value in a detailed analysis and discussion. However, experiments investigating the Mo-contact devices proved to be insightful in understanding the influence of the annealing process and beneficial in realizing further improvement in device performance.

The measurements showed that Mo provides an ohmic contact to IGZO. This was further verified by simulating TFT characteristics using Mo and Al S/D metal and

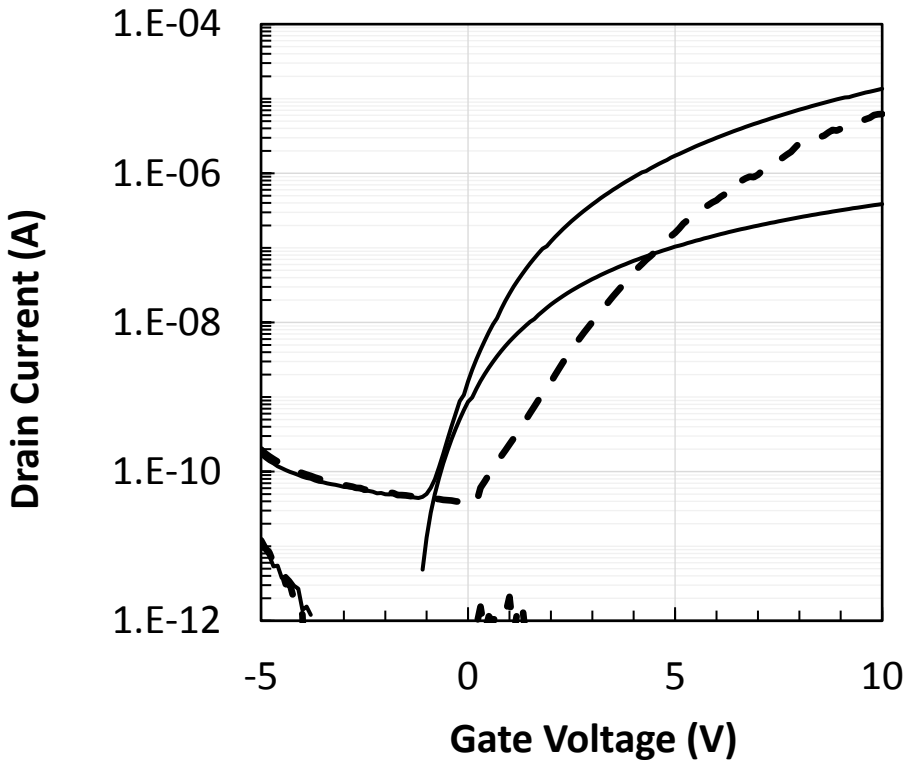

Figure 4.8. Overlay of transfer characteristics for Al-contact devices with a pre-metal (solid line) and a post-metal (dotted line) air ambient anneal at 350 °C for 1 hr. The TFT channel dimensions were L = 9 µm & W = 100 µm. The post-metal anneal treatment under low drain bias (V_{DS} = 0.1V) is without an on-state characteristic.

comparing it with the measured data (see Chapter 5 for IGZO material model). An overlay of simulated and measured on-state transfer characteristics are presented in Figure 4.9. The measured transfer characteristic for the Mo-contact device in Figure 4.9 exhibits behavior that is consistent with the Al-contact simulation more than the Mo-contact simulation, which supports the interpretation of ohmic source/drain contacts. The contact behavior is dominated by interface states which facilitate carrier injection. The match between the measured and simulated characteristics under ohmic contact conditions in on-state operation is quite reasonable, with a slight discrepancy in subthreshold state.

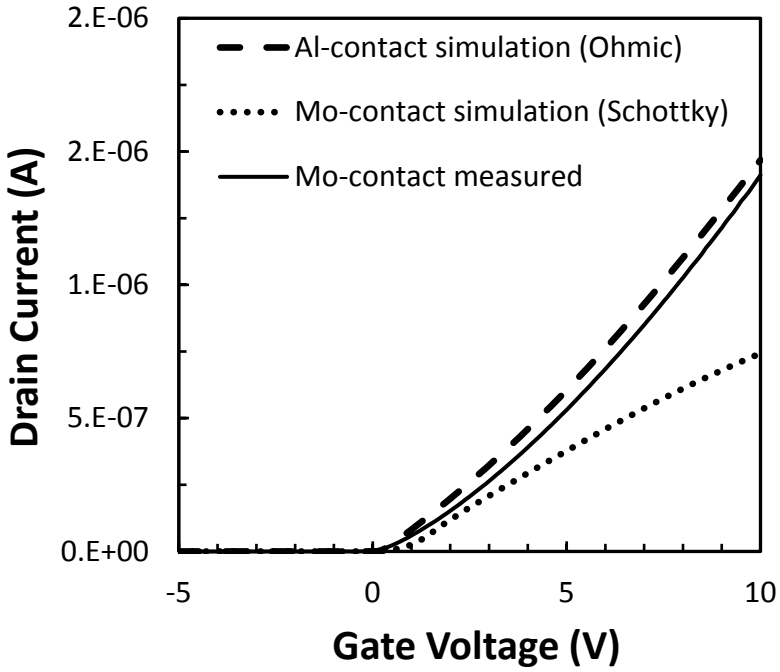

Figure 4.9. Overlay of a measured linear-mode (V_{DS} = 0.1 V) transfer characteristic of Mo-post-metal annealed TFT (solid line), along with simulated characteristics consistent with M-S contact conditions for Al (dashed line) and Mo (dotted line). The TFT channel dimensions were L = 21 µm & W = 100 µm.

4.2.3 Effective Source/Drain Series Resistance

I-V curves suggest the behavior of the Mo-contact TFT to be ohmic source/drain contacts to the IGZO, rather than Schottky barrier M-S contacts which may be expected when considering the metal workfunction, Figure 4.5. Establishing the quality of the contacts is important. Terada-Muta analysis of transistor characteristics was performed to calculate the S/D contact resistance ($R_{S/D}$) and effective channel length (L_{eff}) [164]. The total resistance (R_{tot}) of the TFT can be expressed as:

$$R_{tot} = r_{ch}L + R_{SD} \qquad (4.1)$$

where r_{ch} is the channel resistance per unit length and $R_{S/D}$ is the resistance offered by the S/D contacts. Using Equation (4.1), R_{tot} can be written as:

$$R_{tot} = \frac{V_{DS}}{I_{DS}}\Big|_{V_{DS_{lin}}} = \frac{L}{WC_{ox}\mu(V_{GS} - V_T)} = r_{ch}L + R_{SD} \qquad (4.2)$$

Figure 4.10 shows the R_{tot} vs L plot at different V_{GS} for standard devices. The average value of R_{SD} and L_{eff} can be extracted from the unique intersection point of all the curves and r_{ch} can be found by the slope. The $\Delta L \sim 3$ µm is due to the lift-off resist process used to define S/D metal, so the L_{eff} is 3 µm less than the mask defined channel length. This has been verified through optical image of the device (see Figure 4.4). The current flow is dominated by transistor operation (*i.e.* channel resistance); series resistance is essentially negligible as shown by the intersection point (y=0) in Figure 4.10.

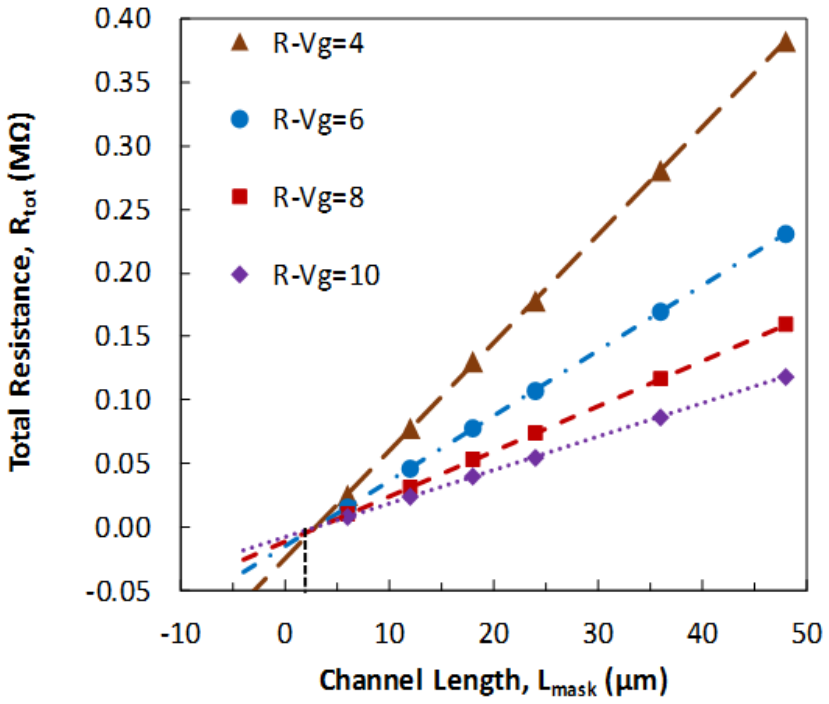

Figure 4.10: Terada-Muta analysis of IGZO TFTs. The extracted $\Delta L \sim 3$ µm is consistent with microscopic images of LoR coated wafers shown in Figure 4.4.

The quality of contact can be assessed from the output curves of TFT. Figure 4.11(a) shows the output characteristics of post-metal N_2/O_2 annealed TFTs with Mo contacts. A non-ohmic S/D contact manifests itself as a non-linear response of I_D at low

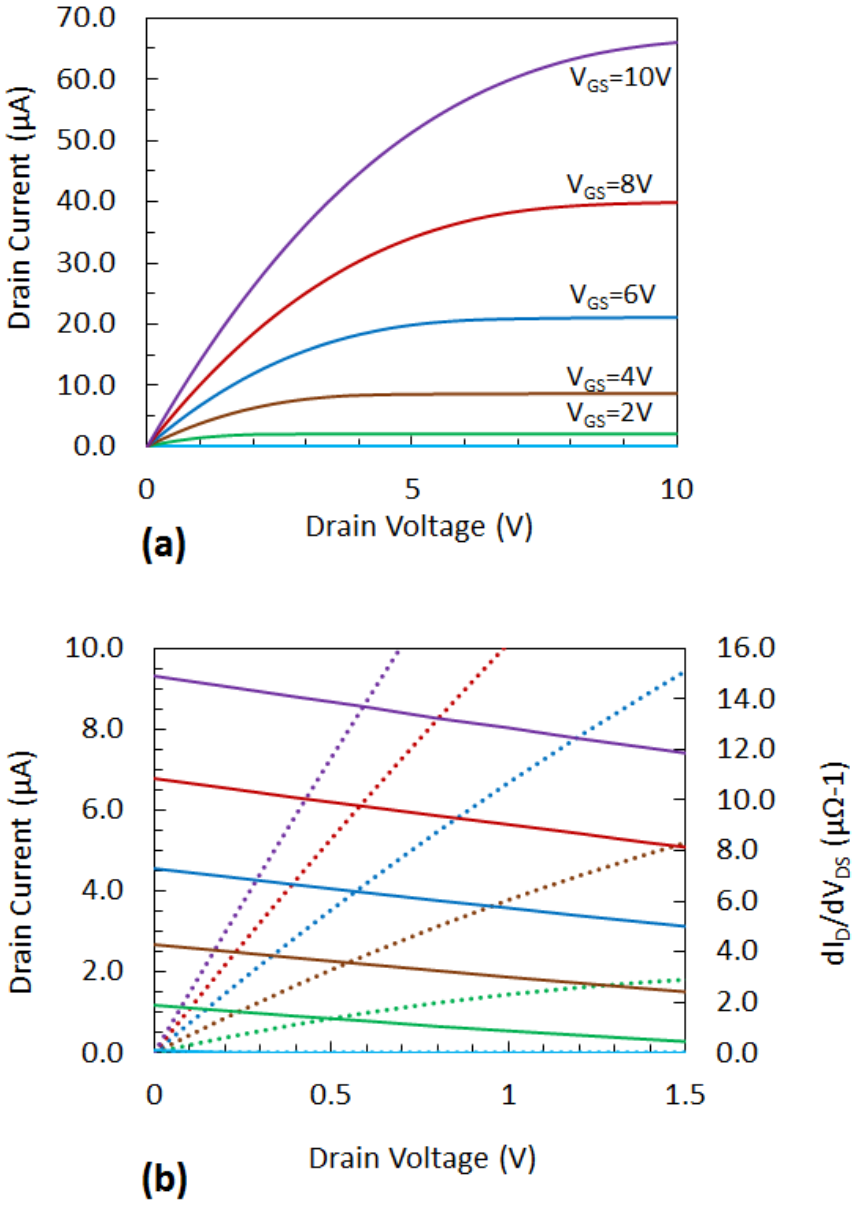

Figure 4.11: (a) Output characteristics of IGZO TFT. The TFT channel dimensions were L = 21 μm & W = 100 μm. The device shows a clear saturation. (b) I_D-V_{DS} of the same device near origin. The $\delta I_D/\delta V_{DS}$ (dotted line) is plotted on y2- axis showing no current crowding, thus verifying the ohmic nature of the Mo-IGZO contact.

V_{DS} values. Figure 4.11(b) shows the I_D-V_{DS} data near the origin. In case of non-ohmic contacts or high bulk defect density in semiconductor, these curves show non-linear response in this region generally referred to as "current crowding" [165]. The absence of current crowding suggests a good ohmic contact established between Mo and IGZO. This can be easily seen in the derivative of output characteristics (dI_D/dV_{DS}), on the *y2*-axis on Figure 4.11(b). The dI_D/dV_{DS} is linearly decreasing with V_{DS} with no inflection point, which follows the gradual channel approximation theory of transistors [166] and confirms the ohmic behavior of the contact [59].

4.3 IMPACT OF ANNEALING ON UNPASSIVATED TFTS

Though there are reports of IGZO devices which demonstrate good characteristics without thermal treatment [150], [152], the effectiveness of annealing of IGZO TFTs to reduce sub-gap states (e.g. oxygen vacancies, V_O) and thus improve performance has been almost universally accepted [97], [103], [144]. Several groups have published results on annealing in various ambient conditions [97], [167]. While the IGZO properties will depend on the deposition process parameters such as sputter power [168] or oxygen partial pressure [152], the importance of subtle recipe details and the impact of annealing on contact performance have been understated in the literature.

4.3.1 Oxidizing Ambient Annealing

After determining that the post-metal anneal with Mo contacts produce better performing devices, the next step was to explore different anneal ambient and temperature. Since air post-metal anneal at 350 °C produced reasonably better characteristics, for the next set of

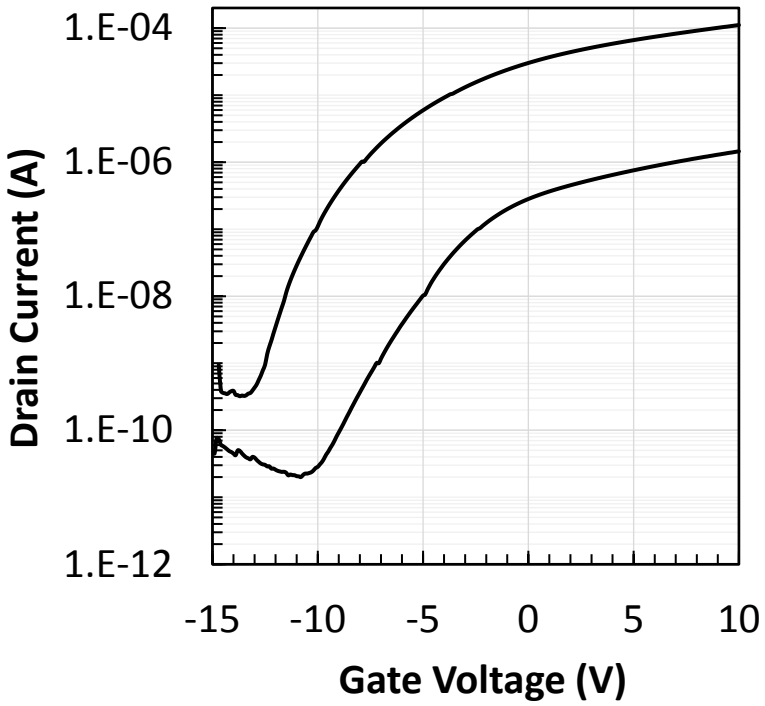

Figure 4.12. Transfer characteristics of a Mo-contact device following a post-metal air ambient anneal for 30 min at 400 °C. The device shows distortion in characteristics due to over-oxidation. The TFT channel dimensions were L = 21 µm & W = 100 µm.

devices, annealing was performed in air at 400 °C. The transfer characteristics of TFT measured after anneal are shown in Figure 4.12. The devices exhibited a significant loss in gate control, especially at high V_{DS}. The current drive of the device was higher, which is due to enhanced IGZO conductivity rather than a higher transconductance. Although annealing in air should ideally reduce oxygen vacancy defects [103], this aggressive oxidation treatment appears to actually generate additional defects which increases the free carrier concentration [169].

This result was followed by additional Mo-contact post-metal anneal experiments using oxygen and nitrogen ambient at 400 °C, however ramp-down conditions were still in an air environment. The ramp-down rate in air was approximately constant, decreasing

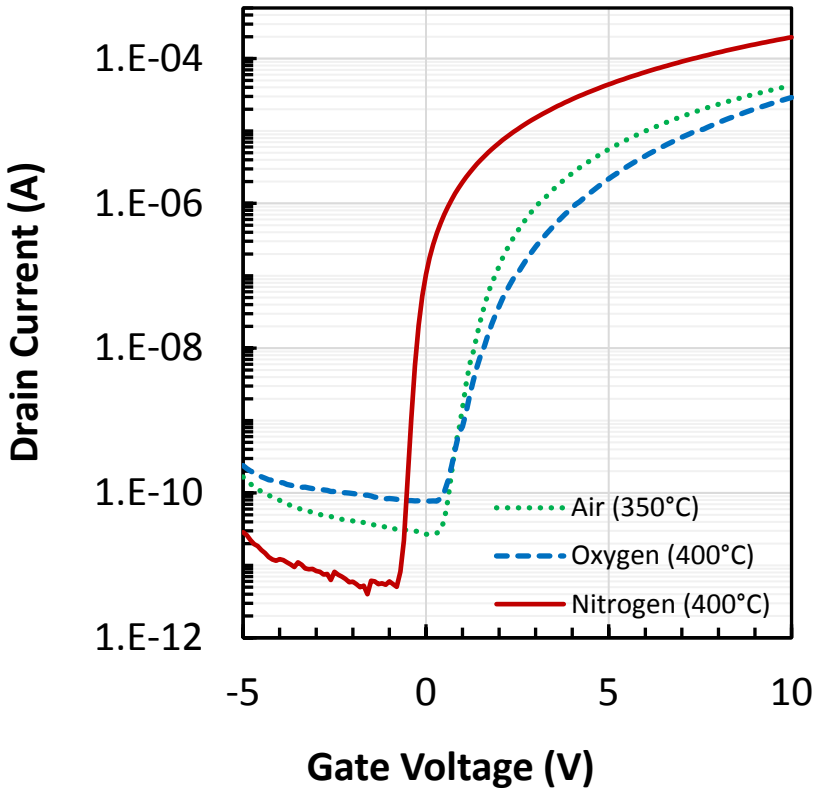

Figure 4.13. Overlay of saturation-mode (V_{DS}=10 V) transfer characteristics for Mo-contact post-metal anneal treatments in air (350 °C), O_2 (400 °C) and N_2 (400 °C). Ramp-down conditions for each treatment were in air ambient. The TFT channel dimensions were L = 9 µm & W = 100 µm. Extracted parameters are listed in Table 4-I.

from 400 °C to 150 °C over 3 h. Figure 4.13 shows the overlay of saturation current after annealing at 400 °C for 30 min in either O_2 or N_2, along with the post-metal air anneal at 350 °C shown previously in Figure 4.7. The device parameters extracted from transfer characteristics are shown in Table 4-I.

The post-metal N_2 anneal with air ramp-down shows improvement over the air-anneal result. In contrast, the post-metal O_2 anneal demonstrated degradation in both SS and on-state performance, with distortion indicating the presence of trap states. This suggests that the degree of oxidation that takes place during the air-ambient ramp-down

Table 4-I: Parameters for Mo-contact IGZO TFTs with post-metal anneal treatments in air, O_2 and N_2 with ramp-down in air ambient.

	V_T (V)	**μ_{sat} ($cm^2/V{\cdot}s$)**	**SS (mV/dec)**
Air (350 °C)	1.0	2.7	250
O_2/air (400 °C)	1.1	1.9	420
N_2/air (400 °C)	-0.4	9.5	120

following the N_2 anneal is closer to the optimum conditions, thus both time and temperature in air ambient are important in establishing electrical behavior. The N_2 anneal treatment demonstrates a left-shift in V_T compared to the other anneal treatment. The channel mobility (μ_{sat}) and subthreshold (*SS*) show improvements over results listed in Table 4-I.

The "standard" unpassivated IGZO TFT was established to have Mo contact metallurgy with post-metal N_2/air anneal at 400 °C for 30 mins. To clarify the role of N_2 during annealing, devices were annealed in N_2 and ramped-down in O_2 (for better environment control). Results were compared with devices who were simply ramped down in O_2 without any N_2 soak time. The mobility and SS for devices only ramped down in O_2 was inferior to the devices annealed in N_2 and ramped down in O_2. The role of N_2 soak-time is to bring the IGZO channel to the appropriate state and anneal out the defect states created during sputter deposition. The subsequent O_2 ramp-down afterwards regulates the amount of V_O in the film and reduces the number of charge carriers. This establishes a semiconducting state of IGZO channel as confirmed by XPS analysis discussed in Section 3.3.3.

4.3.2 Inert Ambient Annealing

Mo-contact TFTs that were processed with a 400 °C post-metal anneal without being subjected to air or O_2 above 150 °C reinforced the importance of the oxidizing ambient. IGZO film samples that were annealed at 400 °C in vacuum become very conductive, with a measureable sheet resistance of ~ 8 kΩ/□. Transfer characteristics of TFTs that had annealing done in N_2 or vacuum, including the ramp-down stage, demonstrated very little gate modulation as shown in Figure 4.14.

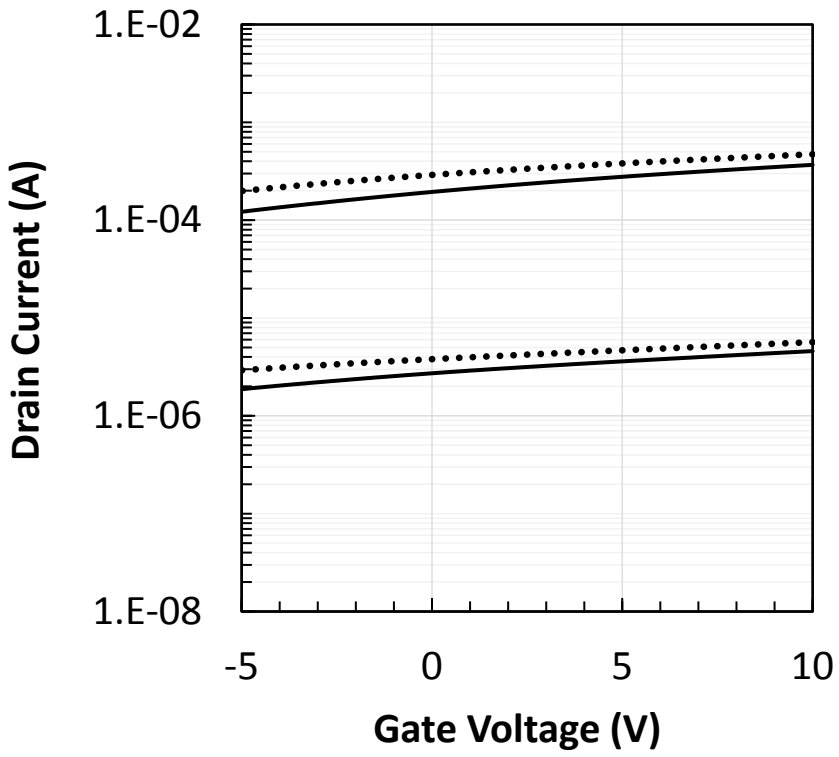

Figure 4.14: Transfer characteristics of IGZO TFT devices with a post-metal N_2 anneal (solid line) and vacuum anneal (dotted line) without any exposure to air during ramp-down. The devices show no gate modulation due to high carrier concentration. The TFT channel dimensions were L = 21 µm & W = 100 µm.

4.4 GATE DIELECTRIC INVESTIGATION

In the previous section, results of TFT with silicon dioxide as gate dielectric were discussed. The devices showed good TFT characteristics. Nevertheless, it was important to study the quality of this interface because the presence of interface defects at gate dielectric/IGZO interface can manifest itself during the transistor electrical response through degraded *SS*, shift in V_T or hysteresis in transfer characteristics. In literature, there have been reports on the application of various gate dielectrics such as alumina [170]–[173] and silicon nitride [122], [149], [161], [162], [174] and high permittivity dielectrics [51], [175]–[177] claiming improvements in device performance.

This study involves an investigation on the choice of gate dielectric material on the transistor characteristics. Devices were fabricated using the process described in Section 4.1.1. Silicon dioxide, silicon nitride and aluminum oxide were investigated as gate dielectric materials. The electrical results are used to extract the interface defect states for different gate dielectrics/IGZO interface.

4.4.1 Silicon Nitride / IGZO Interface

A 100 nm silicon nitride is deposited by low pressure chemical vapor deposition (LPCVD) using SiH_4 and NH_3 precursors at 810 °C. One sample with Si_3N_4 went through wet oxidation to grow a thin oxide over nitride (NO) to have an oxide interface with IGZO. Though the process is not glass compatible, the aim of this study was to explore the interface quality of nitride and NO with IGZO. The transfer characteristics of such devices are shown in Figure 4.15. For Si_3N_4 as gate dielectric, the I_D-V_{GS} curves show a crossover of low drain and high-drain characteristics where the high drain bias appears to have higher

threshold voltage (see Figure 4.15(a)). This is in response to the slow traps present at the Si_3N_4/IGZO interface. When the gate voltage is swept with drain voltage held at 0.1 V, these interface states capture the electrons and are filled during low drain sweep. These defect states do not release the trapped electrons instantly. During the high drain sweep, the trapped electrons repel the gate-induced electrons and make it less favorable for the gate to create an accumulation layer. This manifests itself as an effective increase in the threshold voltage during the second sweep.

The same device was tested again immediately and the results are plotted in Figure 4.15(b). During the second sweep (solid-blue curve), the characteristics are right shifted and show a perfect overlay (both high & low drain bias sweeps) with the very first sweep (dotted-red curve). This verifies the electrons trapping at the interface during initial sweep of V_{GS} and a positive shift in the characteristics for subsequent measurements. The device again demonstrates this crossover when tested after a few minutes (not shown) because during the wait-time the traps release the captured electrons. The characteristics are left shifted for Si_3N_4 gate dielectric compared to SiO_2 dielectric due to the presence of positive fixed charges at the interface [122].

The I_D-V_{GS} curves for TFTs with NO/IGZO interface, Figure 4.15(c), exhibit a perfect overlay of low and high drain bias curves. The non-ideal behavior (crossing-over) was not observed even when the "short" integration time was used for measurement. This suggests that either the surface states are absent or "fast" surface states are present which do not affect the normal operation of transistor. The characteristics are shifted to right suggesting the absence of the positive charges present in case of Si_3N_4. The NO interface

shows improved device operation compared to nitride interface, but the characteristics are inferior to SiO_2 as gate dielectric.

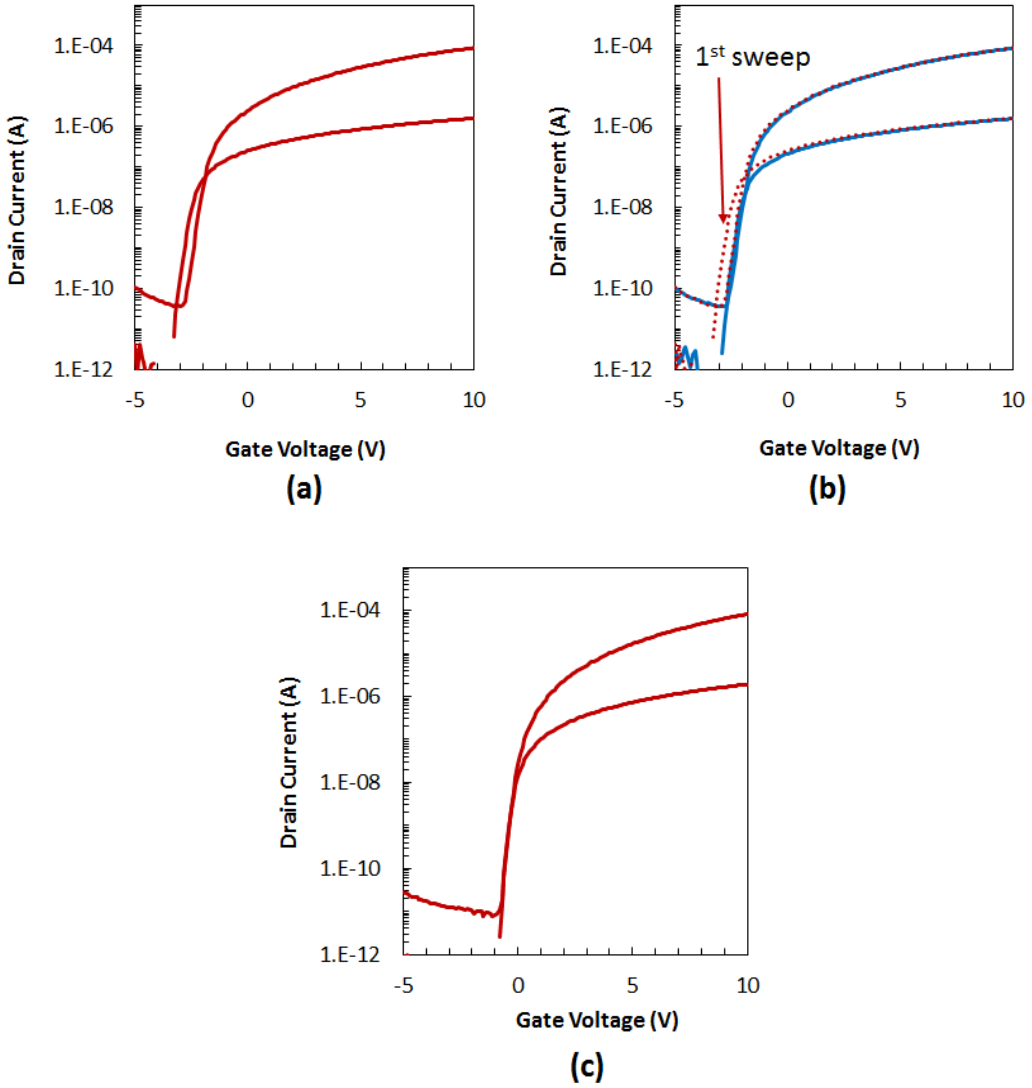

Figure 4.15: (a) Transfer characteristics of IGZO TFT with Si_3N_4 as the gate dielectric. The characteristics for Si_3N_4 are left shifted due to the presence of positive fixed charge at the nitride/IGZO interface. The low and high drain biases crossover suggests the presence of slow traps at the interface. (b) The same device retested immediately (blue solid line). No crossover between low and high drain biases is observed because the electrons captured at the interface states during the first test-sweep are not released and therefore subsequent testing shows perfect overlay with initial high-drain bias data. (c) I_D-V_{GS} data for oxynitride interface showing right shifted characteristics compared to (a) and no crossover suggesting the absence of slow traps at NO/IGZO interface.

4.4.2 Aluminum Oxide / IGZO Interface

Alumina is deposited by e-beam assisted evaporation process and atomic layer deposition (ALD). The application of 100 nm evaporated alumina as the gate dielectric yielded devices with very high leakage and could not be turned off even at V_{GS} = -10 V (data not shown). The evaporated alumina film has pinholes that provide the paths for leakage. Therefore, a SiO_2/AlO_X bilayer was used as the gate dielectric. The representative transfer characteristics are shown in Figure 4.16(a). Much like Si_3N_4/IGZO devices, the TFT exhibits the presence of slow traps at the interface, evident from the cross-over between low and high drain bias sweeps. From the right-shifted transfer characteristics of these devices, it is apparent that AlO_X may retain more negative fixed charge at the IGZO interface. The presence of negative charge will push away the electrons and a higher gate bias will be needed to create the same accumulation charge in the channel.

ALD alumina was deposited in a TFS 500 Beneq, single wafer system using trimethylaluminum (TMA) and water as precursors. A 20 nm ALD Al_2O_3 film was deposited on TEOS SiO_2. The TFT shows excellent transfer characteristics, Figure 4.16(b), with perfect overlay of low and high drain bias. The subthreshold swing for ALD Al_2O_3 devices is steep and the interface appears to be as good as SiO_2/IGZO interface.

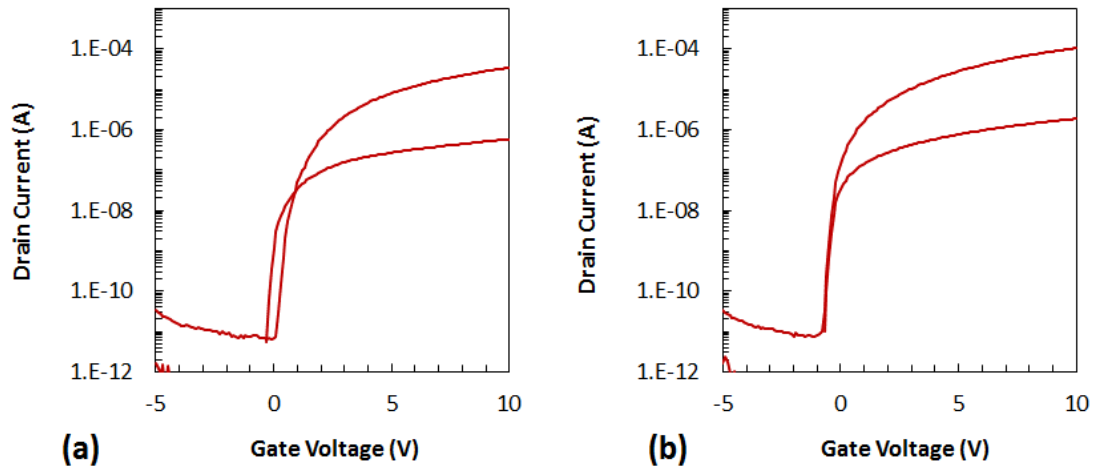

Figure 4.16: Transfer characteristics of TFTs fabricated using (a) SiO_2/AlO_X (evaporated) and (b) SiO_2/Al_2O_3 (ALD) as the gate dielectric. AlO_X exhibited slightly right-shifted characteristics which may be due the creation of negative fixed charge at AlO_X/IGZO interface. The crossover of low and high drain bias sweeps is attributed to the presence of slow trap states at the gate dielectric/IGZO interface. ALD alumina interface seems to be free from the slow traps operative in evaporated alumina interface.

4.4.3 Density of States (DOS) Calculation

The SS of transistor is related to the density of sub-gap states (D_S) through following relations [103], [163], [178]:

$$D_S = C_{ox}\left(\frac{SS}{\ln(10).(k_BT)} - \frac{1}{q}\right) \tag{4.3}$$

$$D_S = \int_0^d N_b dx + N_{it} \tag{4.4}$$

where C_{ox} is gate capacitance per unit area, k_B is Boltzmann constant, q is electronic charge, N_b is the bulk charge density due to O_V donor states and N_{it} is the interface defect state density and d is the IGZO thickness. Assuming N_b distribution is constant across the thickness of IGZO, Equation (4.4) can be simplified to [103], [178]:

$$D_S = N_b . d_s + N_{it} \qquad (4.5)$$

Note that these calculations assume N_b and N_{it} are independent of energy [179]. However, it can still be used for a comparative study and extracting an approximate DOS. To extract N_{it} from Equation (4.5), value of N_b is required which can be calculated from TFT data with different IGZO thickness. Figure 4.17 shows the transfer characteristics of standard TFTs with 30 nm and 50 nm IGZO thickness.

Using Equation (4.3), D_S values for both IGZO thicknesses is calculated with the values shows in Table 4-II. Using these values of D_S in Equation (4.5) and assuming N_{it} constant for both cases, N_B can be calculated. This assumption is reasonable because the IGZO channel material is deposited on the gate dielectric, which is same in both cases.

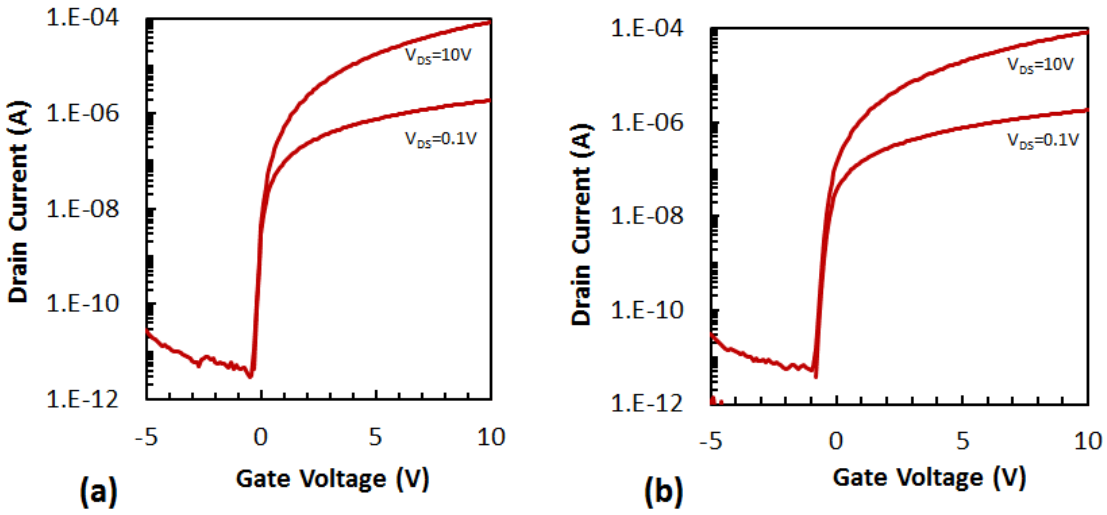

Figure 4.17: Transfer characteristics of TFTs with (a) 30 nm and (b) 50 nm thick IGZO channel.

Table 4-II: Density of sub-gap states calculated from SS values using Equation (4.3).

IGZO thickness (nm)	**SS *(mV/dec)***	D_s (cm^{-2})
30	100	1.5×10^{11}
50	120	2.2×10^{11}

The extracted value of $N_B = 3.5\times10^{16}$ cm^{-3} is used for extracting the interface defect density from Equation (4.5) for different dielectric. The value of N_b is assumed constant for each gate dielectric, which is a reasonable assumption as IGZO was deposited over the dielectric and therefore the bulk properties of IGZO should not be affected by different gate-dielectric deposition process. The threshold voltage shift between low and high drain (ΔV_{LH}) can be used to approximate the density of slow traps at the interface ($N_{tr.sl}$) using [69]:

$$N_{tr.sl} = \frac{\Delta V_{LH}}{q}.C_{OX} \qquad (4.6)$$

Table 4-III shows the *SS* and ΔV_{LH} values for various gate dielectric employed in this study. The density of the slow traps is extracted using Equation (4.6). The extracted density of states and slow traps are shown in Table 4-IV.

Table 4-III: Extracted parameters for various gate dielectrics used to calculate the interface trap density and amount of charge in slow traps.

Gate dielectric/interface	***SS (mV/dec)***	***ΔV_{LH} (V)***
PECVD SiO_2 (O)	120	0.0
Si_3N_4 (N)	250	0.4
Oxynitride (NO)	175	0.0
SiO_2/AlO_X (evaporated)	150	0.5
SiO_2/Al_2O_3 (ALD)	125	0.0

Table 4-IV: Interface defect density (N_{it}) and charge in slow traps ($N_{tr.sl}$) for different gate dielectric choices.

Gate dielectric/interface	***N_{it} (cm^{-2})***	***$N_{tr.sl}$ (cm^{-2})***
PECVD SiO_2 (O)	4.5×10^{10} *	NA
Si_3N_4 (N)	1.2×10^{12}	1.7×10^{11}
Oxynitride (NO)	6.7×10^{11}	NA
SiO_2/AlO_X (evaporated)	1.7×10^{11}	1.2×10^{11}
SiO_2/Al_2O_3 (ALD)	7.8×10^{10}	NA

**Note this method is not reliable for $N_{it} < 5\times10^{10}$ cm^{-2}.*

These calculations use some simplifications in terms of the defect density distribution in the channel region and therefore do not provide the exact distribution of density of states. In spite of the simplifications, these results are still insightful for a comparative study of different dielectric/IGZO interfaces. Nevertheless, the order of

magnitude of the states is consistent with TCAD simulation, which uses a more realistic distribution of the defect states in the band gap as discussed in Chapter 5.

4.5 BACK-CHANNEL PASSIVATION OF IGZO TFT

The exposed back-channel for bottom-gate TFTs promotes instability in device behavior due to the interaction with atmospheric conditions (e.g. oxygen, humidity) [108], [180]. The transfer characteristics of a standard TFT after a month of room ambient storage are shown in Figure 4.18. The characteristics shift left over time suggesting a more conductive channel due to absorption of moisture [180]. Therefore a passivation layer is required for device stability and process integration.

However, complexities in process integration and issues with device stability have been challenging to overcome [62], [108], [142], [180], [181]. The surface of IGZO is very sensitive to deposition conditions of passivation materials; the passivation process compromises the TFTs performance due to subjecting the IGZO back channel to exposure of some combination of vacuum, plasma, and elevated temperature [62], [142], [182]. In general additional oxygen vacancies are created which renders the IGZO conductive, and can be reversed by annealing in oxidizing ambient conditions [62], [142], [181]. In this section, investigation on silicon dioxide and aluminum oxide as materials for back-channel passivation is presented.

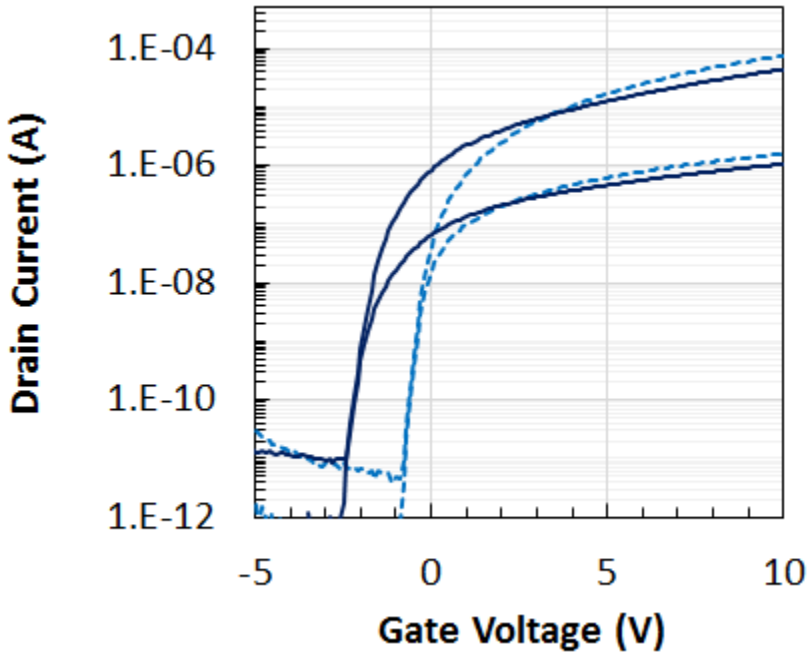

Figure 4.18: Transfer characteristics of standard unpassivated IGZO TFT tested a day after annealing (dotted) and after a month of storage in room-ambient (solid).

4.5.1 Process Integration

TFTs were fabricated using the baseline fabrication process for unpassivated devices as presented in Section 4.1.1. Silicon oxide was deposited using RF sputtering and PECVD. Alumina was deposited by e-beam evaporation and ALD. Contact openings through silicon oxide and ALD alumina were etched using an HF solution. E-beam evaporated alumina was patterned by lift-off resist process. The schematic cross-section of the fabricated device is shown in Figure 4.19.

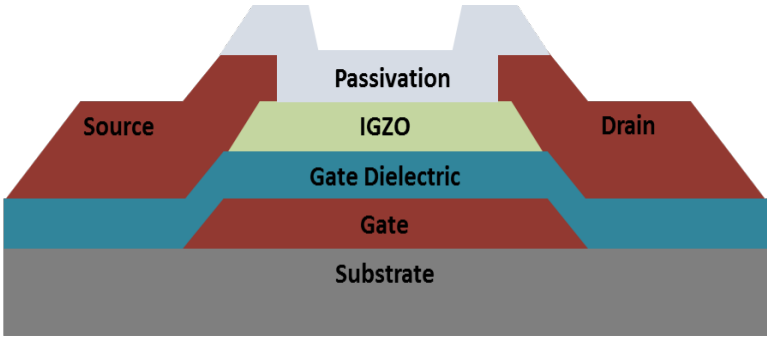

Figure 4.19: Cross-section schematic of a bottom-gate IGZO TFT with back-channel passivation material.

4.5.2 Aluminum Oxide Passivation

ALD alumina has been reported to provide good passivation for oxide semiconductor TFTs [26], [142], [197]. Alumina was deposited using TFS 500 Beneq system with trimethylaluminum (TMA) and water as precursors at 200 °C. After deposition of alumina, "standard" working devices did not show any gate modulation due to a low resistivity value of ρ~0.003 Ω·cm of channel, Figure 4.22a. The conductivity of the IGZO channel is increased during ALD which is performed at 200 °C in vacuum. It has been shown previously that IGZO films annealed in vacuum exhibit higher conductivity due to the creation of V_O [97]. Also water, used as a precursor, could also contribute to the increased conductivity as it has been reported to behave as a donor in IGZO [121], [142], [180]. Regardless of the mechanism of enhanced conductivity, it was irreversible even with the aggressive anneal treatment (4 h in O_2 at 400 °C) because of the high integrity of the thin ALD alumina layer. Due to their excellent properties as a barrier to oxidants, ALD alumina films were later used for encapsulation of final devices, see Section 7.3.1.

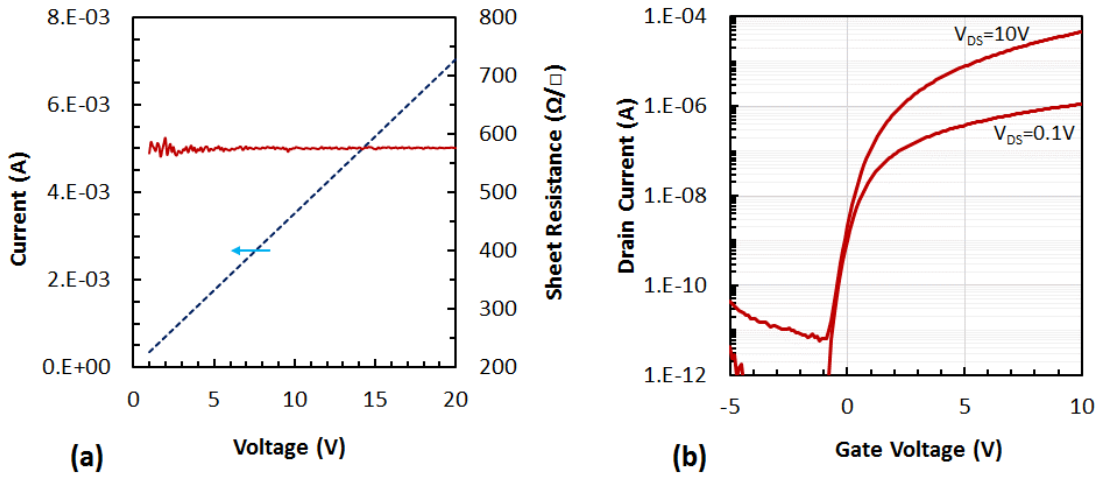

Figure 4.20: (a) Sheet resistance (solid line) of IGZO after ALD alumina passivation (b) Transfer characteristics of evaporated alumina passivated TFTs. Both measurements were taken after a 30 min anneal at 400 °C in air ambient.

Evaporated alumina has been used for passivation of IGZO TFTs [159]. E-beam evaporation of alumina was investigated for the passivation of IGZO TFTs. The device showed poor characteristics after the passivation material deposition. The TFTs showed improvement after an anneal at 400 °C for 30 min in air ambient. The transfer characteristics of annealed TFT are shown in Figure 4.20b.

While TFTs with passivation material offer improvements in stability and resistance to aging, they often have an increased sensitivity to back-channel defects that is not apparent on TFTs without passivation material. Exposure of an unprotected back-channel to chemicals involved in lithographic patterning and contact metallization may compromise device performance, thus process activity before application of back-channel protection should be avoided.

A two-step passivation method has been employed to address the effects of process-induced surface degradation. Annealing conditions have been modified to account for observed differences in oxidant transport. In the original process#1 the passivation material (option for standard devices) has been deposited at the end of fabrication, while in the modified two-step process#2 a thin 20 nm layer of alumina is deposited after IGZO sputtering to protect the back-channel surface, with a thicker 80 nm application at the end of fabrication.

Process#2 devices exhibit better μ_{sat} and *SS* values compared to devices fabricated using process#1 (compare Figure 4.20b and Figure 4.21). This improvement is attributed to a superior back-channel condition due to protection from chemical or physical exposure during processing. The subthreshold performance is comparable to unpassivated devices. While the channel mobility was lower than the unpassivated devices, this result may be due, in part, to process variation of physical parameters. To determine the influence of aging, passivated devices stored for more than six months in room ambient were tested, with a near-perfect overlay shown in Figure 4.21. A variant of process#2 that investigated the influence of an intermediate anneal following the 20 nm AlO_X application produced inferior results and was not pursued further.

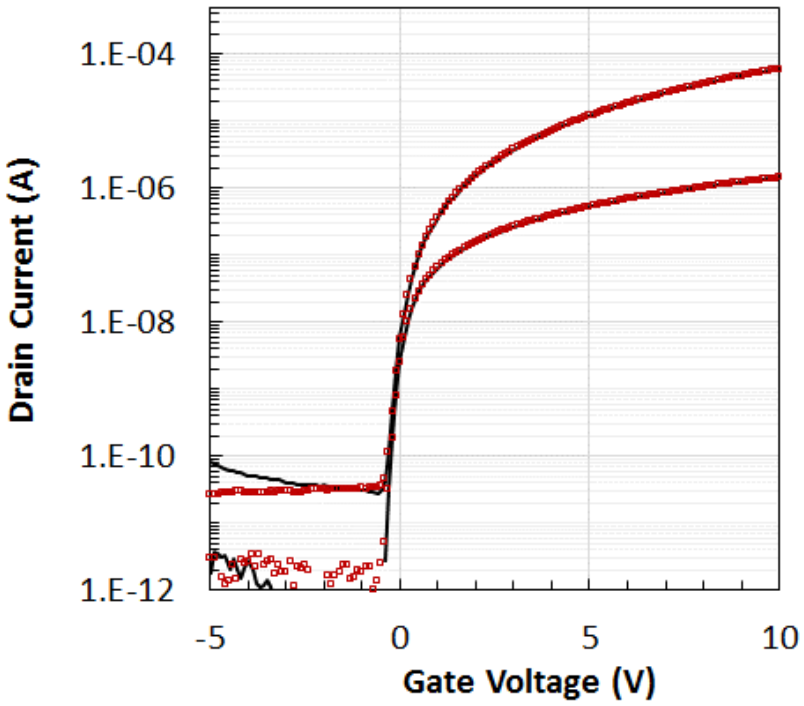

Figure 4.21: Process#2 device with 100 nm evaporated alumina (combined 20 nm + 80 nm), solid line. A comparison of I-V characteristics taken over six months of aging (square) demonstrates near-perfect overlay. Differences in the off-state leakage are attributed to voltage sweep conditions.

Though the I_D-V_{GS} characteristics of process#2 AlO_X passivated devices look very promising, further processing on these devices at $T > 150$ °C shifted the transistor characteristics. This is attributed to the inferior quality of e-beam evaporated AlO_X films, which ironically enabled the anneal to adjust the IGZO electronic properties. Therefore, further attempts were focused on establishing a process for SiO_2 passivated IGZO transistors.

4.5.3 Silicon Oxide Passivation

Silicon oxide deposited using sputter, evaporation and PECVD was investigated for the passivation of IGZO TFT back-channel. A 100 nm quartz film was sputtered on a working

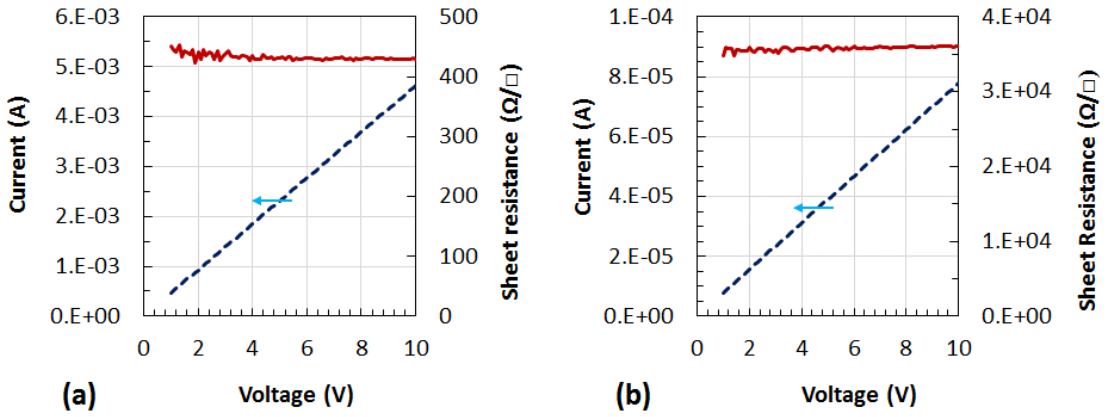

Figure 4.22: Sheet resistance of IGZO film after (a) sputter deposition of quartz and (b) e-beam evaporation of quartz. Sheet resistance values (solid line) are plotted on y2-axis. The sputter process made IGZO highly conductive.

TFT which made IGZO channel extremely conductive. The sheet resistance measured on the Van der Pauw structure is shown in Figure 4.22(a). Plasma exposure of IGZO film created defect states in IGZO channel which increased the conductivity of the films [112], [183]. E beam evaporated quartz also decreased the resistivity of channel, Figure 4.22b.

Silicon dioxide, deposited using AMAT P5000 plasma enhanced chemical vapor deposition (PECVD) tool at 390 °C using tetraethyl orthosilicate (TEOS) precursor, was investigated for IGZO TFT passivation. After a 100 nm PECVD SiO_2 deposition, a typical "standard" unpassivated device showed no gate control due to low resistivity of the channel. Figure 4.23 shows the I_D-V_{GS} characteristics along with the sheet resistance measured using 4 pt. probe analysis. The resistivity values of the IGZO film is very low which explains the absence of any channel charge modulation by the gate. PECVD is a plasma process and exposing the IGZO back-channel to the plasma creates a high degree of defect states in the IGZO channel and interface, thereby increasing the conductivity of the IGZO film [109], [183]. Passivation using PECVD deposited SiO_2 rendered the IGZO

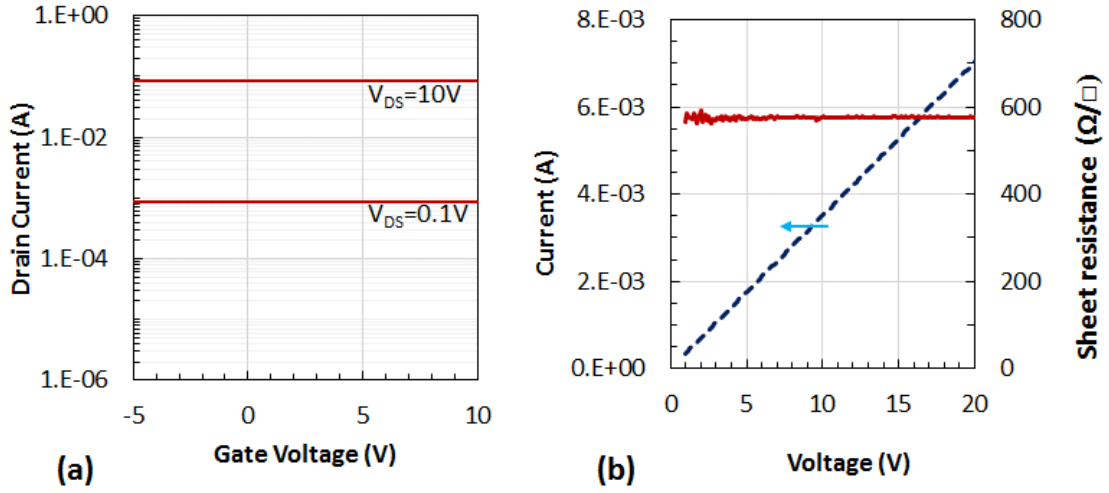

Figure 4.23: (a) Transfer characteristics of PECVD SiO_2 passivated IGZO TFT. The devices did not show any gate modulation and could not be turned off due to very high conductivity of the channel. (b) Sheet resistance (dashed line) measurement on the Van der Pauw structure.

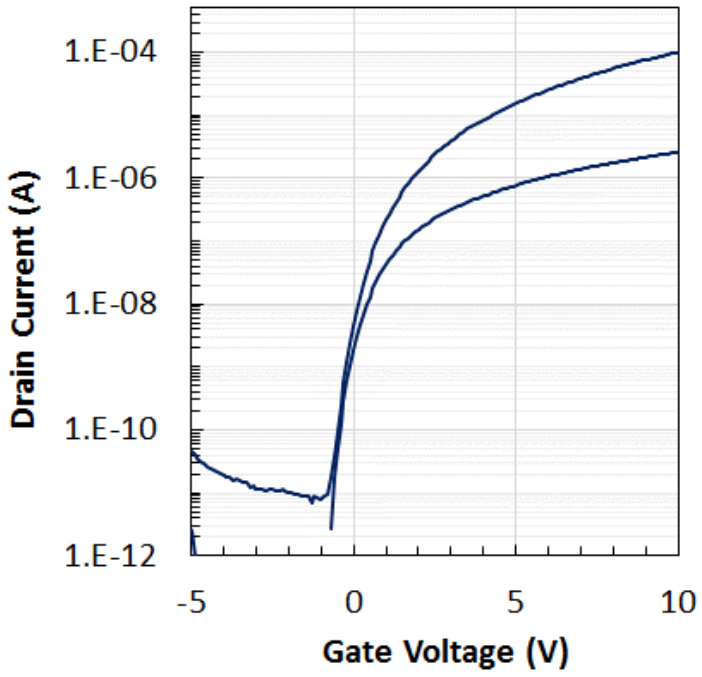

Figure 4.24: Transfer characteristics of PECVD SiO_2 passivated TFT. An aggressive anneal was required for PECVD SiO_2 passivated devices.

channel very conductive (ρ = 0.003 Ω·cm). The devices did not exhibit any gate control after the 30 min 400 °C anneal established for AlO_X passivation. This suggests that the 30 min anneal is not sufficient to reduce the V_O. A longer 4 h anneal in O_2 ambient at 400 °C produced working TFTs with characteristics shown in Figure 4.24.

4.6 CONCLUSION

The details of various annealing processes on Al-contact and Mo-contact IGZO TFTs have been presented. The annealing ambient and arrangement of process steps were found to have a significant influence on the contact behavior and electrical characteristics of TFTs. Pre-metal annealing in air ambient resulted in similar I_D-V_{GS} characteristics on Mo-contact and Al-contact devices. A post-metal anneal for Mo-contact devices resulted in higher on-state current and steeper subthreshold slope, whereas the Al-contact devices experienced severe degradation suggesting the formation of an AlO_X interface layer. While simulations suggest that Mo-contact to IGZO should result in a potential barrier, actual Mo-contacts demonstrated low resistance ohmic behavior, most likely due to M-S interface states that help facilitate carrier injection.

Mo-contact TFTs with post-metal anneal treatments typically demonstrated performance improvements over pre-metal anneal treatments. However, certain treatment combinations, such as annealing in air at 400 °C, resulted in degraded characteristics. These results suggest that there is an optimum degree of oxidant exposure that may be realized by the right combination of time and temperature, thus resulting in a low concentration of defect states. Annealing in an inert ambient at 400 °C followed by a ramp-down in air demonstrated improvements in both on-state and off-state performance. The

role of the oxidizing ambient ramp down was found to be crucial for yielding such high quality IGZO transistors. The lack of oxidizing ambient during annealing renders the IGZO too conductive to be used as a channel layer material for TFT applications; attributed to the level of oxygen vacancies.

Standard unpassivated TFTs became extremely conductive after application of passivation material (see Table 3-III), thus an anneal-last process integration strategy was necessary. ALD alumina was incompatible with an oxidizing ambient anneal to establish the semiconducting properties of IGZO. Passivated TFTs with evaporated AlO_X resulted in transfer characteristics with slight degradation in *SS* and μ_{sat} compared to unpassivated devices. The two-step alumina passivation process resulted in high performance passivated TFT characteristics, with a notable reduction in interface trap density to $N_{IT} \sim 10^{11}\,cm^{-2}$. Alumina passivated devices showed good transfer characteristics however subsequent processing demonstrated instability. A preferred process using PECVD SiO_2 back-channel passivation with adjusted annealing conditions demonstrated improved stability with only slight compromise in subthreshold performance. This result became the foundation for further study in alternative passivation schemes and device configurations as will be discussed in subsequent chapters.

Chapter 5. IGZO MATERIAL MODELING FOR TCAD SIMULATION

IGZO exhibits n-type conductivity due to the presence of defects *viz.* oxygen vacancies (V_O). The process variables may contribute to the defect levels and degrade the transistor characteristics; therefore, it is important to understand the influence of these defects on the device operation. Device simulation captures the influence of each variable on the transistor operation independently. Furthermore, it allows visualization of various physical effects such as the potential distribution in the TFT channel region and defect state occupancy, which assists in understanding the underlying physics of defect mechanisms.

There has been a significant amount of work published on the extraction of defect state parameters by applying analytical solutions to measured *C-V* and *I-V* characteristics on TFT structures [184]–[186]. While this may lead to a reasonable match between measured and simulated *I-V* and *C-V* characteristics, these techniques are limited in the allowable degrees of freedom. Typically, such models do not differentiate between bulk-film defects and interface defects (e.g. fixed charge, interface traps) which may dominate non-ideal behavior [185], [187], [188]. Analytical solutions are mathematically very complex and require several assumptions and simplifications to reach to a closed form solution, which is not required for TCAD simulation.

In this chapter, the correlation between *I-V* and *C-V* measurements taken on TFTs and interdigitated capacitors (IDCs) respectively is presented. The IGZO material model is presented, with details on the density of states (DOS) distribution within the energy band

gap. The Silvaco® Atlas™ TCAD device simulator has been used for simulation. The bulk defect material model is refined using the *I-V* and *C-V* characteristics of unpassivated devices, with further modification and the inclusion of interface states needed to represent the operation of passivated TFTs due to the existence of back-channel defects as discussed in Section 4.5.

Amorphous materials have a high density of sub-gap states due to incomplete bonding, random arrangements of atoms and variations in bonding angle [12]. The Atlas TFT module allows the energy distribution of states to be defined, which is essential for accurate simulation of disordered material systems such as IGZO. Amorphous semiconductor trap states can be donor-like or acceptor-like, and are described by exponentially decaying band-tail states, and deep states following a Gaussian distribution. The following four functions serve as the mathematical definition of the trapping mechanisms in a disordered channel film for a TFT. For the numerical analysis in ATLAS, these densities of states are defined as [189]:

$$g_{TA}(E) = N_{TA} \exp\left(\frac{E - E_c}{W_{TA}}\right) \tag{5.1}$$

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_v - E}{W_{TD}}\right) \tag{5.2}$$

$$g_{GA}(E) = N_{GA}\, exp\left[-\left(\frac{E_{GA} - E}{W_{GA}}\right)^2\right] \tag{5.3}$$

$$g_{GD}(E) = N_{GD}\, exp\left[-\left(\frac{E - E_{GD}}{W_{GD}}\right)^2\right] \tag{5.4}$$

- $g_{TA}(E)$ and $g_{TD}(E)$ represent the density of acceptor-like conduction band-tail states and donor-like valence band-tail states, respectively
- E_c and E_v are energy levels at the conduction band (CB) and valance band edge (VB)
- N_{TA} (N_{TD}) is the density of acceptor-like (donor-like) states in the tail distribution at the conduction band (valence band) edge
- W_{TA} (W_{TD}) is the characteristic decay energy of conduction (valance) band-tail states
- $g_{GA}(E)$ and $g_{GD}(E)$ represent the density of acceptor-like and donor-like states (oxygen-vacancies, V_O)
- N_{GA} (N_{GD}) is the peak value for acceptor-like (donor-like) states, defining a Gaussian distribution
- E_{GA} (E_{GD}) is the mean energy defining a Gaussian distribution for acceptor-like (donor-like) states
- W_{GD} (W_{GD}) is the standard deviation of Gaussian distribution for acceptor-like (donor-like) states.

Once the DOS is defined using Equations (5.1)-(5.4), the density of ionized acceptor and donor-like states is given by [189]:

$$p_T = \int_{E_v}^{E_c} g_{TA}(E) \cdot f_{TA}(E,n,p)dE + \int_{E_v}^{E_c} g_{GA}(E) \cdot f_{GA}(E,n,p)dE \qquad (5.5)$$

$$n_T = \int_{E_v}^{E_c} g_{TD}(E) \cdot f_{TD}(E,n,p)dE + \int_{E_v}^{E_c} g_{GD}(E) \cdot f_{GD}(E,n,p)dE \quad (5.6)$$

where $f_{TA}(E,n,p)$ and $f_{GA}(E,n,p)$ are the ionization probabilities for the tail & Gaussian acceptor states and $f_{TD}(E,n,p)$and $f_{GD}(E,n,p)$ are the ionization probabilities for the donor states.

The above equations for ionized trap states consider a continuous distribution of defect states. When using discrete energy levels, the integral terms are replaced by summations over the number of discrete energy levels, defined by *NUMA* and *NUMD* for acceptor and donor states respectively.

$$p_T = \sum_{i=0}^{NUMA} \left(f_{TA}(E_i,n,p) \cdot \int_{-\infty}^{+\infty} g_{TA}(E)dE + f_{GA}(E_i,n,p) \cdot \int_{-\infty}^{+\infty} g_{GA}(E)\,dE \right) \quad (5.7)$$

$$n_T = \sum_{i=0}^{NUMD} \left(f_{TD}(E,n,p) \cdot \int_{-\infty}^{+\infty} g_{TD}(E)dE + f_{GD}(E,n,p) \cdot \int_{-\infty}^{+\infty} g_{GD}(E)dE \right) \quad (5.8)$$

The default model parameters used in Atlas for IGZO material are given in Table 5-I. The difference between the continuous and discrete trap state distribution is shown in Figure 5.1, using the parameters from Table 5-I.

Table 5-I: Model parameters used for IGZO material. The notation in brackets is used to be consistent with the earlier notations used e.g. V_O for oxygen vacancies.

Symbol	Value
Band gap	3.05 eV
Electron affinity	4.16 eV
Relative permittivity	10
Intrinsic Electron mobility	15.0 $cm^2/V \cdot s$
V_O (Gaussian)	
N_{GD} (N_{Vo})	6.5×10^{16} $cm^{-3}eV^{-1}$
E_{GD} (E_{Vo})	2.9 eV
W_{GD} (W_{Vo})	0.1 eV
Band-Tail States	
N_{TA} (CB_{TN})	1.55×10^{20} $cm^{-3}eV^{-1}$
W_{TA} (CB_{WN})	0.013 eV
N_{TD} (VB_{TP})	1.55×10^{20} $cm^{-3}eV^{-1}$
W_{TD} (VB_{WP})	0.12 eV

For solutions with a continuous distribution of defect states, Atlas defaults to mathematical interpolation, and thus defects defined by a discrete trap states distribution is preferred. Optimized settings of 128 and 64 levels for acceptor and donor states, respectively, were implemented which balanced the tradeoff between accuracy and simulation run-time [148]. The increased accuracy in using a discrete DOS distribution compared to a continuous distribution is shown in Figure 5.1; most evident in the comparison of Gaussian distributed states. Increasing the number of these levels to 512 drastically increased the simulation run-time by a factor of twenty (*e.g.* 3 hour vs. 10 min) with a negligible difference in simulation results.

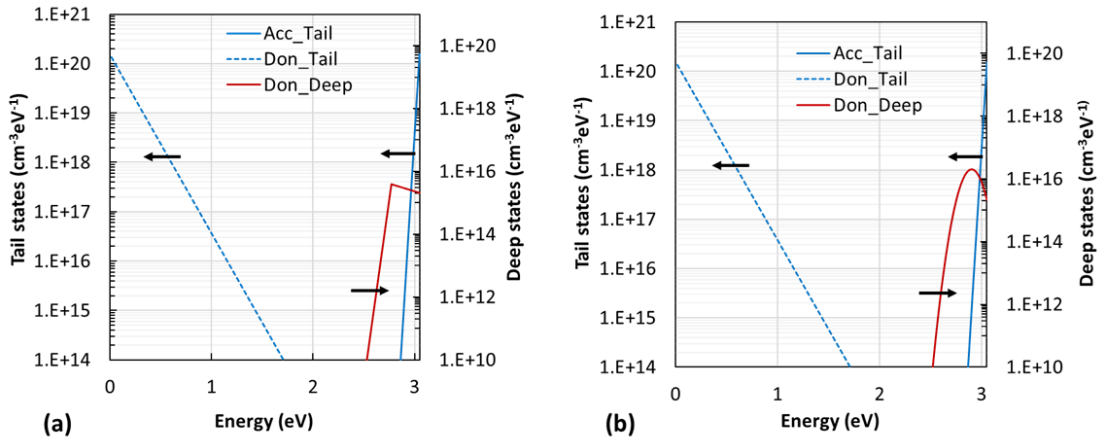

Figure 5.1: Density of states (DOS) distribution in the energy gap of IGZO in Atlas simulation. (a) By default a continuous distribution of states is used which solves Equations (5.5) and (5.6) for optimizing the run-time but loses accuracy. (b) Defining discrete levels gives user control over the trade-off in run-time and accuracy.

Additional material model parameters were defined to represent electrical properties. A constant-mobility model was used which is taken to be independent of doping concentration, carrier densities and electric field. The Schottky contact model was used to define the effective contact potential between the contact metal and IGZO. Regarding carrier statistics, the Fermi-Dirac model was implemented to account for degenerate semiconductor behavior [148].

5.1 DEVICE SIMULATION

The default defect distribution in IGZO material is shown in Figure 5.1b. Acceptor-like and donor-like tail states are defined using exponential distribution, plotted on *y1*-axis. V_O are represented by Gaussian like distribution of donor states near the CB (*y2*-axis). Figure 5.2 shows a representation of defect states in the IGZO energy band gap. The band-tail states extend from VB and CB while V_O is represented by the Gaussian distribution very

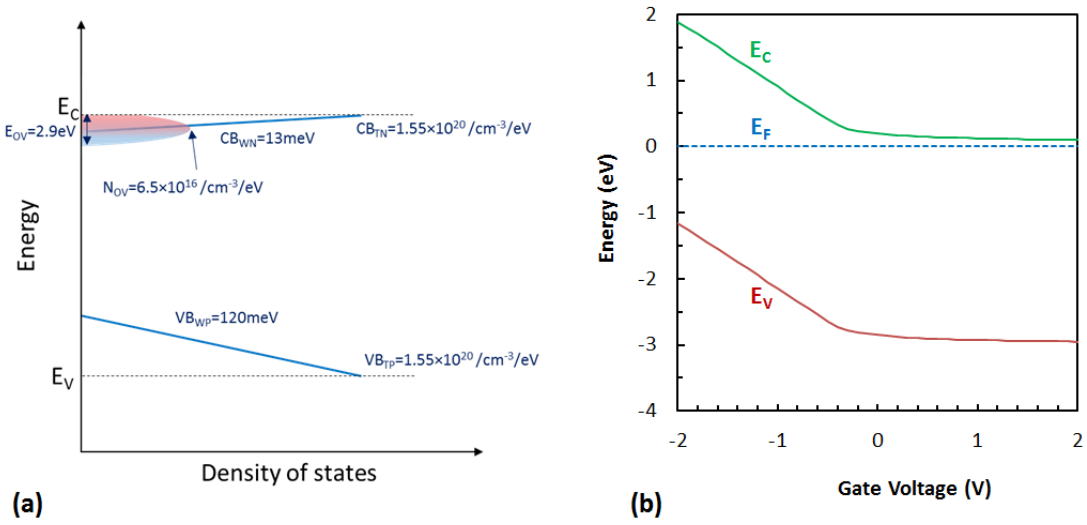

Figure 5.2: (a) Schematic representation of defect distribution in IGZO material. (b) Simulated location of E_F, with respect to E_C and E_V, as a function of gate voltage.

close to the CB. Figure 5.2b shows the Fermi level (E_F) location, with respect to E_C and Ev, as a function of gate voltage (V_{GS}); details of device structure to follow.

5.1.1 Simulation Structure

The TCAD structure film thicknesses are consistent with actual fabricated device describes in Section 4.1.1. The device structure and mesh configuration used for simulation are shown in Figure 5.3, with modifications in source/drain regions (*e.g.* contact dimensions, gate overlap) that enabled reasonable simulation time without compromise in simulation accuracy. The gate and S/D overlap of 1 µm is used. In fabricated TFTs this overlap is 4 µm, however, decreasing it to 1 µm did not change the simulation results. Therefore an overlap of 1 µm is used to reduce the simulation time. A channel length of *L*=3 µm is used

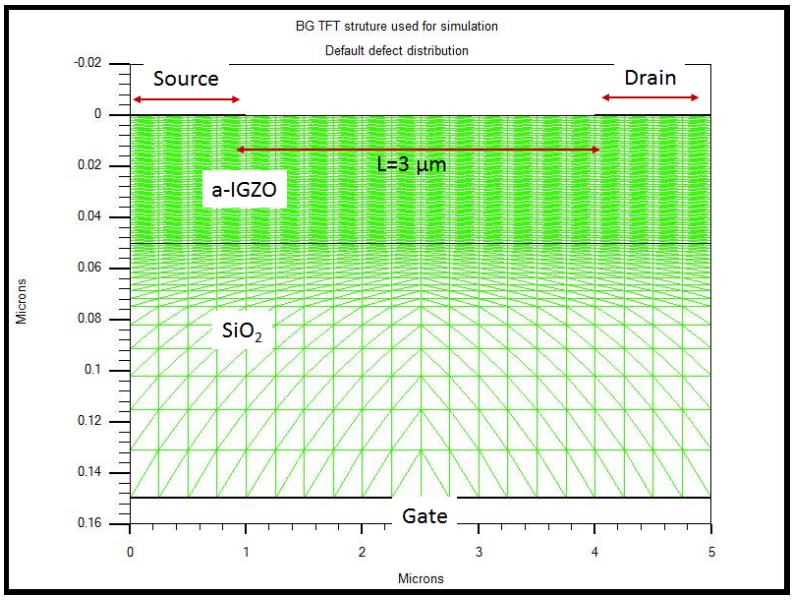

Figure 5.3: Cross-section of BG TFT structure showing the mesh used for simulation. Finer mesh is used in IGZO channel and at IGZO/SiO_2 interface for improved accuracy. The channel length is 3 µm. The gate and S/D overlap is 1 µm.

for explaining the structure and model parameters effect as it reduces the computing time. Molybdenum was used as the gate metal defined by the work function (ϕ_{Mo} = 4.53 eV). For S/D contact regions the metal work function was set to ϕ_M = 4.13 eV (ϕ_M of aluminum) to accurately represent the true M-S contact which is dominated by interface states and demonstrates ohmic behavior, explained in detail in Section 4.2.

The electron concentration across the IGZO channel, for the default defect distribution, is shown in Figure 5.4 for zero bias condition. Due to difference in metal work-function, the IGZO regions below S/D show accumulation of electrons near the contacts. The Mo gate electrode creates slight depletion region towards the IGZO/SiO_2 interface for the same reason. The electron concentration in the bulk IGZO is around

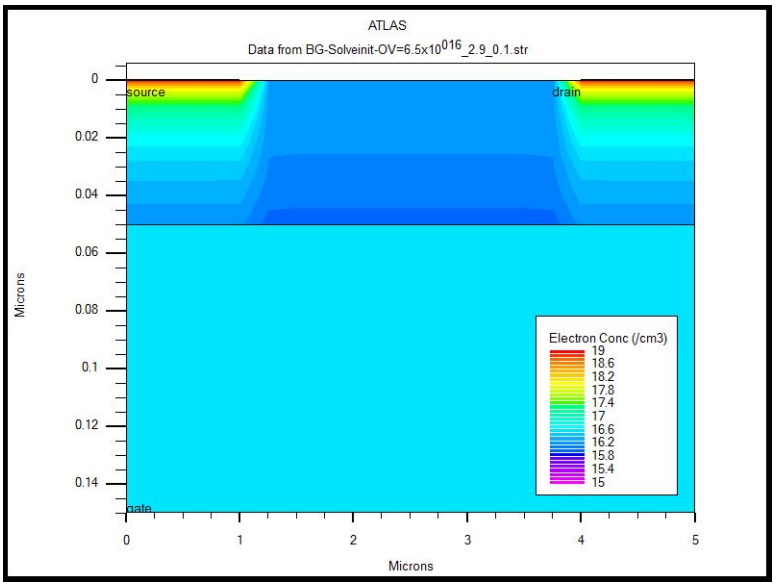

Figure 5.4: Electron concentration contours in IGZO channel for zero bias condition. The default defect distribution is used. Higher electron density near the S/D metal (aluminum) is due to the M-S workfunction difference.

6.5×10^{16} cm^{-3} as defined by the V_O. The extracted interface trap density from subthreshold swing was less than 5×10^{10} cm^{-2}, see Section 4.4.3, which is practically negligible. Therefore the IGZO/SiO_2 gate dielectric interface is treated to be free from any fixed charge or interface traps.

5.1.2 Electrical Results

The simulated I_D-V_{GS} characteristics of the device structure shown in Figure 5.3 are shown in Figure 5.5. The electrical results show transistor operation with steep *SS* and a negative turn-on voltage. Figure 5.6 shows the current density at V_{GS} =10 V and V_{DS} =0.1 V near the drain electrode. It can be seen that majority of the current flow near the IGZO/SiO_2 interface. In addition, the current flow extends only to 0.3 µm below the drain current, which validates the reduction in gate to S/D overlay from 4 µm to 1 µm.

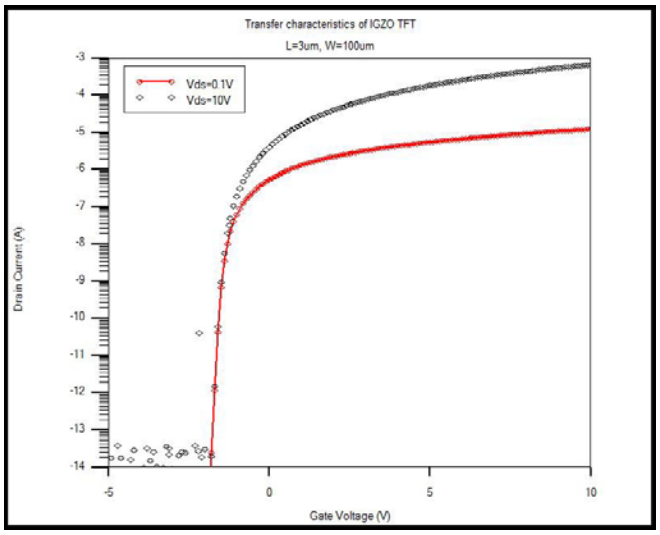

Figure 5.5: Simulated transfer characteristics of IGZO TFT using the default material model. (L=3 µm and W=100 µm)

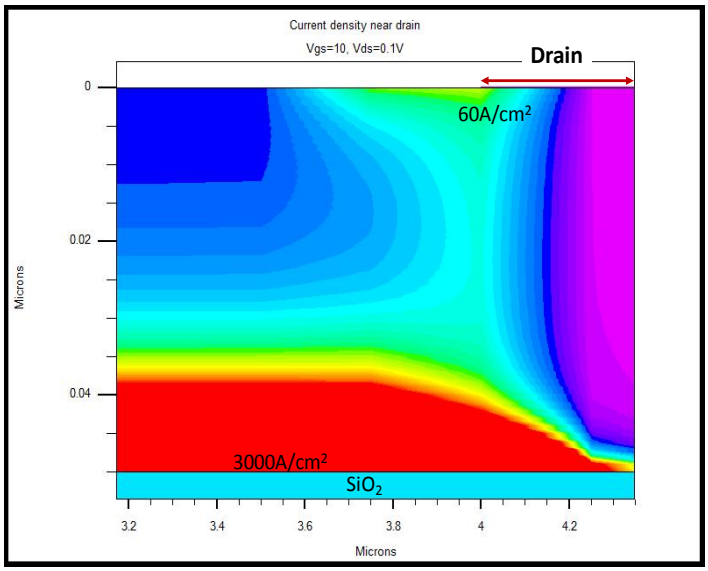

Figure 5.6: Current density in IGZO channel region near drain, at V_{GS}=10 V and V_{DS}=0.1 V. Majority of the current flows near the IGZO/SiO_2 interface. The current flow extends to ~0.3 µm below the drain electrode. (L=3 µm and W=100 µm)

5.2 ROLE OF MATERIAL MODEL PARAMETERS

This section discusses the influence of defect state parameters on transistor operation. Transfer characteristics of simulated TFTs using the default IGZO material model are presented.

5.2.1 Oxygen Vacancies (V_O)

The V_O are treated as donor-like states placed very close to the conduction band. They are defined by three parameters, N_{Vo} represents the peak of V_O, E_{Vo} defines the average energy of these vacancies measured from E_V and W_{Vo} represents the width of the Gaussian distribution of V_O. Changing the density of V_O (N_{Vo}), while keeping all other parameters constant, causes a left shift in I-V characteristics, as shown in Figure 5.7. V_O in essence act as donor ions in IGZO. Increasing N_{Vo} makes IGZO lose its semiconductor properties and behave more like a metal. The TFT performance is extremely sensitive to the N_{Vo} values; for $N_{Vo} > 1\times10^{18}$ $cm^{-3}eV^{-1}$, a complete loss of gate control over the channel is observed. Such behavior was observed experimentally for unpassivated devices annealed in absence of oxidizing ambient (*i.e.* N_2 or vacuum); see Section 4.3.2.

The effect of the energy distribution of V_O is shown in Figure 5.8. As the mean energy of V_O (E_{Vo}) moves away from the CB (*i.e.* $E_{Vo} < 2.9$ eV), the device characteristics show distortion in the subthreshold regime. This distortion disappears for $E_{Vo} < 2.2$ eV. The characteristics are shifted towards higher threshold voltage, and lose dependence on the E_{Vo} value. This can be explained based on the ionization of V_O with V_{GS} as shown in Figure 5.9. For the default material model ($E_{Vo} = 2.9$ eV), the E_F lies at 0.16 eV below E_C. At this point the V_O (0.15 eV below *Ec*) are ionized. With the increase in V_{GS}, E_F moves

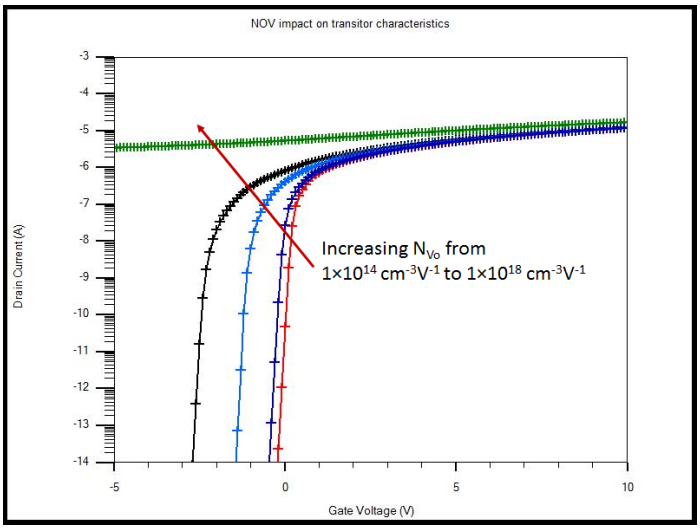

Figure 5.7: Influence of N_{Vo} on the transfer characteristics of IGZO TFTs (V_{DS} = 0.1 V). A parallel shift in characteristics is seen with no appreciable change in current drive when N_{Vo} was varied from 1×10^{14} cm^{-3}eV^{-1} to 1×10^{16} cm^{-3}eV^{-1}. For N_{Vo} > 1×10^{18} cm^{-3}eV^{-1} a complete loss in gate control is observed. (L=3 µm and W=100 µm)

closer to the E_C and these states start trapping electrons. For E_{Vo} =2.9 eV, this occurs in the device on-state (V_{GS} = -0.5 V) and the influence of this trapping is minimal in the device characteristics. The channel region is in accumulation mode and the trapping causes only an order of magnitude reduction in donor state. When the position of these V_O is changed, such as to E_{Vo} = 2.5 eV, the E_F crosses over the V_O during the subthreshold region (V_{GS} = 0 V). The trapping of electrons by the donor type V_O causes a noticeable decrease in effective electron concentration and therefore results in a distortion in the subthreshold region. The resultant doping decreases by eight orders of magnitude. For E_{Vo} = 2.0 eV, the donor states are already filled with electrons in the off-state which reduces the net electron concentration in the channel. This decrease in effective doping leads to a shift of E_F away from E_C and therefore a positive shift in the transfer characteristics is observed. So depending on the location of V_O in the band gap, they can act either as

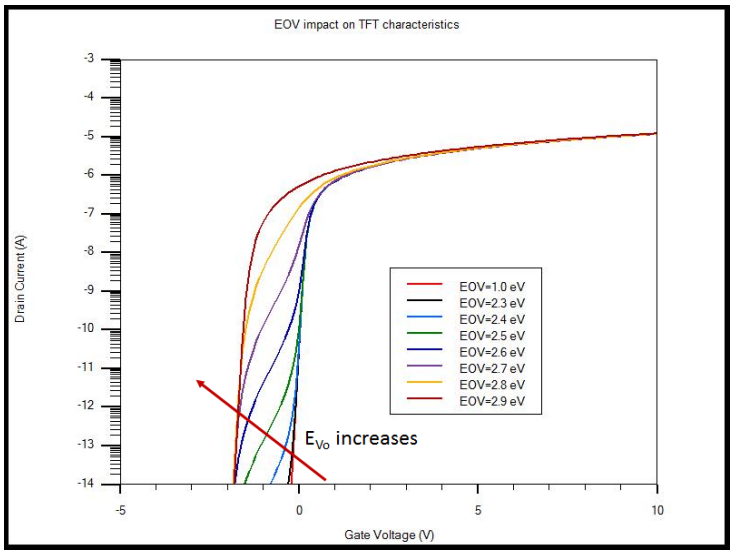

Figure 5.8: Influence of E_{Vo} on the transfer characteristics of IGZO TFT (V_{DS} = 0.1 V). As the location of V_O moves away from Ec, the characteristics show distortions. (L=3 µm and W=100 µm)

electron donor or as trapping sites. The V_O can be regulated by the thermal anneal process [190].

5.2.2 Band-Tail States

Band-tail states are defined using a peak density (CB_{TN}) of 1.55×10^{20} $cm^{-3}eV^{-1}$ at the CB edge and a slope (CB_{TW}) of 0.1 eV. The effect of changing the CB_{TN} is shown in Figure 5.10. When the V_{GS} increases, the E_F moves closer to the E_C and the acceptor like tail states start filling by trapping the accumulated electrons. This results in a lower level of accumulation charge and a lower transconductance (g_m) until the electron traps are full, and is responsible for the concave-up transfer characteristic as shown in the inset. This kind of behavior is characteristics of amorphous semiconductor materials which makes the

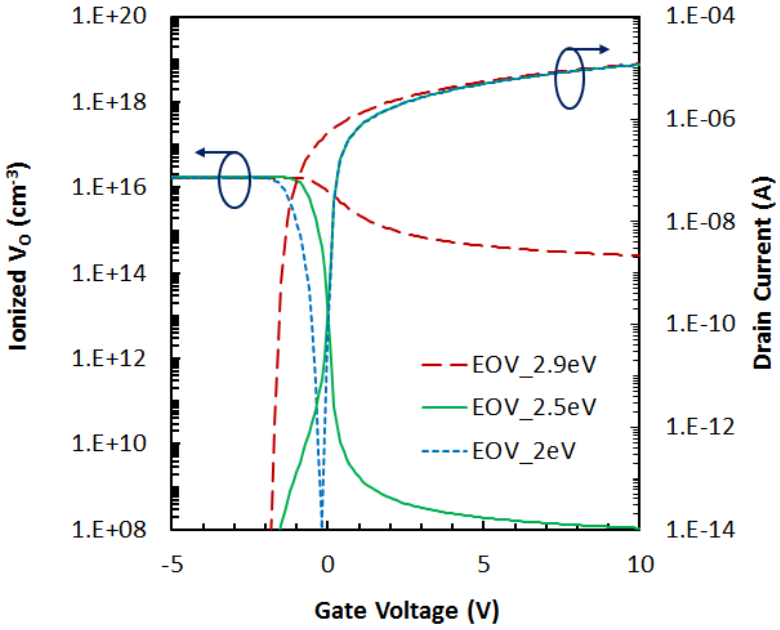

Figure 5.9: Ionized V_O (y1-axis) plotted against V_{GS} at V_{DS}=0.1 V. As V_{GS} increases, the E_F moves closer to E_C, filling more V_O and thereby reducing the density of ionized V_O. When E_F crosses E_{Vo}, V_O start behaving like electron traps. If the trapping occurs in the subthreshold region, it manifests itself as a distortion in the transfer characteristics (e.g. for E_{Vo} =2.5 eV, y2-axis). (L=3 µm and W=100 µm)

conventional device modeling and parameter extraction procedures inapplicable [163], [191]. A complete discussion on this is provided in Chapter 6.

The influence of CB_{TW} on device performance is shown in Figure 5.11. The on-state current drive decreases with increasing the slope of tail states. The total density of acceptor like traps increases by increasing the slope of the tail states. Therefore more electrons are trapped which causes a decrease in current. The transition from subthreshold to on-state also suffers. This is because the gate accumulated electrons start trapping in the tail states at lower V_{GS}. This leads to an effective drop of accumulation charge earlier.

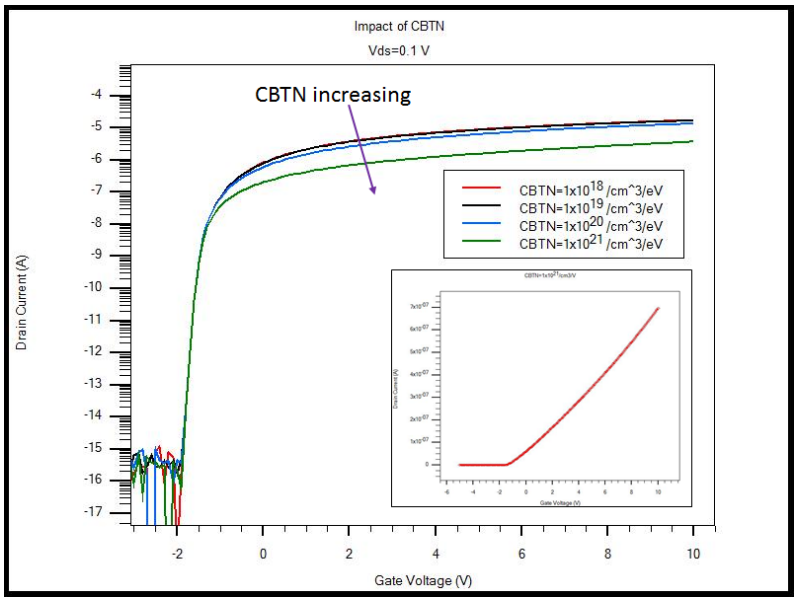

Figure 5.10: Influence of CB_{TN} on the transfer characteristics of IGZO TFT (V_{DS} = 0.1 V). As the tail states density increases, more electrons are trapped and the on-state current lowers. This causes a concave-upwards curvature in drain current as shown in the inset for CB_{TN} =1×10^{21} cm^{-3}eV^{-1}. (L=3 µm and W=100 µm)

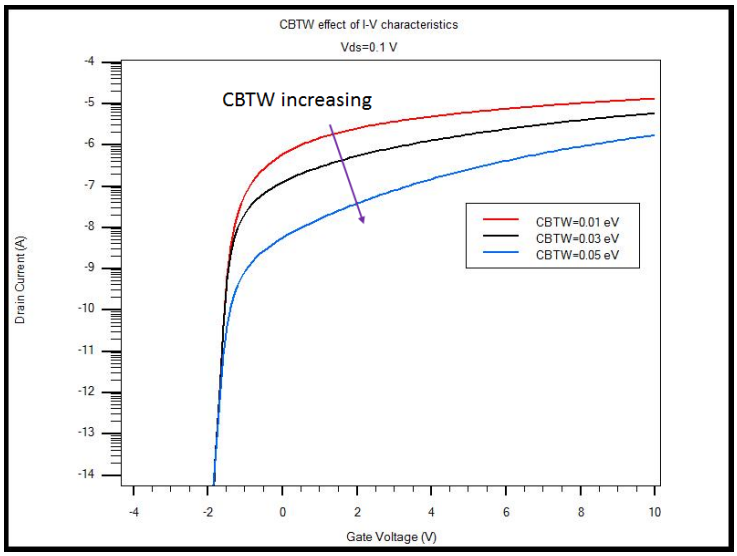

Figure 5.11: Influence of CB_{TW} on the transfer characteristics of IGZO TFTs. As CB_{TW} increases, the on-state current level drops. (L=3 µm and W=100 µm)

The donor-like band-tail states are located near the valence band. The donor-states are neutral when filled. Since the E_F is far from these states and does not cross these states in the on state, therefore the charge state of these defects does not change. For this reason, any change in these states is not reflected in the transistor operation. However, in amorphous materials tail states are present, near the conduction and valence band, due to the variation in bond angle. These states may play some role during bias stress measurements [101].

5.3 INTERDIGITATED CAPACITORS

The interpretation of non-ideal current-voltage (*I-V*) characteristics is not always unambiguous due to issues that may be related to carrier injection. Capacitance-voltage (*C-V*) analysis provides complementary information that is valuable in separating the influence of material and interface defects from other factors that influence transistor operation.

5.3.1 Challenges with 2D C-V Analysis

Performing *C-V* analysis on thin-film devices is a 2D problem, and the interpretation is not as straightforward as the 1-D case (*i.e.* bulk semiconductor). While *C-V* analysis can be done directly on TFTs [143], [184], [192], interdigitated capacitors (IDCs) can be designed to be representative of the actual TFT structure. Furthermore, the capacitance value for a typical TFT is very low (<1 pF) and therefore is prone to measurement errors and requires additional instrumentation [143]. Large area IDCs may be fabricated to circumvent this issue while still representing the actual TFT channel area.

5.3.2 IDC: Design & Fabrication

A testchip was designed which included both TFT and IDC devices. The IDC was designed to be consistent with the TFT structure considering process exposure to the back-channel region, and overlap regions between the bottom-gate and top-contact (source/drain) electrodes. The IDC layout is shown in Figure 5.12. The design layers insure that, regardless of process options, the gated areas in IDCs receive the same process treatment as the TFT channel region. The structure has 12 interdigitated gate fingers extending across the IGZO mesa. Each gated region has a width of 44 µm, and 5 µm side overlaps between the top-contact metal and the bottom-gate metal. The total gated area is ~ 0.002 cm^2.

High-frequency C-V characteristics were measured on IDCs using a Materials Development Corporation (MDC) system with an HP 4284A precision LCR meter, taken in slow-sweep mode (-10 V to 10 V sweep in ~ 7 min) with V_{ac} = 50 mV peak-peak at f = 1 MHz.

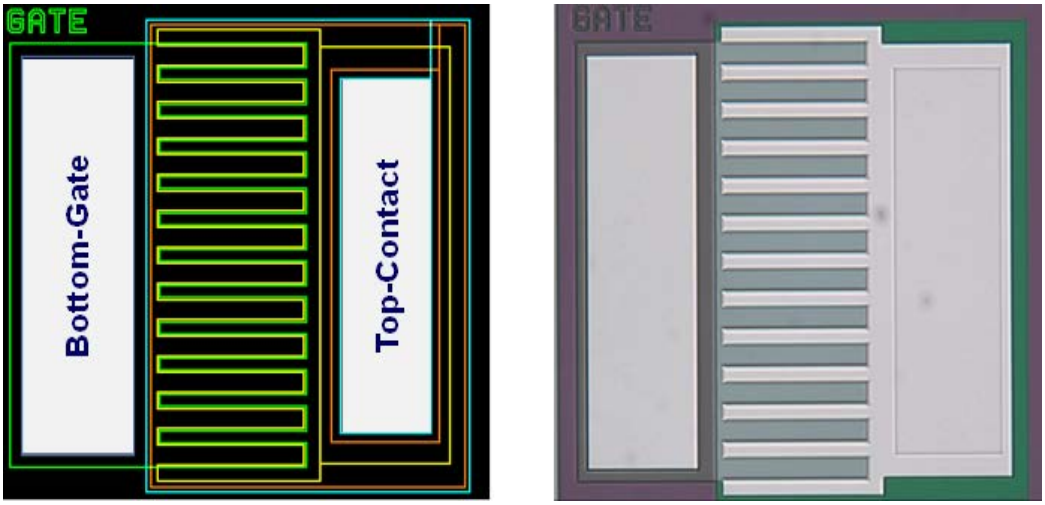

Figure 5.12: ICD layout (left), with twelve interdigitated fingers extending across the IGZO mesa. Each gated region has a width of 44 µm, and 5 µm side overlaps between the top-contact metal and the bottom-gate metal. The total gated area is ~ 0.002 cm^2. The micrograph of fabricated IDC is shown on right.

5.4 TCAD MATERIAL MODEL REFINEMENT

TCAD provides the ability to simulate both TFT and IDC structures, and develop material and device models that are consistent with both *I-V* and *C-V* measurements. In this section, the TCAD material model discussed in Section 5.2 is refined to simulate the measurements taken on TFT and IDC structures.

5.4.1 Unpassivated Back-Channel IGZO Devices

The overlay of electrical simulation using the default material model and the measured data is shown in Figure 5.13. The measured transfer characteristics are right-shifted compared

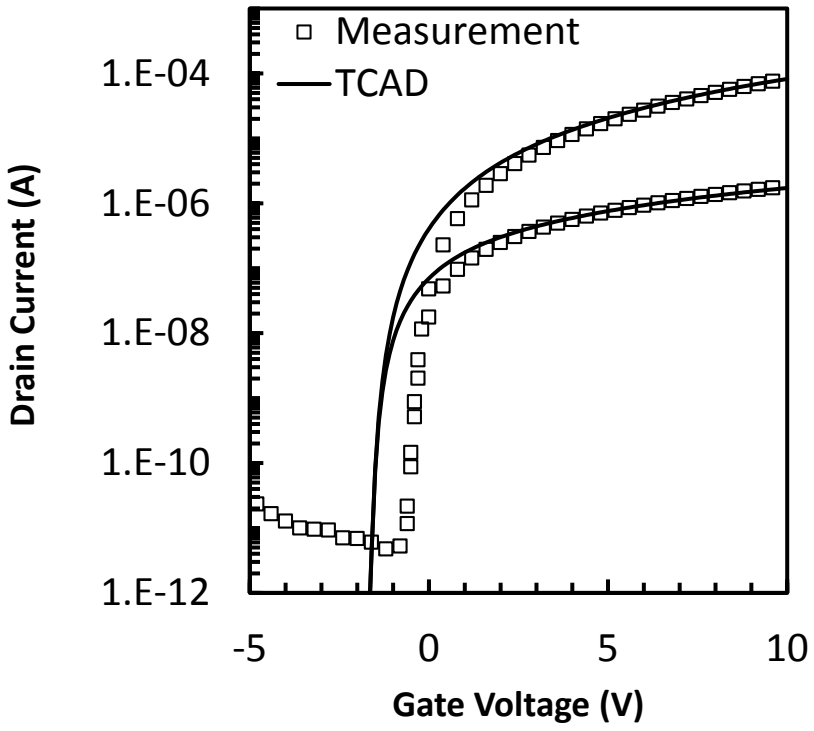

Figure 5.13: An overlay of measured (markers) and simulated (line) transfer characteristics of IGZO TFT using the default material model. The simulated characteristics are left shifted compared to measured data, suggesting a lower N_{Vo} in fabricated devices. (L=21 µm and W=100 µm)

to the simulation. The parallel shift suggests the difference in N_{Vo} (charge carriers) in the IGZO channel, as discussed in Section 5.2.1. Decreasing the N_{Vo} value from 6.5×10^{16} $cm^{-3}eV^{-1}$ to 2.0×10^{16} $cm^{-3}eV^{-1}$ shifted the I_D-V_{GS} characteristics towards right; however, the current drive is slightly higher. Reducing the mobility value from 15.0 $cm^2/V{\cdot}s$ to 12.7 $cm^2/V{\cdot}s$ gave a perfect overlay of simulation with the experimental data, both in linear and saturation mode. This modified value of mobility is also consistent with the TFT model discussed in Chapter 6. The overlay plots of simulated and measured transfer characteristics are shown in Figure 5.14.

The overlay of simulated and measured output characteristics is shown in Figure 5.15. The perfect overlay over all drain/gate biases validates the accuracy material model used. The model parameters that were adjusted from the default model [189] were N_{Vo} and μ_{eff}, representing the peak density of oxygen-vacancy donor states and effective electron mobility. The parameters are given in Table 5-II.

The representative IDC structure shown in Figure 5.16 was employed as a minimized 2D version of the device shown in Figure 5.12 for simulation purposes. The structure has two gate-fingers while the actual fabricated IDC has 12 interdigitated fingers. The area between the top-source electrodes is defined as vacuum, as Atlas requires a planar mesh structure. Note that the *C*-*V* model did require some adjustments to correct for distributed resistance (slight offset in IDC gated region width) and account for parasitic capacitance (level shift).

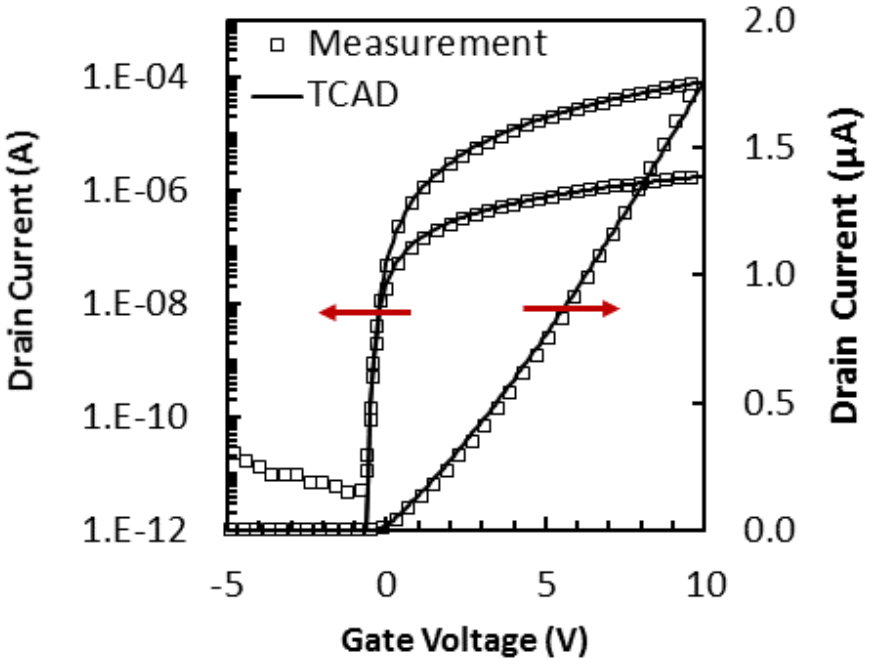

Figure 5.14: An overlay of measured (markers) and simulated (line) transfer characteristics of IGZO TFT using the refined material model plotted on log scale (y1-axis, V_{DS} = 0.1 V & 10 V) and linear scale (y2-axis, V_{DS} = 0.1 V). (L=21 µm and W=100 µm)

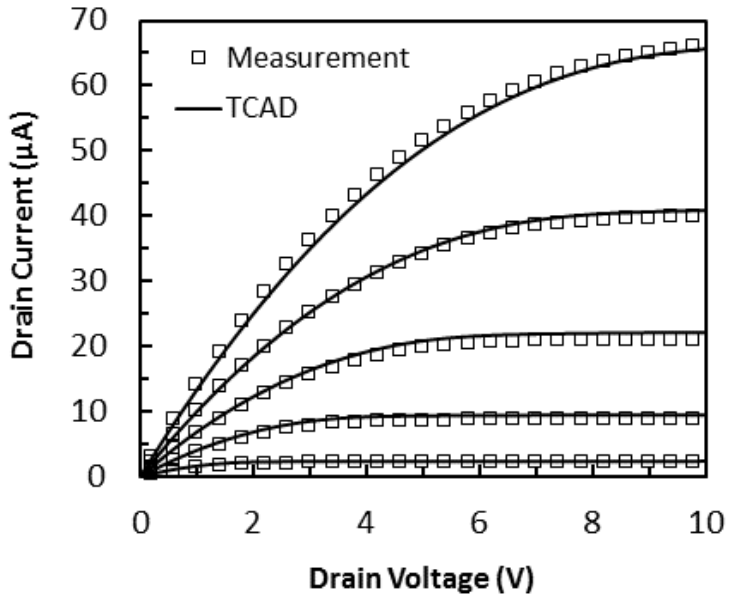

Figure 5.15: An overlay of measured (markers) and simulated (line) output characteristics of IGZO TFTs with V_{GS} = 2-10 V in steps of 2 V. (L=21 µm and W=100 µm)

Table 5-II: IGZO material parameters used for the simulation. N_{Vo} and μ_{eff}, representing the peak density of oxygen-vacancy donor states and effective intrinsic electron mobility are the only parameters changed from the Atlas default model.

Symbol	Value
Band gap	3.05 eV
Electron affinity	4.16 eV
Relative permittivity	10
Intrinsic Electron mobility*	12.7 $cm^2/V \cdot s$ *
V_O (Gaussian)	
N_{GD} (N_{Vo})*	2×10^{16} $cm^{-3}eV^{-1}$ *
E_{GD} (E_{Vo})	2.9 eV
W_{GD} (W_{Vo})	0.1 eV
Tail States	
N_{TA} (CB_{TN})	1.55×10^{20} $cm^{-3}eV^{-1}$
W_{TA}	0.013 eV
N_{TD}	1.55×10^{20} $cm^{-3}eV^{-1}$
W_{TD}	0.12 eV

** parameters modified from the default model*

Figure 5.16 shows the electron concentration in the IDC in accumulation mode (V_{GS} = 10 V). Figure 5.17 shows a high-frequency *C-V* characteristic of an IDC from the same testchip taken at f =1 MHz.

Both the *I-V* and *C-V* characteristics have the same material model parameters for the simulation overlay which are listed in Table 5-II. The consistency between simulation and measurements for both *I-V* and *C-V* characteristics provides further confidence in the material definition parameters listed in Table 5-II, with V_O and CB_{TN} bulk defect states responsible for device behavior.

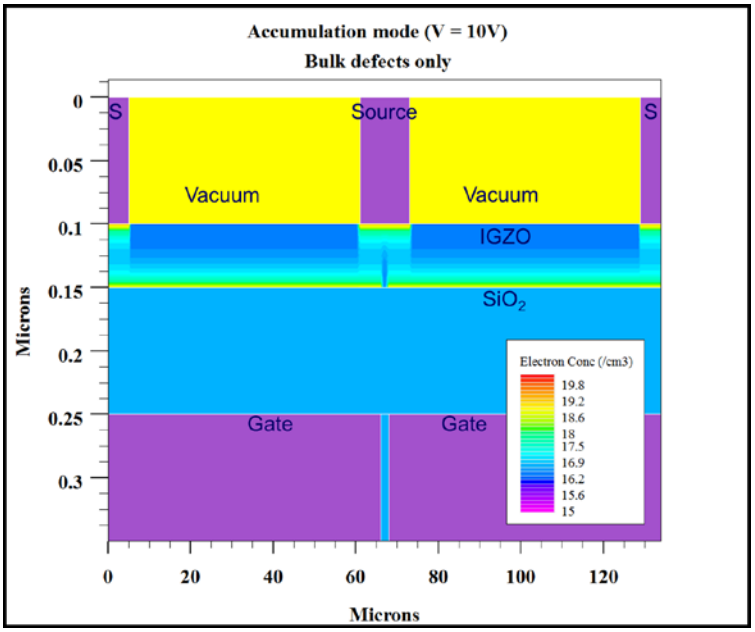

Figure 5.16: TCAD simulated IDC structure showing the electron concentration contours in accumulation (V_{GS}=10 V) .

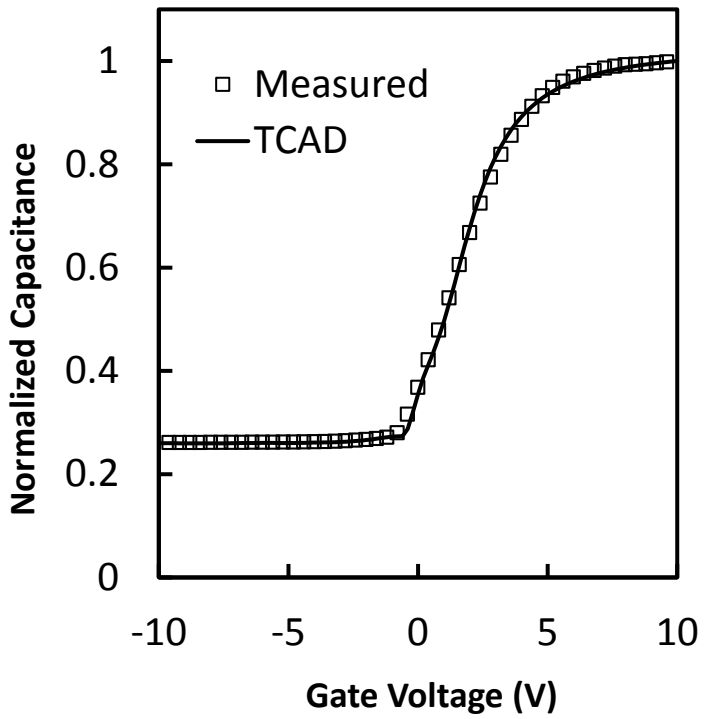

Figure 5.17: An overlay of measured (markers) and simulated (line) C-V characteristics of an IDC with the same material model used for TFTs. Material model parameters are listed in Table 5-II

5.4.2 Passivated Back-Channel IGZO Devices

Electrical characteristics from devices fabricated with electron-beam deposited alumina as a back-channel passivation material are shown in Figure 5.18. While the TFT performance was compromised compared to unpassivated TFT results (Figure 5.14), the changes in characteristics over a month of testing were essentially negligible, demonstrating an improved long-term stability after passivation of the exposed back-channel of IGZO.

It has been discussed in Section 4.5 that interface defect states at IGZO/passivation material interface remain following the application of a passivation material and oxidizing ambient anneal. For the simulation of alumina passivated devices the same bulk IGZO material shown in Table 5-II was used, however additional parameters were added which establish charge centers and interface traps at the back-channel material interface between the IGZO and alumina to account for these defect states. A fixed charge density N_f = -1.9×10^{12} cm^{-2} and a Gaussian distribution of donor-like interface traps (N_{Voi}) were used to provide a reasonable match to the *I-V* and *C-V* characteristics shown in Figure 5.18. The E_{Vo} and W_{Vo} parameters are the same as those listed in Table 5-II for the Gaussian distribution of donor-like states in the IGZO material. The modified material model included both interface traps and fixed charge to account for the shift in threshold voltage after AlO_X passivation. These interface parameters are listed in Table 5-III.

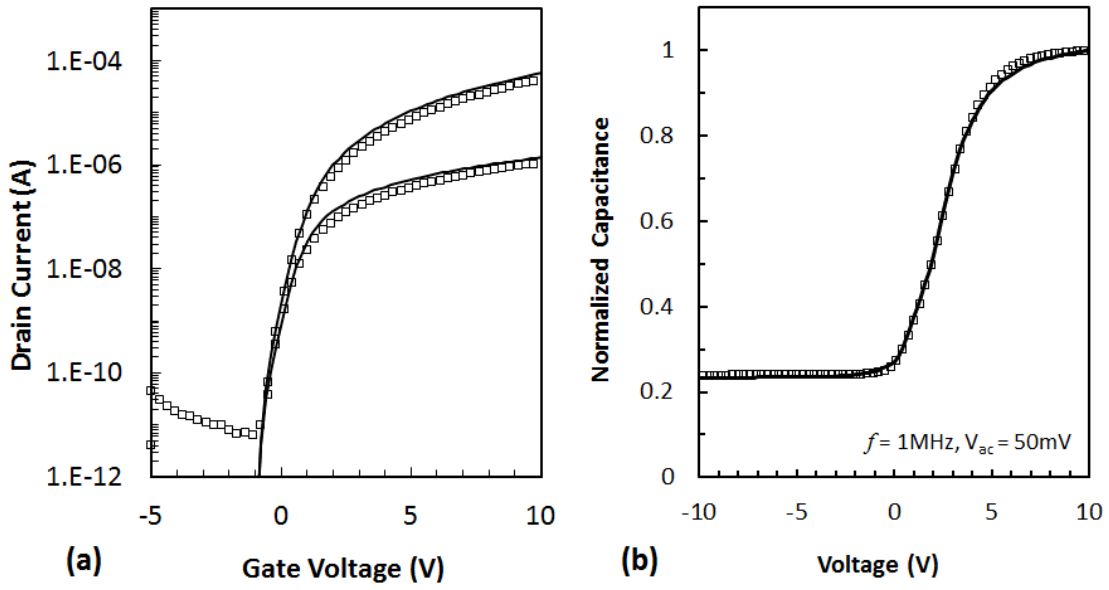

Figure 5.18: An overlay of measured (markers) and simulated (line) (a) I_D-V_{GS} transfer characteristics of IGZO TFT with alumina passivation. (b) C-V characteristics of an IDC with the same set of model parameters. The TFT channel dimensions were L = 21 µm & W = 100 µm. Bulk material model parameters are consistent with Table 5-II, with additional interface parameters and extracted properties listed in Table 5-III.

Table 5-III: Back-channel interface parameters and TFT parameters of the alumina passivated devices shown in Figure 5.18

Symbol	Value
N_{Voi} (donor-like interface traps)	2×10^{12} cm^{-2}eV^{-1}
E_{Voi}	2.9 eV
W_{Voi}	0.1 eV
N_f (fixed charge)	-1.9×10^{12} cm^{-2}
Extracted IGZO TFT parameters	
Field-effect mobility	5 cm^2/V·s
Threshold voltage	-0.1 V
Subthreshold swing	300 mV/dec

In this case the area density peak is set to $N_{Voi} = 2\times10^{12}$ cm^{-2}/eV, which brings the total integrated donor (positive) interface trapped charge state density to $N_{IT} \sim 5\times10^{11}$ cm^{-2}, and a net back-channel surface state density of $N_{SS} \sim -1.4\times10^{12}$ cm^{-2} when all donor states are ionized. The behavior of interface traps are consistent with the energy distribution of oxygen vacancy donor states defined for the IGZO material. The total space charge in the IGZO material due to oxygen vacancies integrated over both energy and film thickness is $N_{bulk} \sim 2.5\times10^{10}$ cm^{-2}, so it is reasonable that interface states can dominate the device behavior. While the interface defect parameter settings provide a reasonable simulation match to the non-ideal TFT and IDC characteristics, the canceling behavior of positive and negative interface charge levels, and the origin of negative fixed charge remain in question and suggest the possibility of misinterpretation.

High-frequency (1 MHz) measurements taken on IDCs demonstrate the ability to move channel charge in and out from gated regions, which is influenced by lateral travel distances and accumulated channel charge. The time to move carriers from the center of the channel to the source electrode is limited by the channel conductance, and results in a spreading of *C-V* characteristics. In addition, carrier traps within the IGZO material or associated interfaces cause distortion in high frequency characteristics relating to their energy level and physical distribution. An overlay of multi-frequency measurements and simulations of IDC *C-V* characteristics are shown in Figure 5.19. The dispersion of the *C-V* characteristics is attributed to trap states as well as distributed channel resistance which is a function of gate voltage. As the measurement frequency increases, the influence of resistance becomes more significant, which decreases the sensitivity to defect states. As the measurement frequency is lowered the series resistance influence is less, however the

discrepancy between the measurement and simulation is apparent at lower gate voltage where there is a high sensitivity to defect states in the transition from depletion to accumulation. Variable series resistance (*i.e.* gate voltage dependent) at the source/drain M-S contacts is assumed to be responsible for the inability to determine a constant series resistance using traditional parameter extraction methods on TFTs of varying channel length (see Section 6.1.4). This effect may be the primary reason for the simulation discrepancy, and is unfortunately confounded with the influence of trap states. Variation in trap state response time (i.e. slow traps *vs* fast surface states) further complicates the interpretation. For these reasons further efforts to refine the analysis of defect states, and distinguish between bulk and interface defects, were directed towards charge transport analysis in TFTs.

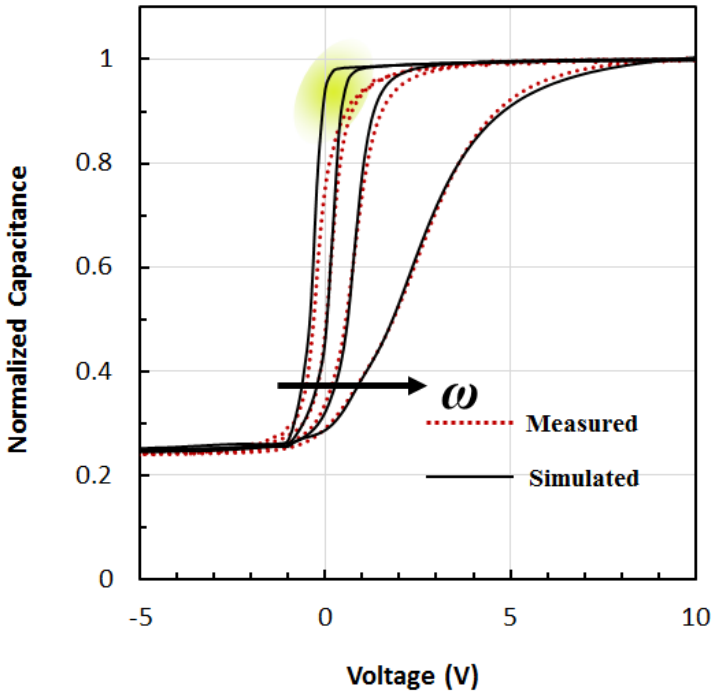

Figure 5.19: Overlay of simulated and measured C-V characteristics at 1 kHz, 10 kHz, 100 kHz and 1 Mhz. The simulation showed inconsistencies at lower frequencies and lower gate voltage conditions which support a high sensitivity to defect states.

5.5 CHARGE TRANSPORT IN IGZO

The conduction mechanism in IGZO material is studied through low temperature measurements taken on TFTs. IGZO TFTs without any back-channel passivation material were used to avoid the influence of interface defect states at the IGZO/passivation material interface. TFTs were tested in Lakeshore cryogenic probe station. The test-chip was loaded and the system was allowed to cool down to 10 K using liquid helium. The transfer characteristics were measured while increasing the temperature from 10 K to room temperature.

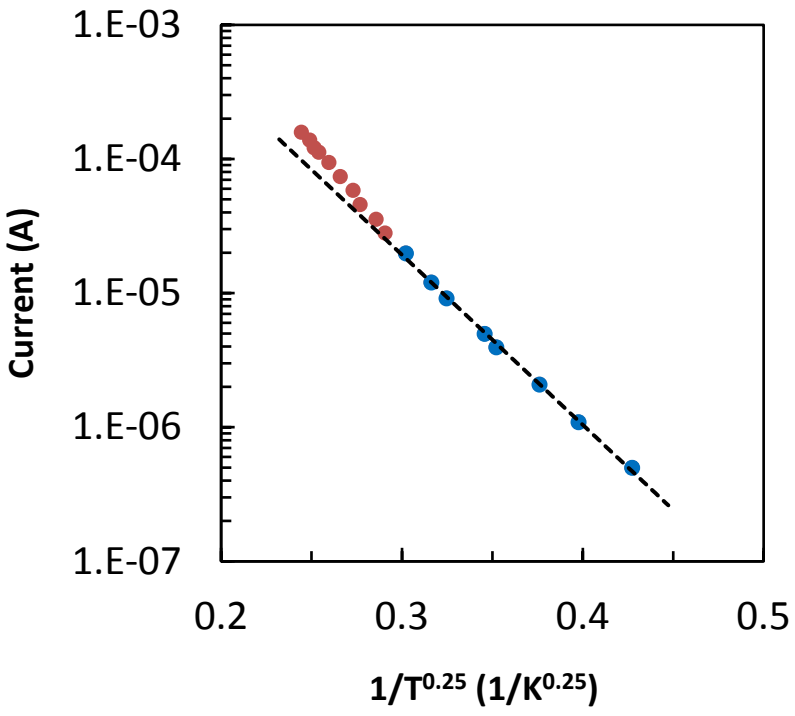

Figure 5.20: Drain current versus temperature plot at V_{GS}=V_{DS}=10 V. The linear dependence of log(I_D) on $1/T^{0.25}$ over temperature (10 K- 130 K) indicates variable range hopping as the carrier transport mechanism at low temperature (T<130 K).

5.5.1 Low-Temperature Range (10 K to 130 K)

The drain current (I_D) values are plotted against the temperature ($1/T^{0.25}$) at V_{GS}=V_{DS} =10 V) in Figure 5.20. Below 130 K, current showed a weak thermal dependence and followed Mott's law [193], [88]:

$$I_D = I_{D_O} \exp\left(-\frac{B}{T^{\frac{1}{4}}}\right) \tag{5.9}$$

where I_{DO} is a drain current prefactor, B depends on the material properties. This behavior is a characteristic of variable range carrier hopping in amorphous materials [194]. Measurements indicated this as the dominant mechanism at low temperature range.

5.5.2 High-Temperature Range (>130 K)

At T >130 K, the current vs temperature response followed the Arrhenius behavior [195]:

$$I_D = I_{D_O} exp\left(\frac{-E_a}{k_b T}\right) \tag{5.10}$$

where E_a is the activation energy (E_C -E_F) [88], I_{DO} is a drain current prefactor and k_b is the Boltzmann constant. The activation energy is gate voltage dependent and decreases with increase in V_{GS} [196].

The Arrhenius fit indicates the thermally activated band activation as the carrier transport mechanism. The extracted range of activation energy is 40-70 meV for V_{GS} = 10 V and -5 V respectively. Activation energy is a measure of the energy difference between conduction band (E_C) and Fermi level (E_F). As V_{GS} increases the E_F moves closer to the E_C and therefore the value of activation energy decreases. The Arrhenius fit suggested that the charge transport in IGZO at room temperature, unlike a-Si, is through

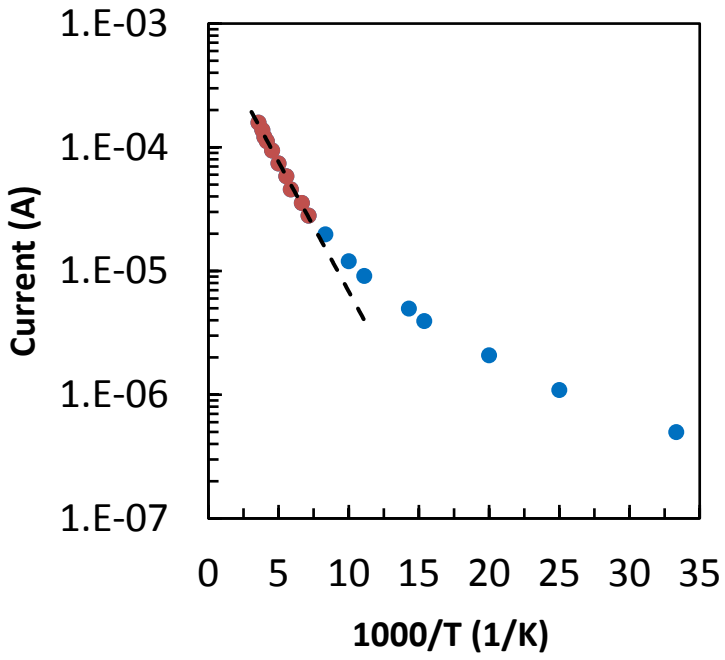

Figure 5.21: Drain current versus temperature plot at V_{GS}=V_{DS}=10 V. Charge transport follows Arrhenius behavior for T >130 K, indicating thermally activated band conduction as the charge transport mechanism.

the thermal activation rather. Therefore the mobility should not be associated to the free/trapped charge ratio as in a-Si [197]. The presence of tail-states however, change the charge concentration in the channel which can be incorporated in charge ratio rather than a decrease in mobility. A thorough discussion on parameter extraction and device modeling presented in Chapter 6.

5.5.3 Defect Density Calculations

The value of *B* in Equation (5.9) can be extracted from the slope of ln(I_D) *vs* $1/T^{0.4}$ plot. The theoretical value of *B* is related to the density of states at E_F by [88], [198]:

$$B = 2\left(\frac{\alpha^3}{k_b N(E)}\right)^{\frac{1}{4}} \quad (5.11)$$

where α is the inverse of Bohr radius (a) and is related to the overlap of wave functions of two localized states and can be calculated from:

$$a = \frac{a_0 \varepsilon_r}{m^*/m_0} \quad (5.12)$$

where a_0 is the Bohr radius of hydrogen atom (0.53 Å), ε_r is the relative permittivity of IGZO (11.5) [199], m^* is the effective mass of electron in IGZO ($0.34m_o$) where m_o is the free electron mass [54]. From Equation (5.12), a is approximately 17.9 Å. Once the value of B is known, $N(E)$ can be calculated from Equation (5.11). Similarly, E_a can be extracted from I_D *vs* $1/T$ plot (Figure 5.21). A plot of $N(E)$ *vs* E_a is shown in Figure 5.22 and the data is fitted to:

$$N(E) = N(E_C)\exp\left(-\frac{E_a}{E_0}\right) \quad (5.13)$$

where $N(E_C)$ is the DOS and E_0 is the band tail slope. The value extracted from Figure 5.22 are $N(E_C)$=2×10^{21} $cm^{-3}eV^{-1}$ and E_0=9.5 meV. The value of $N(E_C)$ is an order of magnitude higher compared to the $N(E_C)$ used in IGZO material model for TCAD simulation. The value of E_C is used in TCAD simulation is 13 meV. The discrepancy in the measurement is most likely due to the use of unpassivated devices. The back-channel was exposed during the measurement. It is suspected that during cryogenic cooling some of the water vapors present in the system might have condensed on the unprotected IGZO channel. This suspicion was also supported by the fact that working TFTs after cryogenic

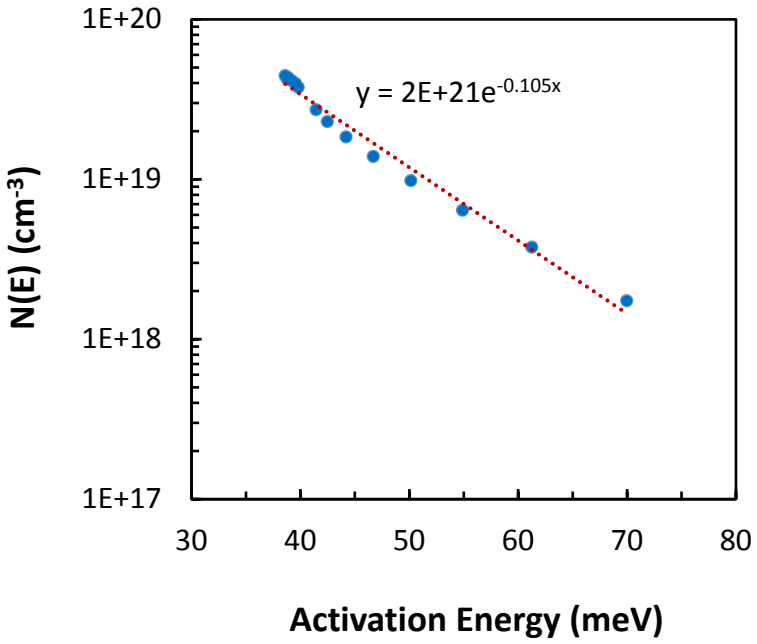

Figure 5.22: DOS at E_F (N(E)) versus activation energy (E_a).

measurements showed a negative shift of -8 V in V_T. A passivated IGZO TFT should produce more consistent results.

5.6 SILICON DIOXIDE PASSIVATION

TFTs passivated with PECVD SiO_2 were also simulated using the IGZO material model discussed earlier. The interface defect density was adjusted for a match with experimental data. Figure 5.23 shows that transfer characteristics of a SiO_2 passivated TFT after 4 h annealing in O_2 ambient at 400 °C. Further details regarding simulation of SiO_2 passivation are provided in Section 7.1.5.

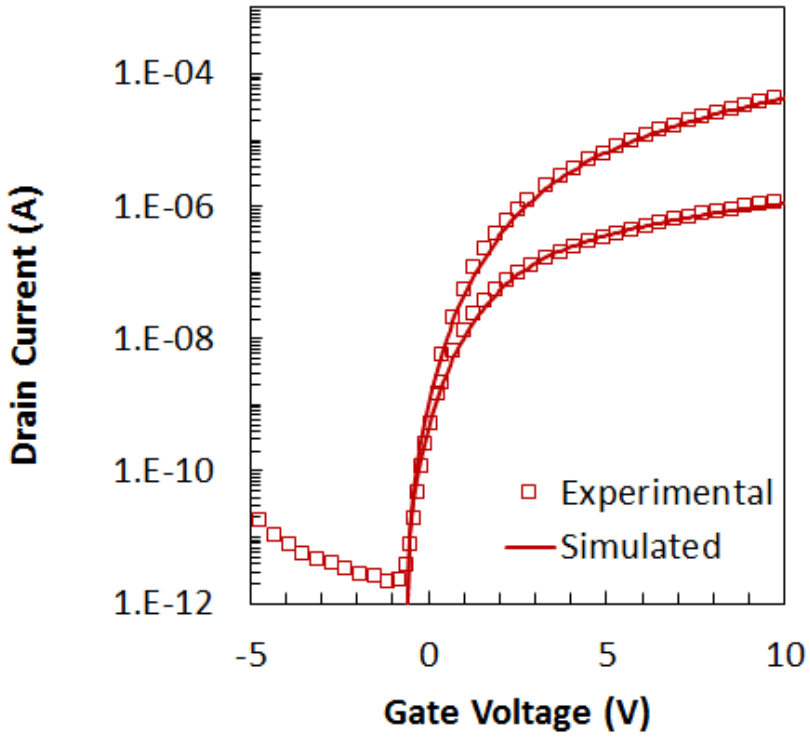

Figure 5.23: An overlay of measured (markers) and simulated (line) transfer characteristics of IGZO TFT with SiO_2 passivation. (L=21 µm and W=100 µm)

5.7 CONCLUSION

In this chapter, the experimental results are compared with TCAD simulations using commercially available software package Silvaco® Atlas™. The IGZO defect states were defined and there influence on electrical characteristics of transistors is presented.

A methodology which uses both *I-V* and *C-V* analysis in the interpretation of defect states in IGZO devices has been described. *C-V* measurements taken on IDCs are complementary to *I-V* measurements on TFTs, and TCAD simulation offers the ability to establish material and device model parameters that consider both datasets. The application to devices which had optimum annealing conditions and did not have any back-

channel passivation material demonstrated an excellent match between simulation and measurements using an established material defect model with only minor adjustments. The use of electron-beam deposited alumina as back-channel passivation material resulted in improved device stability; however both *I-V* and *C-V* measurements revealed the influence of interface traps. The shortcomings of *C-V* measurements using IDC structures are discussed and an approach to identify the interface defect states using transistors fabricated in different gate electrode configurations is proposed. These results are discussed in Section 7.1.5.

Cryogenic measurements were utilized for extraction of density of states (DOS) in IGZO. The extracted values of DOS and band tail states slope were not in agreement with reported values [148], [200]. A similar discrepancy in DOS extraction from low-temperature measurements have been reported by others [88]. Nevertheless, the study confirmed that at room temperature thermally activated band conduction was the charge transport mechanism. On contrary, variable range hopping is the conduction mechanism for amorphous silicon [12], [197], [201]. This difference in charge transport is manifested during the device operation modeling where a-Si:H TFT model is not applicable to IGZO TFTs. A novel device operation model is presented in the Chapter 6.

A device model implementing fixed charge and donor-like interface traps that are consistent with oxygen vacancies resulted in a reasonable match to measured characteristics for SiO_2 passivated devices.

Chapter 6. 2D DEVICE MODEL FOR ON-STATE OPERATION

The development of a consistent and reliable parameter extraction model is of paramount importance if a quantitative analysis and comparison of different treatments is required. It is crucial for the method to add minimum error so that any differences observed can be accounted for by processing differences. One of the fundamental parameter of MOSFET is threshold voltage (V_T) which broadly signifies the onset of the channel inversion (or accumulation for TFTs). For crystalline silicon (c-Si), numerous methodologies for V_T extraction have been employed over the years for device characterization and modeling [202]–[204]. These techniques have been extended to model silicon based transistors *i.e.* a-Si:H and poly-Si TFTs.

In recent years, much work has been done in the field of amorphous oxide semiconductors, most notably indium gallium zinc oxide (IGZO). The amorphous nature of IGZO offers benefit in terms of performance uniformity. IGZO also offers process simplicity because source/drain implantations are not required. However, these advantages also present challenges in the extraction of simple transistor parameters *i.e.* threshold voltage (V_T) and channel mobility (μ_{ch}) due to the presence of defect states and gate voltage dependent (V_{GS}) source/drain contacts resistance (R_{SD}) which manifests itself in non-ideal response of current to voltage as described further in coming sections. Thus, the traditional methods used for silicon devices are not effective.

In this chapter, various conventional methods for V_T and μ_{ch} extractions using drain current measurements have been compared and the associated shortcomings are discussed. To ensure consistent parameter extraction an accurate model must be implemented and for that a novel approach for V_T and μ_{ch} is proposed. A new device model for the on-state operation of IGZO TFTs is presented, which accounts for the interaction effects that band-tail states have with the gate and drain voltages on *I-V* relationships. TCAD simulation is used as a tool for model development, which ensures a physical connection and enables the interpretation of effects that have complex interactions. The model elements which account for adjustment of free electron charge and spreading of the output conductance are expressed empirically, rather than through rigorous mathematical derivation which is arguably not possible. The result resembles a Level 2 SPICE model with unique physical interpretation, and demonstrates an excellent match to transfer and output characteristics over all on-state bias conditions.

6.1 CONVENTIONAL PARAMETER EXTRACTION

The existence of defect states in amorphous semiconductor materials such as indium-gallium-zinc oxide (IGZO) results in non-ideal electrical characteristics that render conventional device models inadequate. Thus common operating parameters that are used to characterize device operation must be appropriately redefined for a device model to be physically meaningful and useful in circuit simulation. There is general agreement in the assignment of non-ideal behavior in *I-V* characteristics to band-tail states [143], [163], [205]. The conventional gradual-channel approximation (GCA) equation expressed in

Equations (6.1) and (6.2) is sufficient to represent the on-state device operation in the absence of band-tail states.

$$I_{Dlin} = \frac{\mathrm{W}}{\mathrm{L}} \mathrm{C_{ox}} \mu_{ch} \left(\left(V_{GS} - V_{T_{lin}} \right) . V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (6.1)$$

$$I_{Dsat} = \frac{\mathrm{W}}{2\mathrm{L}} \mathrm{C_{ox}} \mu_{ch} \left(V_{GS} - V_{T_{sat}} \right)^2 \quad (6.2)$$

where *W*, *L* & C_{OX} are channel width, length and oxide capacitance per unit area respectively.

The above equations work well for the first order calculations. However, the c-Si MOSFETs show normal field degradation which can be incorporated in the mobility model as:

$$\mu_{ch} = \frac{\mu_0}{1 + \theta (V_{GS} - V_T)} \quad (6.3)$$

where μ_0 is the "true" mobility of the material and θ is a fitting parameter which accounts for the normal field degradation. Figure 6.1 shows an overlay of transfer characteristics of c-Si NMOS and IGZO TFT. Unlike c-Si, IGZO TFT does not show any normal field degradation; in contrary, the slope of the I_D-V_{GS} curve keeps increasing with V_{GS} which makes the extraction of parameter subjective for such devices.

In this section, various conventional methods for parameter extraction are discussed along with the shortcomings and inconsistencies associated with them when applied to IGZO TFTs.

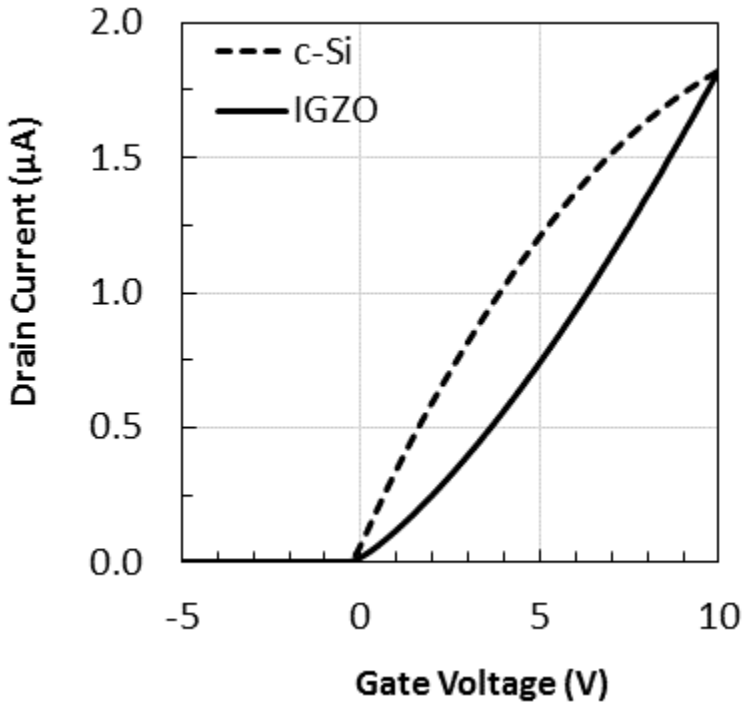

Figure 6.1: I_D-V_{GS} measurements on c-Si NMOS and IGZO TFT showing the concave down and up characteristics due to normal field degradation (c-Si) and tail-states (IGZO) respectively. The c-Si NMOS data is scaled down. (V_{DS}=0.1V)

6.1.1 Constant Current Method

One of the simplest and common method for parameter extraction is to use fixed current value (typically ~ 10^{-7}-10^{-9} A) as an indicator of V_T (or V_{ON}) [160], [167], [206], [207]. This method is popular among TFT community because of its simplicity. However, a thorough review of published articles reveals that the value of current is chosen arbitrarily. In some cases, it is left as vague as "the gate voltage at which an appreciable amount of current starts flowing" [157], [208]. Also, μ_{ch} calculated Equation (6.1) is V_{GS} dependent. Although the V_T and μ_{ch} calculations using constant current method have merit in terms of

simplicity, it does not provide a uniquely consistent approach and the parameter extraction remains subjective and ambiguous.

6.1.2 Extrapolation Method

Another common method to extract V_T is to use x-axis intercept of the linear fit to I_{Dlin}-V_{GS} (or $\sqrt{I_{Dsat}}$-V_{GS}) at the maximum slope of I_D-V_{GS} [209], [147], [150]. For c-Si devices, this method provides consistent values of V_T and μ_{ch} as shown in Figure 6.2.

In case of IGZO devices, I_D tends to be concave upward as shown in Figure 6.3. This upward curvature makes the linear fit somewhat subjective. For instance, when the linear fit is taken at V_{GS1} =3 V and V_{GS2} =9 V, the extracted threshold voltages are V_{T1}=0.5 V and V_{T2} =2.2 V. Mobility values calculated at V_{GS} =10 V using Equation (6.1) are

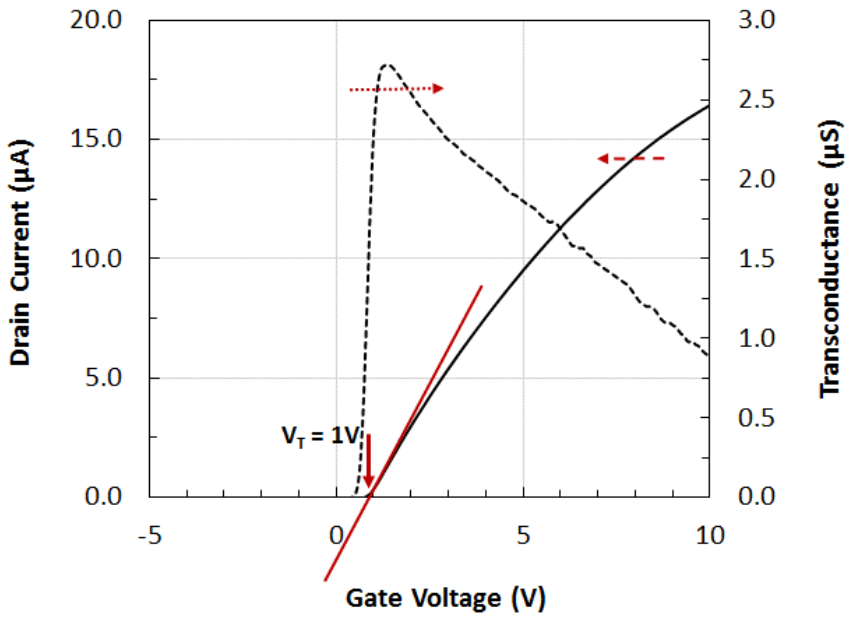

Figure 6.2: V_T extraction for c-Si MOSFET using the x-axis intercept to the linear mode transfer characteristics.

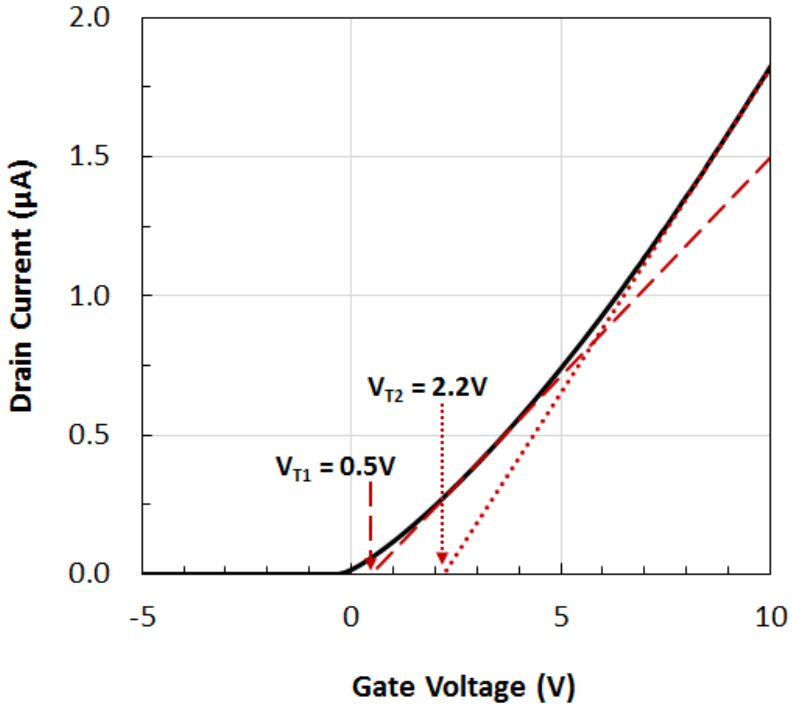

Figure 6.3: V_T extraction for IGZO TFT using the x-axis intercept to the linear mode transfer characteristics. The slope of I_{Dlin} keeps increasing and therefore does not provide a unique point for extraction of V_T.

15.3 cm^2/V·s (V_{T1}) and 18.6 cm^2/V·s (V_{T2}), a difference of 16%. The μ_{ch} values are not only dependent on the choice of V_T but also on the V_{GS} values, with higher V_{GS} giving higher values of μ_{ch}. These inconsistencies in extraction of V_T and subsequently μ_{ch} can lead to false interpretation of the results and therefore careful consideration should be given to parameter extraction.

6.1.3 Differential Transconductance Method

The V_T for MOS transistor can also be defined as the voltage at which the rate of change of transconductance (g_m) is maximum. This can be determined by the peak of the derivative of g_m (*i.e.* g'_m) with V_{GS}. Figure 6.4 shows the g'_m *vs* V_{GS} graph, the derivative

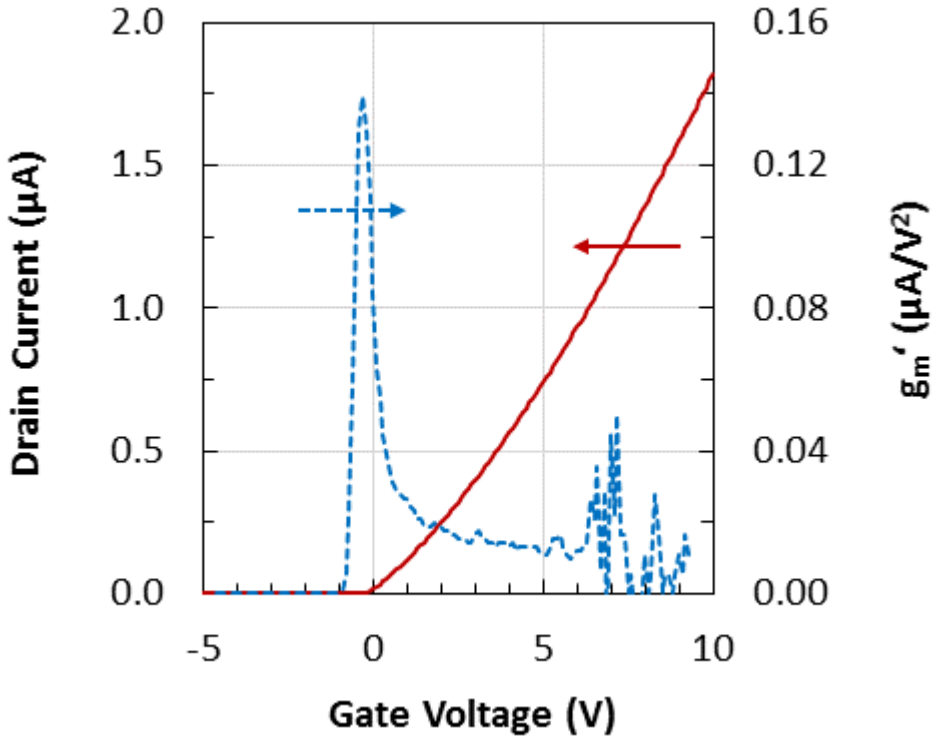

Figure 6.4: Differential transconductance method for V_T extraction, the position of the peak of g'_m is taken as the V_T. (L = 21 μm, W = 100μm).

is smoothed over five point (excluding minimum and maximum values) to avoid any erratic data points during measurement. A V_T = -0.3 V is extracted from the value of V_{GS} corresponding to the peak of g'_m. This provides a consistent interpretation of threshold voltage and avoids issues with continuously increasing slope of I_{Dlin} (or g_m). However, for V_T =-0.3 V, V_{GS}-V_T is negative and therefore normal transistor Equation (6.1) is not valid for those data points

For mobility extraction, transconductance (g_m) method can be used which is independent of V_T. This can be arrived at by differentiating Equation (6.1) with respect to V_{GS}, as:

$$\mu = \frac{g_m L}{W.C_{OX}.V_{DS}} \qquad (6.4)$$

The resulting μ_{ch} is plotted in Figure 6.5. The μ_{ch} values using Equation (6.4) (solid line) are higher than extracted from Equation (6.1) (broken line) and are a function of V_{GS}. To circumvent this issue, a voltage dependent mobility model $\mu_{ch}(V_{GS})$ is also proposed to account for apparent increase in mobility, however a physical connection is not established [208].

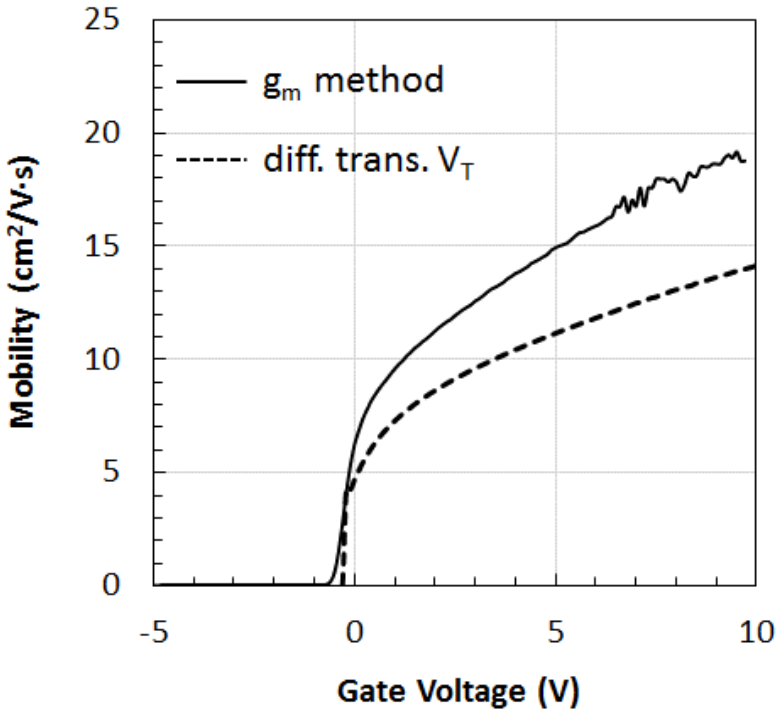

Figure 6.5: Mobility calculation using g_m (Equation (6.4)) and I-V (Equation (6.1), V_T extracted through differential transconductance method. In both cases, the μ_{ch} value increases with V_{GS}.

6.1.4 Extraction Through Terada-Muta Analysis

Terada-Muta analysis has been widely used for the extractions effective channel length (L_{eff}) and contact resistance (R_{SD}) as shown in Section 4.2.3. T-M method can be extended to calculate the mobility and threshold voltage of transistors [163]. The total resistance of the TFT, R_{tot}, can be written as [163]:

$$R_{tot} = r_{ch}L + R_{SD} \tag{6.5}$$

where r_{ch} is the channel resistance per unit length and R_{SD} is the resistance offered by the S/D contacts. Using Equation (6.1), R_{tot} can be written as:

$$R_{tot} = \frac{V_{DS}}{I_{DS}}\bigg|_{V_{DS_{lin}}} = \frac{L}{WC_{ox}\mu_{ch}(V_{GS} - V_T)} = r_{ch}L + R_{SD} \tag{6.6}$$

Using Equation (6.6), the R_{tot} *vs* L data can be plotted for different V_{GS} values and r_{ch} value can be extracted from the slope. The effect of the R_{SD} in Equation (6.6) can be decoupled by defining intrinsic mobility (μ_i) and intrinsic threshold voltage (V_{Ti}) defined as the mobility and threshold voltage values without the influence of the series resistance. Equation (6.6) therefore can be rewritten as:

$$r_{ch} = \frac{1}{WC_{ox}\mu_i(V_{GS} - V_{Ti})} \tag{6.7}$$

$$\frac{1}{r_{ch}} = WC_{ox}\mu_i V_{GS} - WC_{ox}\mu_i V_T \tag{6.8}$$

Once r_{ch} is known for each V_{GS} (from the slope of R_{tot} *vs* L), the μ_i and V_{Ti} values can be extracted by plotting $1/r_{ch}$ vs V_{GS}. The plot of $1/r_{ch}$ against V_{GS}, with a linear fit, is shown in Figure 6.6, the extracted values are V_{Ti}=1.0 V and μ_i=13.6 cm^2/V·s.

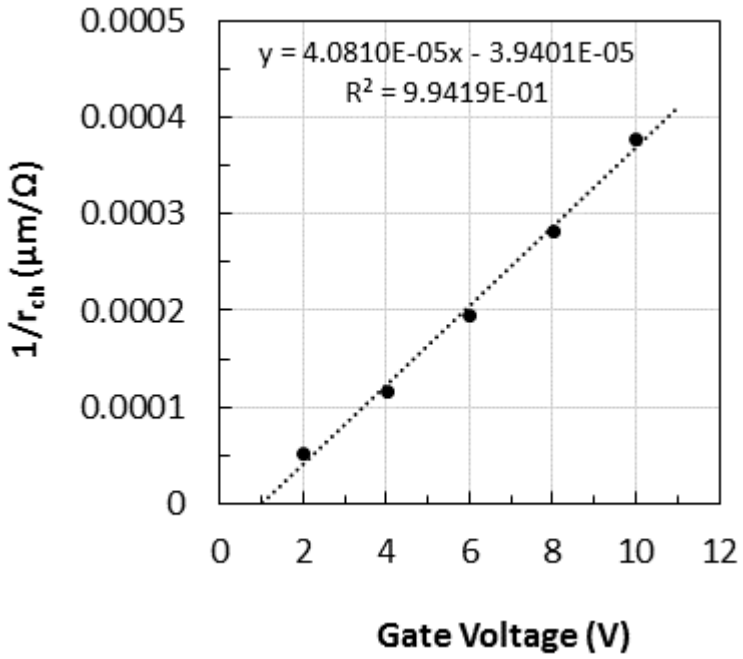

Figure 6.6: Linear fit to $1/r_{ch} - V_{GS}$ for the extraction of V_{Ti} and μ_i using Terada-Muta analysis.

This approach has been effectively used for extracting parameters for c-Si and a-Si:H transistors where the S/D regions are heavily doped. For IGZO TFTs, the S/D contact relies on the gate to S/D overlap. In on-state, V_{GS} creates an accumulation layer in the entire channel, this region (G-S/D overlap) then effectively behaves as doped S/D area. This contact is inherently V_{GS} dependent (*i.e.* $R_{SD}(V_{GS})$). Owing to this dependence, Equation (6.6) may not always be uniquely solvable and the extrapolated R_{SD} changes with V_{GS}. This also leads to a non-linear response of $1/r_{ch}$-V_{GS} and therefore V_{GS} dependent V_{Ti} and μ_i values as shown in Figure 6.7. Both V_{Ti} and μ_i increase with V_{GS}, such inconsistencies undermine the validity of this method.

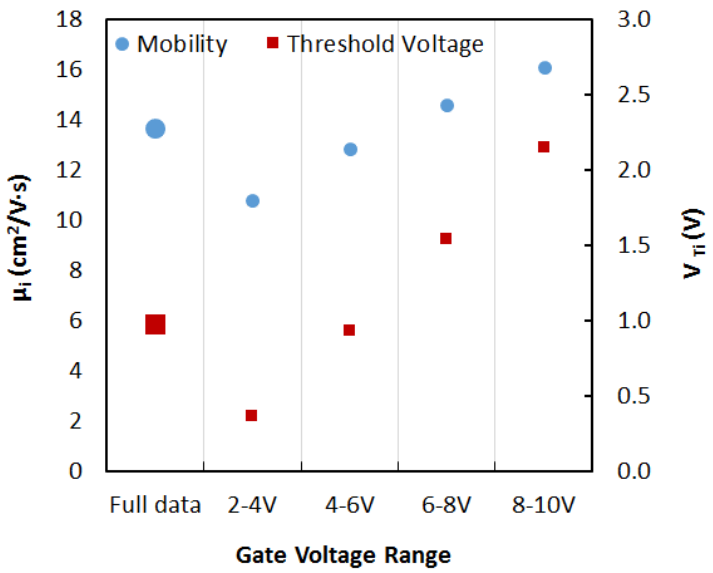

Figure 6.7: V_{GS} dependence of V_{Ti} and μ_i values extracted from $1/r_{ch}$-V_{GS} data using Terada-Muta analysis.

To further reveal R_{SD} dependence on V_{GS}, TCAD simulation is used to extract the electron concentration in IGZO below the source electrode. The electron concentration in IGZO at different points along the channel thickness with V_{GS} is shown in Figure 6.8. Majority of the current flows near the IGZO/gate dielectric interface where the electron concentration is a strong function of V_{GS} (blue solid line) and changes by 13 orders of magnitude for a sweep of V_{GS} from -5 V to 10 V. This indicates that the R_{SD} should not be treated as constant and the simplification from Equation (6.6) to Equation (6.7) is not valid. This simplification corrupts the interpretation of Terada-Muta analysis for IGZO TFTs.

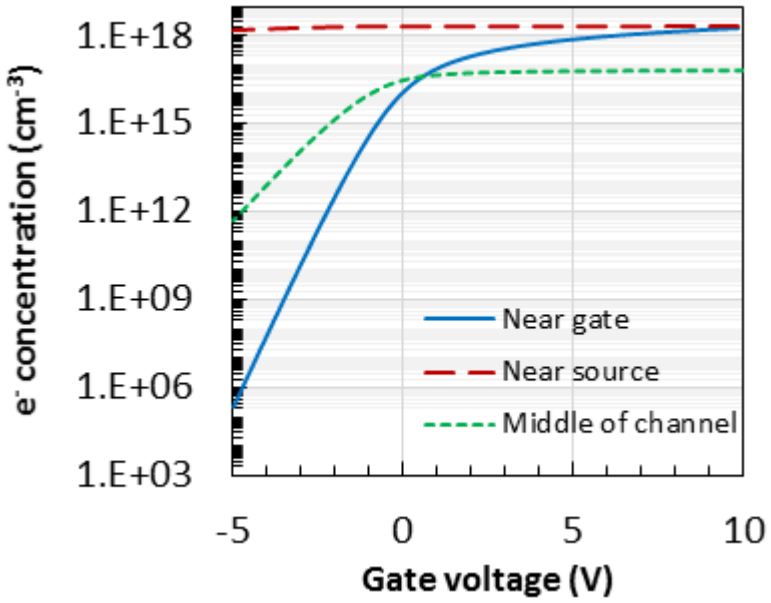

Figure 6.8: Electron concentration below the source electrode at various depths in IGZO channel with respect to gate voltage. (V_{GS}=10 V, V_{DS}=0 V)

6.2 AMORPHOUS SEMICONDUCTOR MATERIALS

The gate voltage dependent g_m is also observed in a-Si:H TFTs [205], [210]. As discussed earlier, the amorphous materials have band-tail states close to the conduction and valence band. The ever increasing slope in transfer characteristics of such semiconductor material device is attributed to the presence of these band tail-states.

6.2.1 Departure from GCA

Silvaco® Atlas™ TCAD has been used to simulate IGZO TFT operation using the electrical model discussed in Section 5.4, without inclusion of high-field effects or advanced carrier transport phenomenon (*e.g.* hopping between localized states). With the

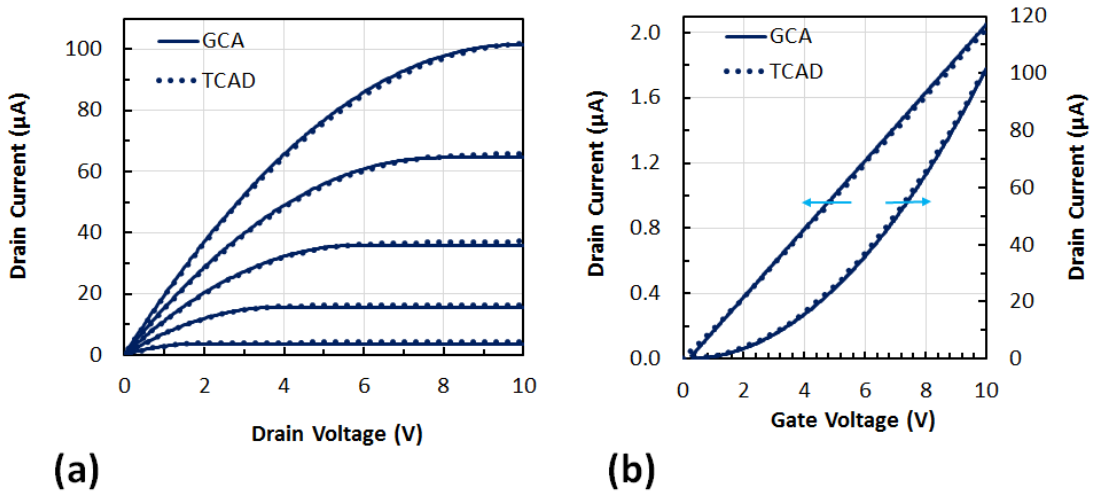

Figure 6.9: TCAD simulated I-V characteristics of IGZO TFT without band-tail states (dotted line) with a nearly perfect match to the GCA model (solid line). (a) Output characteristics with V_{GS} = 2-10 V in steps of 2 V. (b) Transfer characteristics in linear mode (y1-axis, V_{DS} = 0.1 V) and saturation mode (y2-axis, V_{DS} = 10 V). (L = 21 µm, W = 100 µm)

specific exclusion of band-tail states, TCAD simulated transfer and output characteristics match exceedingly well with the GCA relationships (Equations (6.1) and Equation (6.2)) as shown in Figure 6.9 without consideration of series resistance or non-ohmic contacts.

The same TCAD model with the inclusion of band-tail states demonstrates an excellent match with measured *I-V* characteristics as shown in Figure 6.10 (see Section 5.4). This infers that the departure from the GCA is solely due to the influence of band-tail states. While both sets of output characteristics appear qualitatively similar, the inclusion of band-tail states results in a notable decrease in current drive which is not associated with series resistance, and cannot be modeled by current scaling via mobility adjustments.

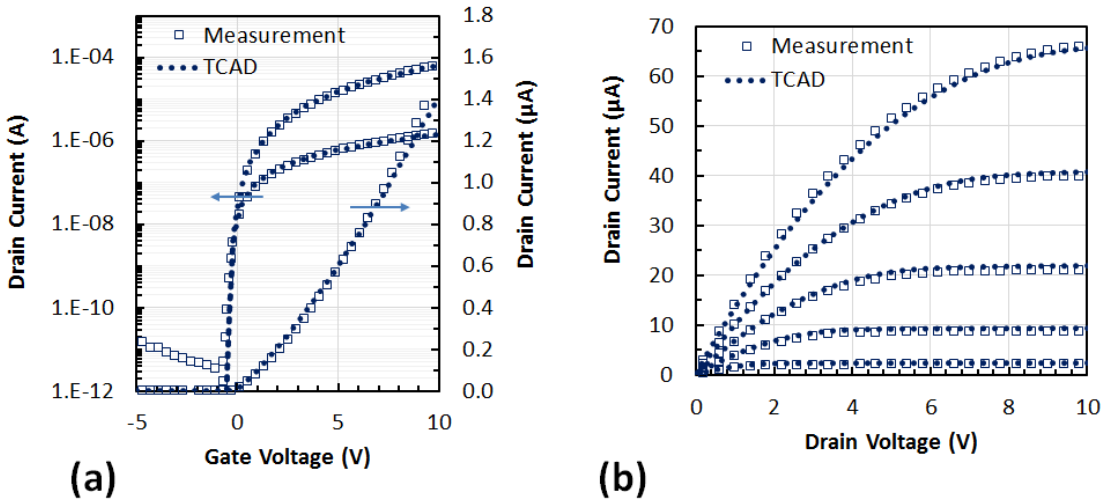

Figure 6.10: TCAD simulated I-V characteristics with band-tail states (dotted line) with a good match with measured data (a) Output characteristics with V_{GS} = 2-10 V in steps of 2 V. (b) Transfer characteristics with V_{DS} = 0.1 V & 10 V.

6.2.2 Mobility versus Channel Charge

In describing carrier transport in amorphous semiconductor materials, the electrons trapped in the tail states are associated with the mobility and models typically employ an effective field-effect channel mobility expressed in Equation (6.9) [211].

$$\mu_{eff} = \mu_{ch}\left(\frac{Q_{free}}{Q_{free} + Q_{trap}}\right) = \mu_{ch}\left(\frac{Q_{free}}{Q_{total}}\right) \qquad (6.9)$$

where Q_{free}, Q_{trap}, and Q_{total} represent the free electron charge, trapped charge, and total charge, respectively. In the case of amorphous silicon (a-Si), associating the free/total charge ratio with an effective channel mobility is appropriate because the carrier mean free path is on the order of the chemical bond length [197]. The process of electron capture in localized states and re-emission into extended states degrades the effective carrier mobility.

The electron mean free path in IGZO is significantly more than the interatomic distance [35], [212] and electron transport is dominated by band conduction behavior as discussed in Section 5.5 [35], [54]. Charge trapped in band-tail states indeed coincides with a deficit in free electrons, however the effect on device operation can be considered independent of the electron channel mobility. As the gate voltage is applied, some of the induced charge is trapped in tail-states and lowers the level of accumulation charge available for channel conduction. When the gate voltage is further increased, the E_F moves closer to conduction band (stronger accumulation) and provides more and more electrons in the conduction band and hence higher current drive. Due to the continuous decrease in available states, the g_m for IGZO devices shows a gradual increase with V_{GS}. This is depicted by simulation shown in Figure 6.11 where the g_m keeps increasing with the V_{GS}

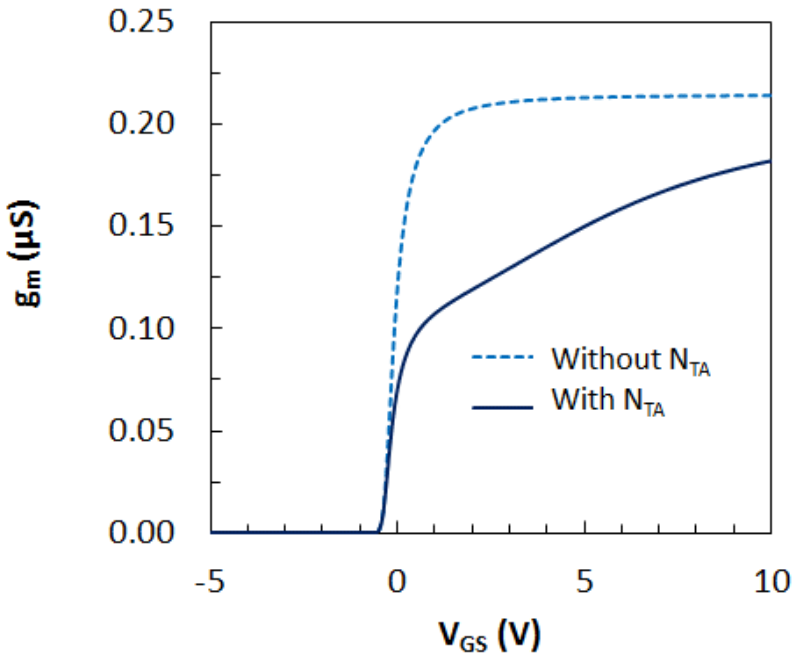

Figure 6.11: Simulated transconductance (g_m) for IGZO TFTs at V_{DS} = 0.1 V, with and without the use of band-tail states in the material model.

when tail states are incorporated in the material model. Without band-tail states g_m reaches a maximum value and remains constant, reflecting a linear I_D-V_{GS} relationship. This V_{GS} dependent transconductance (g_m) is purely related to channel charge and should not be interpreted as an increase in channel mobility.

6.3 IGZO TFT MODELING

There have been several reports of analytical solutions for the electrostatic operation of IGZO transistors that incorporate the influence of band-tail states. In analytical models that consider the level of free electron charge and trapped charge only as a function of gate bias, the ratio Q_{free}/Q_{total} typically ignores the influence of the drain voltage on the occupancy of band-tail states and the corresponding alteration in free electron charge [213]–[215]. Furthermore, analytical derivations often lead to transcendental equations which have no closed-form solutions, and require an intermediate electrical response (*e.g.* surface potential [216]–[219] charge density [220]–[223]) to serve as an independent variable and enable a solution for the output-input (*i.e. I-V*) relationship. Such physically based models may resort to empirical relationships to represent the device operation in a useable form with departure from the physical origin [214], [224].

6.3.1 Gate-Impressed 1D Model

A 1D gate-impressed modification in free channel charge due to the filling of band-tail trap states is presented in Equation (6.10).

$$\frac{Q_{free(1D)}}{Q_{total}} \approx \eta_G = \frac{1}{1+\theta'[V_{DD}-(V_{GS}-V_T)]} \quad (6.10)$$

where η_G represents the gate-impressed free charge ratio, and θ' is a fitting parameter which accounts for the effective loss of accumulation charge due to trapping. The symbol θ' was chosen to represent this effect because of the similarity in modeling the effect of normal-field degradation on channel mobility for traditional MOS transistors. In this case θ' accounts for an increase in the rate of change of accumulation charge with respect to V_{GS}, which eventually becomes constant as the rate of change of trap filling is diminished. This is illustrated in Figure 6.12.

Using $\mu_0\eta_G$ in place of μ_{ch} in Equation (6.1), the following relation is obtained:

$$I_D = \frac{W}{L} C'_{OX}\mu_0\eta_G\,[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}] \quad (6.11)$$

Replacing η_G from Equation (6.10), I_D can be written as a function of V_T, μ_0 and θ'.

$$I_D = \frac{W}{L} C'_{OX}\mu_0\,[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}]\cdot\frac{1}{1+\theta'[V_{DD}-(V_{GS}-V_T)]} \quad (6.12)$$

The values of V_T, μ_0 and θ' can be found using regression analysis with minimum mean square error to measured transfer characteristics taken at low drain bias. As previously discussed, traditional methods of parameter extraction for threshold voltage and electron channel mobility are not possible with a g_m characteristic shown in Figure 6.11. Other methods of extracting these parameters that have been proposed for IGZO TFTs are highly dependent upon specific device behavior and often result in ambiguous interpretation [192], [208], [225]–[227]. The μ_0 term represents a voltage-independent electron channel

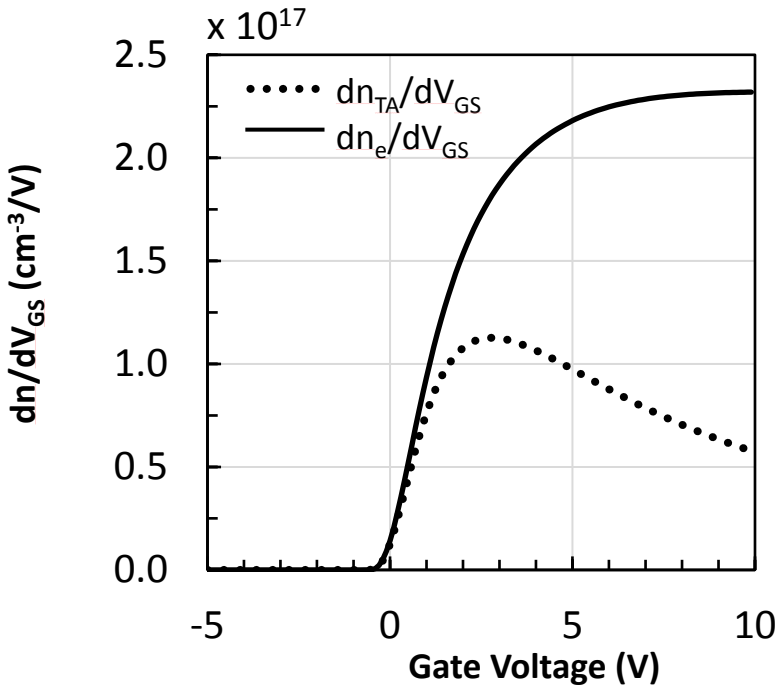

Figure 6.12: Simulated rate of change of electron concentration (n_e) & ionized acceptor band-tail states (n_{TA}) adjacent to the gate dielectric at the center of the channel.

mobility, not just an empirical fitting parameter [214], [218], and matches well with the TCAD intrinsic electron mobility, having agreement within 6% which is comparable to uncertainty in the true physical channel length (see Table 6-I).

6.3.2 Drain-Impressed 2D Model

The combination of applied gate and drain voltages determines the occupancy condition of band-tail states, and thus establishes the amount of free electron charge available. As the drain bias is increased, there is a release of trapped electrons from the acceptor-like tail-states as E_F lowers, as depicted in Figure 6.13, with an associated loss in free electron channel charge. The influence of drain-impressed deionization is strong until saturation as shown in Figure 6.14a, resulting in a spreading of the output conductance.

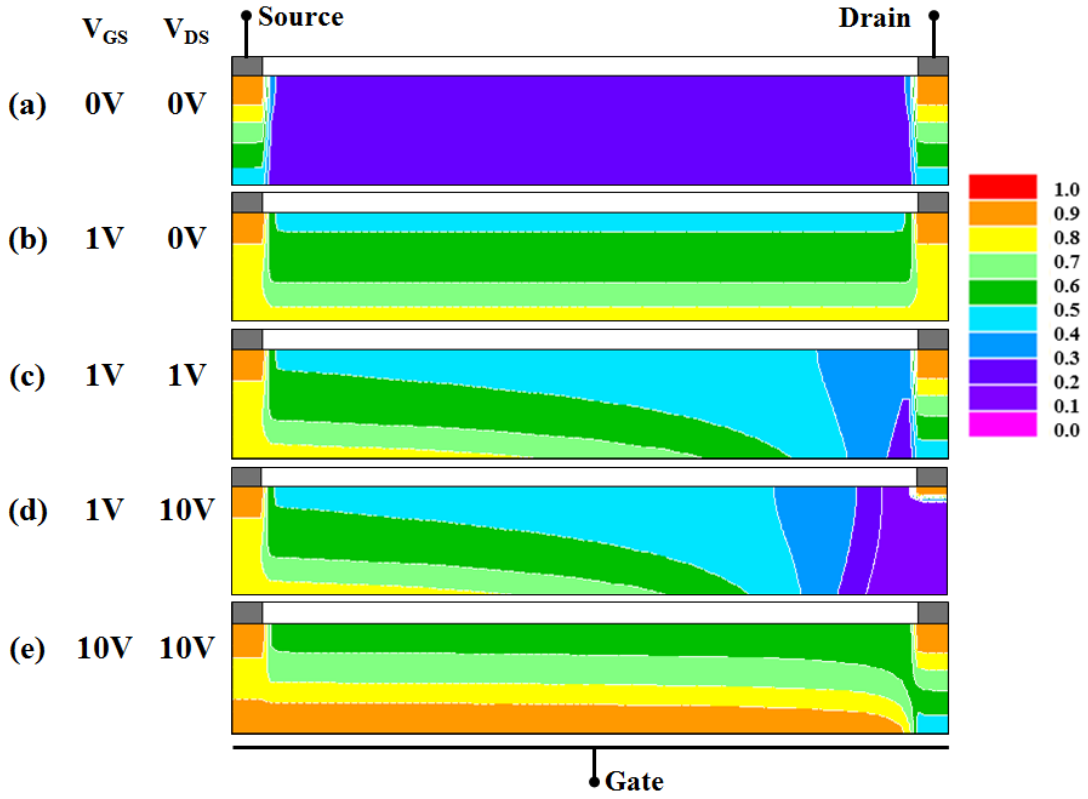

Figure 6.13: 2D contours of the probability of occupation of band-tail states within the IGZO body under different bias conditions as indicated. (a) Zero-bias condition where most of the states are empty. (b) 1D case where state occupation follows V_{GS}. (c) Drain-impressed deionization under low bias conditions, showing a significant 2D effect. This occurs in a continuous fashion over all drain bias conditions. (d) Intensified deionization in saturation, where V_{DS} >> V_{GS}. (e) Gate reclaims dominant control over state occupation as V_{GS} is increased, however 2D effect remains.

The effect of drain-impressed deionization translates to an effective potential loss at applied V_{DS} values lower than $V_{(Dsat)}$, and a measurable loss in saturation current (I_{Dsat}). The effective drain-source voltage can be expressed by applying a proportionality constant (α) to V_{DS} as follows.

$$V'_{DS} = \alpha V_{DS} \qquad (6.13)$$

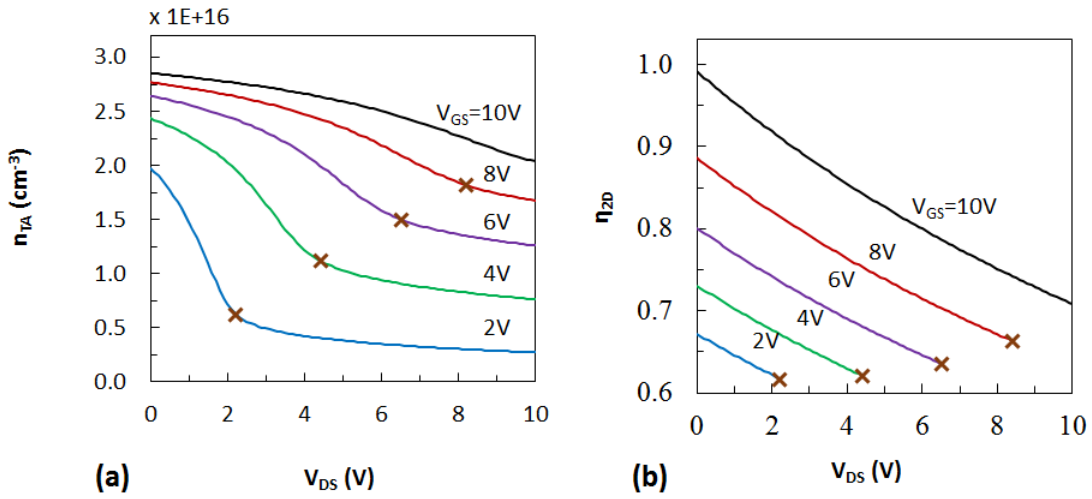

Figure 6.14: (a) Ionized acceptor band-tail state density in the IGZO channel adjacent to the drain over the full range of gate and drain bias conditions. The effect of drain-impressed deionization is decreased once $V_{DS} \geq V_{(Dsat)}$, identified with × points and defined in Equation (6.17). (b) The free/total charge ratio over the full range of gate and drain bias conditions. Note that the η_{2D} ratio is only meaningful in non-saturation.

The lower I_{Dsat} can be explained by a corresponding decrease in Q_{free}. A drain-impressed modification in free channel charge is given by Equation (6.14).

$$\frac{Q_{free(2D)}}{Q_{free(1D)}} \approx \eta_D = \frac{1}{(1 + V'_{DS}/V_C)} \tag{6.14}$$

where η_D represents the drain-impressed free charge ratio, and V_C is a characteristic voltage related to the occupancy of trap states. Note that this mathematical adjustment strongly resembles a Level 2 SPICE model for velocity saturation, though η_D is significant under relatively low electric fields. The superposition of the gate-impressed and drain-impressed adjustments in free electron channel charge is the product of Equation (6.10) and Equation (6.14), expressed in Equation (6.15).

$$\frac{Q_{free(2D)}}{Q_{total}} \approx \eta_{2D} = \eta_G \times \eta_D \qquad (6.15)$$

where η_{2D} represents the free charge ratio under specific gate and drain voltage conditions. This ratio is shown in Figure 6.14b, which corresponds to the concentration of ionized band-tail states shown in Figure 6.14a.

Using $\mu_o \eta_{2D}$ in place of μ_{ch} and replacing V_{DS} with V'_{DS} in Equation (6.1), the on-state device operation can be accurately represented by Equation (6.16) as shown in Figure 6.15, with model parameters found using least squares regression analysis, listed in Table 6-I. Note that Equation (6.16) is applicable for all applied 0 V ≤ V_{DS} ≤ V_{Dsat} and $V_{GS} \geq V_T$.

$$I_D = \frac{W}{L} C'_{OX} \mu_o \eta_{2D} [(V_{GS} - V_T) V'_{DS} - \frac{(V'_{DS})^2}{2}] \qquad (6.16)$$

Table 6-I also lists the TCAD value for electron mobility as a material input, and the simulated flatband voltage (V_{FB}). The difference between the device model and TCAD mobility values is less than 6% and the model V_T is a perfect match to V_{FB}, both of which exemplify the physical connection.

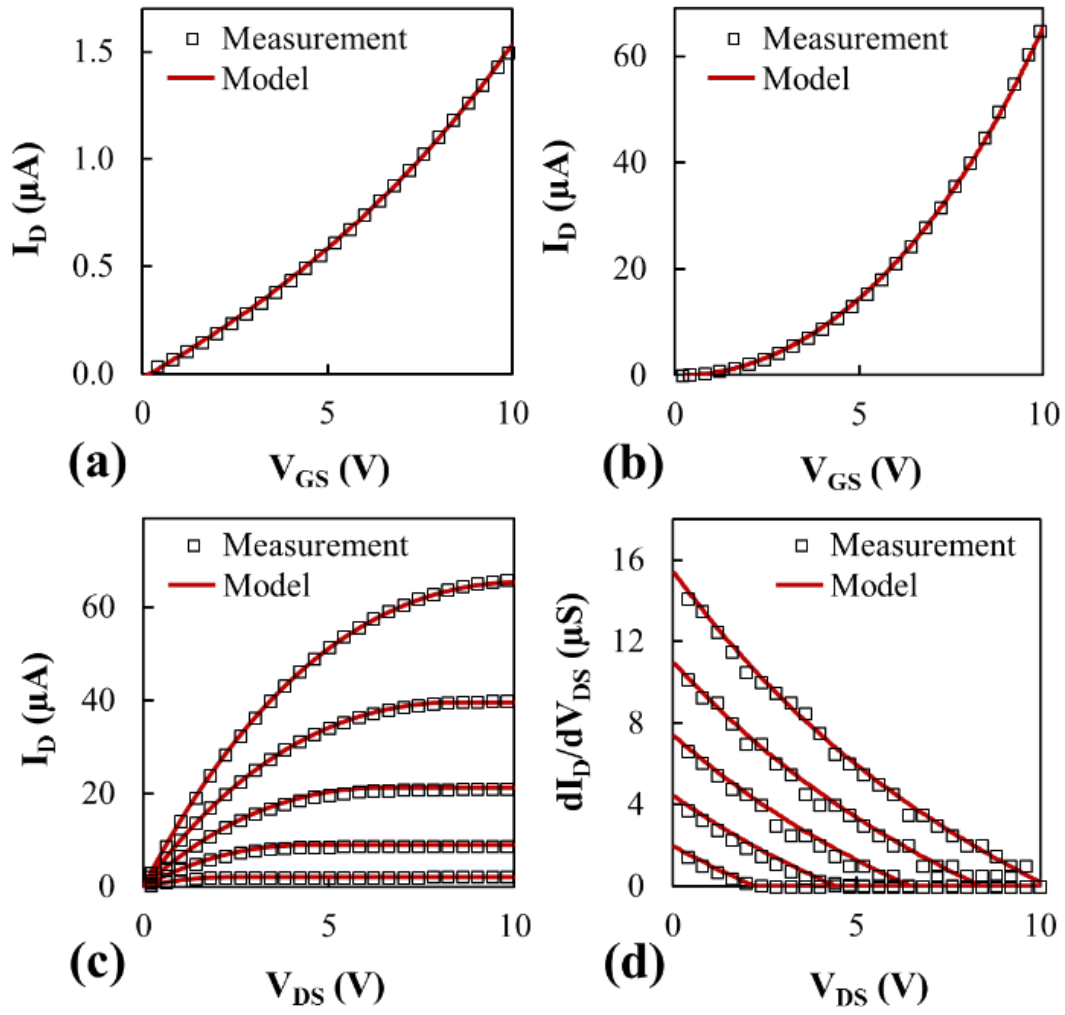

Figure 6.15: Overlay of transfer and output characteristics of measured data and the presented model. Transfer characteristics are shown in linear mode (a) with V_{DS} = 0.1 V, and saturation mode (b) with V_{DS} = 10 V. (c) Output characteristics with V_{GS} = 2-10 V in steps of 2 V. (d) Differential output conductance over the same V_{GS} range as in (c), showing an excellent match with the model.

Table 6-I: Electrical parameters extracted using the 2D device model and TCAD simulation.

Device Model					*TCAD*	
V_T	μ_0	θ'	α	V_C	μ_{TCAD}	V_{FB}
0.14 V	12 $cm^2/V{\cdot}s$	0.06 V^{-1}	0.8	20 V	12.7 $cm^2/V{\cdot}s$	0.14 V

Figure 6.15 shows an excellent match between the model and the measured data. Alternative model adjustments such as drain current scaling, gate voltage scaling, or inclusion of a series resistance can indeed result in lower current levels, however the overall match to output characteristics is poor without additional bias-dependent fitting parameters. As shown in Figure 6.15c, the model provides an accurate transition into the saturation regime as V_{DS} approaches V_{Dsat}. The accuracy of Equation (6.16) is reinforced in Figure 6.15d, which shows the differential output conductance over the entire range of bias conditions.

By differentiating Equation (6.16) with respect to V_{DS} and setting the result equal to zero, the solution for V_{Dsat} is given by:

$$V_{D_{sat}} = \frac{\sqrt{{V_C}^2 + 2V_C(V_{GS} - V_T)} - V_C}{\alpha} \qquad (6.17)$$

which approaches $(V_{GS} - V_T)/\alpha$ at small V_{GS}. The clear definition of V_{Dsat} in Equation (6.17) enables a straightforward accommodation of channel length modulation as required by shorter channel devices.

6.4 CONCLUSION

In this chapter, various conventional methods for V_T and μ_{ch} extractions using drain current measurements have been compared and the associated shortcomings are discussed. The presence of band-tail states and V_{GS} dependent $R_{S/D}$ manifests itself in non-ideal response of current to voltage. Therefore the traditional methods used for silicon devices are not adequate for IGZO TFT modeling.

This work presents a new device model for the on-state operation of IGZO TFTs, which considers the influence of the drain bias on the occupancy of band-tail states and free channel charge. Deviation from non-ideal *I-V* behavior is entirely attributed to the ionization and deionization of acceptor-like band-tail states, as controlled by both the gate and drain bias conditions. The model includes two parameters which regulate the level of free channel charge, and one parameter which accounts for spreading of the output conductance. The parameters are used in model elements which preserve the distinction between the gate-impressed and drain-impressed response, with dissociation from an effective channel mobility. The model provides an excellent match to both measured and TCAD simulated transfer and output characteristics over all on-state bias conditions. Additional advantages of the presented model are the physical foundation, mathematical simplicity, and compatibility with a Level 2 SPICE model platform.

Chapter 7. INTERPRETATION OF NATIVE AND STRESS-INDUCED ANOMALIES

IGZO is intrinsically an n-type semiconductor due to the presence of oxygen vacancies (V_O) acting as donors [66] which also makes the IGZO surface very sensitive to the ambient oxygen [56], [70]. The readiness of IGZO surface to interact with the ambient air is also responsible for some non-ideal electrical response observed in transistors such as threshold voltage shift under room ambient storage [228], bias-stress induced instabilities [107], [229] and other distortions observed in transfer characteristics [169], [180], [230]. This chapter is devoted to the investigation of process integration schemes to address such behavior.

One such non-ideal electrical response is the separation of low and high drain bias transfer characteristics in subthreshold region which is reminiscent of drain induced barrier lowering (DIBL) observed in conventional MOSFETs. Electrical measurements and TCAD simulations are used to develop the hypothesis on the origin of non-ideal behavior observed, which can be suppressed by appropriate process and/or device modifications.

It is important to perform bias-induced instability tests on TFTs as the application of this technology in flat panel display products requires prolonged on/off states. The devices must be stable against any subsequent processing after passivation for TFT integration in display array. This was investigated by application of thermal stress on finished devices. Gate electrode configurations and process integration schemes which improve the device stability against thermal and bias stress, are also discussed.

7.1 TRAP ASSOCIATED BARRIER LOWERING

Figure 7.1 shows the DIBL-like behavior in the transfer characteristics of an unpassivated long-channel bottom-gate (BG) device tested immediately after anneal (dashed line). This behavior has been presented in literature, but the issue has been generally omitted from discussion [9] or assigned to short-channel behavior even when the channel dimensions are in micrometer range [231]. TCAD simulation shows that with the IGZO material model, including interface traps, and the physical device structure parameters, DIBL should not become apparent until the channel length is scaled below 1 μm. Therefore, a proper understanding of the underlying physical mechanism behind this phenomenon in "long" channel IGZO devices is required.

It is proposed that this DIBL-like effect is due to inhomogeneity of donor trap states at the topside IGZO interface that presents regions with distinctly different effective charge levels. Due to the involvement of traps, this phenomenon is referred as Trap Associated Barrier Lowering (TABL). This section presents a comprehensive investigation on the TABL resulting in a hypothesis on its origin that is further supported by TCAD simulation.

7.1.1 IGZO Back-Channel Ripening

The device shown in Figure 7.1 exhibited improvement after two days of storage in air ambient (solid line), with perfect overlay of low and high drain bias curves. Note that devices stored in vacuum after anneal did not exhibit any improvement over time which inferred that the ripening process relies of the IGZO back-channel to the room-ambient air. The manifestation of this phenomenon in an L = 21 μm TFT demonstrates that it is not a short-channel effect.

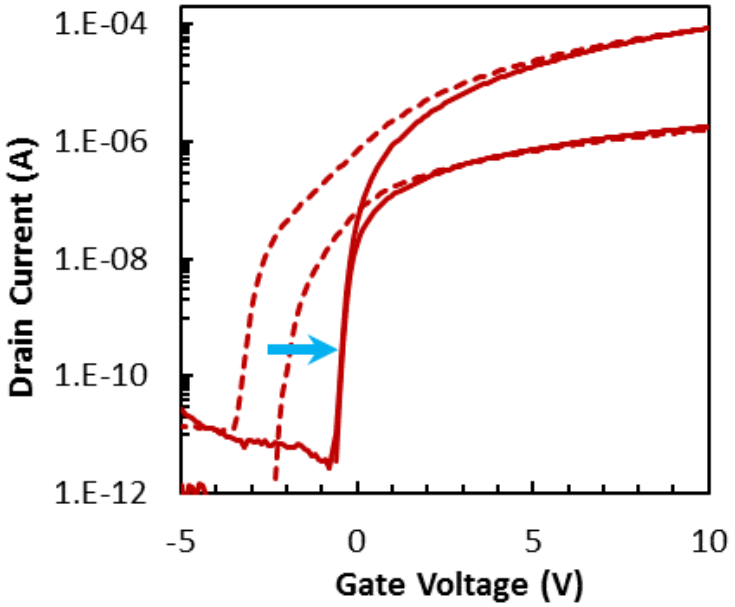

Figure 7.1: Transfer characteristics of an unpassivated TFT tested immediately after annealing (dashed line) showing TABL. After a two-day storage in room ambient the characteristics do not exhibit TABL (solid line).

The TABL mechanism has been attributed in literature to the moisture absorption in the IGZO channel [180] or back-channel defects [232]. However, an electrical model has not been reported. It is important to point out that the ripening time is channel length dependent. For a long-channel device (L = 21 µm), one day of ripening is sufficient while a short-channel TFT (L = 3 µm) may require a week. The behavior is also statistical in nature i.e., 90% of L = 21 µm devices show TABL when tested immediately after annealing, however the percentage drops down to 10% after a day of room ambient storage.

For passivated devices, the IGZO back-channel is not exposed to interact with the room air ambient. The back-channel passivation process does not support ambient ripening and TABL did not disappear over time. Figure 7.2 shows the TABL for BG passivated

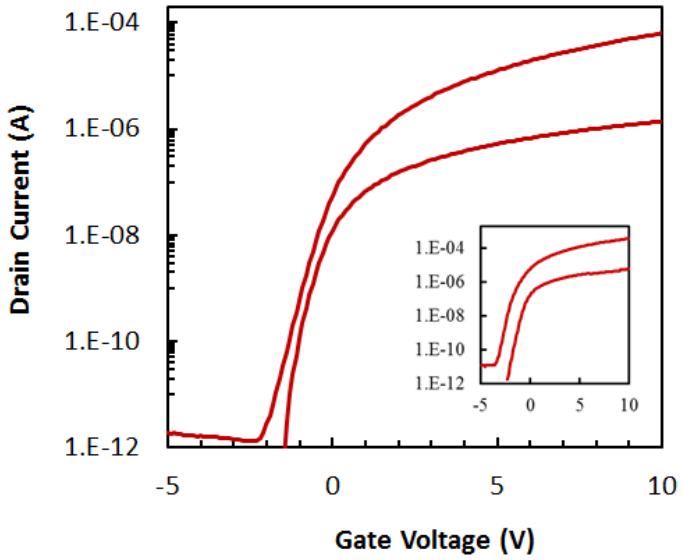

Figure 7.2: Measured data for a L=21 µm BG device with 100 nm SiO_2 passivation, showing TABL. Inset shows the transfer characteristics for L=3 µm device showing pronounced distortions for a scaled device.

device. An L = 3 µm TFT transfer characteristics show the severity of the distortions for scaled devices, see the inset of Figure 7.2.

7.1.2 Ripening of Revealed IGZO Back-Channel

To investigate if ripening is a surface phenomenon, the device shown in Figure 7.1 was partially etched in dilute HCl to remove the back-channel surface layer. Figure 7.3 shows the evolution of transfer characteristics for this device. The partially etched TFT showed TABL just like a fresh device. A two-day ripening alleviated these distortions. These investigations suggest that TABL is a surface phenomenon and exposed IGZO surface has high density of trap states which need to be passivated through interaction with air ambient.

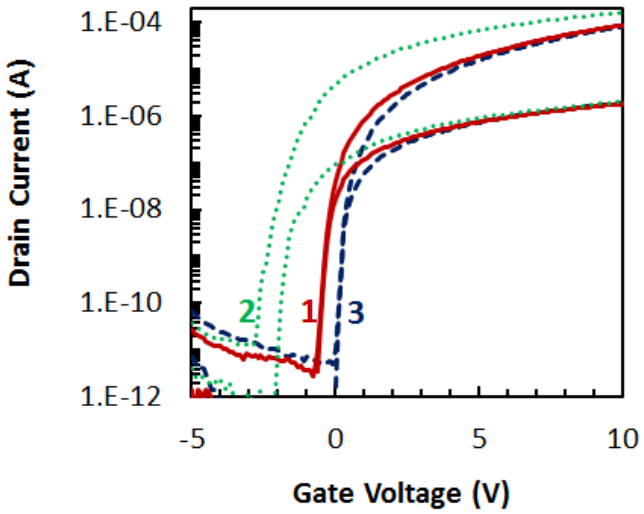

Figure 7.3: Same device as shown in Figure 7.1 after partial etch of the aged back-surface; device started exhibiting TABL '2'. These distortions are alleviated by a two-day ripening process '3'. The difference in V_T for ripened device before '1' and after '3' etch is due to the difference in the IGZO channel thickness.

7.1.3 Hypothesis on the Mechanism of TABL

It is proposed that the TABL is due to the inhomogeneous passivation of the donor traps at the IGZO interface that presents regions with distinctly different effective charge levels. This results in a series/parallel network of channel regions to complete the electron pathway from source to drain. Figure 7.4a shows a schematic model of this concept. If donor-rich interface regions are separated from each other by narrow gap regions without donor states, then the accumulation of gaps can be represented by a single gap within the channel. TCAD structures for "gap" devices were developed using the same material and interface state models as used for passivated devices (Section 5.4.2). The gap is a 0.4 µm region void of donor interface trap states positioned in the center of the channel. While the simulation model uses oxygen donor interface states to represent the donor-rich regions,

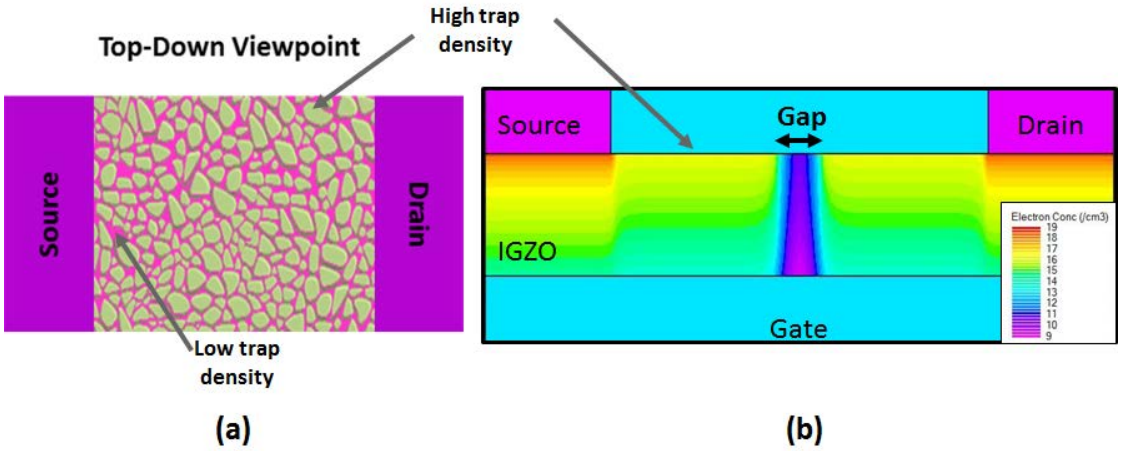

Figure 7.4: (a) Schematic model for the TABL origin, showing a cobblestone arrangement of donor-rich interface defect regions separated by low-charge gaps. (b) Simplified structure for TCAD simulation, representing the low-charge gaps as a single gap in the middle of the channel. The contours show the electron concentration at zero-bias, with values in donor-rich interface defect regions and the low-charge gap differing by several orders of magnitude. Note that the scales used for the X & Y axes are significantly different.

another donor mechanism may be operative such as the incorporation of hydrogen [233] or water [108]. Figure 7.4b shows the TCAD structure for the gap device.

Figure 7.5 shows the conduction band energy across the channel at low and high drain biases. At high V_{DS}, the drain dominates causing the lowering of barrier associated with back surface traps. This lowering of barrier results in an earlier turn-on at high drain bias. For low drain bias, the pockets of low charge dominate and the device turns on at higher V_{GS}. This difference in on-voltage for low and high drain bias is revealed as TABL. The current flow is dominated by highly resistive (low surface charge) regions; a long channel device has a higher probability to create low-charge gap regions during a short ripening process time. Shorter channel devices have a lower probability to create a separation distance that dominates turn-on behavior, and thus require longer ripening time.

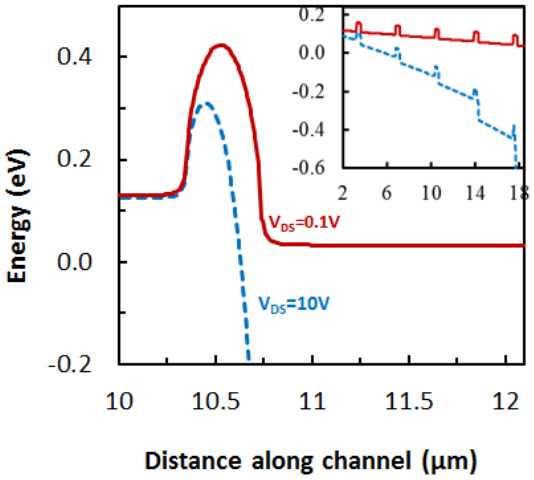

Figure 7.5: Conduction band energy across the channel at low and high drain bias showing the barrier created by the low charge pocket (gap) shown in Figure 7.4b. At high drain bias (dashed line) the barrier is lowered. The inset shows TABL in distributed fashion.

TABL is attributed to the random distribution of donor trap states at IGZO back-surface. In BG configuration gate is located on the other side of the defect-rich surface and therefore has weaker control over the trap states. Figure 7.6a shows the simulation of TABL for BG and DG configuration with respect to IGZO thickness for an L = 3 µm device. TABL is quantified by measuring the separation between low and high drain bias characteristics at I_D =100 pA. As IGZO thickness increases, the influence of bottom gate on the back-channel trap states reduces and larger TABL is seen. The effect of gap spacing on TABL is shown in Figure 7.6b. A 10 nm thick IGZO channel is used for these simulations which allowed to use very fine mesh for accurate modeling. The TABL is negligible for extreme cases *i.e.* fresh device (all surface donor-traps) and ripened device (no surface donor-traps). Once the gap spacing is longer then a minimum distance, drain can no longer overcome the gap. Both low and high drain biases turn on at the same V_{GS}.

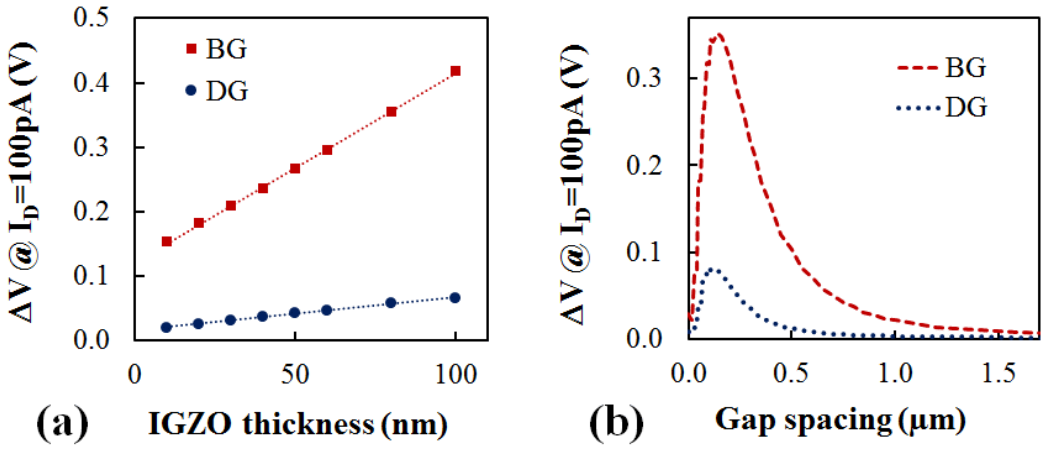

Figure 7.6: (a) TABL plotted against the gap spacing for a L= 3 μm device. TABL is characterized by measuring the separation between low & high drain bias characteristics at I_D=100 pA. The effect is suppressed for DG structure. (b) TABL with respect to IGZO channel thickness. The effect is pronounced for thicker IGZO channel as gate control over interface states is weakened.

The simulations also suggest that a double-gate configuration suppresses the TABL as shown in Figure 7.6.

Electrical simulations for gap device along with no-gap references are shown in Figure 7.7a. Simulation data of TFT with DG configuration are shown in Figure 7.7b. The dotted and broken line references included for comparison in each of the plots in Figure 7.7 demonstrate the high-drain bias (saturation operation) behavior with "all" donor interface traps (fresh device), and the low-drain bias (linear operation) without interface traps (ripened device). These conditions represent left-shift and right-shift limits for a device tested at high-drain bias and low-drain bias, respectively. The BG gap device demonstrates TABL (Figure 7.7a), whereas this effect is completely suppressed in the DG gap device (Figure 7.7b). While the values chosen for interface trap density and gap

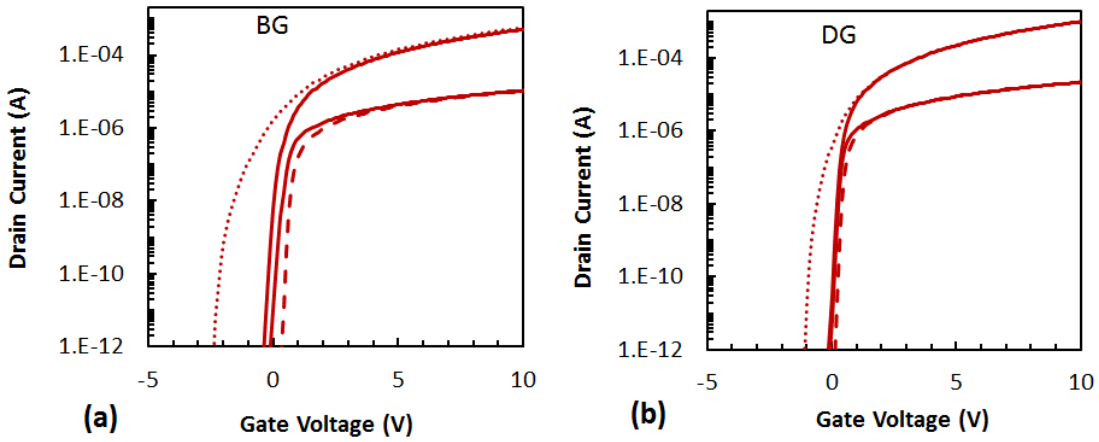

Figure 7.7: Simulation of BG (a), and DG (b) gap devices with all interface traps (fresh device) and no interface traps (ripened state) limits for high (dotted) and low (dashed) drain bias operation. Simulations of single-gate structures exhibit TABL behavior, while this effect appears insignificant on DG devices.

spacing were for demonstration purposes, the TCAD simulations model the TABL of the BG device characteristics quite well (compare Figure 7.7a to Figure 7.2).

7.1.4 Double Gate IGZO TFT

Simulation predicts that TABL can be suppressed for DG TFT. TFTs with BG and DG configurations were fabricated. The DG process is an extension of the BG process sequence, and these device types were fabricated simultaneously on the same wafers. A molybdenum gate electrode was sputtered and patterned, followed by a 100 nm SiO_2 gate dielectric deposited by PECVD (TEOS precursor, 390°C). A 50 nm IGZO layer was sputtered using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen, and then patterned and etched using dilute HCl. The source/drain contact metal stack (50 nm Mo/250 nm Al) was then defined using a lift-off resist process.

A second 100 nm PECVD SiO_2 layer, which serves as the passivation material for BG and top gate dielectric for the DG device, was then deposited. This was followed by a

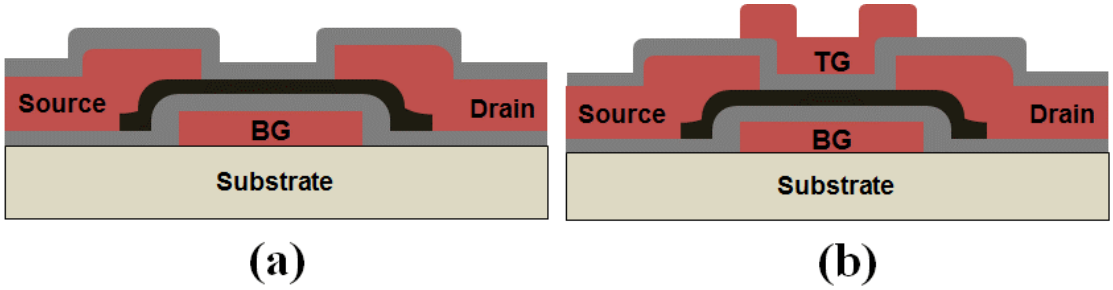

Figure 7.8: Cross-section schematics of passivated BG and DG TFTs. The DG device has the staggered electrode configuration of the BG device, with the addition of a co-planar top gate. Note that the bottom and top gate electrodes in the DG device are electrically connected through a contact not shown.

4 h O_2 anneal at 400°C with a 5 h controlled ramp-down in O_2 ambient. The gate contact regions were opened, and top-gate electrodes were then defined for DG devices using evaporated aluminum with a lift-off resist process. Source/drain contacts were then opened for electrical probing. The schematic cross-section of the devices is shown in Figure 7.8.

The transfer characteristics of short-channel (L = 3 µm) DG TFT fabricated using the described process flow are shown in Figure 7.9. These devices were made on the same wafer as passivated BG TFTs shown in Figure 7.2. As predicted by the simulation, the DG TFTs did not show any TABL even for scaled devices (compare Figure 7.7b to Figure 7.9).

7.1.5 Refined TCAD Model for Back-Channel SiO_2

Figure 7.10 shows the measured and simulated transfer characteristics of a SiO_2 passivated device after 4 h anneal in O_2 ambient at 400 °C as shown in Section 5.6. The interface defect states used for the simulation are presented in Table 7-I. The bulk defect states distribution are common to unpassivated devices. Values have been adjusted for interface traps density of states and fixed charge.

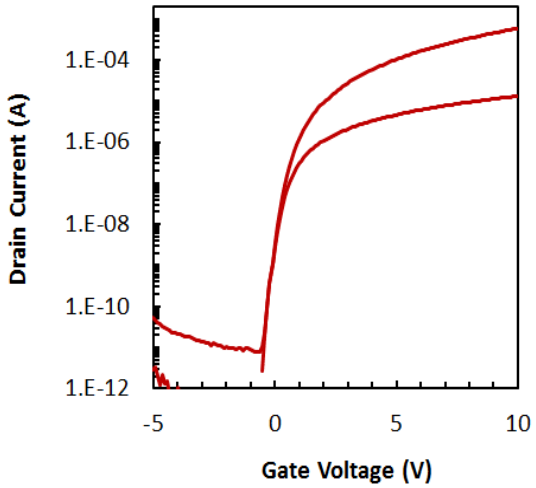

Figure 7.9: Transfer characteristics of a L=3 µm DG device showing complete suppression of TABL. This can be directly compared with BG device in Figure 7.2.

Table 7-I: Back-channel interface parameters used for simulation of PECVD SiO_2 passivated devices.

Symbol	Value
N_{Voi} (donor-like interface traps)	5×10^{11} $cm^{-2}eV^{-1}$
E_{Voi}	2.9 eV
W_{Voi}	0.1 eV
N_f (fixed charge)	-5.5×10^{11} cm^{-2}

The passivated devices exhibited improved stability over time compared to devices without any passivation material but the current drive and subthreshold slope suffered minor degradation. TCAD simulation demonstrates that this compromise can be mitigated if another controlling gate electrode is placed above this interface in a double-gate (DG) configuration. The placement of gate electrode towards the interface with higher defect states provides better control on the defects and suppress their role in device operation. Figure 7.11a shows a cross-section of a DG TFT channel region during the saturation mode showing the creation of two accumulation regions towards both bottom and top gate sides.

Figure 7.11b shows the overlay of TCAD simulations which compares bottom gate and double gate electrode configurations with common material and interface model parameters, as specified in Table 7-I. The double-gate (DG) arrangement shows significant improvement with clear benefits in both on-state and off-state operation.

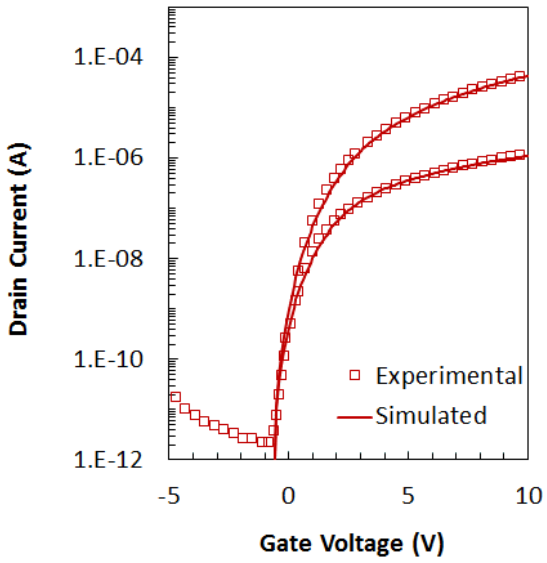

Figure 7.10: An overlay of measured (markers) and simulated (line) characteristics of a SiO_2 passivated BG IGZO TFT.

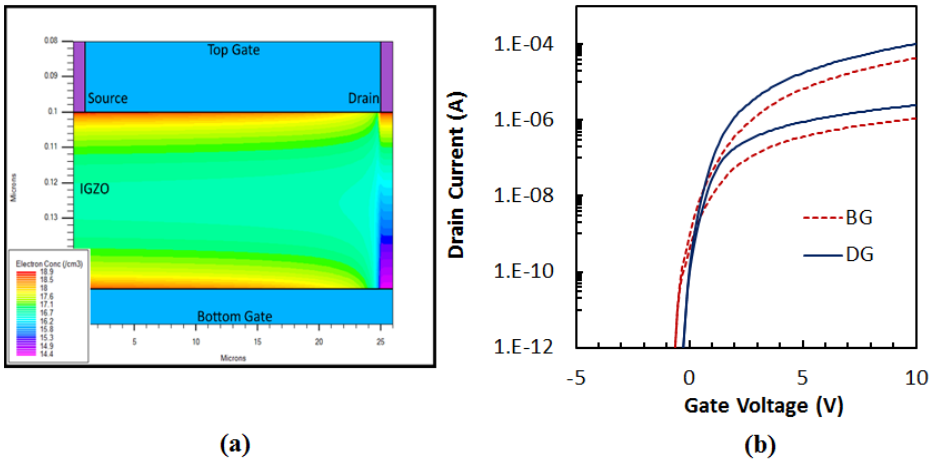

Figure 7.11: (a) Electron concentration contour at $V_{GS}=V_{DS}=10$ V in IGZO channel. (b) Simulated transfer characteristics of BG and DG electrode configurations showing improvements in current-drive and SS for DG TFT.

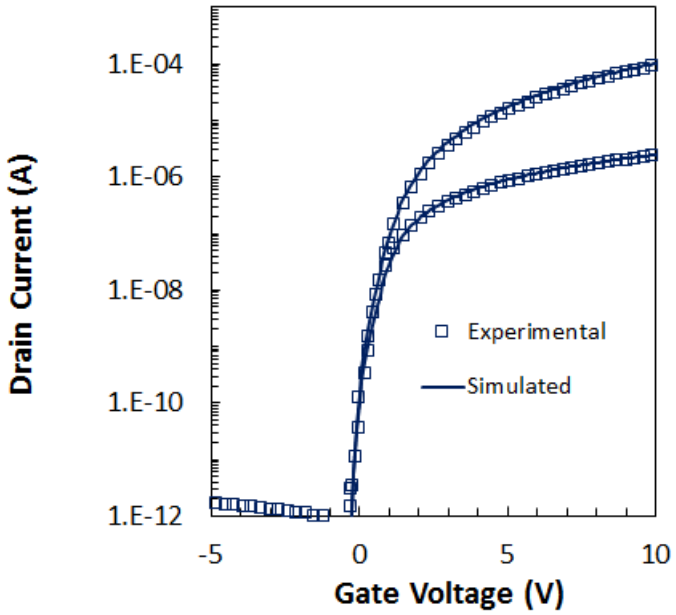

Figure 7.12: An overlay of measured (markers) and simulated (line) characteristics of a SiO_2 passivated DG IGZO TFT. The DG TFT demonstrate steeper SS and higher current drive compared to BG TFT shown in Figure 7.10.

The transfer characteristics measured on fabricated devices are shown in Figure 7.12 along with the simulated transfer characteristics. The excellent match between measurements and the simulations supported the interface defect distribution model employed. DG devices showed marked improvement in terms of a steeper subthreshold, a V_T that is right shifted from the BG device, and added current drive due to the additional accumulated electron charge.

7.2 BIAS INDUCED INSTABILITY

The response to bias-stress was investigated for both BG and DG device configuration. Positive bias-stress (PBS) and negative bias-stress (NBS) tests involved an application of +10 V and -10 V to the gate respectively, with source and drain held at reference ground.

Measurements were taken at various intervals over an accumulated time of 10,000 seconds under bias-stress, with results summarized in Table 7-II. Each device type demonstrated distinct response behavior. A characteristic shift in response to bias-stress can be attributed to the creation or trapping of charge in the dielectric region, the IGZO/SiO_2 interfaces, or the bulk IGZO material. Charge trapped in a dielectric or interface region that remains fixed induces a lateral characteristic shift, whereas changes in interface traps cause differences in characteristic distortion and spreading.

Table 7-II: BG and DG TFTs response to 10,000 seconds of bias-stress

	Voltage shift (V)	
	PBS	NBS
BG	-0.17	-1.3
DG	1.9	0.53

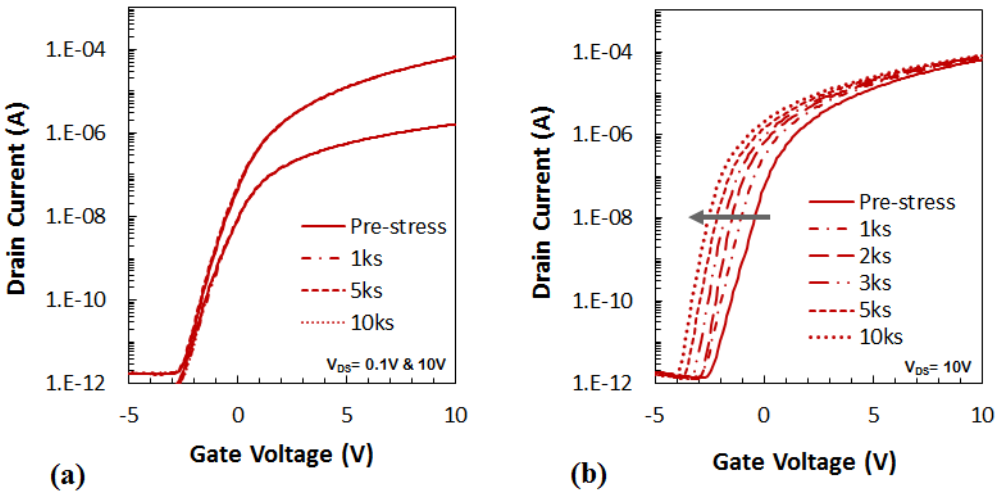

Figure 7.13: Select responses to PBS and NBS over 10,000 seconds for BG TFT. (a) BG response to PBS, showing no shift in characteristics (b) Response to NBS showing a pronounced left-shift and subthreshold steepening.

The BG devices had a negligible response to PBS, however NBS resulted in significant left-shifting (shift ~ -1.5 V) and subthreshold steepening as shown in Figure 7.13. The starting characteristic has a shallow subthreshold slope, indicating poor gate control over interface traps. Time under NBS appears to convert some of these donor-like traps into positive charge that remains fixed during transfer characteristic measurements.

A significant parallel right-shift was observed on DG devices for both PBS and NBS conditions, as shown in Figure 7.14. The evolution of threshold voltage shift with time for DG devices under PBS and NBS is shown in Figure 7.15a. The parallel right shift under PBS (shift ~ +2 V) is associated with electron injection and trapping in the SiO_2 regions in between the overlapped co-planar top-gate and source/drain electrodes (Figure 7.15b). Similar to PBS, under NBS conditions there will still be electron charge injection and trapping in the SiO_2 regions which supports a right-shift; however the magnitude of the observed shift is less than the PBS shift. The NBS left-shift response of

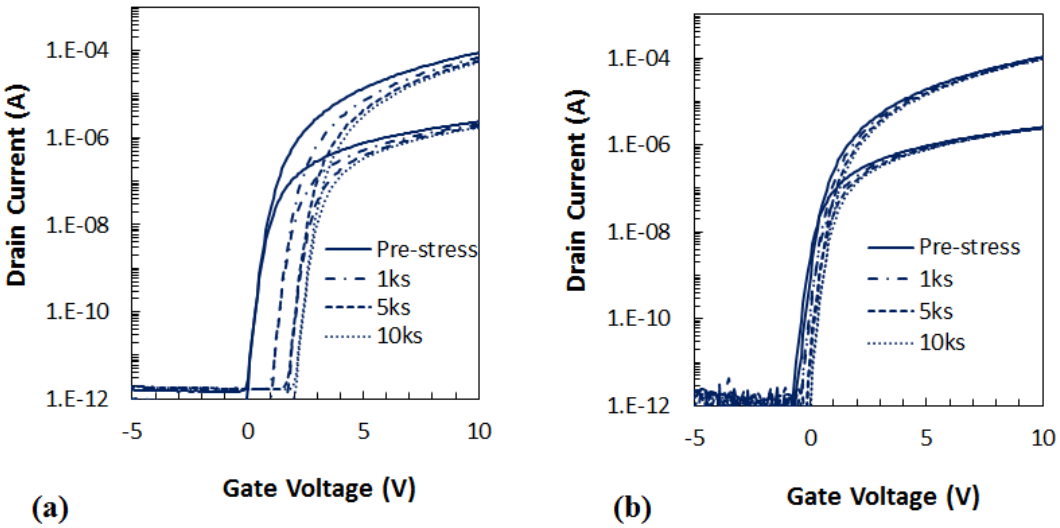

Figure 7.14: DG response to (a) PBS and (b) NBS showing parallel right-shift in both cases.

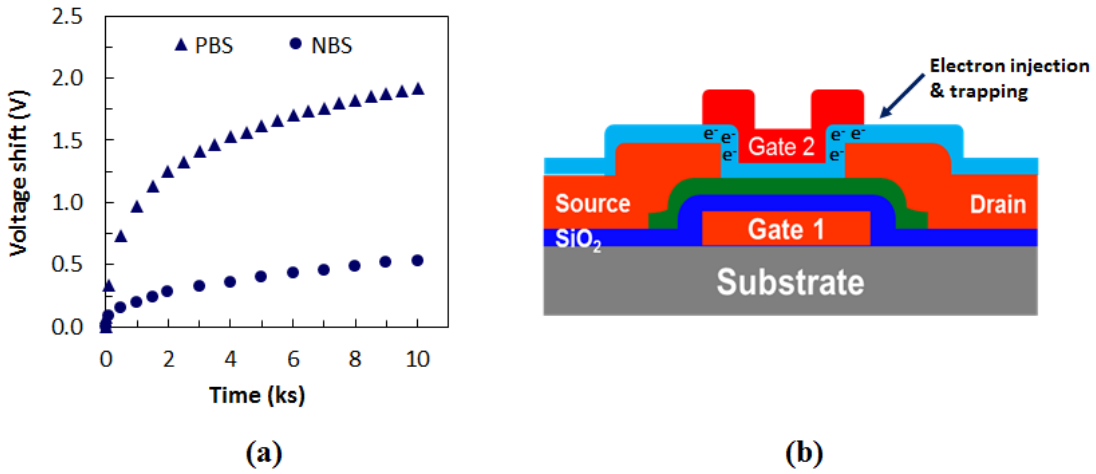

Figure 7.15: (a) DG device transfer characteristic voltage shift over time under NBS & PBS. (b) The positive shift which is operative under both PBS and NBS is attributed to the charge injection in the top-gate and S/D overlap region as shown in the schematic.

the BG device should be simultaneously operative on the DG device, thus the resulting response is attributed to the superposition of the two distinctive charge mechanisms (shift ~ +0.5 V). The DG transfer characteristics are steep throughout bias-stress testing due to improved electrostatics, as discussed earlier in Section 7.1.5.

Despite the noticeable improvement in device characteristics in DG TFT, the bias-induced instability remained a challenge. The results indicated that the electron injection in top gate dielectric is one of the reason for instability. A longer 8 h anneal at 400 °C was investigated to improve the TFT performance and dielectric quality [99], [108]. Figure 7.16 shows the transfer characteristics of 8 h annealed BG device under bias stress. The TFT performance exhibited marked improvements when compared with a shorter 4 h anneal (compare with Figure 7.13). This improvement in device operation after a longer anneal is attributed to the improved interface quality and oxidation state of IGZO channel during an 8 h anneal. Therefore, further investigations were conducted on devices with longer anneal.

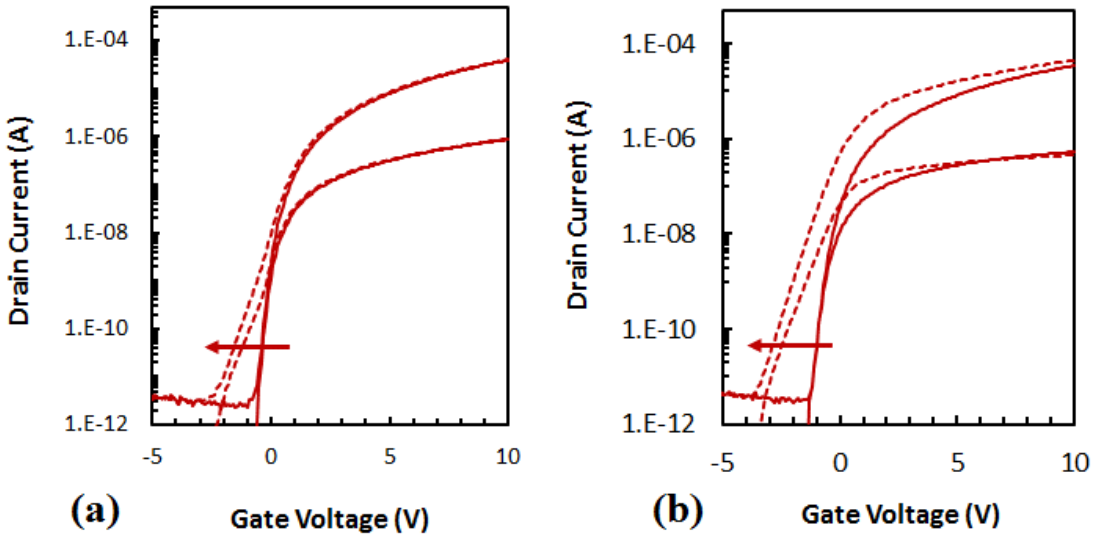

Figure 7.16: BG TFT response to (a) PBS and (b) NBS after an 8 h anneal in oxidizing ambient.

For bias stress, the devices showed distortions under PBS which were not observed for 4 h anneal TFTs (compare Figure 7.13a and Figure 7.16a). However the transfer characteristics post-PBS (Figure 7.16a) resemble the original response of 4 h annealed TFTs (Figure 7.13a). It indicates that the defect states responsible for the distortions in Figure 7.16a are already operative during the normal transistor operation for shorter anneal (Figure 7.13a). These defects are reconfigured through a longer anneal process, however under PBS they temporarily become operative. The origin of these states is not yet clear; several hours after PBS the characteristics were observed to return back to the initial state. The BG TFT annealed for 8 h also showed distortions in characteristics under NBS. Such distortions are attributed to the interaction of IGZO channel with the water, discussed previously in Section 2.4 [158], [235]. The TEOS SiO_2 passivation layer is susceptible to water vapor absorption present in room-air ambient. While investigating the temperature

dependence of bias-stress it was discovered that the devices degraded significantly at temperature above 100 °C, which signifies an interaction between water and IGZO.

7.3 THERMAL STABILITY OF IGZO TFT

To investigate the device behavior under thermal stress, devices were exposed to elevated temperature using a hot-plate bake. The initial measurements were taken at room temperature and then the hot plate temperature was increased in steps and transfer characteristics were measured. The voltage control of IGZO TFTs degrades significantly after exposure to thermal stress above 140 °C. Figure 7.17 shows the shift in transfer characteristics of BG and DG IGZO TFT after the thermal treatment for 1 h. This degradation is attributed to the reaction of water absorbed by the PECVD SiO_2 used for passivation with IGZO channel. The PECVD deposited SiO_2 is prone to water absorption present in the form of water vapors in air ambient. During thermal anneal the water diffuses towards the IGZO channel and causes an increase in the carrier concentration as water behaves as dopant in IGZO [108]. To alleviate this instability, process integration schemes to minimize the interaction of finished devices with the ambient were investigated.

It was shown in Section 4.5.2 that ALD alumina films are excellent barrier against the oxidants transport even at elevated temperatures which made it the primary choice for investigations as an encapsulation material.

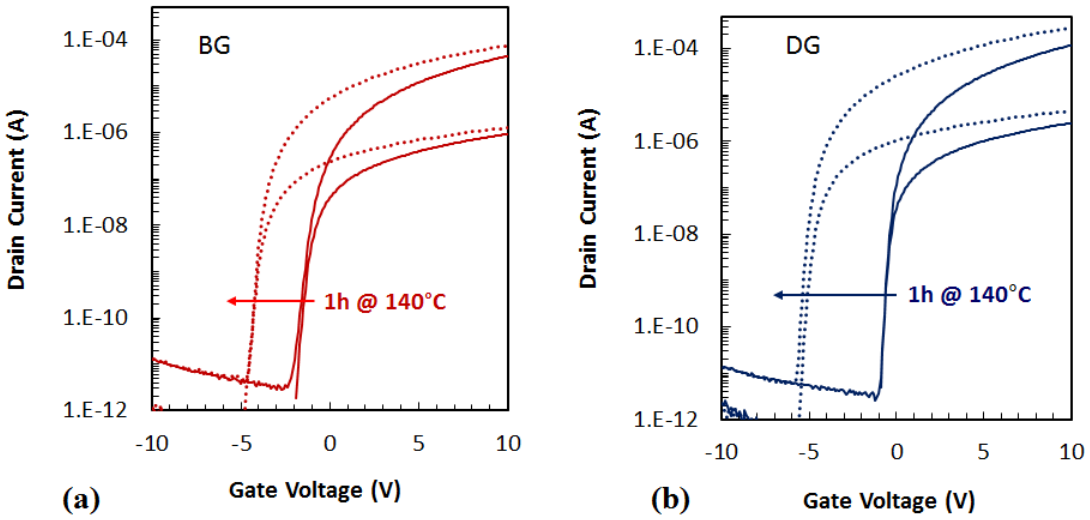

Figure 7.17: Transfer characteristics of (a) PECVD SiO_2 passivated BG TFT and (b) DG TFT. After one hour of thermal treatment at 140 °C the characteristics shifted left by ~ 3 V and 5 V for BG and DG respectively.

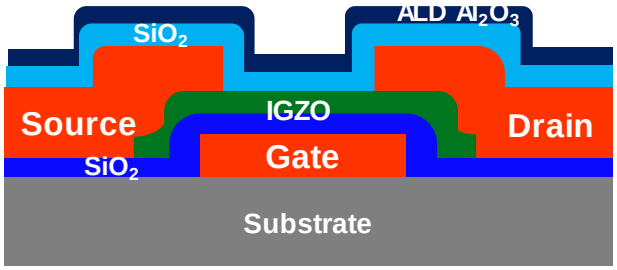

Figure 7.18: Schematic of ALD alumina encapsulated BG TFT.

7.3.1 IGZO TFT Encapsulation

Passivated BG devices were fabricated using the process flow discussed in Section 7.1.4 and annealed at 400 °C for 8 h. A 15 nm ALD alumina film was deposited immediately after the thermal anneal which was followed by contact opening using 10:1 BOE. The

schematic cross-section of final device is shown in Figure 7.18. For DG with ALD alumina, Al gate was evaporated and patterned subsequently.

7.3.2 Electrical Results for Encapsulated TFTs

The transfer characteristics of alumina encapsulated BG and DG TFTs are shown in Figure 7.19. The devices did not show any shift after an hour of thermal stress at 140 °C. This supports the hypothesis that the interaction of passivation/top gate-dielectric SiO_2 with room air ambient was responsible for the thermal instability. Minimizing the interaction of this PECVD SiO_2 with air ambient suppressed the thermal instability.

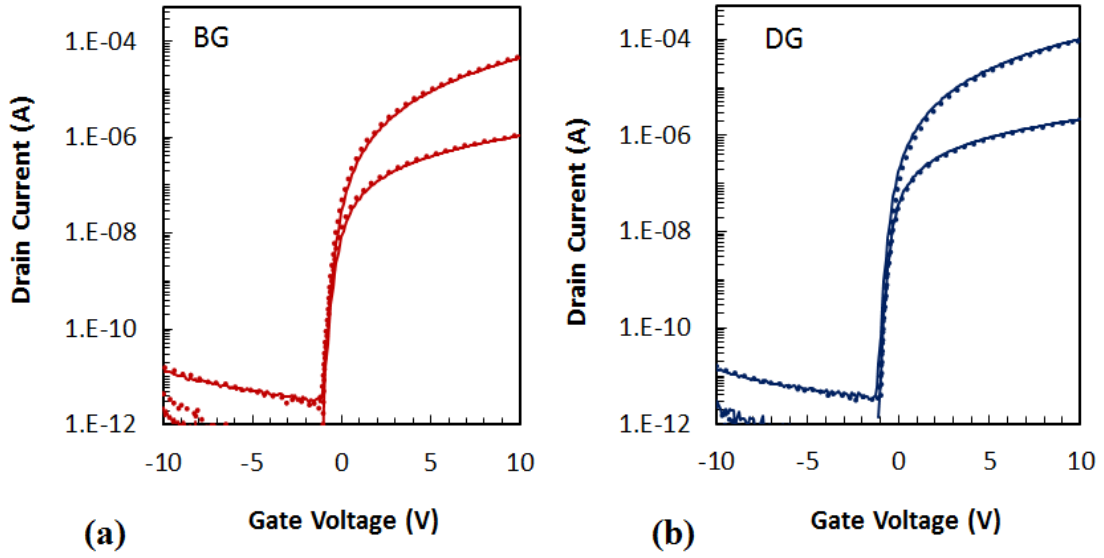

Figure 7.19: Transfer characteristics of alumina encapsulated (a) BG and (b) DG TFTs before (solid line) and after one hour thermal stress at 140 °C (dotted line), showing no shift in the characteristics.

7.3.3 Bias-Stress on Encapsulated TFTs

Water molecules or related complexes are reported to act as carrier trap centers which increase the instability under bias stress [121]. To minimize the role of water in bias-induced instability, further investigations on bias-stress were conducted on ALD Al_2O_3 encapsulated TFTs. Encapsulated BG devices, annealed at 400 °C for 8 h in O_2 ambient were tested against bias-stress. The results are shown in Figure 7.20.

The encapsulated devices showed good resistance against NBS compared to devices without encapsulation (see Figure 7.16b). Under PBS, the devices showed distortions similar to devices without encapsulation layer (Figure 7.16a). This suggests that the defect states responsible are not water related. Electrically, the distortions in characteristics appear due to the change in the electronic energy state of V_O (see Section 5.2.1). A decrease in V_O energy level from 2.9 eV to 2.6 eV would explain such

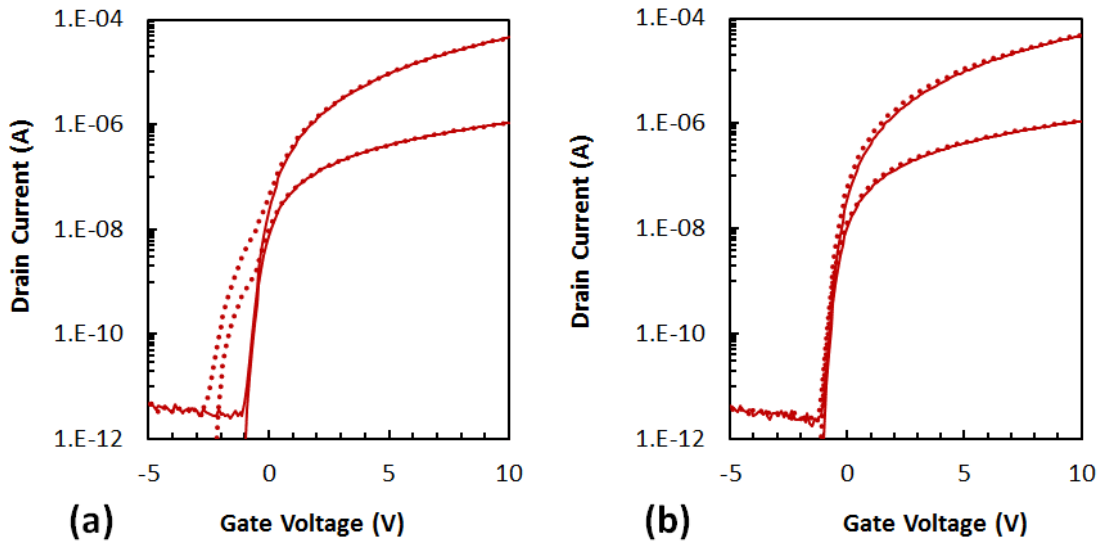

Figure 7.20: Response of BG TFTs under (a) PBS and (b) NBS stress for 10 ks. The solid and dotted lines show the transfer characteristics before and after stress respectively. TFT showed distortion under PBS, however no shift was observed under NBS.

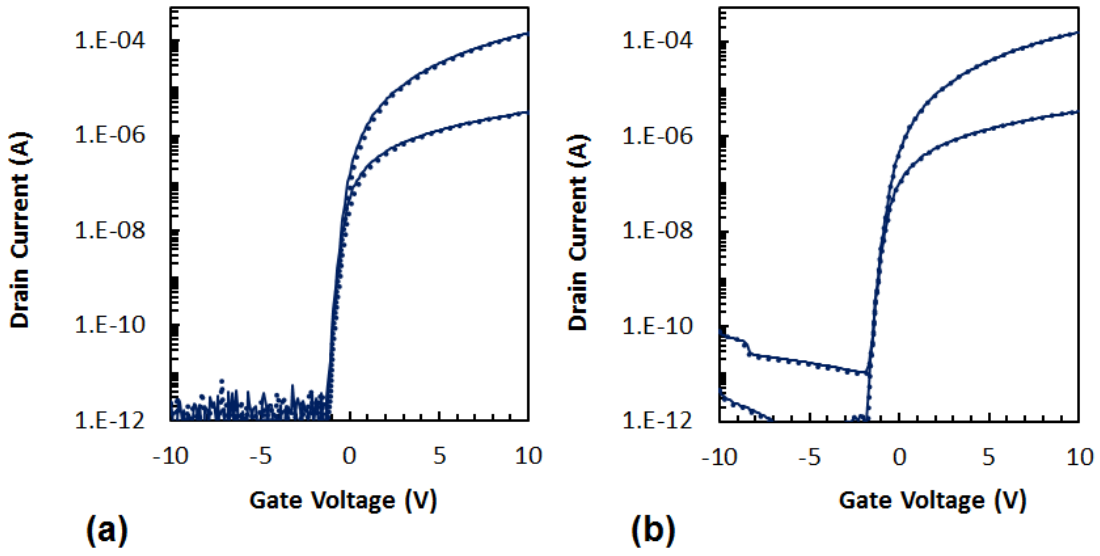

Figure 7.21: Response of DG TFTs with ALD alumina capping layer under (a) PBS and (b) NBS stress for 10 ks. The solid and dotted lines show the transfer characteristics before and after stress respectively. The devices show excellent resistance to bias stress. Note that the off-state under NBS is the artifact of the probe-station and the actual off-state is in pA range.

distortions. The physical origin of these states is typically associated with donor-like traps related to V_O [236]–[238]. Nevertheless, DG devices with an 8 h anneal and ALD alumina capping layer showed excellent resistance to both PBS and NBS due to the elimination of water and improved electrostatics.

7.4 Further Examinations

A remaining challenge in IGZO process development is understanding the interaction with air ambient over time. Through engineering solutions these defects can be regulated for improved electrical performance yet from a scientific standpoint some questions remained unanswered. The XPS measurements supported the decrease in V_O after oxidizing ambient

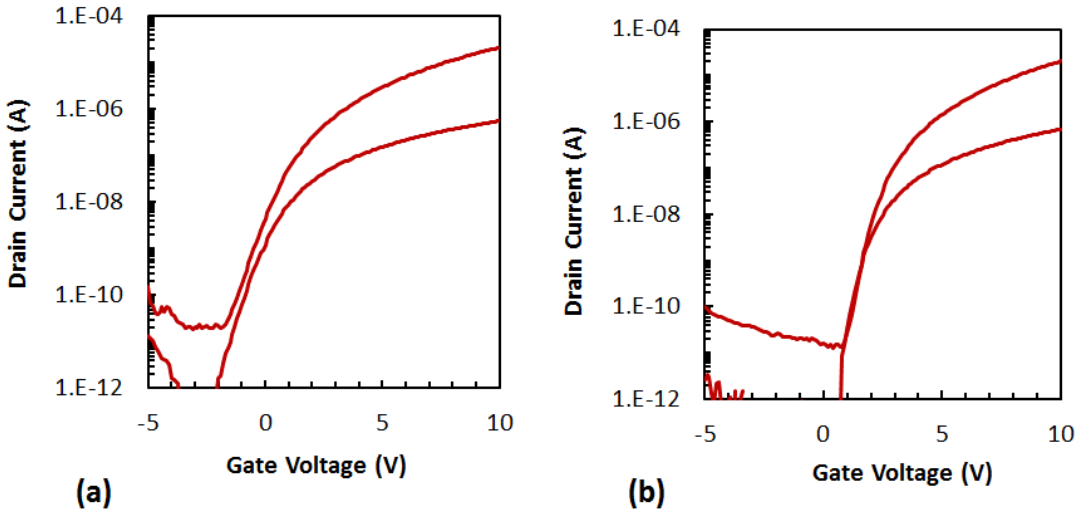

Figure 7.22: Transfer characteristics of a 5 nm thick IGZO TFT after (a) fabrication and (b) 3 weeks. The device characteristics improved over time through interaction of IGZO channel with ambient. The device exhibits transistor operation without any thermal anneal indicating the self-diffusion of oxygen.

anneal which was shown to decrease the IGZO conductivity through TFT operation demonstrating the role of V_O as donors in IGZO (Section 3.3.3). TFT with 5 nm IGZO channel thickness did not require any annealing for exhibiting semiconductor properties as shown in Figure 7.22 which supports V_O reduction in IGZO thin film at room temperature. This process was rather slow and the device performance kept improving over a few weeks as shown in Figure 7.22b. The diffusion of oxidants in IGZO at room temperature has certain characteristic depth and as IGZO channel thickness was increased this room-air interaction with IGZO did not yield working TFTs. This behavior is consistent with the ripening process with thicker IGZO films as discussed in Section 7.1.1. Note that furnace annealing of the 5 nm IGZO device resulted in catastrophic failure.

The over-oxidation of IGZO TFTs on thicker films, discussed in Section 4.3.1, also showed some interesting results. An unpassivated 50 nm IGZO TFT was over-oxidized (400 °C 4 h in O_2), the characteristics are shown in Figure 7.23a. The device showed

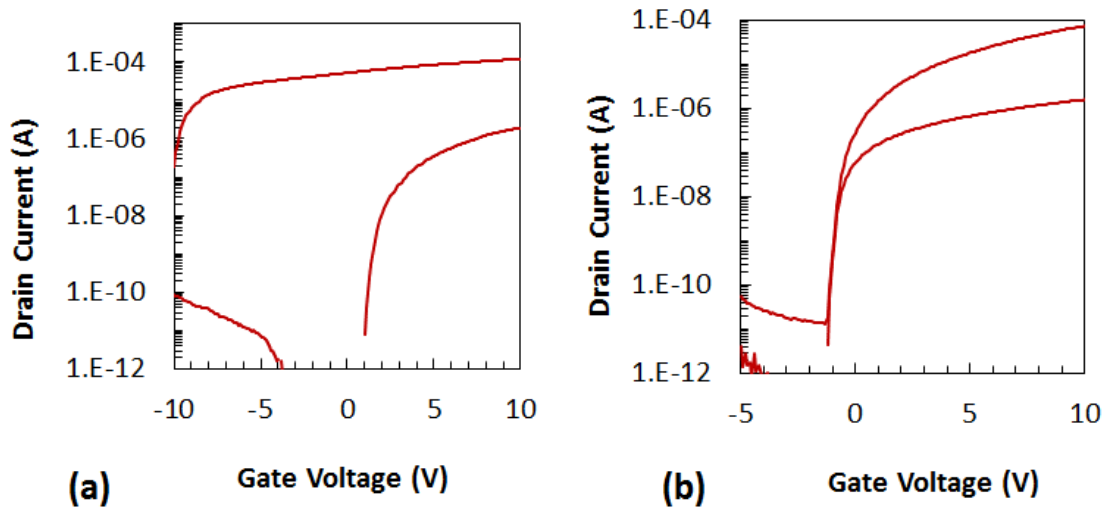

Figure 7.23: Transfer characteristics of an over-oxidized unpassivated IGZO TFT after (a) anneal and (b) six months of room-air storage. The TFT performance improved markedly over time.

distorted characteristics after the anneal, however the same device when tested after six months demonstrated excellent TFT response as shown in Figure 7.23b. It appears that over-oxidation creates electronic defect states, most likely related to the interstitial oxygen. Over time these electronic defects disappear as the system approaches a thermal equilibrium state.

The role of interstitial oxygen may also be operative during annealing of passivated devices. It was also observed that when the IGZO film is passivated within a couple of days of deposition for expedited fabrication, the resulting device showed characteristics that resembled over-oxidation. IGZO films deposited at the same time but processed a few weeks later produced characteristics as shown in Figure 7.24. This suggests that as-deposited films have a supersaturated level of interstitial oxygen which out-diffuses over time; however if devices are passivated before this process is completed, it results in

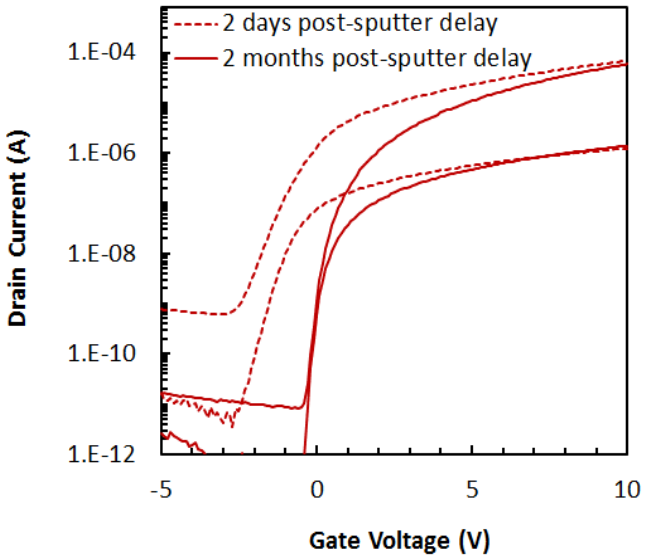

Figure 7.24: Transfer characteristics of BG passivated TFT with different delay times between IGZO sputter and passivation material application. The reduced delay time (dashed line) suggests over-oxidation.

degraded film quality. Note that this condition is certainly dependent upon sputter process conditions, particularly on the partial pressure of oxygen.

All three topics that require further examinations are related to an exchange of oxygen with air ambient, which must be managed to avoid electronic defect states responsible for degraded I-V characteristics. For passivated devices, it is critical to have the right combination of IGZO sputter, annealing conditions and process integration scheme.

7.5 CONCLUSION

A hypothesis on the origin of TABL was presented based on inhomogeneity at the topside IGZO interface, resulting in donor-rich defect regions separated by low-charge gaps. A simplified model for TCAD simulation provided insight on the advantage of the DG device

in its ability to overcome this effect. It has been reported that the top IGZO layer has higher defect states compared to the bulk [239]. These donor-rich defect regions are attributed to these high interface trap region. The ripening process passivates these defect states through interaction with room air and suppresses the TABL over time.

The classic BG device structure demonstrated weak ability to overcome the influence of interface traps and control the transistor operation, with poor subthreshold slope and TABL on long-channel devices. The BG device also demonstrated instability during bias-stress testing. The DG device was prepared by adding an overlapping co-planar top-gate to the BG device, and the improved electrostatics resulted in excellent on-state and off-state performance on scaled TFTs with a channel length L = 3 μm. However a limitation of the DG device was recognized during bias-stress testing, which revealed that the overlapping co-planar top-gate design was susceptible to electron charge injection and trapping in SiO_2 near the overlap regions. This resulted in a significant characteristic shift under both NBS and PBS conditions. A longer anneal improved the device characteristics as well as the SiO_2 resistance to electron injection. However, the longer annealed BG devices exhibited distortions in transfer characteristics under bias-stress, which was attributed to the interaction of water as verified by thermal stress testing.

IGZO TFTs exhibited a significant left shift after a thermal treatment, which is attributed to the water absorbed in the SiO_2 passivation layer. The stability against the thermal stress showed remarkable improvement after encapsulating the passivated device suing ALD Al_2O_3 layer and minimizing the interaction of SiO_2 with the air ambient. The encapsulated BG devices showed no shift under NBS and a distortion in characteristics

under PBS. DG configuration with ALD alumina capping layer offers further advantages in terms of device performance as well as device stability under both NBS and PBS.

Topics discussed for further examinations are challenging to quantify through a direct measurement. Further experimentation is required to confirm hypotheses with measured data and analysis.

Chapter 8. A COMPLEMENTARY SILICON BASED TECHNOLOGY

AOS offers an order of enhancement in mobility over a-Si:H while maintaining low cost, and even opens the realm of transparent and flexible electronics. Oxide semiconductors have undergone tremendous advancement in recent years and they offer an alternative technology to directly replace a-Si:H TFTs. Oxide semiconductors can be deposited over large glass panels, as well as on flexible substrates because of the low deposition temperature. In LCD displays, TFTs are used as pixel switches and unipolar TFTs (n-type or p-type) are sufficient for this demand. The logic circuits are fabricated on c-Si material and are connected to the LCD panel. For future technology and realizing concepts like system on glass (SoG), active devices will need to be fabricated on glass panel. Despite the continuous efforts, the p-type doping in oxide semiconductor has been elusive [240]–[242] Low temperature polycrystalline silicon (LTPS) can facilitate CMOS technology for future display devices. It enables both n-channel and p-channel FETs with high carrier mobility, supporting finer resolution displays.

Low temperature poly-silicon (LTPS) using Excimer Laser Annealing (ELA) has enabled higher levels of integration and device performance, and is already in production for switching matrix in small-format display products. However the ELA process is expensive and its extension to larger size glass panels is questionable due to both feasibility and cost. Currently the technology is not compatible with backplane manufacturing for large-format displays made on Gen8 glass panels and larger, which continues to motivate investigations on LTPS process techniques for improved manufacturability and lower cost.

Alternative strategies for crystallizing a-Si deposited on glass have been extensively researched. These include solid-phase crystallization (SPC), metallization-induced crystallization (MIC), and flash-lamp annealing (FLA). This chapter provides a brief overview of LTPS technology candidates for TFT backplanes in high-performance display applications. The discussion will then focus on recent developments using FLA for polycrystalline silicon TFTs, or FLAPS.

This work presents TFT results from an investigation on the electrical quality of FLAPS, with a demonstration of both NMOS and PMOS TFTs fabricated on the same glass substrate. The grains in the active channel region are aligned in the direction of current flow thereby limiting the grain boundaries interaction during the device operation. This can be utilized to improve the variations in the device performance in FLAPS.

8.1 LOW-TEMPERATURE POLYCRYSTALLINE SILICON (LTPS)

Even with hydrogen passivation, defect states in amorphous silicon hinder the flow of electrons. In a-Si:H the electron mobility is low which was good enough for TFT used as switching device in LCD until the need for higher performance display surfaced. In polycrystalline phase the mobility improves appreciably. The various techniques to crystallize a-Si deposited on glass substrates are briefly discussed in the following subsections.

8.1.1 Solid-Phase Crystallization (SPC)

Solid-Phase Crystallization (SPC) is the conventional and most simple way for crystallization. In Si case, thin films of a-Si deposited on glass are annealed in furnace at

high temperature. Higher the temperature easier is the crystallization of silicon and bigger are the grains. The constraint in this process is the temperature limit imposed by the underlying glass. This limits the highest temperature at which films can be annealed, which is ~ 600 °C on the highest quality (low alkali ion) display glass. The grain size and grain quality achieved using SPC are inferior to ELA; the grains suffer from a high density of twin-boundaries which degrades the mobility [243]. The crystallization time typically takes several hours which makes it unattractive from a manufacturing viewpoint.

8.1.2 Excimer Laser Annealing (ELA)

Thin-film a-Si absorbs excimer laser light (XeCl-308 nm) very efficiently without heating the underlying glass substrate. The a-Si on glass is melted by the scanning laser beam, and polycrystalline material results upon solidification. Beam scanning on large glass sheets is complex and process throughput is limited. The uniformity of the laser needs to be exceptionally good for uniform performance of fabricated devices. Due to the polycrystalline nature of LTPS, the performance uniformity suffers due to the presence of grain boundaries. The non-uniformity among different pixels necessitates the use of external compensating circuits and/or more than one TFT for each sub-pixel [244]. Despite these challenges, ELA is dominating the high-end display for mobile phones. A variant of the ELA process is Sequential Laser Solidification (SLS) in which annealing is done in two steps [245].

8.1.3 Metal-Induced Crystallization (MIC)

The addition of specific metals to a-Si reduces the time and temperature for crystallization during SPC [246]–[248]. Nickel has been widely used for inducing crystallization of silicon [249], [250]. A thin layer of Ni is deposited over a-Si and then it is furnace annealed. The Ni reacts and forms a silicide during annealing, which acts as a seed for crystallization [250]. This facilitates crystallization with a significant reduction in time and temperature. MIC combined with ELA can be used for crystallization of a-Si; the term Continuous Grain Silicon (CGS) is coined for this process and published work suggests that it may be used in manufacturing [251].

While work has been done in utilizing MIC for TFTs, the devices usually demonstrate higher levels of leakage current due to residual Ni. To circumvent this problem lateral crystallization, by depositing Ni far from the channel region, has also been investigated and termed Metal-Induced Lateral Crystallization (MILC) [252]. Jang *et al* deposited a silicon nitride (SiN) capping layer over a-Si and then deposited Ni [253]. Since SiN deposited by PECVD is porous therefore during annealing small amount of Ni seeped through SiN and reacted with underlying Si inducing the crystallization. All these variant techniques/approaches are used to reduce nickel content from the device active area.

8.1.4 Flash-Lamp Annealing (FLA)

Flash-lamp annealing (FLA) uses a series of short but intense bursts of broad spectrum light from xenon flash lamps. Flash-Lamp Annealing (FLA) has been shown to be capable of achieving ultra-shallow junctions for MOSFET [254], [255]. FLA has been used for fabrication of Si nanocrystals [256] and GaAs nanocrystals [257] in Si for optoelectronic

applications. It has been used for crystallization of a-Si film on glass for solar cell applications and flat panel display applications [258], [259]. However solar-cells use thicker a-Si layers [260], and thin-film applications do not usually present electrical characteristics of fabricated TFTs [259], [261]. FLA has demonstrated the ability to crystalize amorphous silicon [259] and activate implanted dopants [262]. Such a process would be potentially extendable to accommodate arbitrarily large substrates, such as those in flat panel manufacturing.

FLA is a promising way of producing high quality poly-Si films with less thermal impact on a glass substrate. FLA can be done in millisecond (ms) time scale, filling the gap between Rapid Thermal Annealing (RTA) and ELA. Major advantage of FLA is the high throughput by using a large high-intensity xenon light source with suitable pulse duration. Conventional RTA has an annealing time in second time scale that may have a significant thermal impact on a glass substrate. On the other hand, ELA with pulse duration on the order of tens of nanoseconds has a very small coverage area due to the laser beam width, limiting the backplane size and resulting in low production throughput. While there have been recent reports of FLA Polycrystalline Silicon (FLAPS) that focus on photovoltaics [263], reports on TFTs have been very limited [264], [265], with none appearing in the literature within the last five years.

8.2 FLASH LAMP ANNEALED POLYCRYSTALLINE SILICON

Results that have been reported on TFTs fabricated with FLA LTPS have been encouraging. Saxena *et al* showed the applicability of FLA for LTPS TFT, with results shown in Figure 8.1 [264]. The substrate was kept at elevated temperature (550 °C) during

the FLA process, which results in a higher surface temperature while maintaining low thermal stress in the glass. Figure 8.1a shows the optical image of the poly-Si film. The grain boundaries are visible in the micrograph. The mobility of the TFTs degraded appreciably as the number of grain boundaries increased in the active channel region (from 138 $cm^2/V{\cdot}s$ to 75 $cm^2/V{\cdot}s$). These variations in the TFT performance within a 13 cm × 8 cm area are highly undesirable. A process which enables alignment of the grains in the direction of the current flow may reduce the variations among the TFT performance. Figure 8.1b shows the transfer characteristics of a TFT fabricated using the FLA process. Only low-drain PMOS devices were reported which raises question about the performance of these devices under high-drain bias conditions. Also, NMOS devices fabricated using FLA process were not reported suggesting the challenges in donor-type dopant activation or diffusion of dopants along the long grain boundaries. Despite these deficiencies, this work shows the potential of FLA technology in TFT applications and provided the motivation to invest efforts in finding engineering solutions to improve the FLA process.

The lack of improvement of PMOS devices and the lack of demonstration of NMOS devices is likely to be due to variation in the resulting polycrystalline film morphology and difficulties in process control and optimization. This work presents TFT results from an investigation on the electrical quality of FLAPS, with a demonstration of both NMOS and PMOS TFTs fabricated on the same glass substrate. While presented devices show variation in electrical characteristics with certain non-ideal behavior, the extracted values of channel mobility can be compared to reported values extracted from TFTs fabricated on Corning's crystalline Silicon-on-Glass (SiOG) material [266]. Thus, this technique may

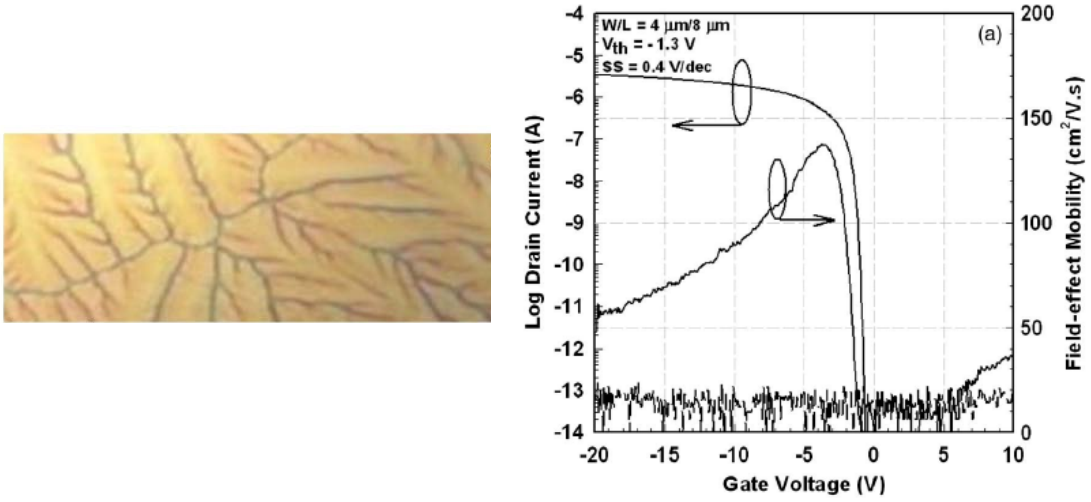

Figure 8.1: (a) Optical image of the FLA crystallized film. (b) Transfer characteristics of the crystallized films of FLA poly-Si TFT [264]

be a viable candidate for polycrystalline silicon backplane manufacturing on large glass panels.

8.2.1 Device Fabrication

A 60 nm hydrogenated amorphous silicon (a-Si:H) layer was deposited via Plasma-Enhanced Chemical Vapor Deposition (PECVD) on 150 mm diameter Corning EAGLE XG® display glass wafers with an SiO_2 barrier layer. The samples were dehydrogenated at 450 °C for 2 hours. The a-Si super-mesa patterns were defined and etched using reactive-ion etching (RIE). The super-mesa provides sacrificial real estate that extends beyond the mesa, or active device region. A 100 nm SiO_2 capping layer was then deposited which serves three important functions, including a thermal buffer to the surface, an anti-reflective layer for the FLA exposure, and a screen oxide layer to position the boron and

phosphorus implant profiles within the a-Si layer. The source/drain implant regions were patterned and received high-dose ($\phi = 4\times10^{15}$ cm^{-2}) implants of boron and phosphorus done at energies of 35 keV and 60 keV, respectively.

The FLA system used in this work is a NovaCentrix PulseForge 3300 configured with two Xe lamps, with a 75 mm × 150 mm exposure window. The FLA exposure served to crystallize a Si and activate the implanted dopant. A high temperature ambient control chamber maintained a temperature of 550 °C with a nitrogen purge at atmospheric pressure. Single-shot FLA exposures were done with lamp voltage supplies at 600 V and a time of 200 µsec, with bolometer measurements showing an integrated energy of ~ 6 J/cm^2. Following FLAPS formation the screen oxide was removed in buffered hydrofluoric acid, and the mesa definition was patterned and etched via RIE to remove the sacrificial super-mesa regions. The gate oxide was deposited via PECVD and was followed by a 630 °C, 12 hour furnace anneal in nitrogen ambient, which was found to be important for stress relaxation and may also offer other benefits such as additional dopant activation and defect reduction. Contact regions were then patterned and etched in buffered HF. An optical image of the FLAPS TFT at this point in the process is shown in Figure 8.2. Aluminum was deposited using thermal evaporation, and the source/drain and gate electrodes were patterned and etched. Finally the devices were sintered in a forming gas ambient (5% H_2 in N_2) at 450 °C for 30 min.

8.2.2 Electrical Characterization

CMOS TFTs were realized following the described process details, with a high percentage of devices within an acceptable exposed region demonstrating transistor operation. An

overlay plot of long-channel transfer characteristics is shown in Figure 8.3, where the mask-defined channel length (L_{mask}) is 32 µm. Variation in device behavior is attributed to limitations in process uniformity, as well as the influence of interface traps and bulk defects. The best-case device results are depicted in Figure 8.4. The Terada-Muta (T-M) method was used to establish the effective electrical channel length (L_{eff}), with plots shown in Figure 8.5 [164]. Note that only L_{mask} = 32 µm and 20 µm were available for the analysis. Shorter devices demonstrated inferior characteristics and were prone to fail, with very few working devices at L_{mask} < 20 µm.

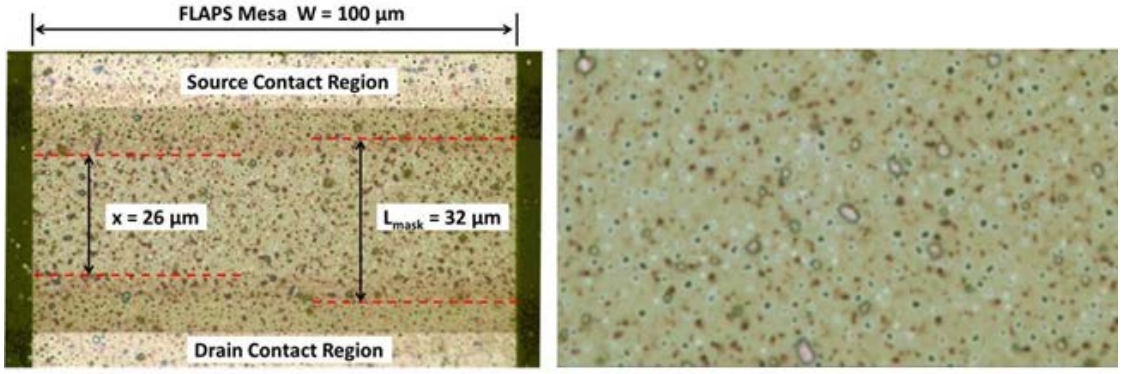

Figure 8.2: Optical microscope images of FLAPS during TFT fabrication. The left image shows a boron-implanted mesa following FLA exposure and oxide etch for the source/drain contacts. The outer set of red dashed lines represents a demarcation between the implanted and channel regions, with L_{mask} = 32 µm indicating the mask-defined channel length. The inner set of red dashed lines delineates an observed boundary, with the label x = 26 µm indicating a visual separation that may be the result of lateral diffusion. The right image is a further magnified view of the center channel region showing circular voids (white borders) as well as other optical artifacts.

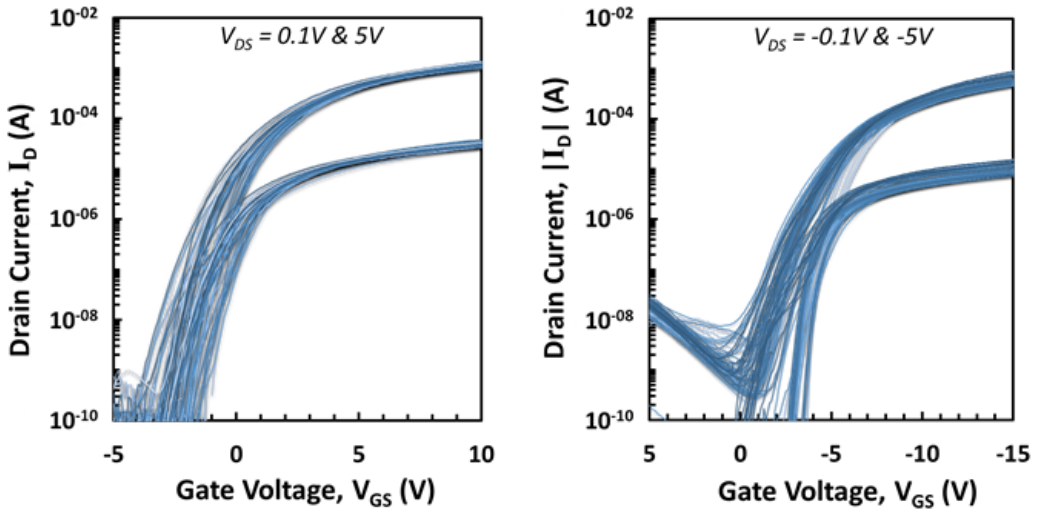

Figure 8.3: NMOS (left) and PMOS (right) transfer characteristics from devices with L_{mask} = 32 µm and W = 100 µm. Note differences in x-axis scale. Each plot has an overlay of over 30 devices measured within a single-shot FLA exposed region.

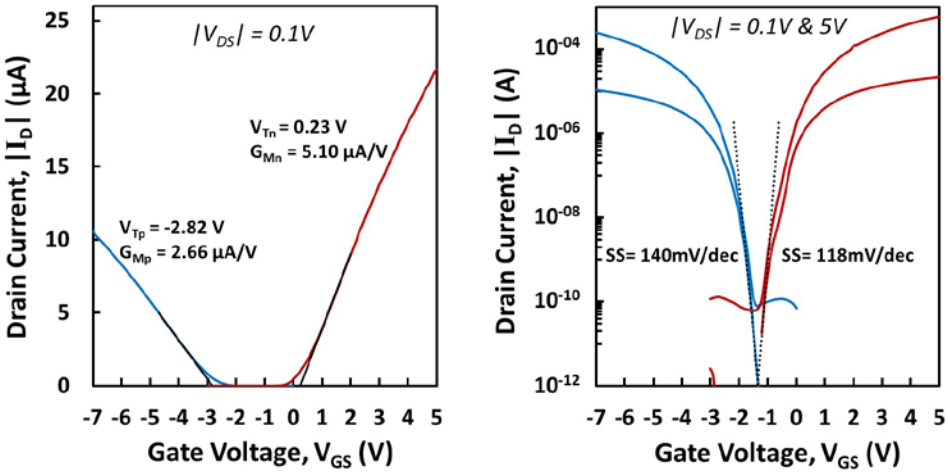

Figure 8.4: Best-case linear & log scale CMOS transfer characteristics from FLAPS TFTs with L_{mask} = 32 µm and W = 100 µm.

The T-M analysis worked reasonably well on both NMOS and PMOS devices; however lower $|V_{GS} - V_T|$ values were excluded for the PMOS analysis due to minor inconsistencies in extrapolated intercepts presumed to be related to trap states. The channel length offset (ΔL) values were 6.3 µm and 13.4 µm for NMOS and PMOS devices,

respectively; much larger than expected, particularly for the PMOS device. The on-state and off-state operational parameters for the best-case transfer characteristics shown in Figure 8.4 were extracted once L_{eff} was established, with results listed in Table 8-I. The width (W) of the TFTs was taken as the designed value of 100 µm. The oxide capacitance was calculated from the 100 nm deposition thickness. The channel mobility values were calculated from the maximum transconductance at $|V_{DS}|$ = 0.1 V. The extracted channel mobility values are 380 $cm^2/V{\cdot}s$ and 143 $cm^2/V{\cdot}s$ for electrons and holes, respectively. Off-state parameters were also noteworthy, with minimum subthreshold swing (SS) values below 150 mV/dec, and ~ 1 pA/µm leakage current at $|V_{DS}|$ = 5 V.

The extracted channel mobility values are notably high and may raise question on the analysis. The electron/hole channel mobility ratio is ~ 2.7, which is indeed consistent with crystalline silicon. Further analysis found that these electrical results correspond to full melting of the super-mesa during FLA, which supports large polycrystalline silicon grains. It also provides an explanation for the large ΔL from the T-M analysis as a result

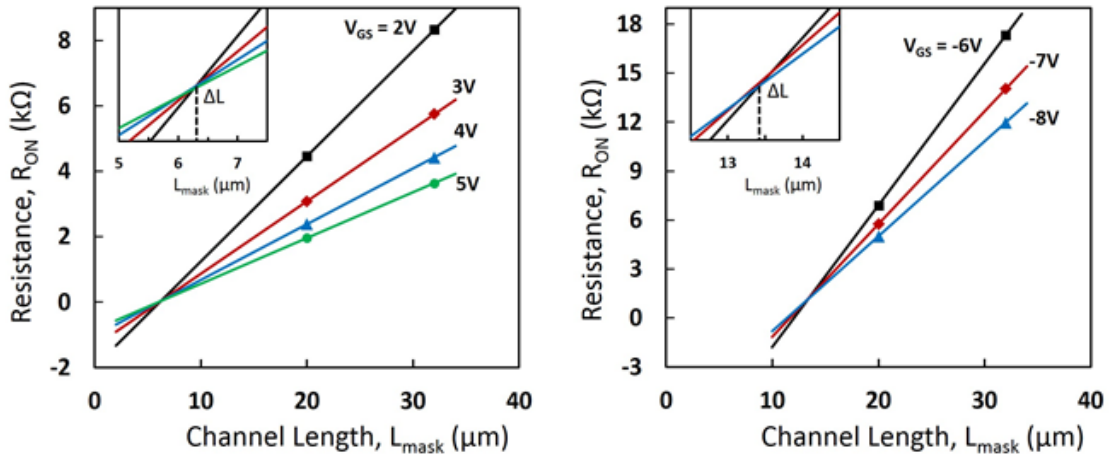

Figure 8.5: Terada-Muta analysis plots for NMOS (left) and PMOS (right) FLAPS TFTs. The insets show an enlargement of the intersection identifying the channel length offset (ΔL) needed to arrive at the effective electrical channel length (L_{eff}).

of the diffusivity of phosphorus and boron in liquid phase silicon. Scanning Electron Microscopy (SEM) and Electron Backscatter Diffraction (EBSD) images shown in Figure 8.6 further reveal the FLAPS microstructure. These images were taken from a functional device after chemical etching of the aluminum electrodes and gate oxide layer. The channel region remains intact; however the source/drain regions that were in contact with aluminum were partially consumed during the aluminum sinter process. The images of the channel regions indicate a smooth surface with voids scattered throughout. This suggests full melting of the silicon mesa during the FLA process with some dewetting prior to freezing, leaving regions completely void of silicon. Although there are voids, the TFTs demonstrate performance consistent with high quality LTPS. The EBSD mapping suggests an edge-directed nucleation/growth process, with some grains that appear to extend completely across the channel region.

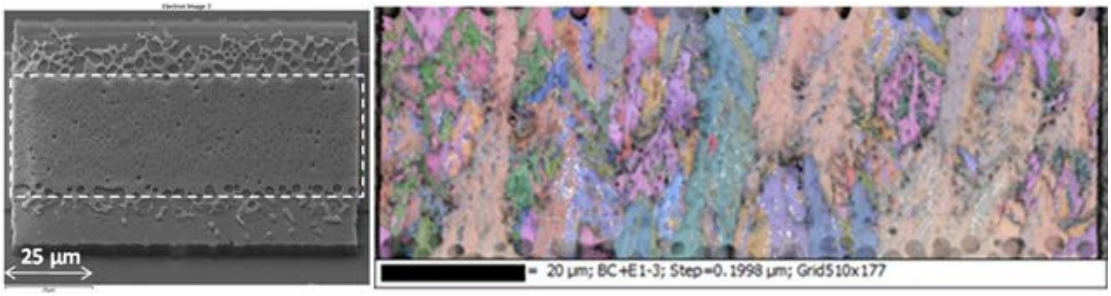

Figure 8.6: SEM image (left) and EBSD mapping (right) of a FLAPS TFT channel region taken from a deprocessed PMOS device verified operational. The boxed region on the SEM image was used for EBSD analysis. Each color represents a different crystal orientation.

Table 8-I: Summary of best-case CMOS TFT operational parameters.

	Parameter	NMOS	PMOS
Physical	L_{mask}	32 µm	32 µm
	ΔL	6.3 µm	13.4 µm
	L_{eff}	25.7 µm	18.6 µm
	W	100 µm	100 µm
	W/L_{eff}	3.89	5.38
	C_{ox}'	34.5 nF/cm^2	34.5 nF/cm^2
On-State	V_T	0.23 V	-2.82 V
	$g_{m(max)}$ @ $\lvert V_{DS}\rvert$= 0.1V	5.10 µA/V	2.66 µA/V
	$\mu_{ch(max)}$	380 cm^2/V·s	143 cm^2/V·s
Off-State	$I_{(leak)}$ @ $\lvert V_{DS}\rvert$= 5V	~ 1 pA/µm	~ 1 pA/µm
	$SS_{(min)}$	120 mV/dec	140 mV/dec

8.3 CONCLUSION

Despite the improved performance over a-Si:H TFT and scalability, IGZO technology does not support CMOS capability. For finer resolution in display and SoG capabilities, Si-based technology has been investigated. ELA-LTPS has emerged as a dominant technology for high-performance TFTs used in LCD and OLED display products; however there are challenges in scaling ELA techniques for backplane manufacturing on extra-large glass panels. This provides the motivation to investigate alternative process techniques for silicon-based technology which are easily scalable and manufacturable in comparison to current ELA based LTPS. Alternative strategies for LTPS include SPC, MIC, and FLA.

While SPC offers the simplicity of processing, it is afflicted by the substrate temperature constraint and extremely long duration for crystallization. MIC offers an advantage over SPC but still the anneal time is in hours compared to seconds for ELA and contaminates the channel with metal impurities. For this reason, research has been directed towards the alternative methods to crystallize amorphous silicon deposited on glass substrates.

This work shows a high potential for FLAPS that until now has not been reported, with best-case operational parameters comparable to ELA-LTPS. However the existence of trap states is evident by the CMOS transfer characteristics resulting in distortion, degraded *SS*, and inflated V_T separation. Electrical results indicate that the presence of voids within the channel region may be tolerable for long-channel devices, however a void-free channel will become necessary as devices are scaled down to smaller dimensions. In addition the non-self-aligned transistor structure has serious limitations due to the presence of dopants during the FLA process. It is clear that a self-aligned TFT structure is required for scaled devices. These identified challenges must be addressed through optimization of conditions involving materials, device structure, FLA parameters and process integration. Techniques that were developed for self-aligned CMOS TFTs on SiOG [266] may also apply to FLAPS.

Chapter 9. CONCLUSIONS

The primary focus of this work was to interpret and regulate the electronic defect states in IGZO TFTs through material analysis and process integration strategies. This goal was attained through the following accomplished objectives:

- Established the relationships between processes associated with IGZO TFT operation including IGZO sputter deposition, annealing conditions and back-channel passivation, and developed a process integration scheme that supports device stability when subjected to thermal and bias stress.
- Developed TCAD material and device models for BG and DG configurations that depict the role of defect states on device operation, as well as provide insight and support of a presented hypothesis on DIBL-like device behavior associated with back-channel interface trap inhomogeneity.
- Developed a SPICE-compatible 2D on-state operation model for IGZO TFTs that is consistent with TCAD simulation.

This chapter provides a summary of the important findings and contributions of this research work, with recommended areas for further study as IGZO continues to evolve and mature as a mainstream manufacturing technology.

9.1 KEY CONTRIBUTIONS

The study of the role of electronic defect states on the device operation, and the regulation of these states through process integration schemes has presented many challenges.

Materials analysis, electrical characterization, TCAD simulation and device modeling have all been essential to attain a clear understanding of the underlying mechanisms involved. Key contributions of this work towards the IGZO body of research are now summarized.

9.1.1 Process Integration

The spectrum of IGZO deposition parameters and corresponding anneal conditions suggest that there is no "unique" process for producing high-quality TFTs. Differences in as-deposited films can be accommodated using an appropriate thermal anneal process which reduces the sub-gap states and regulates the amount of oxygen vacancies. Prior to thermal annealing the IGZO films were established as too conductive for use as a TFT channel material. An annealing process in oxidizing ambient was required to lower the free electron concentration by reducing oxygen vacancy donors, confirmed using XPS analysis.

The exposed IGZO surface readily interacts with oxygen and water vapor present in the room air ambient, which causes instability in the device operation over time as well as under bias stress. The application of a passivation material at the IGZO back-channel is imperative, however this requires modifications of thermal anneal conditions for sufficient oxidant transport. Initial passivated devices exhibited a compromise in device performance in terms of subthreshold swing and on-state current drive, which is attributed to the presence of defect states at IGZO/passivation material interface. The influence of these interface states was mitigated by optimizing the annealing conditions and the addition of a top-gate electrode. The interpretation of experimental results was supported by TCAD simulation of unpassivated BG, passivated BG, and DG TFT configurations.

Water absorbed by PECVD SiO_2 at the IGZO back-channel was found to be detrimental to device stability over time and following thermal and bias stress. An ALD alumina capping layer, deposited on the PECVD SiO_2 following the annealing process, was investigated as a water barrier. This process integration scheme resulted in TFTs that exhibited excellent device performance and resistance to bias-stress as shown in Figure 9.1.

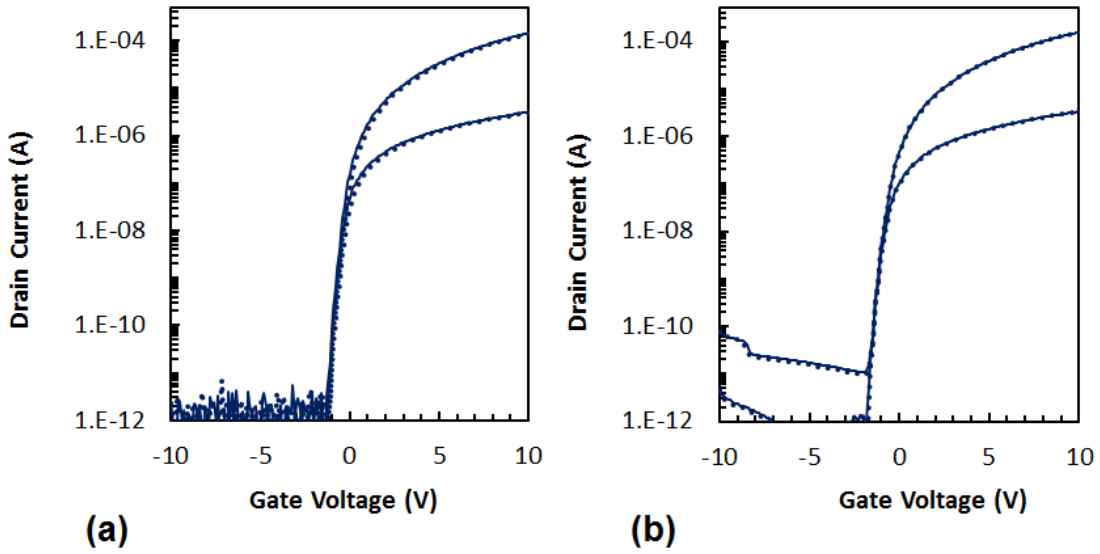

Figure 9.1: Response of DG TFTs with ALD alumina capping layer under (a) PBS and (b) NBS stress for 10 ks. The solid and dotted lines show the transfer characteritics before and after stress, respectively. The devices show excellent resistance to bias stress.

9.1.2 TCAD Simulation & Trap-Associated Barrier Lowering

Device simulation is an indispensable tool in the study of electronic devices. TCAD simulation was employed to understand the underlying physics of device operation and role of defect states. For unpassivated IGZO TFTs, the oxygen-vacancy donor

concentration was adjusted from the default Silvaco ATLAS material model, providing an improved match to experimental results. A proposed mechanism to describe DIBL-like behavior observed on long-channel unpassivated devices relatively soon after annealing is attributed to the inhomogeneity of trap states at the IGZO back-channel interface, and is referred as trap associated barrier lowering (TABL). A qualitative representation of this behavior is demonstrated using a simplified TCAD simulation model shown in Figure 9.2.

The application of back-channel passivation material required the addition of defect states at the IGZO/dielectric interface. This material/interface model was used for an accurate simulation of BG TFTs passivated with PECVD SiO_2, and further extended to illustrate the advantages of a DG device structure. TCAD simulation produced an excellent match to measured characteristics, with improved subthreshold performance and elimination of TABL as shown in Figure 9.2c.

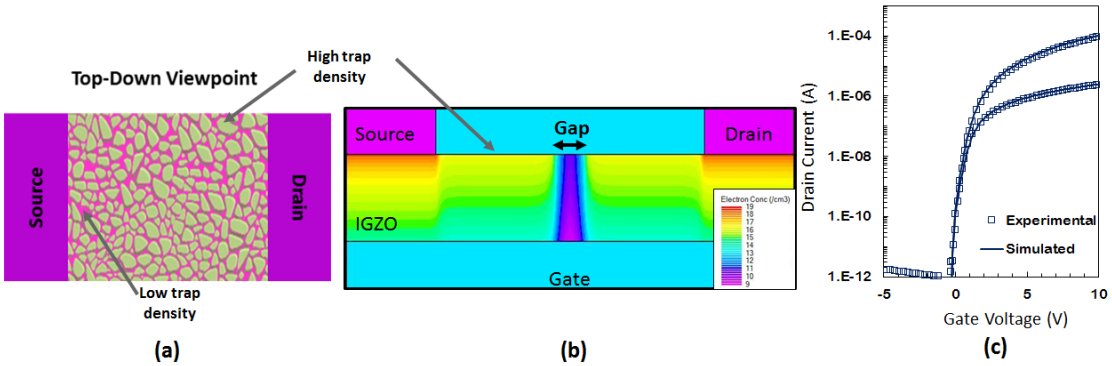

Figure 9.2: (a) Schematic model for the TABL origin, showing a cobblestone arrangement of donor-rich interface defect regions separated by low-charge gaps. (b) Simplified structure for TCAD simulation, representing the low-charge gaps as a single gap in the middle of the channel. The contours show the electron concentration at zero-bias, with values in donor-rich interface defect regions and the low-charge gap differing by several orders of magnitude. (c) An overlay of measured (markers) and simulated (line) characteristics of a SiO_2 passivated DG IGZO TFT. The DG TFT demonstrate steeper SS and higher current drive compared to BG TFT. DG device shows complete suppression of TABL.

9.1.3 Device Modeling

Due to the presence of band-tail states, conventional SPICE model parameters are inadequate for IGZO TFT modeling. A novel device model for the on-state operation of IGZO TFTs has been presented. The uniqueness of the model is the integration of drain-impressed deionization, which results in a 2D modification of free channel charge. An analytical expression that relates the ionization of band-tail states and dependence of free electron charge on the applied drain bias was not derived; rather TCAD simulation was used as a tool for this purpose. The model provides an excellent match to TCAD simulation and measured data over the entire range of bias conditions, and preserves the physical connection to device operation. The model fit for devices is virtually indistinguishable from measured data, with the on-state well represented by five operational parameters.

Model parameters are extracted using regression analysis, with the resulting threshold voltage and channel mobility values consistent with TCAD analogs. The extracted mobility value provides a direct connection to the primitive intrinsic electron mobility in the TCAD material model. The model is compatible with a Level 2 SPICE model platform, and can utilize traditional parameters necessary to accommodate short-channel and high-field effects that are presented by scaled devices.

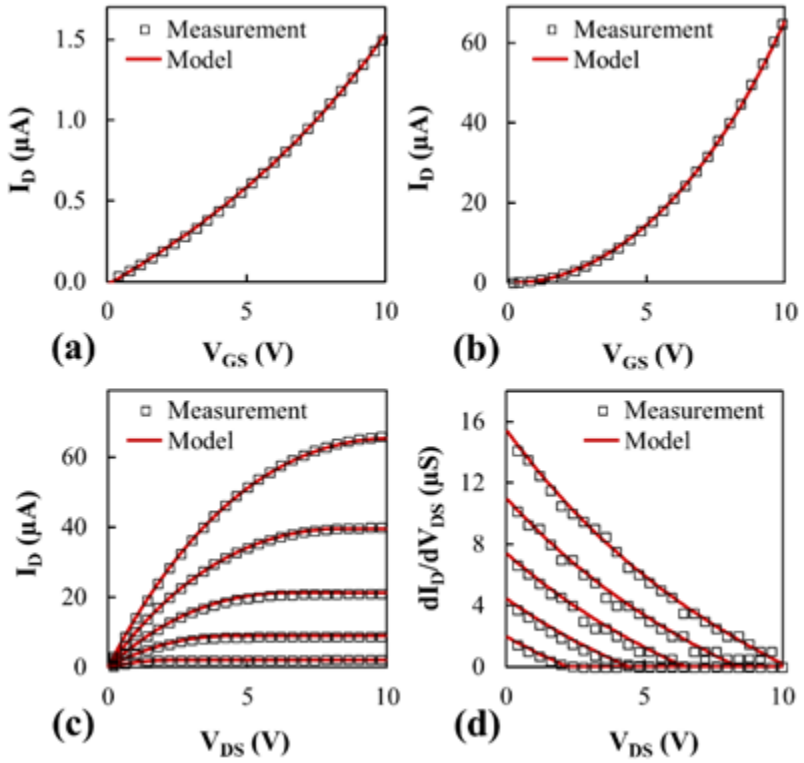

Figure 9.3: Overlay of transfer and output characteristics of measured data and the presented model. Transfer characteristics are shown in linear mode (a) with V_{DS} = 0.1 V, and (b) saturation mode with V_{DS} = 10 V. (c) Output characteristics with V_{GS} = 2-10 V in steps of 2 V. (d) Differential output conductance over the same V_{GS} range as in (c), showing an excellent match with the model.

9.2 FURTHER WORK

This work presents a significant advancement in understanding of the role of defect states in IGZO TFTs, and regulation through materials and processes. Nonetheless, there are areas that require further investigation to address certain inconsistencies in interpretation or shortcomings in device performance.

One element that is lacking in the literature is a band-tail DOS model that demonstrates consistency between temperature-dependent electron transport behavior (*i.e.*

cryogenic) and TCAD simulation. Inconsistencies have been previously noted [88], however the models continue to remain disparate. Efforts towards resolving this inconsistency within this work were hindered by instabilities presented by TFTs under cryogenic testing which was most likely related to issues with water adsorption/absorption. Cryogenic transport measurements must be done on a device with an ALD alumina capping layer to suppress any influence of water and ensure stability under stress conditions.

While the presented TCAD material & device models accurately represent both BG and DG device configurations with consistent defect parameters, there have been observed inconsistencies with alternative electrode arrangements (*e.g.* top-gate TFT). However, in such cases invariably other issues compromised the interpretation. A new IGZO testchip has been designed which incorporates several gate-source/drain electrode configurations that will be realized simultaneously, thus presenting the same material and interface conditions for TCAD simulation of the various device structures.

Another area that warrants further investigation is directed towards advancing the understanding and elimination of bias-stress instability. While it can be argued that the problem is resolved by the DG TFT structure, an explanation for this based on differences between the bias-stress electrostatic conditions remains uncertain. Furthermore, the additional cost associated with a DG process may be prohibitive in a manufacturing application. BG devices still demonstrate a temporary response to PBS which may be related to interstitial oxygen defects [267]–[269]. A minor temporary response to NBS, observed on some BG TFTs, may have similar origin. These remaining instabilities may be addressed by a refined investigation on the sputter deposition and annealing processes. Oxygen interstitials were mentioned in a hypothesis regarding dependency on the time in

between IGZO sputter deposition and passivation/annealing processes, which requires further experimental verification. Another consideration is the application of a front-channel interface layer such as ALD alumina prior to IGZO deposition. Experiments investigating both post-sputter delay time and the application of ALD alumina at the front-channel interface are currently in progress.

9.3 CLOSING REMARKS

IGZO technology has the potential to replace the current a-Si:H based TFT technology to address the needs of advanced display products while maintaining process simplicity. As in the case of a-Si:H, defect states in IGZO establish the electronic properties of the material as well as anomalies in device behavior. The interpretation and regulation of electronic defect states in IGZO TFTs through materials and processes has resulted in significant advancements in TFT performance. This work has provided significant contributions towards a better understanding of IGZO device behavior which is vital to address the challenges that remain as active research topics in the scientific community [118], [270]–[276].

IGZO has already been introduced into production of display products [277], with advantages in low temperature processing and transparency to light that are particularly attractive for flexible and transparent display devices. However, IGZO is not a suitable technology candidate for certain high performance applications due to the lack of complementary device operation where LTPS remains unchallenged. The introduction of flash-lamp annealing (FLAPS) as an alternative LTPS technology shows the potential for scalability to large panel substrates; however the engineering challenges that remain are

significant. Research and development in FLAPS technology is still in an initial phase, and will require a significant investment in time and resources to advance the technology towards inception in flat panel manufacturing. Nonetheless, it appears as a promising solution for the integration of high performance TFT circuits on large glass panels at a lower production cost than excimer laser annealing.

While FLAPS may target future device applications, IGZO technology offers a direct replacement for current a-Si:H technology with superior performance. The needs of the display industry continue to evolve, which will direct efforts towards advancement of these TFT technologies to meet the performance and manufacturing requirements for a wide range of product applications.

REFERENCES

[1] L. J. Edgar, “Device for Controlling Electric Current,” US Patent 1900018 A, 1933.

[2] P. K. Weimer, “The TFT - A New Thin-Film Transistor,” *Proceedings of the IRE*, vol. 50, no. 6, pp. 1462–1469, 1962.

[3] T. P. Brody, J. A. Asars, and G. D. Dixon, “6X6 Inch 20 Lines-per-Inch Liquid-Crystal Display Panel,” *IEEE Transactions on Electron Devices*, vol. 20, no. 11, pp. 995–1001, 1973.

[4] P. G. LeComber, W. E. Spear, and A. Ghaith, “Amorphous-Silicon Field-Effect Device and Possible Application,” *Electronics Letters*, vol. 15, no. 6, pp. 179–181, 1979.

[5] A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. LeComber, and A. J. Hughes, “Application of Amorphous-Silicon Field-Effect Transistors in Addressable Liquid-Crystal Display Panels,” *Applied Physics*, vol. 24, no. 4, pp. 357–362, 1981.

[6] R. Tani, J.-S. Yoon, S.-I. Yun, W.-J. Nam, S. Takasugi, J.-M. Kim, *et al.*, “Panel and Circuit Designs for the World’s First 65-inch UHD OLED TV,” *SID Symposium Digest of Technical Papers*, vol. 46, no. 1, pp. 950–953, 2015.

[7] Z. Wu, G. Yuan, H. Xie, K. Cao, Y. Li, S. Zeng, *et al.*, “Development of 55-inch UHD AMOLED TV,” *SID Symposium Digest of Technical Papers*, vol. 46, no. 1, pp. 954–957, 2015.

[8] C. Ha, H.-J. Lee, J.-W. Kwon, S.-Y. Seok, C.-I. Ryoo, K.-Y. Yun, *et al.*, “High Reliable a-IGZO TFTs with Self-Aligned Coplanar Structure for Large-Sized Ultrahigh-Definition OLED TV,” *SID Symposium Digest of Technical Papers*, vol. 46, no. 1, pp. 1020–1022, 2015.

[9] B.-L. Yeh and C.-N. Lin, “High-Performance 4K x 2K 65-in. TV with BCE-Type Oxide TFTs,” *SID Symposium Digest of Technical Papers*, vol. 46, no. 1, pp. 943–945, 2015.

[10] S. Steudel, J. P. J. Steen, M. Nag, T. H. Ke, S. Smout, T. Bel, *et al.*, “Power Saving Through State Retention in IGZO-TFT AMOLED Displays for Wearable Applications,” *Journal of the Society for Information Display*, vol. 25, no. 4, pp. 222–228, 2017.

[11] Y.-M. Ha, S. K. Kim, H. Choi, S.-G. Lee, K.-S. Park, and I. Kang, “Oxide TFT Development for AMLCDs and AMOLEDs,” *SID Symposium Digest of Technical Papers*, vol. 47, no. 1, pp. 940–943, 2016.

[12] Y. Kuo, “Thin Film Transistors 1: Amorphous Silicon Thin Film Transistors,” Kluwer Academic Publishers, 2004, pp. 17–32.

[13] P. H. Miller, “The Electrical Conductivity of Zinc Oxide,” *Physical Review*, vol. 60, no. 12, pp. 890–895, 1941.

[14] T. Minami, “Transparent Conducting Oxide Semiconductors for Transparent

Electrodes," *Semiconductor Science and Technology*, vol. 20, no. 4, pp. S35–S44, 2005.

[15] T. Kamiya, H. Hosono, K. Nomura, H. Hosono, J. Kim, N. Miyokawa, *et al.*, "Material Characteristics and Applications of Transparent Amorphous Oxide Semiconductors," *Journal of Physical Chemistry C*, vol. 11, no. 4, pp. 15–22, 2010.

[16] H. Hosono, M. Yasukawa, and H. Kawazoe, "Novel Oxide Amorphous Semiconductors: Transparent Conducting Amorphous Oxides," *Journal of Non-Crystalline Solids*, vol. 203, pp. 334–344, 1996.

[17] Y. Vygranenko, K. Wang, and A. Nathan, "Stable Indium Oxide Thin-Film Transistors with Fast Threshold Voltage Recovery," *Applied Physics Letters*, vol. 91, no. 26, p. 263508, 2007.

[18] J. H. Noh, S. Y. Ryu, S. J. Jo, C. S. Kim, S.-W. Sohn, P. D. Rack, *et al.*, "Indium Oxide Thin-Film Transistors Fabricated by RF Sputtering at Room Temperature," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 567–569, 2010.

[19] K. Matsuzaki, H. Yanagi, T. Kamiya, H. Hiramatsu, K. Nomura, M. Hirano, *et al.*, "Field-Induced Current Modulation in Epitaxial Film of Deep-Ultraviolet Transparent Oxide Semiconductor Ga2O3," *Applied Physics Letters*, vol. 88, no. 9, p. 92106, 2006.

[20] R. E. Presley, C. L. Munsee, C.-H. Park, D. Hong, J. F. Wager, and D. A. Keszler, "Tin Oxide Transparent Thin-Film Transistors," *Journal of Physics D: Applied Physics*, vol. 37, no. 20, pp. 2810–2813, 2004.

[21] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-Based Transparent Thin-Film Transistors," *Applied Physics Letters*, vol. 82, no. 5, pp. 733–735, 2003.

[22] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, "Transparent Thin Film Transistors Using ZnO as an Active Channel Layer and Their Electrical Properties," *Journal of Applied Physics*, vol. 93, no. 3, pp. 1624–1630, 2003.

[23] S. Y. Park, B. J. Kim, K. Kim, M. S. Kang, K.-H. Lim, T. Il Lee, *et al.*, "Low-Temperature, Solution-Processed and Alkali Metal Doped ZnO for High-Performance Thin-Film Transistors," *Advanced Materials*, vol. 24, no. 6, pp. 834–838, 2012.

[24] E. Fortunato, P. Barquinha, and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," *Advanced Materials*, vol. 24, no. 22, pp. 2945–2986, 2012.

[25] K. Remashan, D. K. Hwang, S. D. Park, J. W. Bae, G. Y. Yeom, S. J. Park, *et al.*, "Effect of N2O Plasma Treatment on the Performance of ZnO TFTs," *Electrochemical and Solid-State Letters*, vol. 11, no. 3, pp. H55–H59, 2008.

[26] Y. V Li, K. G. Sun, J. I. Ramirez, and T. N. Jackson, "Trilayer ZnO Thin-Film Transistors With In Situ Al2O3 Passivation," *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1400–1402, 2013.

[27] G. Adamopoulos, A. Bashir, P. H. Woebkenberg, D. D. C. Bradley, and T. D.

Anthopoulos, “Electronic Properties of ZnO Field-Effect Transistors Fabricated by Spray Pyrolysis in Ambient Air,” *Applied Physics Letters*, vol. 95, no. 13, p. 133507, 2009.

[28] K. Remashan, D.-K. Hwang, S.-J. Park, and J.-H. Jang, “Effect of Rapid Thermal Annealing on the Electrical Characteristics of ZnO Thin-Film Transistors,” *Japanese Journal of Applied Physics*, vol. 47, no. 4, pp. 2848–2853, 2008.

[29] R. Theissmann, S. Bubel, M. Sanlialp, C. Busch, G. Schierning, and R. Schmechel, “High Performance Low Temperature Solution-Processed Zinc Oxide Thin Film Transistor,” *Thin Solid Films*, vol. 519, no. 16, pp. 5623–5628, 2011.

[30] K. Remashan, Y. S. Choi, S. J. Park, and J. H. Jang, “Enhanced Performance of MOCVD ZnO TFTs on Glass Substrates with Nitrogen-Rich Silicon Nitride Gate Dielectric,” *Journal of Electrochemical Society*, vol. 157, no. 1, pp. H60–H64, 2010.

[31] M. Grundmann, H. Frenzel, A. Lajn, M. Lorenz, F. Schein, and H. von Wenckstern, “Transparent Semiconducting Oxides: Materials and Devices,” *Physica Status Solidi (A) Applications and Materials Science*, vol. 207, no. 6, pp. 1437–1449, 2010.

[32] D. A. Mourey, D. A. Zhao, J. Sun, and T. N. Jackson, “Fast PEALD ZnO Thin-Film Transistor Circuits,” *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 530–534, 2010.

[33] J. F. Wager, B. Yeh, R. L. Hoffman, and D. A. Keszler, “An Amorphous Oxide Semiconductor Thin-Film Transistor Route to Oxide Electronics,” *Current Opinion in Solid State and Materials Science*, vol. 18, no. 2, pp. 53–61, 2014.

[34] J.-Y. Kwon, D.-J. Lee, and K.-B. Kim, “Review Paper: Transparent Amorphous Oxide Semiconductor Thin Film Transistor,” *Electronic Materials Letters*, vol. 7, no. 1, pp. 1–11, 2011.

[35] H. Hosono, “Ionic Amorphous Oxide Semiconductors: Material Design, Carrier Transport, and Device Application,” *Journal of Non-Crystalline Solids*, vol. 352, no. 9, pp. 851–858, 2006.

[36] M. K. Jayaraj, K. J. Saji, K. Nomura, T. Kamiya, and H. Hosono, “Optical and Electrical Properties of Amorphous Zinc Tin Oxide Thin Films Examined for Thin Film Transistor Application,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 26, no. 2, pp. 495–501, 2008.

[37] M.-G. Kim, H. S. Kim, Y.-G. Ha, J. He, M. G. Kanatzidis, A. Facchetti, *et al.*, “High-Performance Solution-Processed Amorphous Zinc-Indium-Tin Oxide Thin-Film Transistors,” *Journal of the American Chemical Society*, vol. 132, no. 30, pp. 10352–10364, 2010.

[38] N. L. Dehuff, E. S. Kettenring, D. Hong, H. Q. Chiang, J. F. Wager, R. L. Hoffman, *et al.*, “Transparent Thin-Film Transistors with Zinc Indium Oxide Channel Layer,” *Journal of Applied Physics*, vol. 97, no. 6, p. 64505, 2005.

[39] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, *et al.*, “Low-Temperature, High-Performance Solution-Processed Metal Oxide Thin-

Film Transistors Formed by a ‘Sol–Gel on Chip’ Process,” *Nature Materials*, vol. 10, no. 1, pp. 45–50, 2011.

[40] R. E. Presley, D. Hong, H. Q. Chiang, C. M. Hung, R. L. Hoffman, and J. F. Wager, “Transparent Ring Oscillator Based on Indium Gallium Oxide Thin-Film Transistors,” *Solid-State Electronics*, vol. 50, no. 3, pp. 500–503, 2006.

[41] S. H. Kim, C. H. Ahn, M. G. Yun, S. W. Cho, and H. K. Cho, “Anomalous Tin Chemical Bonding in Indium-Zinc-Tin Oxide Films and Their Thin Film Transistor Performance,” *Journal of Physics D: Applied Physics*, vol. 47, no. 48, p. 485101, 2014.

[42] E. M. C. Fortunato, L. M. N. Pereira, P. M. C. Barquinha, A. M. B. do Rego, G. Gonçalves, A. Vilà, *et al.*, “High Mobility Indium Free Amorphous Oxide Thin Film Transistors,” *Applied Physics Letters*, vol. 92, no. 22, p. 222103, 2008.

[43] W. Hu, L. Zou, X. Chen, N. Qin, S. Li, and D. Bao, “Highly Uniform Resistive Switching Properties of Amorphous InGaZnO Thin Films Prepared by a Low Temperature Photochemical Solution Deposition Method,” *ACS Applied Materials & Interfaces*, vol. 6, no. 7, pp. 5012–5017, 2014.

[44] P. Barquinha, A. Pimentel, A. Marques, L. Pereira, R. Martins, and E. Fortunato, “Effect of UV and Visible Light Radiation on the Electrical Performances of Transparent TFTs Based on Amorphous Indium Zinc Oxide,” *Journal of Non-Crystalline Solids*, vol. 352, no. 9–20, pp. 1756–1760, 2006.

[45] B. Kumar, H. Gong, and R. Akkipeddi, “High Mobility Undoped Amorphous Indium Zinc Oxide Transparent Thin Films,” *Journal of Applied Physics*, vol. 98, no. 7, p. 73703, 2005.

[46] B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine, “High-Mobility Amorphous In2O3–10wt% ZnO Thin Film Transistors,” *Applied Physics Letters*, vol. 89, no. 6, p. 62103, 2006.

[47] W. J. Maeng, J. Seok Park, H.-S. Kim, T. Sang Kim, K. Seok Son, K.-B. Park, *et al.*, “Effects of Carrier Concentration in the Back and Front Channels of Hf-In-Zn-O Thin Film Transistors,” *Journal of The Electrochemical Society*, vol. 159, no. 2, pp. H147-h150, 2012.

[48] D. Hong and J. F. Wager, “Passivation of Zinc–Tin–Oxide Thin-Film Transistors,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 23, no. 6, pp. L25–L27, 2005.

[49] M. S. Rajachidambaram, A. Pandey, S. Vilayurganapathy, P. Nachimuthu, S. Thevuthasan, and G. S. Herman, “Improved Stability of Amorphous Zinc Tin Oxide Thin Film Transistors Using Molecular Passivation,” *Applied Physics Letters*, vol. 103, no. 17, p. 171602, 2013.

[50] P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, “Toward High-Performance Amorphous GIZO TFTs,” *Journal of The Electrochemical Society*, vol. 156, no. 3, pp. H161–H168, 2009.

[51] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors,” *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.

[52] K. Nomura, T. Kamiya, and H. Hosono, “Highly Stable Amorphous In-Ga-Zn-O Thin-Film Transistors Produced by Eliminating Deep Subgap Defects,” *Applied Physics Letters*, vol. 99, no. 5, p. 53505, 2011.

[53] J. K. Jeong, J. H. Jeong, H. W. Yang, J. S. Park, Y. G. Mo, and H. D. Kim, “High Performance Thin Film Transistors With Cosputtered Amorphous Indium Gallium Zinc Oxide Channel,” *Applied Physics Letters*, vol. 91, no. 11, p. 113505, 2007.

[54] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, *et al.*, “Carrier Transport and Electronic Structure in Amorphous Oxide Semiconductor, a-InGaZnO4,” *Thin Solid Films*, vol. 486, no. 1–2, pp. 38–41, 2005.

[55] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, “Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor,” *Science*, vol. 300, no. 5623, pp. 1269–1272, 2003.

[56] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park, *et al.*, “Amorphous Gallium Indium Zinc Oxide Thin Film Transistors: Sensitive to Oxygen Molecules,” *Applied Physics Letters*, vol. 90, no. 19, p. 192101, 2007.

[57] C.-J. Kim, S. Kim, J.-H. Lee, J.-S. Park, S. Kim, J. Park, *et al.*, “Amorphous Hafnium-Indium-Zinc Oxide Semiconductor Thin Film Transistors,” *Applied Physics Letters*, vol. 95, no. 25. p. 252103, 2009.

[58] T. Aoi, N. Oka, Y. Sato, R. Hayashi, H. Kumomi, and Y. Shigesato, “DC Sputter Deposition of Amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) Films with H2O Introduction,” *Thin Solid Films*, vol. 518, no. 11, pp. 3004–3007, 2010.

[59] T.-C. Fung, K. Abe, H. Kumomi, and J. Kanicki, “Electrical Instability of RF Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors,” *Journal of Display Technology*, vol. 5, no. 12, pp. 452–461, 2009.

[60] M. J. Seok, M. H. Choi, M. Mativenga, D. Geng, D. Y. Kim, and J. Jang, “A Full-Swing a-IGZO TFT-Based Inverter With a Top-Gate-Bias-Induced Depletion Load,” *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1089–1091, 2011.

[61] M. Mativenga, M. H. Choi, J. W. Choi, and J. Jang, “Transparent Flexible Circuits Based on Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors,” *IEEE Electron Device Letters*, vol. 32, no. 2, pp. 170–172, 2011.

[62] K. Nomura, T. Kamiya, and H. Hosono, “Stability and High-Frequency Operation of Amorphous In-Ga-Zn-O Thin-Film Transistors with Various Passivation Layers,” *Thin Solid Films*, vol. 520, no. 10, pp. 3778–3782, 2012.

[63] J. K. Jeong, “Photo-Bias Instability of Metal Oxide Thin Film Transistors for Advanced Active Matrix Displays,” *Journal of Materials Research*, vol. 28, no. 16, pp. 2071–2084, 2013.

[64] H.-K. Noh, K. J. Chang, B. Ryu, and W.-J. Lee, “Electronic Structure of Oxygen-Vacancy Defects in Amorphous In-Ga-Zn-O Semiconductors,” *Physical Review B*,

vol. 84, no. 11, pp. 1–8, 2011.

[65] T. Kamiya, K. Nomura, and H. Hosono, “Origins of High Mobility and Low Operation Voltage of Amorphous Oxide TFTs: Electronic Structure, Electron Transport, Defects and Doping,” *Journal of Display Technology*, vol. 5, no. 7, pp. 273–288, 2009.

[66] T. Kamiya, K. Nomura, and H. Hosono, “Present Status of Amorphous In-Ga-Zn-O Thin-Film Transistors,” *Science and Technology of Advanced Materials*, vol. 11, no. 4, p. 44305, 2010.

[67] H. Omura, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, “First-principles study of native point defects in crystalline indium gallium zinc oxide,” *Journal of Applied Physics*, vol. 105, no. 9, p. 93712, 2009.

[68] P. Ágoston, K. Albe, R. M. Nieminen, and M. J. Puska, “Intrinsic N-Type Behavior in Transparent Conducting Oxides: A Comparative Hybrid-Functional Study of In2O3, SnO2, and ZnO,” *Physical Review Letters*, vol. 103, no. 24, p. 245501, 2009.

[69] A. Suresh and J. F. Muth, “Bias Stress Stability of Indium Gallium Zinc Oxide Channel Based Transparent Thin Film Transistors,” *Applied Physics Letters*, vol. 92, no. 3, p. 33502, 2008.

[70] D. J. Yang, G. C. Whitfield, N. G. Cho, P.-S. Cho, I.-D. Kim, H. M. Saltsburg, *et al.*, “Amorphous InGaZnO4 Films: Gas Sensor Response and Stability,” *Sensors & Actuators B: Chemical*, vol. 171–172, pp. 1166–1171, 2012.

[71] F. Oba, S. R. Nishitani, S. Isotani, H. Adachi, and I. Tanaka, “Energetics of Native Defects in ZnO,” *Journal of Applied Physics*, vol. 90, no. 2, pp. 824–828, 2001.

[72] A. Janotti and C. G. Van de Walle, “Oxygen Vacancies in ZnO,” *Applied Physics Letters*, vol. 87, no. 12, p. 122102, 2005.

[73] L. Liu, Z. Mei, A. Tang, A. Azarov, A. Kuznetsov, Q.-K. Xue, *et al.*, “Oxygen Vacancies: The Origin of N-Type Conductivity in ZnO,” *Physical Review B*, vol. 93, no. 23, p. 235305, 2016.

[74] D. G. Thomas and J. J. Lander, “Hydrogen as a Donor in Zinc Oxide,” *Journal of Chemical Physics*, vol. 25, no. 6, pp. 1136–1142, 1956.

[75] C. G. de Walle, “Hydrogen as a Cause of Doping in Zinc Oxide,” *Physical Review Letters*, vol. 85, no. 5, pp. 1012–1015, 2000.

[76] D. M. Hofmann, A. Hofstaetter, F. Leiter, H. Zhou, F. Henecker, B. K. Meyer, *et al.*, “Hydrogen: A Relevant Shallow Donor in Zinc Oxide,” *Physical Review Letters*, vol. 88, no. 4, p. 45504, 2002.

[77] T. Kamiya, K. Nomura, and H. Hosono, “Subgap States, Doping and Defect Formation Energies in Amorphous Oxide Semiconductor a-InGaZnO4 Studied by Density Functional Theory,” *Physica Status Solidi (A) Applications and Materials Science*, vol. 207, no. 7, pp. 1698–1703, 2010.

[78] T. Toda, D. Wang, J. Jiang, M. P. Hung, and M. Furuta, “Quantitative Analysis of the Effect of Hydrogen Diffusion from Silicon Oxide Etch-Stopper Layer into

Amorphous In-Ga-Zn-O on Thin-Film Transistor," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3762–3767, 2014.

[79] D. Han Kang, J. Ung Han, M. Mativenga, S. Hwa Ha, and J. Jang, "Threshold Voltage Dependence on Channel Length in Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors," *Applied Physics Letters*, vol. 102, no. 8, p. 83508, 2013.

[80] Y. S. Lee, T. W. Yen, C. I. Lin, H. C. Lin, and Y. Yeh, "Electrical Characteristics of Amorphous In-Ga-Zn-O Thin-Film Transistors Prepared by Radio Frequency Magnetron Sputtering with Varying Oxygen Flows," *Displays*, vol. 35, no. 3, pp. 165–170, 2014.

[81] C.-H. Min, S. Cho, S.-H. Lee, D.-Y. Cho, W. G. Park, J. G. Chung, *et al.*, "Effect of Oxygen Partial Pressure on the Fermi Level of ZnO1-x Films Fabricated by Pulsed Laser Deposition," *Applied Physics Letters*, vol. 96, no. 20, p. 201907, 2010.

[82] J. R. Bellingham, A. P. Mackenzie, and W. A. Phillips, "Precise Measurements of Oxygen Content: Oxygen Vacancies in Transparent Conducting Indium Oxide Films," *Applied Physics Letters*, vol. 58, no. 22, pp. 2506–2508, 1991.

[83] H. K. Jeoung and K. M. Lee, "Effects of Flow Rate of Oxygen and Substrate Temperature on the Characteristics of IZO Thin Films for OLEDs," *Journal of Ceramic Processing Research*, vol. 17, no. 4, pp. 281–285, 2016.

[84] M. Orita, H. Ohta, M. Hirano, S. Narushima, and H. Hosono, "Amorphous transparent conductive oxide InGaO3(ZnO)(m) (m <= 4): a Zn 4s conductor," *Philosophical Magazine B: Physics of Condensed Matter; Statistical Mechanics, Electronic, Optical and Magnetic Properties*, vol. 81, no. 5, pp. 501–515, May 2001.

[85] P. G. LeComber, D. I. Jones, and W. E. Spear, "Hall Effect and Impurity Conduction in Substitutionally Doped Amorphous Silicon," *Philosophical Magazine*, vol. 35, no. 5, pp. 1173–1187, 1977.

[86] S. R. Elliott, *Physics of Amorphous Materials*. John Wiley & Sons, Incorporated, 1986.

[87] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, "Local Coordination Structure and Electronic Structure of the Large Electron Mobility Amorphous Oxide Semiconductor In-Ga-Zn-O: Experiment and Ab Initio Calculations," *Physical Review B - Condensed Matter and Materials Physics*, vol. 75, no. 3, p. 35210, 2007.

[88] M. D. H. Chowdhury, P. Migliorato, and J. Jang, "Low Temperature Characteristics in Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors Down to 10 K," *Applied Physics Letters*, vol. 103, no. 15, p. 152103, 2013.

[89] Y.-H. Kim, J.-S. Heo, T.-H. Kim, S. Park, M.-H. Yoon, J. Kim, *et al.*, "Flexible Metal-Oxide Devices Made by Room-Temperature Photochemical Activation of Sol-Gel Films," *Nature*, vol. 489, no. 7414, pp. 128–132, 2012.

[90] Y. Han, Y. Wang, H. T. Dai, S. G. Wang, J. L. Zhao, and X. W. Sun, "Influence of the Metallic Electrodes on the Contact Resistance of the Ink-Jet Printed In-Ga-Zn

Oxide TFTs," *Proceedings of SPIE: Oxide-based Materials and Devices IV*, vol. 8626, p. 86261H, 2013.

[91] J. H. Lim, J. H. Shim, J. H. Choi, J. Joo, K. Park, H. Jeon, *et al.*, "Solution-Processed InGaZnO-Based Thin Film Transistors for Printed Electronics Applications," *Applied Physics Letters*, vol. 95, no. 1, p. 12108, 2009.

[92] R. A. Street, T. N. Ng, R. A. Lujan, I. Son, M. Smith, S. Kim, *et al.*, "Sol–Gel Solution-Deposited InGaZnO Thin Film Transistors," *ACS Applied Materials & Interfaces*, vol. 6, no. 6, pp. 4428–4437, 2014.

[93] W.-F. Chung, T.-C. Chang, H.-W. Li, S.-C. Chen, Y.-C. Chen, T.-Y. Tseng, *et al.*, "Environment-Dependent Thermal Instability of Sol-Gel Derived Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors," *Applied Physics Letters*, vol. 98, no. 15, p. 152109, 2011.

[94] S. Kwon, J. H. Noh, J. Noh, and P. D. Rack, "Quantitative Calculation of Oxygen Incorporation in Sputtered IGZO Films and the Impact on Transistor Properties," *Journal of The Electrochemical Society*, vol. 158, no. 3, pp. H289–H293, 2011.

[95] H. Q. Chiang, B. R. McFarlane, D. Hong, R. E. Presley, and J. F. Wager, "Processing Effects on the Stability of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors," *Journal of Non-Crystalline Solids*, vol. 354, no. 19, pp. 2826–2830, 2008.

[96] Y. Li, X. Hu, Z. Liu, and J. Ren, "Power and Gas Pressure Effects on Properties of Amorphous In-Ga-ZnO Films by Magnetron Sputtering," *Journal of Materials Science: Materials in Electronics*, vol. 23, no. 2, pp. 408–412, 2012.

[97] C. S. Fuh, S. M. Sze, P. T. Liu, L. F. Teng, and Y. T. Chou, "Role of Environmental and Annealing Conditions on the Passivation-Free In-Ga-Zn-O TFT," *Thin Solid Films*, vol. 520, no. 5, pp. 1489–1494, 2011.

[98] M. D. H. Chowdhury, S. H. Ryu, P. Migliorato, and J. Jang, "Effect of Annealing Time on Bias Stress and Light-Induced Instabilities in Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors," *Journal of Applied Physics*, vol. 110, no. 11, p. 114503, 2011.

[99] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, U. K. Kim, *et al.*, "Effect of High-Pressure Oxygen Annealing on Negative Bias Illumination Stress-Induced Instability of InGaZnO Thin Film Transistors," *Applied Physics Letters*, vol. 98, no. 10, p. 103509, 2011.

[100] K. Ide, Y. Kikuchi, K. Nomura, T. Kamiya, and H. Hosono, "Effects of Low-Temperature Ozone Annealing on Operation Characteristics of Amorphous In-Ga-Zn-O Thin-Film Transistors," *Thin Solid Films*, vol. 520, no. 10, pp. 3787–3790, 2012.

[101] J. G. Um, M. Mativenga, and J. Jang, "Mechanism of Positive Bias Stress-Assisted Recovery in Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors from Negative Bias Under llumination Stress," *Applied Physics Letters*, vol. 103, no. 3, p. 33501, 2013.

[102] T. T. T. Nguyen, O. Renault, B. Aventurier, G. Rodriguez, J. P. Barnes, and F. Templier, “Analysis of IGZO Thin-Film Transistors by XPS and Relation with Electrical Characteristics,” *IEEE/OSA Journal of Display Technology*, vol. 9, no. 9, pp. 770–774, 2013.

[103] K. Nomura, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, “Defect Passivation and Homogenization of Amorphous Oxide Thin-Film Transistor by Wet O2 Annealing,” *Applied Physics Letters*, vol. 93, no. 19, p. 192107, 2008.

[104] C.-S. Fuh, P.-T. Liu, L.-F. Teng, S.-W. Huang, Y.-J. Lee, H.-P. D. Shieh, *et al.*, “Effects of Microwave Annealing on Nitrogenated Amorphous In-Ga-Zn-O Thin-Film Transistor for Low Thermal Budget Process Application,” *IEEE Electron Device Letters*, vol. 34, no. 9, pp. 1157–1159, 2013.

[105] G. Eranna, B. C. Joshi, D. P. Runthala, and R. P. Gupta, “Oxide Materials for Development of Integrated Gas Sensors - A Comprehensive Review,” *Critical Reviews in Solid State and Materials Sciences*, vol. 29, no. 3–4, pp. 111–188, 2004.

[106] A. A. Tomchenko, G. P. Harmer, B. T. Marquis, and J. W. Allen, “Semiconducting Metal Oxide Sensor Array for the Selective Detection of Combustion Gases,” *Sensors and Actuators, B: Chemical*, vol. 93, no. 1–3, pp. 126–134, 2003.

[107] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, “Origin of Threshold Voltage Instability in Indium-Gallium-Zinc Oxide Thin Film Transistors,” *Applied Physics Letters*, vol. 93, no. 12, p. 123508, 2008.

[108] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, “Electronic Transport Properties of Amorphous Indium-Gallium-Zinc Oxide Semiconductor Upon Exposure to Water,” *Applied Physics Letters*, vol. 92, no. 7, p. 72104, 2008.

[109] T. C. Chen, T. C. Chang, T. Y. Hsieh, C. T. Tsai, S. C. Chen, C. S. Lin, *et al.*, “Light-Induced Instability of an InGaZnO Thin Film Transistor with and without SiOx Passivation Layer Formed by Plasma-Enhanced-Chemical- Vapor-Deposition,” *Applied Physics Letters*, vol. 97, no. 19, p. 192103, 2010.

[110] J. F. Wager, K. Hoshino, E. S. Sundholm, R. E. Presley, R. Ravichandran, C. C. Knutson, *et al.*, “A Framework for Assessing Amorphous Oxide Semiconductor Thin-Film Transistor Passivation,” *Journal of the Society for Information Display*, vol. 20, no. 10, pp. 589–595, 2012.

[111] M. D. H. Chowdhury, M. Mativenga, J. G. Um, R. K. Mruthyunjaya, G. N. Heiler, T. J. Tredwell, *et al.*, “Effect of SiO2 and SiO2/SiNx Passivation on the Stability of Amorphous Indium-Gallium Zinc-Oxide Thin-Film Transistors Under High Humidity,” *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 869–874, 2015.

[112] J. Li, F. Zhou, H.-P. Lin, W.-Q. Zhu, J.-H. Zhang, X.-Y. Jiang, *et al.*, “Effect of Reactive Sputtered SiOx Passivation Layer on the Stability of InGaZnO Thin Film Transistors,” *Vacuum*, vol. 86, no. 12, pp. 1840–1843, 2012.

[113] S. An, M. Mativenga, Y. Kim, and J. Jang, “Improvement of Bias-Stability in Amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors by using Solution-Processed Y2O3 Passivation,” *Applied Physics Letters*, vol. 105, no. 5, p. 53507,

2014.

[114] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, “Bias-Stress-Induced Stretched-Exponential Time Dependence of Threshold Voltage Shift In InGaZnO Thin Film Transistors,” *Applied Physics Letters*, vol. 93, no. 9, p. 93504, 2008.

[115] W.-S. Kim, Y.-H. Lee, Y.-J. Cho, B.-K. Kim, K. T. Park, and O. Kim, “Effect of Wavelength and Intensity of Light on a-InGaZnO TFTs under Negative Bias Illumination Stress,” *ECS Journal of Solid State Science and Technology*, vol. 6, no. 1, pp. Q6–Q9, 2017.

[116] K.-A. Kim, M.-J. Park, W.-H. Lee, and S.-M. Yoon, “Characterization of Negative Bias-Illumination-Stress Stability for Transparent Top-Gate In-Ga-Zn-O Thin-Film Transistors with Variations in the Incorporated Oxygen Content,” *Journal of Applied Physics*, vol. 118, no. 23, p. 234504, 2015.

[117] M. P. Hung, D. Wang, J. Jiang, and M. Furuta, “Negative Bias and Illumination Stress Induced Electron Trapping at Back-Channel Interface of InGaZnO Thin-Film Transistor,” *ECS Solid State Letters*, vol. 3, no. 3, pp. Q13–Q16, 2014.

[118] X. Zhou, Y. Shao, L. Zhang, X. Xiao, D. Han, Y. Wang, *et al.*, “Investigation of a Hump Phenomenon in Back-Channel-Etched Amorphous In-Ga-Zn-O Thin-Film Transistors Under Negative Bias Stress,” *IEEE Electron Device Letters*, vol. 38, no. 5, pp. 592–595, 2017.

[119] M. D. H. Chowdhury, P. Migliorato, and J. Jang, “Light Induced Instabilities in Amorphous Indium–Gallium–Zinc–Oxide Thin-Film Transistors,” *Applied Physics Letters*, vol. 97, no. 17, p. 173506, 2010.

[120] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang, and S.-H. K. Park, “Photon-Accelerated Negative Bias Instability Involving Subgap States Creation in Amorphous In–Ga–Zn–O Thin Film Transistor,” *Applied Physics Letters*, vol. 97, no. 18, p. 183502, 2010.

[121] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, *et al.*, “The Effect of Moisture on the Photon-Enhanced Negative Bias Thermal Instability in Ga-In-Zn-O Thin Film Transistors,” *Applied Physics Letters*, vol. 95, no. 23, p. 232106, 2009.

[122] K. H. Ji, J. I. Kim, Y. G. Mo, J. H. Jeong, S. Yang, C. S. Hwang, *et al.*, “Comparative Study on Light-Induced Bias Stress Instability of IGZO Transistors with SiNx and SiO2 Gate Dielectrics,” *IEEE Electron Device Letters*, vol. 31, no. 12, pp. 1404–1406, 2010.

[123] S. Takasugi, H. Shin, M. Chang, S. Ko, H. Park, J. Lee, *et al.*, “Advanced Compensation Technologies for Large-Sized UHD OLED TVs,” *Journal of the Society for Information Display*, vol. 24, no. 7, pp. 410–418, 2016.

[124] Y. H. Jang, D. H. Kim, W. Choi, M.-G. Kang, K. Il Chun, J. Jeon, *et al.*, “Internal Compensation Type OLED Display Using High Mobility Oxide TFT,” *SID Symposium Digest of Technical Papers*, vol. 48, no. 1, pp. 76–79, 2017.

[125] T. Orui, J. Herms, Y. Hanyu, S. Ueda, K. Watanabe, I. Sakaguchi, *et al.*, “Charge

Compensation by Excess Oxygen in Amorphous In-Ga-Zn-O Films Deposited by Pulsed Laser Deposition," *Journal of Display Technology*, vol. 11, no. 6, pp. 518–522, 2015.

[126] Y.-S. Lee, E. K.-H. Yu, D.-H. Shim, H.-S. Kong, L. Bie, and J. Kanicki, "Oxygen Flow Effects on Electrical Properties, Stability, and Density of States of Amorphous In-Ga-Zn-O Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 53, no. 12, p. 121101, 2014.

[127] S. O. Ryu, "Effects of Deposition Power and Oxygen Partial Pressure on Low-Temperature-Processed In-Ga-Zn-O Thin-Film Transistors," *Journal of Nanoelectronics and Optoelectronics*, vol. 6, no. 3, pp. 283–287, 2011.

[128] P. T. Liu, Y. T. Chou, L. F. Teng, F. H. Li, and H. P. Shieh, "Nitrogenated Amorphous InGaZnO Thin Film Transistor," *Applied Physics Letters*, vol. 98, no. 5, p. 52102, 2011.

[129] C. H. Jung, D. J. Kim, Y. K. Kang, and D. H. Yoon, "Transparent Amorphous In-Ga-Zn-O Thin Films as Aunction of Various Gas Flows for TFT Applications," *1st International Conference on Microelectronics and Plasma Technology*, vol. 517, no. 14, pp. 4078–4081, 2009.

[130] T. Goto, S. Sugawa, and T. Ohmi, "Impact of the Use of Xe on Electrical Properties in Magnetron-Sputtering Deposited Amorphous InGaZnO Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 52, no. 5, p. 50203, 2013.

[131] Y. J. Tak, B. Du Ahn, S. P. Park, S. J. Kim, A. R. Song, K.-B. Chung, *et al.*, "Activation of Sputter-Processed Indium–Gallium–Zinc Oxide Films by Simultaneous Ultraviolet and Thermal Treatments," *Scientific Reports*, vol. 6, p. 21869, 2016.

[132] H. Hosono, K. Nomura, Y. Ogo, T. Uruga, and T. Kamiya, "Factors Controlling Electron Transport Properties in Transparent Amorphous Oxide Semiconductors," *Journal of Non-Crystalline Solids*, vol. 354, no. 19–25, pp. 2796–2800, 2008.

[133] S. Yamazaki, T. Atsumi, K. Dairiki, K. Okazaki, and N. Kimizuka, "In-Ga-Zn-Oxide Semiconductor and Its Transistor Characteristics," *ECS Journal of Solid State Science and Technology*, vol. 3, no. 9, pp. Q3012–Q3022, 2014.

[134] D. M. Lynch, B. Zhu, B. D. A. Levin, D. A. Muller, D. G. Ast, R. G. Greene, *et al.*, "Characterization of Reactively Sputtered C-Axis Aligned Nanocrystalline InGaZnO4," *Applied Physics Letters*, vol. 105, no. 26, p. 262103, 2014.

[135] C. F. Brucker, "Electron Spectroscopy: Theory, Techniques and Applications," in *Academic Press London*, vol. 2, C. R. Brundle and A. D. Baker, Eds. Academic Press, 1978, pp. 3–7.

[136] S. Yamazaki, J. Koyama, Y. Yamamoto, and K. Okamoto, "Research, Development, and Application of Crystalline Oxide Semiconductor," *SID Symposium Digest of Technical Papers*, vol. 43, no. 1, pp. 183–186, 2012.

[137] D. K. Schroder, "Semiconductor Material and Device Characterization," 3rd ed., Wiley-Interscience, 2006, pp. 654–659.

[138] T. Szörényi, L. D. Laude, I. Bertóti, Z. Kántor, and Z. Geretovszky, “Excimer Laser Processing of Indium-Tin-Oxide Films: An Optical Investigation,” *Journal of Applied Physics*, vol. 78, no. 10, pp. 6211–6219, 1995.

[139] S. Major, S. Kumar, M. Bhatnagar, and K. L. Chopra, “Effect of Hydrogen Plasma Treatment on Transparent Conducting Oxides,” *Applied Physics Letters*, vol. 49, no. 7, pp. 394–396, 1986.

[140] S. Kačiulis, “Influence of Surface Oxygen on Chemoresistance of Tin Oxide Film,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 14, no. 6, pp. 3164–3168, 1996.

[141] M.-G. Kim, M. G. Kanatzidis, A. Facchetti, and T. J. Marks, “Low-Temperature Fabrication of High-Performance Metal Oxide Thin-Film Electronics via Combustion Processing,” *Nature Materials*, vol. 10, no. 5, pp. 382–388, 2011.

[142] T. T. T. Nguyen, B. Aventurier, T. Terlier, J. Barnes, and F. Templier, “Impact of Passivation Conditions on Characteristics of Bottom-Gate IGZO Thin-Film Transistors,” *Journal of Display Technology*, vol. 11, no. 6, pp. 554–558, 2015.

[143] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, “Trap Densities in Amorphous- InGaZnO4 Thin-Film Transistors,” *Applied Physics Letters*, vol. 92, no. 13, p. 133512, 2008.

[144] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, “Origins of Threshold Voltage Shifts in Room-Temperature Deposited and Annealed a-In-Ga-Zn-O Thin-Film Transistors,” *Applied Physics Letters*, vol. 95, no. 1, p. 13502, 2009.

[145] L. Lu and M. Wong, “A Bottom-Gate Indium-Gallium-Zinc Oxide Thin-Film Transistor with an Inherent Etch-Stop and Annealing-Induced Source and Drain Regions,” *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 574–579, 2015.

[146] B. Du Ahn, J. H. Lim, M.-H. Cho, J.-S. Park, and K.-B. Chung, “Thin-Film Transistor Behaviour and the Associated Physical Origin of Water-Annealed In–Ga–Zn Oxide Semiconductor,” *Journal of Physics D: Applied Physics*, vol. 45, no. 41, p. 415307, 2012.

[147] R. Hayashi, M. Ofuji, N. Kaji, K. Takahashi, K. Abe, H. Yabuta, *et al.*, “Circuits Using Uniform TFTs Based on Amorphous In – Ga – Zn – O,” *Journal of the Society for Information Display*, vol. 15, no. 11, pp. 915–921, 2007.

[148] T. C. Fung, C. S. Chuang, C. Chen, K. Abe, R. Cottle, M. Townsend, *et al.*, “Two-Dimensional Numerical Simulation of Radio Frequency Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors,” *Journal of Applied Physics*, vol. 106, no. 8, p. 84511, 2009.

[149] J. Park, C. Kim, S. Kim, I. Song, S. Kim, D. Kang, *et al.*, “Source/Drain Series-Resistance Effects in Amorphous Gallium-Indium Zinc-Oxide Thin Film Transistors,” *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 879–881, 2008.

[150] X. Zou, G. Fang, J. Wan, N. Liu, H. Long, H. Wang, *et al.*, “Enhanced Performance of a-IGZO Thin-Film Transistors by Forming AZO/IGZO Heterojunction

Source/Drain Contacts," *Semiconductor Science and Technology*, vol. 26, no. 5, p. 55003, 2011.

[151] J. Jeong, G. Jun Lee, J. Kim, and B. Choi, "Electrical Characterization of a-InGaZnO Thin-Film Transistors with Cu Source/Drain Electrodes," *Applied Physics Letters*, vol. 100, no. 11, p. 112109, 2012.

[152] J. H. Na, M. Kitamura, and Y. Arakawa, "High Field-Effect Mobility Amorphous InGaZnO Transistors with Aluminum Electrodes," *Applied Physics Letters*, vol. 93, no. 6, p. 63501, 2008.

[153] W. S. Kim, Y. K. Moon, K. T. Kim, J. H. Lee, B. Du Ahn, and J. W. Park, "An Investigation of Contact Resistance Between Metal Electrodes and Amorphous Ggallium-Indium-Zinc Oxide (a-GIZO) Thin-Film Transistors," *Thin Solid Films*, vol. 518, no. 22, pp. 6357–6360, 2010.

[154] P. Barquinha, A. M. Vilà, G. Gonçalves, L. Pereira, R. Martins, J. R. Morante, *et al.*, "Gallium – Indium – Zinc-Oxide-Based Thin-Film Transistors : Influence of the Source / Drain Material," *IEEE Transactions on Electron Devices*, vol. 55, no. 4, pp. 954–960, 2008.

[155] Y. Shimura, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Specific Contact Resistances Between Amorphous Oxide Semiconductor In-Ga-Zn-O and Metallic Electrodes," *Thin Solid Films*, vol. 516, no. 17, pp. 5899–5902, 2008.

[156] J. Y. Bak, S. Yang, M. K. Ryu, S. Hee, K. Park, C. S. Hwang, *et al.*, "Effect of the Electrode Materials on the Drain-Bias Stress Instabilities of In-Ga-Zn-O Thin-Film Transistors," *Applied Materials and Interfaces*, vol. 4, no. 10, pp. 5369–5374, 2012.

[157] K. Hoshino and J. F. Wager, "Operating Temperature Trends in Amorphous In-Ga-Zn-O Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 818–820, 2010.

[158] S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-C. Chen, C.-T. Tsai, M.-C. Hung, *et al.*, "Effects of Ambient Atmosphere on Electrical Characteristics of Al2O3 Passivated InGaZnO Thin Film Transistors during Positive-Bias-Temperature-Stress Operation," *Electrochemical and Solid-State Letters*, vol. 14, no. 4, pp. H177–H179, 2011.

[159] S. Y. Huang, T. C. Chang, M. C. Chen, T. C. Chen, F. Y. Jian, Y. C. Chen, *et al.*, "Improvement in the Bias Stability of Amorphous InGaZnO TFTs Using an Al2O3 Passivation Layer," *Surface and Coatings Technology*, vol. 231, pp. 117–121, 2013.

[160] E. N. Cho, J. H. Kang, and I. Yun, "Contact Resistance Dependent Scaling-Down Behavior of Amorphous InGaZnO Thin-Film Transistors," *Current Applied Physics*, vol. 11, no. 4, pp. 1015–1019, 2011.

[161] W.-S. Kim, Y.-K. Moon, S. Lee, B.-W. Kang, K.-T. Kim, J.-H. Lee, *et al.*, "Amorphous Indium Gallium Zinc Oxide Semiconductor Thin Film Transistors Using O2 Plasma Treatment on the SiNx Gate Insulator," *Japanese Journal of Applied Physics*, vol. 49, no. 8, p. 08JF02, 2010.

[162] A. Tari, C.-H. Lee, and W. S. Wong, “Electrical Dependence on the Chemical Composition of the Gate Dielectric in Indium Gallium Zinc Oxide Thin-Film Transistors,” *Applied Physics Letters*, vol. 107, no. 2, p. 23501, 2015.

[163] R. K. Cherie and A. Paul, Eds., “Thin-Film Transistors,” New York : Marcel Dekker, 2003.

[164] K. Terada, “A New Method to Determine MOSFET Channel Length,” *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 953–959, 1980.

[165] W. Orton, “Characteristics of Amorphous Silicon Staggered-Electrode Thin-Film Transistors,” *Applied Physics Letters*, vol. 45, no. 2, pp. 171–173, 1984.

[166] A. Sato, M. Shimada, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, *et al.*, “Amorphous In-Ga-Zn-O Thin-Film Transistor with Coplanar Homojunction Structure,” *Thin Solid Films*, vol. 518, no. 4, pp. 1309–1313, 2009.

[167] Y.-C. Huang, P.-Y. Yang, H.-Y. Huang, S.-J. Wang, and H.-C. Cheng, “Effect of the Annealing Ambient on the Electrical Characteristics of the Amorphous InGaZnO Thin Film Transistors,” *Journal of Nanoscience and Nanotechnology*, vol. 12, no. 7, pp. 5625–5630, 2012.

[168] Y. Kikuchi, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, “Device Characteristics Improvement of a-In-Ga-Zn-O TFTs by Low-Temperature Annealing,” *Thin Solid Films*, vol. 518, no. 11, pp. 3017–3021, 2010.

[169] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, “Effects of Excess Oxygen on Operation Characteristics of Amorphous In-Ga-Zn-O Thin-Film Transistors,” *Applied Physics Letters*, vol. 99, no. 9, p. 93507, 2011.

[170] B. Shie, H. Lin, R. Lyu, and T. Huang, “Effects of Gate Dielectric and Process Treatments on the Electrical Characteristics of IGZO TFTs,” *IEEE Transactions on Plasma Science*, vol. 42, no. 12, pp. 3742–3746, 2014.

[171] K. Kurishima, T. Nabatame, M. Shimizu, S. Aikawa, K. Tsukagoshi, A. Ohi, *et al.*, “Influence of Al2O3 Gate Dielectric on Transistor Properties for IGZO Thin Film Transistor,” *ECS Transactions Solid State Letters*, vol. 61, no. 4, pp. 345–351, 2014.

[172] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X.-H. Zhang, and B. Kippelen, “Low-Voltage InGaZnO Thin-Film Yransistors with Al2O3 Gate Insulator Grown by Atomic Layer Deposition,” *Applied Physics Letters*, vol. 94, no. 14, p. 142107, 2009.

[173] Z. Wu, Z. Yao, S. Liu, B. Yuan, Y. Zhang, Y. Liang, *et al.*, “Tuning the Electrical Performance of Metal Oxide Thin-Film Transistors via Dielectric Interface Trap Passivation and Graded Channel Modulation,” *Journal of Materials Chemistry C*, no. 5, pp. 1206–1215, 2017.

[174] H. Zan, W. Chen, C. Yeh, and H. Hsueh, “Dual Gate Indium-Gallium-Zinc-Oxide Thin Film Transistor with an Unisolated Floating Metal Gate for Threshold Voltage Modulation and Mobility Enhancement,” *Applied Physics Letters*, vol. 98, no. 15, p. 153506, 2011.

[175] S. Y. Lee, S. Chang, and J. Lee, “Role of High-k Gate Insulators for Oxide Thin

Film Transistors," *Thin Solid Films*, vol. 518, no. 11, pp. 3030–3032, 2010.

[176] Y. S. Chun, S. Chang, and S. Y. Lee, "Effects of Gate Insulators on the Performance of a-IGZO TFT Fabricated at Room-Temperature," *Microelectronic Engineering*, vol. 88, no. 7, pp. 1590–1593, 2011.

[177] X. Zou, G. Fang, L. Yuan, X. Tong, and X. Zhao, "Improved Electrical Characteristics and Reliability of Amorphous InGaZnO Metal–Insulator–Semiconductor Capacitor with High κ HfOxNy Gate Dielectric," *Microelectronics Reliability*, vol. 50, no. 7, pp. 954–958, 2010.

[178] G. Li, B.-R. Yang, C. Liu, C.-Y. Lee, C.-Y. Tseng, C.-C. Lo, *et al.*, "Positive Gate Bias Instability Alleviated by Self-Passivation Effect in Amorphous InGaZnO Thin-Film Transistors," *Journal of Physics D: Applied Physics*, vol. 48, no. 47, p. 475107, 2015.

[179] A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, "Electrical Properties of Amorphous Silicon Transistors and MIS-Devices: Comparative Study of Top Nitride and Bottom Nitride Configurations," *Journal of The Electrochemical Society*, vol. 140, no. 12, pp. 3679–3683, 1993.

[180] K. Hoshino, B. Yeh, and J. F. Wager, "Impact of Humidity on the Electrical Performance of Amorphous Oxide Semiconductor thin-film transistors," *Journal of the Society for Information Display*, vol. 21, no. 7, pp. 310–316, 2013.

[181] D. H. Cho, S. H. Yang, J.-H. Shin, C. W. Byun, M. K. Ryu, J. I. Lee, *et al.*, "Passivation of Bottom-Gate IGZO Thin Film Transistors," *Journal of the Korean Physical Society*, vol. 54, no. 1, pp. 531–534, 2009.

[182] A. Olziersky, P. Barquinha, A. Vilὶ, L. Pereira, G. Goṇalves, E. Fortunato, *et al.*, "Insight on the SU-8 Resist as Passivation Layer for Transparent Ga2O3–In2O3–ZnO Thin-Film Transistors," *Journal of Applied Physics*, vol. 108, no. 6, p. 64505, 2010.

[183] J. Tanaka, Y. Ueoka, K. Yoshitsugu, M. Fujii, Y. Ishikawa, Y. Uraoka, *et al.*, "Comparison Between Effects of PECVD-SiOx and Thermal ALD-AlOx Passivation Layers on Characteristics of Amorphous InGaZnO TFTs," *ECS Journal of Solid State Science and Technology*, vol. 4, no. 7, pp. Q61–Q65, 2015.

[184] S. Lee, S. Park, S. Kim, Y. Jeon, K. Jeon, J.-H. Park, *et al.*, "Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors by Using Multifrequency Capacitance-Voltage Characteristics," *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 231–233, 2010.

[185] M. Bae, D. Yun, Y. Kim, D. Kong, H. K. Jeong, W. Kim, *et al.*, "Differential Ideality Factor Technique for Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 399–401, 2012.

[186] J. H. Park, K. Jeon, S. Lee, S. Kim, S. Kim, I. Song, *et al.*, "Extraction of Density of States in Amorphous GaInZnO Thin-Film Transistors by Combining an Optical Charge Pumping and Capacitance-Voltage Characteristics," *IEEE Electron Device Letters*, vol. 29, no. 12, pp. 1292–1295, 2008.

[187] H. Bae, H. Seo, S. Jun, H. Choi, J. Ahn, J. Hwang, *et al.*, "Fully Current-Based Sub-Bandgap Optoelectronic Differential Ideality Factor Technique and Extraction of Subgap DOS in Amorphous Semiconductor TFTs," *IEEE Transactions on Electron Devices*, vol. 61, no. 10, pp. 3566–3569, 2014.

[188] M. Bae, Y. Kim, S. Kim, D. M. Kim, and D. H. Kim, "Extraction of Subgap Donor States in a-IGZO TFTs by Generation-Recombination Current Spectroscopy," *IEEE Electron Device Letters*, vol. 32, no. 9, pp. 1248–1250, 2011.

[189] "Atlas User's Manual," in *Device Simulation Software*, 2016, pp. 816–833.

[190] T. Kamiya, K. Nomura, M. Hirano, and H. Hosono, "Electronic Structure of Oxygen Deficient Amorphous Oxide Semiconductor a-InGaZnO4-x: Optical Analyses and First-Principle Calculations," *Physica Status Solidi (C) Current Topics in Solid State Physics*, vol. 5, no. 9, pp. 3098–3100, 2008.

[191] M. J. Powell, "The Physics of Amorphous-Silicon Thin-Film Transistors," *IEEE Transactions on Electron Devices*, vol. 36, no. 12, pp. 2753–2763, 1989.

[192] I. T. Cho, I. J. Park, D. Kong, D. H. Kim, J. H. Lee, S. H. Song, *et al.*, "Extraction of the Channel Mobility in InGaZnO TFTs Using Multifrequency Capacitance-Voltage Method," *IEEE Electron Device Letters*, vol. 33, no. 6, pp. 815–817, 2012.

[193] N. F. Mott, "Conduction in Glasses Containing Transition Metal Ions," *Journal of Non-Crystalline Solids*, vol. 1, no. 1, pp. 1–17, 1968.

[194] K. Nomura, T. Kamiya, H. Ohta, K. Ueda, M. Hirano, and H. Hosono, "Carrier Transport in Transparent Oxide Semiconductor with Intrinsic Structural Randomness Probed using Single-Crystalline InGaO3(ZnO)5 Films," *Applied Physics Letters*, vol. 85, no. 11, pp. 1993–1995, 2004.

[195] C. Chen, K. Abe, H. Kumomi, and J. Kanicki, "Density of States of a-InGaZnO From Temperature-Dependent Field-Effect Studies," *IEEE Transactions on Electron Devices*, vol. 56, no. 6, pp. 1177–1183, 2009.

[196] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Temperature-Dependent Transfer Characteristics of Amorphous InGaZnO4 Thin-Film Transistors," *Japanese Journal of Applied Physics*, vol. 48, no. 1R, p. 11301, 2009.

[197] P. G. LeComber and W. E. Spear, "Electronic Transport in Amorphous Silicon Films," *Physical Review Letters*, vol. 25, no. 8, pp. 509–511, 1970.

[198] C.-C. Hsu, J.-K. Sun, and C.-H. Wu, "A Study of Trap-Limited Conduction Influenced by Plasma Damage on the Source/Drain Regions of Amorphous InGaZnO TFTs," *Journal of Physics D: Applied Physics*, vol. 48, no. 44, p. 445104, 2014.

[199] H.-J. Chung, J. H. Jeong, T. K. Ahn, H. J. Lee, M. Kim, K. Jun, *et al.*, "Bulk-Limited Current Conduction in Amorphous InGaZnO Thin Films," *Electrochemical and Solid-State Letters*, vol. 11, no. 3, pp. H51–H54, 2008.

[200] S. Lee and A. Nathan, "Localized Tail State Distribution in Amorphous Oxide Transistors Deduced From Low Temperature Measurements," *Applied Physics Letters*, vol. 101, no. 11, p. 113502, 2012.

[201] T. Kamiya, K. Nomura, and H. Hosono, “Electronic Structures Above Mobility Edges in Crystalline and Amorphous In-Ga-Zn-O: Percolation Conduction Examined by Analytical Model,” *Journal of Display Technology*, vol. 5, no. 12, pp. 462–467, 2009.

[202] A. Ortiz-Conde, F. J. García Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, “A Review of Recent MOSFET Threshold Voltage Extraction Methods,” *Microelectronics Reliability*, vol. 42, no. 4–5, pp. 583–596, 2002.

[203] J. R. Hauser, “Extraction of Experimental Mobility Data for MOS Devices,” *IEEE Transactions on Electron Devices*, vol. 43, no. 11, pp. 1981–1988, 1996.

[204] H. S. Wong, M. H. White, T. J. Krutsick, and R. V Booth, “Modeling of Transconductance Degradation and Extraction of Threshold Voltage in Thin Oxide MOSFET,” *Solid-State Electronics*, vol. 30, no. 9, pp. 953–968, 1987.

[205] M. Shur and M. Hack, “Physics of Amorphous Silicon Based Alloy Field-Effect Transistors,” *Journal of Applied Physics*, vol. 55, no. 10, pp. 3831–3842, 1984.

[206] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J.-S. Park, *et al.*, “High Mobility Bottom Gate InGaZnO Thin Film Transistors with SiOx Etch Stopper,” *Applied Physics Letters*, vol. 90, no. 21, p. 212114, 2007.

[207] K.-H. Choi and H.-K. Kim, “Correlation between Ti Source/Drain Contact and Performance of InGaZnO-Based Thin Film Transistors,” *Applied Physics Letters*, vol. 102, no. 5, p. 52103, 2013.

[208] R. L. Hoffman, “ZnO-Channel Thin-Film Transistors: Channel Mobility,” *Journal of Applied Physics*, vol. 95, no. 10, pp. 5813–5819, 2004.

[209] G. Ghibaudo, “New Method for the Extraction of MOSFET Parameters,” *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988.

[210] M. Shur, M. Hack, and J. G. Shaw, “A New Analytic Model for Amorphous-Silicon Thin-Film Transistors,” *Journal of Applied Physics*, vol. 66, no. 7, pp. 3371–3380, 1989.

[211] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, “SPICE Models for Amorphous Silicon and Polysilicon Thin Film Transistors,” *Journal of The Electrochemical Society*, vol. 144, no. 8, pp. 2833–2839, 1997.

[212] T. Kamiya, K. Nomura, and H. Hosono, “Origin of Definite Hall Voltage and Positive Slope in Mobility-Donor Density Relation in Disordered Oxide Semiconductors,” *Applied Physics Letters*, vol. 96, no. 12, p. 122103, 2010.

[213] K. Abe, N. Kaji, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, *et al.*, “Simple Analytical Model of On Operation of Amorphous In-Ga-Zn-O Thin-Film Transistors,” *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3463–3471, 2011.

[214] J.-H. Shin, W.-S. Cheong, C.-S. Hwang, and S. M. Chung, “Modeling of Amorphous InGaZnO Thin Film Transistors Using an Empirical Mobility Function based on the Exponential Deep and Tail States,” *Thin Solid Films*, vol. 520, no. 10, pp. 3800–3802, 2012.

[215] S. Lee, D. Striakhilev, S. Jeon, and A. Nathan, “Unified Analytic Model for Current – Voltage Behavior in Amorphous Oxide Semiconductor TFTs,” *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 84–86, 2014.

[216] Z. Zong, L. Li, J. Jang, N. Lu, and M. Liu, “Analytical Surface-Potential Compact Model for Amorphous-IGZO Thin-Film Transistors,” *Journal of Applied Physics*, vol. 117, no. 21, p. 215705, 2015.

[217] W. Deng, J. Huang, X. Ma, and T. Ning, “An Explicit Surface-Potential-Based Model for Amorphous IGZO Thin-Film Transistors Including Both Tail and Deep States,” *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 78–80, 2014.

[218] A. Tsormpatzoglou, N. A. Hastas, N. Choi, F. Mahmoudabadi, M. K. Hatalis, and C. A. Dimitriadis, “Analytical Surface-Potential-based Drain Current Model for Amorphous InGaZnO Thin Film Transistors,” *Journal of Applied Physics*, vol. 114, no. 18, p. 184502, 2013.

[219] J.-H. Park, Y. Kim, S. Kim, H. Bae, D. H. Kim, and D. M. Kim, “Surface-Potential-Based Analytic DC I-V Model With Effective Electron Density for a-IGZO TFTs Considering the Parasitic Resistance,” *IEEE Electron Device Letters*, vol. 32, no. 11, pp. 1540–1542, 2011.

[220] M. Ghittorelli, F. Torricelli, and L. Colalongo, “Accurate Analytical Physical Modeling of Amorphous InGaZnO Thin-Film Transistors Accounting for Trapped and Free Charges,” *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 4105–4112, 2014.

[221] Y. W. Jeon, S. Kim, S. Lee, D. M. Kim, D. H. Kim, J. Park, *et al.*, “Subgap Density-of-States-Based Amorphous Oxide Thin Film Transistor Simulator (DeAOTS),” *IEEE Transactions on Electron Devices*, vol. 57, no. 11, pp. 2988–3000, 2010.

[222] M. Bae, K. M. Lee, E. Cho, H. Kwon, D. M. Kim, D. H. Kim, *et al.*, “Analytical Current and Capacitance Models for Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors,” *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3465–3473, 2013.

[223] L. Colalongo, “Compact Model of Amorphous InGaZnO Thin-Film Transistors Based on the Symmetric Quadrature of the Accumulation Charge,” *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 416–418, 2016.

[224] R. L. Hoffman, “A Closed-Form DC Model for Long-Channel Thin-Film Transistors with Gate Voltage-Dependent Mobility Characteristics,” *Solid State Electronics*, vol. 49, no. 4, pp. 648–653, 2005.

[225] A. Zeumault and V. Subramanian, “Improved Technique for Quantifying the Bias-Dependent Mobility of Metal-Oxide Thin-Film Transistors,” *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 855–861, 2015.

[226] A. I. T. Transistors, L. Qiang, and R. Yao, “A New Definition of the Threshold Voltage for Amorphous InGaZnO Thin-Film Transistors,” *IEEE Transactions on Electron Devices*, vol. 61, no. 7, pp. 2394–2397, 2014.

[227] C.-L. Chen, W.-F. Chen, L. Zhou, W.-J. Wu, M. Xu, L. Wang, *et al.*, “A Physics-

Based Model of Threshold Voltage for Amorphous Oxide Semiconductor Thin-Film Transistors," *AIP Advances*, vol. 6, no. 3, p. 35025, 2016.

[228] C.-S. Fuh, P.-T. Liu, Y.-T. Chou, L.-F. Teng, and S. M. Sze, "Role of Oxygen in Amorphous In-Ga-Zn-O Thin Film Transistor for Ambient Stability," *ECS Journal of Solid State Science and Technology*, vol. 2, no. 1, pp. Q1–Q5, 2013.

[229] S.-Y. Sung, J. H. Choi, U. Bin Han, K. C. Lee, J.-H. Lee, J.-J. Kim, *et al.*, "Effects of Ambient Atmosphere on the Transfer Characteristics and Gate-Bias Stress Stability of Amorphous Indium-Gallium-Zinc Oxide Thin-Film Transistors," *Applied Physics Letters*, vol. 96, no. 10, p. 102107, 2010.

[230] Z. Xiao, K. Domen, T. Kamiya, and H. Hosono, "Apparent High Mobility Similar to 30cm(2)/Vs of Amorphous In-Ga-Zn-O Thin-Film Transistor and Its Origin," *Journal of the Ceramic Society of Japan*, vol. 121, no. 1411, pp. 295–298, 2013.

[231] S. C. Kim, Y. S. Kim, E. K.-H. Yu, and J. Kanicki, "Short Channel Amorphous In-Ga-Zn-O Thin-Film Transistor Arrays for Ultra-High Definition Active Matrix Liquid Crystal Displays: Electrical Properties and Stability," *Solid-State Electronics*, vol. 111, pp. 67–75, 2015.

[232] J. H. Choi, J. Pi, C. Hwang, J. Yang, G. H. Kim, Y. Kim, *et al.*, "Toward Sub-Micron Oxide Thin-Film Transistors for Digital Holography," *Journal of the Society for Information Display*, vol. 25, no. 2, pp. 126–135, 2017.

[233] B. Du Ahn, H. S. Shin, H. J. Kim, J.-S. Park, and J. K. Jeong, "Comparison of the Effects of Ar and H2 Plasmas on the Performance of Homojunctioned Amorphous Indium Gallium Zinc Oxide Thin Film Transistors," *Applied Physics Letters*, vol. 93, no. 20, p. 203506, 2008.

[234] M. P. Hung, D. Wang, and M. Furuta, "Investigating Effect of Postannealing Time on Positive Bias Stress Stability of In-Ga-Zn-O TFT by Conductance Method," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3697–3702, 2015.

[235] Y. Han, C. Cui, J. Yang, M.-Y. Tsai, T.-C. Chang, and Q. Zhang, "H2O Induced Hump Phenomenon in Capacitance-Voltage Measurements of a-IGZO Thin-Film Transistors," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 1, pp. 20–24, 2016.

[236] C.-Y. Jeong, D. Lee, S.-H. Song, J. I. Kim, J.-H. Lee, and H.-I. Kwon, "A Study on the Degradation Mechanism of InGaZnO Thin-Film Transistors Under Simultaneous Gate and Drain Bias Stresses Based on the Electronic Trap Characterization," *Semiconductor Science and Technology*, vol. 29, no. 4, p. 45023, 2014.

[237] H. Im, H. Song, J. Jeong, Y. Hong, and Y. Hong, "Effects of Defect Creation on Bidirectional Behavior with Hump Characteristics of InGaZnO TFTs Under Bias and Thermal Stress," *Japanese Journal of Applied Physics*, vol. 54, no. 3, p. 03CB03, 2015.

[238] S. Choi, H. Kim, C. Jo, H.-S. Kim, S.-J. Choi, D. M. Kim, *et al.*, "The Effect of Gate and Drain Fields on the Competition Between Donor-Like State Creation and Local Electron Trapping in In-Ga-Zn-O Thin Film Transistors Under Current Stress,"

IEEE Electron Device Letters, vol. 36, no. 12, pp. 1336–1339, 2015.

[239] K. Nomura, T. Kamiya, E. Ikenaga, H. Yanagi, K. Kobayashi, and H. Hosono, "Depth Analysis of Subgap Electronic States in Amorphous Oxide Semiconductor, a-In-Ga-Zn-O, Studied by Hard R-Ray Photoelectron Spectroscopy," *Journal of Applied Physics*, vol. 109, no. 7, p. 73726, 2011.

[240] M. D. McCluskey and S. J. Jokela, "Defects in ZnO," *Journal of Applied Physics*, vol. 106, no. 7, p. 71101, 2009.

[241] J. C. Fan, K. M. Sreekanth, Z. Xie, S. L. Chang, and K. V Rao, "P-Type ZnO Materials: Theory, Growth, Properties and Devices," *Progress in Materials Science*, vol. 58, no. 6, pp. 874–985, 2013.

[242] K. Kobayashi, Y. Kohno, Y. Tomita, Y. Maeda, and S. Matsushima, "Possibility for Hole Doping into Amorphous InGaZnO4 Films Prepared by RF Sputtering," *Physica Status Solidi (C) Current Topics in Solid State Physics*, vol. 8, no. 2, pp. 531–533, 2011.

[243] M. Miyasaka and J. Stoemenos, "Excimer Laser Annealing of Amorphous and Solid-Phase-Crystallized Silicon Films," *Journal of Applied Physics*, vol. 86, no. 10, pp. 5556–5565, 1999.

[244] M. D. Ker, C. K. Deng, and J. L. Huang, "On-Panel Output Buffer with Offset Compensation Technique for Data Driver in LTPS Technology," *IEEE/OSA Journal of Display Technology*, vol. 2, no. 2, pp. 153–159, 2006.

[245] F. Simon, "New Technology for Creation of LTPS with Excimer Laser Annealing," *Proceedings Asia Display/IMID 04*, vol. 4, pp. 319–321, 2004.

[246] J. Kim, A. M. Piwowar, R. Nowak, J. A. Gradella, and W. A. Anderson, "Cobalt-Induced Polycrystalline Silicon Film Growth," *Applied Surface Science*, vol. 253, no. 6, pp. 3053–3056, 2007.

[247] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M. A. Hasan, "Al Induced Crystallization of a-Si," *Journal of Applied Physics*, vol. 69, no. 9, pp. 6394–6399, 1991.

[248] L. Hultman, A. Robertsson, H. T. G. Hentzell, I. Engstrom, and P. A. Psaras, "Crystallization of Amorphous-Silicon During Thin-Film Gold Reaction," *Journal of Applied Physics*, vol. 62, no. 9, pp. 3647–3655, 1987.

[249] S. Y. Yoon, J. Y. Oh, C. O. Kim, and J. Jang, "Low Temperature Solid Phase Crystallization of Amorphous Silicon at 380 C," *Journal of Applied Physics*, vol. 84, no. 11, pp. 6463–6465, 1998.

[250] R. C. Cammarata, C. V. Thompson, C. Hayzelden, and K. N. Tu, "Silicide Precipitation and Silicon Crystallization in Nickel Implanted Amorphous Silicon Thin Films," *Journal of Materials Research*, vol. 5, no. 10. pp. 2133–2138, 1990.

[251] C. J. Brown, H. Kato, K. Maeda, and B. Hadwen, "A Continuous-Grain Silicon-System LCD with Optical Input Function," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12. pp. 2904–2912, 2007.

[252] Z. Jin, K. Moulding, H. S. Kwok, and M. Wong, “The Effects of Extended Heat Treatment on Ni Induced Lateral Crystallization of Amorphous Silicon Thin Films,” *IEEE Transactions on Electron Devices*, vol. 46, no. 1, pp. 78–82, 1999.

[253] J. C. Kim, J. H. Choi, S. S. Kim, and J. Jang, “Stable Polycrystalline Silicon TFT with MICC,” *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 182–184, 2004.

[254] T. Ito, T. Iinuma, A. Murakoshi, H. Akutsu, K. Suguro, T. Arikado, *et al.*, “10-15 nm Ultrashallow Junction Formation by Flash-Lamp Annealing,” *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 41, no. 4B, pp. 2394–2398, 2002.

[255] T. Gebel, M. Voelskow, W. Skorupa, G. Mannino, V. Privitera, F. Priolo, *et al.*, “Flash Lamp Annealing with Millisecond Pulses for Ultra-Shallow Boron Profiles in Silicon,” *Nuclear Instruments and Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms*, vol. 186, no. 1–4, pp. 287–291, 2002.

[256] G. A. Kachurin, I. E. Tyschenko, K. S. Zhuravlev, N. A. Pazdnikov, V. A. Volodin, A. K. Gutakovsky, *et al.*, “Visible and Near-Infrared Luminescence from Silicon Nanostructures Formed by Ion Implantation and Pulse Annealing,” *Nuclear Instruments and Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms*, vol. 122, no. 3, pp. 571–574, 1997.

[257] S. Prucnal, M. O. Liedke, S. Zhou, M. Voelskow, A. Muecklich, M. Turek, *et al.*, “Conductivity Type and Crystal Orientation of GaAs Nanocrystals Fabricated in Silicon by Ion Implantation and Flash Lamp Annealing,” *Nuclear Instruments and Methods in Physics Research, Section B: Beam Interactions with Materials and Atoms*, vol. 312, pp. 104–109, 2013.

[258] Y. W. Lee, S.-J. Kim, S.-Y. Lee, W.-G. Lee, K.-S. Yoon, H.-J. Lee, *et al.*, “Comparison of Electrical Properties and Bias Stability of Double-Gate a-HIZO TFTs According to TFT Structure,” *IEEE Electron Device Letters*, vol. 33, no. 6, pp. 821–823, 2012.

[259] B. Pecz, L. Dobos, D. Panknin, W. Skorupa, C. Lioutas, and N. Vouroutzis, “Crystallization of Amorphous-Si Films by Flash Lamp Annealing,” *Applied Surface Science*, vol. 242, no. 1–2, pp. 185–191, 2005.

[260] K. Ohdaira and H. Matsumura, “Liquid-Phase Explosive Crystallization of Electron-Beam-Evaporated a-Si Films Induced by Flash Lamp Annealing,” *Journal of Crystal Growth*, vol. 362, pp. 149–152, 2013.

[261] D.-H. Kim, B.-K. Kim, H. J. Kim, and S. Park, “Crystallization of Amorphous Silicon Thin-Film on Glass Substrate Preheated at 650 C Using Xe Arc Flash of 400 us,” *Thin Solid Films*, vol. 520, no. 21, pp. 6581–6588, 2012.

[262] T. Mudgal, C. Reepmeyer, R. G. Manley, D. Cormier, and K. D. Hirschman, “Crystallization of Amorphous Silicon and Dopant Activation Using Xenon Flash-Lamp Annealing (FLA),” *MRS Proceedings*, vol. 1666, 2014.

[263] T. Watanabe and K. Ohdaira, “The Formation of Poly-Si Films on Flat Glass Substrates by Flash Lamp Annealing,” *Thin Solid Films*, vol. 595, pp. 235–238, 2015.

[264] S. Saxena, D. Kim, and J. Park, “Polycrystalline Silicon Thin-Film Transistor Using Xe Flash-Lamp Annealing,” *IEEE Electron Device Letters*, vol. 31, no. 11, pp. 1242–1244, 2010.

[265] S. Saxena and J. Jang, “Protrusions of Super Grains Formed by Ultrashort Xe Flash-Lamp Annealing of Amorphous Silicon and Its Effect on the Performances of Thin-Film Transistors,” *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2638–2643, 2011.

[266] R. Manley, G. Fenger, P. Meller, K. Hirschman, C. A. Kosik Williams, D. Dawson-Elli, *et al.*, “Development of Integrated Electronics on Silicon-on-Glass (SiOG) Substrate,” *ECS Transactions*, vol. 16, no. 9, pp. 371–380, 2008.

[267] E. Lee, M. D. H. Chowdhury, M. S. Park, and J. Jang, “Effect of Top Gate Bias on Photocurrent and Negative Bias Illumination Stress Instability in Dual Gate Amorphous Indium-Gallium-Zinc Oxide Thin-Film Transistor,” *Applied Physics Letters*, vol. 107, no. 23, p. 233509, 2015.

[268] J. H. Song, N. Oh, B. Du Anh, H. D. Kim, and J. K. Jeong, “Dynamics of Threshold Voltage Instability in IGZO TFTs: Impact of High Pressurized Oxygen Treatment on the Activation Energy Barrier,” *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 1054–1058, 2016.

[269] S. Oh, J. H. Baeck, J. U. Bae, K.-S. Park, and I. B. Kang, “Effect of Interfacial Excess Oxygen on Positive-Bias Temperature Stress Instability of Self-Aligned Coplanar InGaZnO Thin-Film Transistors,” *Applied Physics Letters*, vol. 108, no. 14, p. 141604, 2016.

[270] X. D. Huang, J. Q. Song, and P. T. Lai, “Improved Stability of a-InGaZnO Thin-Film Transistor under Positive Gate Bias Stress by Using Fluorine Plasma Treatment,” *IEEE Electron Device Letters*, vol. 38, no. 5, pp. 576–579, 2017.

[271] S. Choi, J. Jang, H. Kang, J. H. Baeck, J. U. Bae, K.-S. Park, *et al.*, “Systematic Decomposition of the Positive Bias Stress Instability in Self-Aligned Coplanar InGaZnO Thin-Film Transistors,” *IEEE Electron Device Letters*, vol. 38, no. 5, pp. 580–583, 2017.

[272] K. Y. Shin, Y. J. Tak, W.-G. Kim, S. Hong, and H. J. Kim, “Improvement of Electrical Characteristics and Stability of Amorphous Indium Gallium Zinc Oxide Thin Film Transistors Using Nitrocellulose Passivation Layer,” *ACS Applied Materials & Interfaces*, vol. 9, no. 15, pp. 13278–13285, 2017.

[273] J. Yang, P.-Y. Liao, T.-C. Chang, B.-W. Chen, H.-C. Huang, W.-C. Su, *et al.*, “Investigation of an Anomalous Hump Phenomenon in Via-Type Amorphous In-Ga-Zn-O Thin-Film Transistors Under Positive Bias Temperature Stress,” *Applied Physics Letters*, vol. 110, no. 14, p. 143508, 2017.

[274] X. Zhou, Y. Shao, L. Zhang, X. Xiao, D. Han, Y. Wang, *et al.*, “Oxygen Adsorption Effect of Amorphous InGaZnO Thin-Film Transistors,” *IEEE Electron Device Letters*, vol. 38, no. 4, pp. 465–468, 2017.

[275] A. Abliz, Q. Gao, D. Wan, X. Liu, L. Xu, C. Liu, *et al.*, “Effects of Nitrogen and Hydrogen Codoping on the Electrical Performance and Reliability of InGaZnO Thin

-Film Transistors," *ACS Applied Materials & Interfaces*, vol. 9, no. 12, pp. 10798–10804, 2017.

[276] T. Goto, F. Imaizumi, and S. Sugawa, "Improvement in the Negative Bias Illumination Stress Stability for Silicon-Ion Implanted Amorphous InGaZnO Thin-Film Transistors," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 345–348, 2017.

[277] For a comprehensive list of IGZO products see: J. F. Wager, "Oxide TFTs: A Progress Report," *Information Display*, 2016. [Online]. Available: http://informationdisplay.org/IDArchive/2016/JanuaryFebruary/FrontlineTechnologyOxideTFTsReport.aspx.